4096 BIT HIGH SPEED STATIC MOS RANDOM ACCESS MEMORY

DESCRIPTION

The μPD410 is a very high speed 4K bit static random access memory. It is organized as 4096 words by 1 bit per word and fabricated using N channel silicon gate MOS technology.

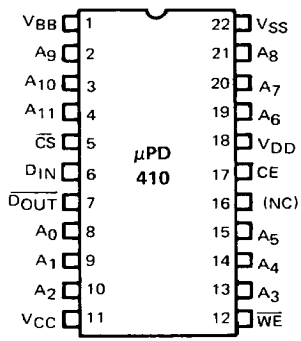
All signals to the device are TTL compatible except for Chip Enable which is standard +12 Volt MOS level.

Circuit operation starts with the rising edge of CE. Data is latched and valid until falling edge of CE. Address and Chip Select signals are latched on-chip to simplify system timing requirements.

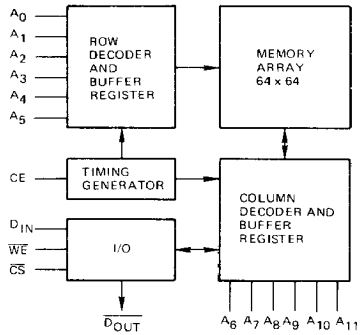
FEATURES

- 4096 Words x 1 Bit Organization
- Fully Decoded
- TTL Compatible (except CE)
- High Speed-Access Time: 90 ns max.
- Cycle Time: 220 ns min.
- Static Operation — No Refresh Required
- Standby Power: 75 mW max.
- Active Power: 470 mW typ.
- Supply Voltages: V_{DD} = +12V, V_{CC} = +5V, V_{BB} = -5V
- Address Registers on the Chip
- Three State Output
- Standard 22 Pin Ceramic Dual-in-Line Package
- Pin Compatible with μPD411 and Other 4K Dynamic RAMs

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
All Output Voltages	-0.3 to +20 Volts①
All Input Voltages	-0.3 to +20 Volts①
Supply Voltage V_{DD}	-0.3 to +20 Volts①
Supply Voltage V_{CC}	-0.3 to +20 Volts①
Supply Voltage V_{SS}	-0.3 to +20 Volts①
Power Dissipation	1.0W

Note: ① Relative to V_{BB}

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

*T_a = 25°C
T_a = 0°C to 70°C; V_{DD} = 12V ± 5%; V_{CC} = 5V ± 5%; V_{BB} = -5V ± 5%; V_{SS} = 0V

PARAMETER		SYMBOL	LIMITS MIN	LIMITS MAX	UNIT	TEST CONDITIONS
Input Leakage Current		I_{LI}		10	μA	V_{IN} = V_{IL}MIN to V_{IH}MAX
CE Input Leakage Current		I_{LC}		10	μA	V_{IN} = V_{ILC}MIN to V_{IHC}MAX
Output Leakage Current		I_{LO}		10	μA	CE = V_{ILC} or $\overline{CS}$ = V_{IH} V_O = 0V to 5.25V
V_{DD} Supply Current during CE off		I_{DDOFF}		200	μA	CE = -1.0V to 0.6V
V_{DD} Supply Current during CE on		I_{DDON}		20	mA	CE = V_{IHC}
Average V_{DD} Current	μPD410	I_{DDAV}		24	mA	Minimum Cycle Time
	μPD410-1	I_{DDAV}		32	mA	
	μPD410-2	I_{DDAV}		45	mA	
	μPD410-3	I_{DDAV}		45	mA	
V_{BB} Supply Current		I_{BB}		100	μA	
V_{CC} Supply Current during CE off		I_{CCOFF}		15	mA	CE = V_{ILC} or $\overline{CS}$ = V_{IH}
Average V_{CC} Current		I_{CCAV}		21	mA	D_{OUT} = No load
Input Low Voltage		V_{IL}	-1.0	0.6	V	
Input High Voltage		V_{IH}	2.4	V_{CC}+1	V	
CE Input Low Voltage		V_{ILC}	-1.0	0.6	V	
CE Input High Voltage		V_{IHC}	V_{DD}-1	V_{DD}+1	V	
Output Low Voltage		V_{OL}	0	0.4	V	I_{OL} = 3.2 mA
Output High Voltage		V_{OH}	2.4	V_{CC}	V	I_{OH} = 2.0 mA

CAPACITANCE

T_a = 0°C to 70°C; V_{DD} = 12V ± 5%; V_{CC} = 5V ± 5%; V_{BB} = -5V ± 5%; V_{SS} = 0V

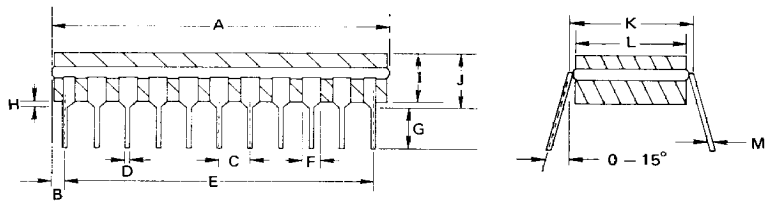
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Address Capacitance	C_{AD}		4	6	pF	V_{IN} = V_{SS}
$\overline{CS}$ Capacitance	C_{CS}		4	6	pF	V_{IN} = V_{SS}
D_{IN} Capacitance	C_{IN}		8	10	pF	V_{IN} = V_{SS}
$\overline{D_{OUT}}$ Capacitance	C_{OUT}		5	7	pF	V_{OUT} = V_{SS}
$\overline{WE}$ Capacitance	C_{WE}		8	10	pf	V_{IN} = V_{SS}
CE Capacitance	C_{CE}		18	27	pf	V_{IN} = V_{SS}

AC CHARACTERISTICS

T_a = 0°C to 70°C; V_{DD} = 12V ± 5%; V_{CC} = 5V ± 5%; V_{BB} = -5V ± 5%; V_{SS} = 0V

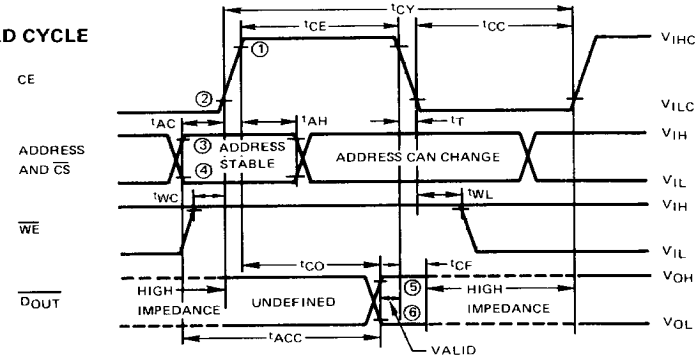
PARAMETER	SYMBOL	LIMITS 410 MIN	410 MAX	410-1 MIN	410-1 MAX	410-2 MIN	410-2 MAX	410-3 MIN	410-3 MAX	UNIT	TEST CONDITIONS
READ, WRITE AND READ-MODIFY-WRITE											
Address to CE Set Up Time	t_{AC}	0		0		0		0		ns	
Address Hold Time	t_{AH}	90		70		50		50		ns	
CE Off Time	t_{CC}	190		140		90		90		ns	
CE Transition Time	t_T	0	40	0	40	0	40	0	40	ns	
CE off to Output High Impedance State	t_{CF}	0	90	0	90	0	90	0	90	ns	
READ											
Cycle Time	t_{CY}	440		330		220		220		ns	t_T = 10 ns
CE on Time	t_{CE}	230	2000	170	2000	110	2000	110	2000	ns	
CE Output Delay	t_{CO}		190		140		90		80	ns	Load = 50 pF + 1TTL, Ref = 2.0 or 0.8V
Access Time	t_{ACC}		200		150		100		90	ns	$t_{ACC} = t_{AC} + t_{CO} + t_T$
CE to $\overline{WE}$	t_{WL}	20		20		20		20		ns	
$\overline{WE}$ to CE on	t_{WC}	0		0		0		0		ns	
WRITE											
Cycle Time	t_{CY}	440		330		220		220		ns	t_T = 10 ns
CE on Time	t_{CE}	230	2000	170	2000	110	2000	110	2000	ns	
$\overline{WE}$ to CE off	t_W	130		100		70		70		ns	
CE to $\overline{WE}$	t_{CW}	130		100		70		70		ns	
D_{IN} to $\overline{WE}$ Set Up	t_{DW}	0		0		0		0		ns	
D_{IN} Hold Time	t_{DH}	60		40		20		20		ns	
$\overline{WE}$ Pulse Width	t_{WP}	130		100		70		70		ns	
READ-MODIFY-WRITE											
Read-Modify-Write (RMW) Cycle Time	t_{RWC}	560		420		280		280		ns	t_T = 10 ns
CE Width During RMW	t_{CRW}	350	2000	260	2000	170	2000	170	2000	ns	
$\overline{WE}$ to CE on	t_{WC}	0		0		0		0		ns	
$\overline{WE}$ to CE off	t_W	130		100		70		70		ns	
$\overline{WE}$ Pulse Width	t_{WP}	130		100		70		70		ns	
D_{IN} to $\overline{WE}$ Set Up	t_{DW}	0		0		0		0		ns	
D_{IN} Hold Time	t_{DH}	60		40		20		20		ns	
CE to Output Delay	t_{CO}		190		140		90		80	ns	Load = 50 pF + 1TTL, Ref = 2.0 or 0.8V
Access Time	t_{ACC}		200		150		100		90	ns	$t_{ACC} = t_{AC} + t_{CO} + t_T$

PACKAGE OUTLINE μPD410D

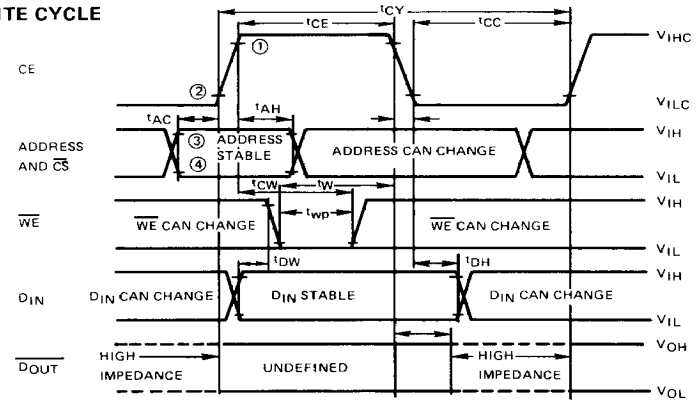


ITEM	MILLIMETERS	INCHES
A	27.43 Max.	1.079 Max.
B	1.27 Max.	0.05 Max.
C	2.54 ± 0.1	0.10
D	0.42 ± 0.1	0.016
E	25.4 ± 0.3	1.0
F	1.5 ± 0.2	0.059
G	3.5 ± 0.3	0.138
H	3.7 ± 0.3	0.145
I	4.2 Max.	0.165 Max.
J	5.08 Max.	0.200 Max.
K	10.16 ± 0.15	0.400
L	9.1 ± 0.2	0.358
M	0.25 ± 0.05	0.009

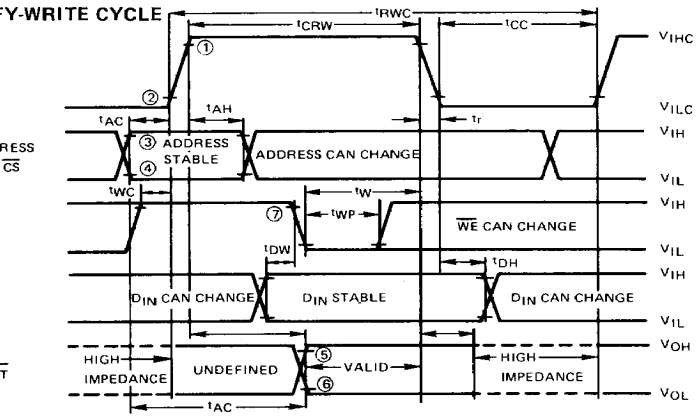
READ CYCLE



WRITE CYCLE



READ-MODIFY-WRITE CYCLE



Notes:

① V_{DD} − 2V is the reference level for measuring timing of CE.

② V_{SS} + 2V is the reference level for measuring timing of CE.

③ V_{IHMIN} is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$ and D_{IN}.

④ V_{ILMAX} is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$ and D_{IN}.

⑤ V_{SS} + 2.0V is the reference level for measuring timing of $\overline{D_{OUT}}$.

⑥ V_{SS} + 0.8V is the reference level for measuring timing of $\overline{D_{OUT}}$.

⑦ $\overline{WE}$ must be at V_{IH} until end of t_{CO}.