4096 × 1 STATIC NMOS RAM

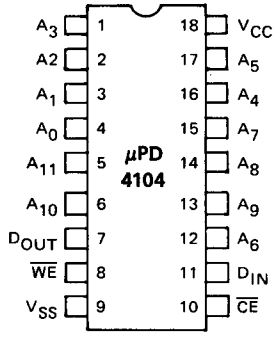
DESCRIPTION

The μPD4104 is a high performance 4K static RAM. Organized as 4096 x 1, it uses a combination of static storage cells with dynamic input/output circuitry to achieve high speed and low power in the same device. Utilizing NMOS technology, the μPD4104 is fully TTL compatible and operates with a single +5V ± 10% supply.

FEATURES

- Fast Access Time – 200 ns (μPD4104-2)
- Very Low Stand-By Power – 28 mW Max.
- Low V_{CC} Data Retention Mode to +3 Volts.
- Single +5V ±10% Supply.
- Fully TTL Compatible.
- Available in 18 Pin Plastic and Ceramic Dual-in-Line Packages.
- 3 Performance Ranges:

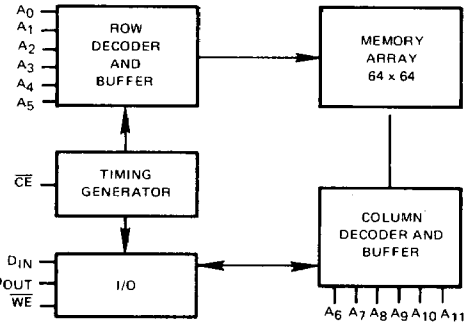
	ACCESS TIME	R/W CYCLE	SUPPLY CURRENT		
			ACTIVE	STANDBY	LOW V_{CC}
μPD4104	300 ns	460 ns	21 mA	5 mA	5 mA
μPD4104-1	250 ns	385 ns	21 mA	5 mA	3.3 mA
μPD4104-2	200 ns	310 ns	25 mA	5 mA	3.3 mA



PIN NAMES

A_0-A_{11}	Address Inputs
$\overline{CE}$	Chip Enable
D_{IN}	Data Input
D_{OUT}	Data Output
V_{SS}	Ground
V_{CC}	Power (+5V)
$\overline{WE}$	Write Enable

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . −65°C to +150°C
Voltage on Any Pin . . . . . −1 to +7 Volts ①
Power Dissipation . . . . . 1 Watt
Short Circuit Output Current . . . . . 50 mA

Note: ① With respect to V_{SS}

$T_a = 25°C$

* COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS ① ⑥

$T_a = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 10\%$

PARAMETER		SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Supply Voltage		V_{CC}	4.5	5.0	5.5	V	①
Logic "1" Voltage All Inputs		V_{IH}	2.2	−3	7.0	V	
Logic "0" Voltage All Inputs		V_{IL}	−1.0		0.8	V	
Average V_{CC} Power Supply Current	μPD4104	I_{CC1}			21	mA	②
	μPD4104-1	I_{CC1}			21	mA	
	μPD4104-2	I_{CC1}			25	mA	
Standby V_{CC} Power Supply Current		I_{CC2}			5	mA	③
Input Leakage Current (Any Input)		I_{IL}	−10		10	μA	④
Output Leakage Current		I_{OL}	−10		10	μA	③ ⑤
Output Logic "1" Voltage I_{OUT} −500 μA		V_{OH}	2.4			V	
Output Logic "0" Voltage I_{OUT} 5mA		V_{OL}			0.4	V	

CAPACITANCE ①

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		4	6	pF	⑦
Output Capacitance	C_{OUT}		6	7	pF	⑦

Notes: ① All voltages referenced to V_{SS}

② I_{CC1} is related to precharge and cycle times. Guaranteed maximum values for I_{CC1} may be calculated by

$$I_{CC1}\ [mA] = (5t_p + 13\ (t_C - t_p) + 3420)\ t_C$$

where t_p and t_C are expressed in nanoseconds. Equation is referenced to the **−2 device**, other devices derate to the same curve.

③ Output is disabled (open circuit), $\overline{CE}$ is at logic 1.

④ All device pins at 0 volts except pin under test at 0. $V_{IN} = 5.5$ volts.

⑤ $0V \leq V_{OUT} \leq +5.5V$.

⑥ During power up, $\overline{CE}$ and $\overline{WE}$ must be at V_{IH} for minimum of 2 ms after V_{CC} reaches 4.5V, before a valid memory cycle can be accomplished.

⑦ Effective capacitance calculated from the equation $C = \frac{\Delta t}{\Delta V}$ with ΔV equal to 3V and V_{CC} nominal.

AC CHARACTERISTICS ② ⑦

T_a = 0°C to +70°C, V_{CC} = +5V ± 10% ①

PARAMETER	SYMBOL	LIMITS 4104 MIN	4104 MAX	4104-1 MIN	4104-1 MAX	4104-2 MIN	4104-2 MAX	UNIT	TEST CONDITIONS
Read or Write Cycle Time	t_C	460		385		310		ns	⑧
Random Access	t_{AC}		300		250		200	ns	③
Chip Enable Pulse Width	t_{CE}	300	10,000	250	10,000	200	10,000	ns	
Chip Enable Precharge Time	t_P	150		125		100		ns	
Address Hold Time	t_{AH}	165		135		110		ns	
Address Set-Up Time	t_{AS}	0		0		0		ns	
Output Buffer Turn-Off Delay	t_{OFF}	0	75	0	65	0	50	ns	⑨
Read Command Set-Up Time	t_{RS}	0		0		0		ns	④
Write Enable Set-Up Time	t_{WS}	−20		−20		−20		ns	④
Data Input Hold Time Referenced to $\overline{WE}$	t_{DIH}	25		25		25		ns	
Write Enabled Pulse Width	t_{WW}	90		75		60		ns	
Modify Time	t_{MOD}	0	10,000	0	10,000	0	10,000	ns	⑤
$\overline{WE}$ to $\overline{CE}$ Precharge Lead Time	t_{WPL}	105		85		70		ns	⑥
Data Input Set-Up Time	t_{DS}	0		0		0		ns	
Write Enable Hold Time	t_{WH}	225		185		150		ns	
Transition Time	t_T	5	50	5	50	5	50	ns	
Read-Modify-Write Cycle Time	t_{RMW}	565		470		380		ns	⑩

Notes: ① All voltages referenced to V_{SS}

② During power up, $\overline{CE}$ and $\overline{WE}$ must be at V_{IH} for minimum of 2 ms after V_{CC} reaches 4.5V, before a valid memory cycle can be accomplished.

③ Measured with load circuit equivalent to 2 TTL loads and CL = 100 pF.

④ If $\overline{WE}$ follows $\overline{CE}$ by more than t_{WS} then data out may not remain open circuited.

⑤ Determined by user. Total cycle time cannot exceed t_{CE} max.

⑥ Data-in set-up time is referenced to the later of the two falling clock edges $\overline{CE}$ or $\overline{WE}$.

⑦ AC measurements assume t_T = 5 ns. Timing points are taken as V_{IL} = 0.8V and V_{IH} = 2.2V on the inputs and V_{OL} = 0.4V and V_{OH} = 2.4V on the output waveform.

⑧ $t_C = t_{CE} + t_P + 2t_T$.

⑨ The true level of the output in the open circuit condition will be determined totally by output load conditions. The output is guaranteed to be open circuit within t_{OFF}.

⑩ $t_{RMW} = t_{AC} + t_{WPL} + t_P + 3t_T + t_{MOD}$.

STANDBY CHARACTERISTICS

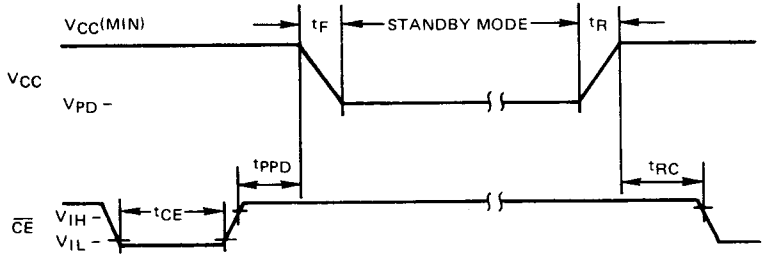
T_a = 0°C to +70°C

PARAMETER	SYMBOL	LIMITS 4104 MIN	4104 MAX	4104-1 MIN	4104-1 MAX	4104-2 MIN	4104-2 MAX	UNIT	TEST CONDITIONS
V_{CC} In Standby	V_{PD}	3.0		3.0		3.0		V	
Standby Current	I_{PD}		5.0		3.3		3.3	mA	①
Power Supply Fall Time	T_F	100		100		100		μs	
Power Supply Rise Time	T_R	100		100		100		μs	
Chip Enable Pulse $\overline{CE}$ Width	T_{CE}	300		250		200		μs	
Chip Enable Precharge to Power Down Time	T_{PPD}	150		125		100		ns	
"I" Level $\overline{CE}$ Min Level	V_{IH}	2.2		2.2		2.2		V	
Standby Recovery Time	T_{RC}	500		500		500		μs	

Note: ① Maximum value for V_{PD} minimum value (= 3 V).

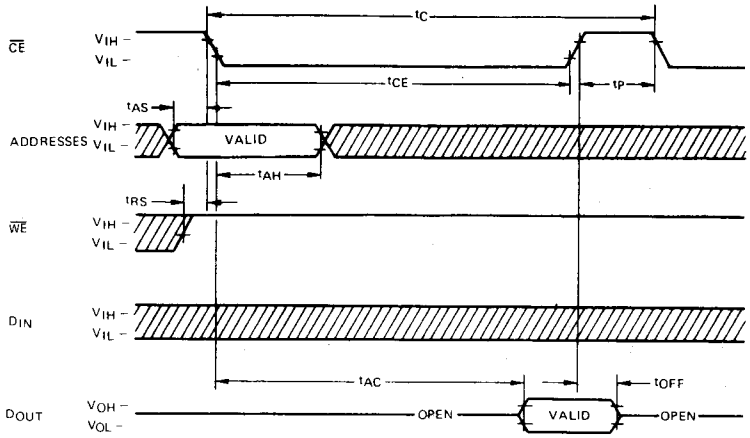
TIMING WAVEFORMS

POWER DOWN

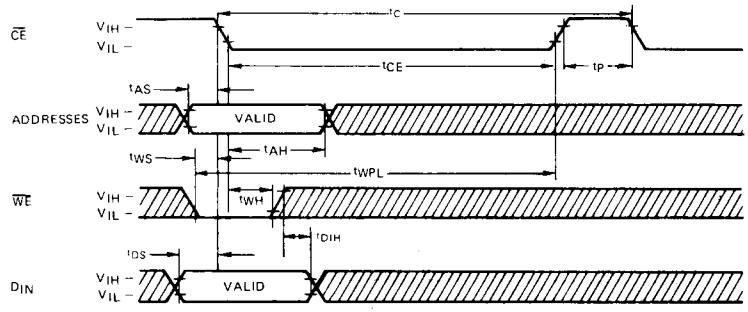


TIMING WAVEFORMS (CONT.)

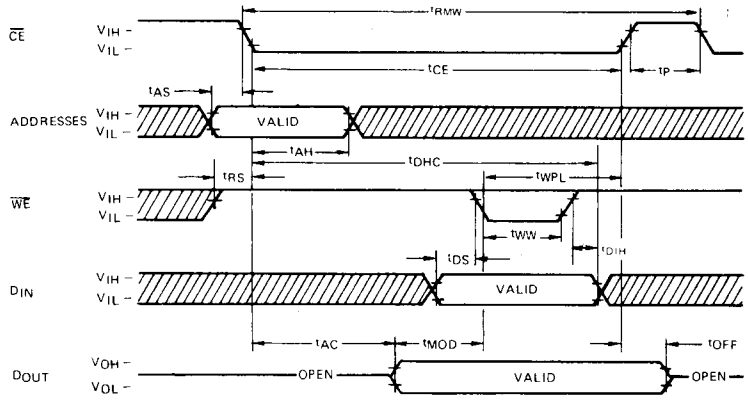
READ CYCLE



WRITE CYCLE



READ-MODIFY-WRITE CYCLE



OPERATIONAL DESCRIPTION

READ CYCLE

The selection of one of the possible 4096 bits is made by virtue of the 12 address bits presented at the inputs. These are latched into the chip by the negative going edge of chip enable ($\overline{CE}$). If the write enable ($\overline{WE}$) input is held at a high level (V_{IH}) while the $\overline{CE}$ input is clocked to a low level (V_{IL}), a read operation will be performed. At the access time (t_{AC}), valid data will appear at the output. Since the output is unlatched by a positive transition of $\overline{CE}$, it will be in the high impedance state from the previous cycle until the access time. It will go to the high impedance state again at the end of the current cycle when $\overline{CE}$ goes high.

The address lines may be set up for the next cycle any time after the address hold time has been satisfied for the current cycle.

WRITE CYCLE

Data to be written into a selected cell is latched into the chip by the later negative transition of $\overline{CE}$ or $\overline{WE}$. If $\overline{WE}$ is brought low before $\overline{CE}$, the cycle is an "Early Write" cycle, and data will be latched by $\overline{CE}$. If $\overline{CE}$ is brought low before $\overline{WE}$, as in a Read-Modify-Write cycle, then data will be latched by $\overline{WE}$.

3

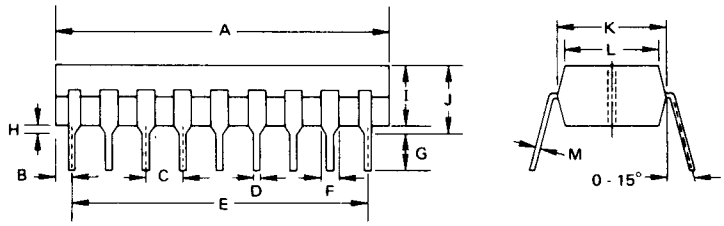
If the cycle is an "Early Write" cycle, the output will remain in the high impedance state. For a Read-Modify-Write cycle; the output will be active for the Modify and Write portions of the memory cycle until $\overline{CE}$ goes high. If $\overline{WE}$ is brought low after $\overline{CE}$ but before the access time, the state of the output will be undefined. The desired data will be written into the cell if data-in is valid on the leading edge of $\overline{WE}$, t_{DIH} is satisfied, and $\overline{WE}$ occurs prior to $\overline{CE}$ going high by at least the minimum lead time (t_{WPL}).

READ-MODIFY-WRITE

Read and Write cycles can be combined to allow reading of a selected location and then modifying that data within the same memory cycle. Data is read at the access time and modified during a period defined by the user. New data is written between $\overline{WE}$ low and the positive transition of $\overline{CE}$. Data out will remain valid until the rising edge of $\overline{CE}$. A minimum R-M-W cycle time can be calculated by $t_{RMW} = t_{AC} + t_{MOD} + t_{WPL} + t_P + 3\,t_T$; where t_{RMW} is the cycle time, t_{AC} is the access time, t_{MOD} is the user defined modify time, t_{WPL} is the $\overline{WE}$ to $\overline{CE}$ lead time, t_P is the $\overline{CE}$ high time, and t_T is one transition time.

POWER DOWN MODE

In power down, data may be retained indefinitely by maintaining V_{CC} at +3V. However, prior to V_{CC} going below V_{CC} minimum ($\leq$4.5V) $\overline{CE}$ must be taken high (V_{IH} = 2.2V) and held for a minimum time period t_{PPD} and maintained at V_{IH} for the entire standby period. After power is returned to V_{CC} min or above, $\overline{CE}$ must be held high for a minimum of t_{RC} in order that the device may operate properly. See power down waveforms herein. Any active cycle in progress prior to power down must be completed so that t_{CE} min is not violated.

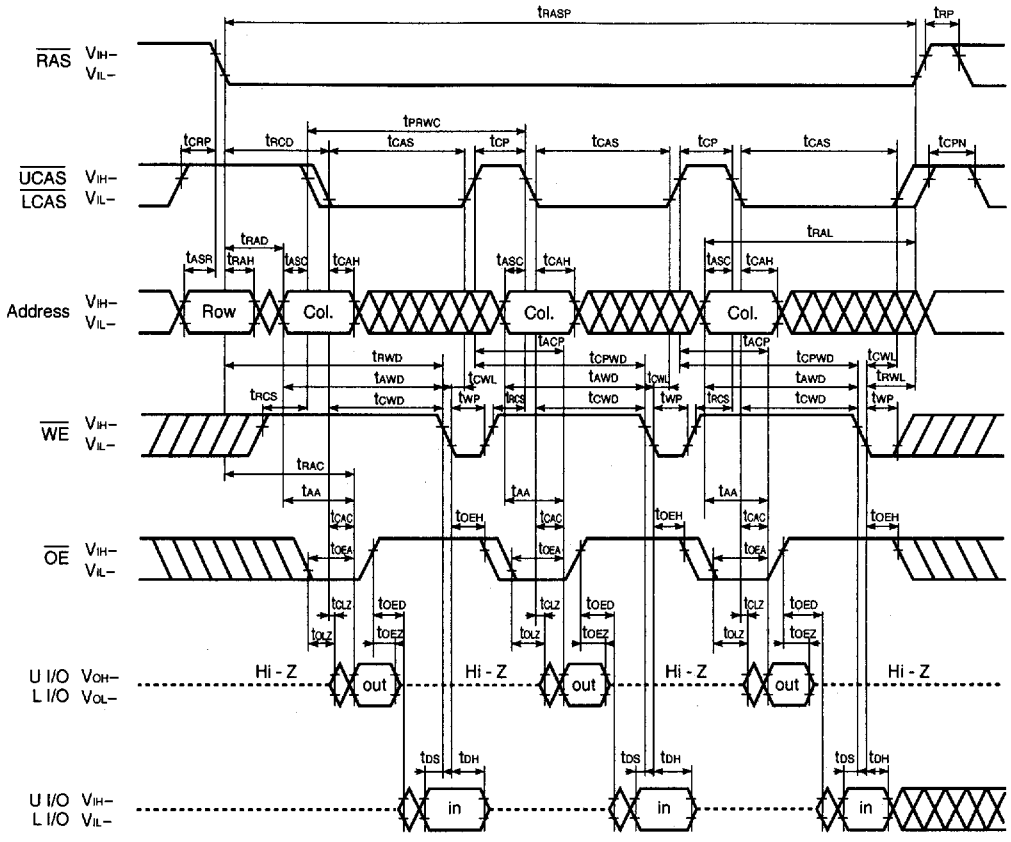


PACKAGE OUTLINES
μPD4104C

Plastic

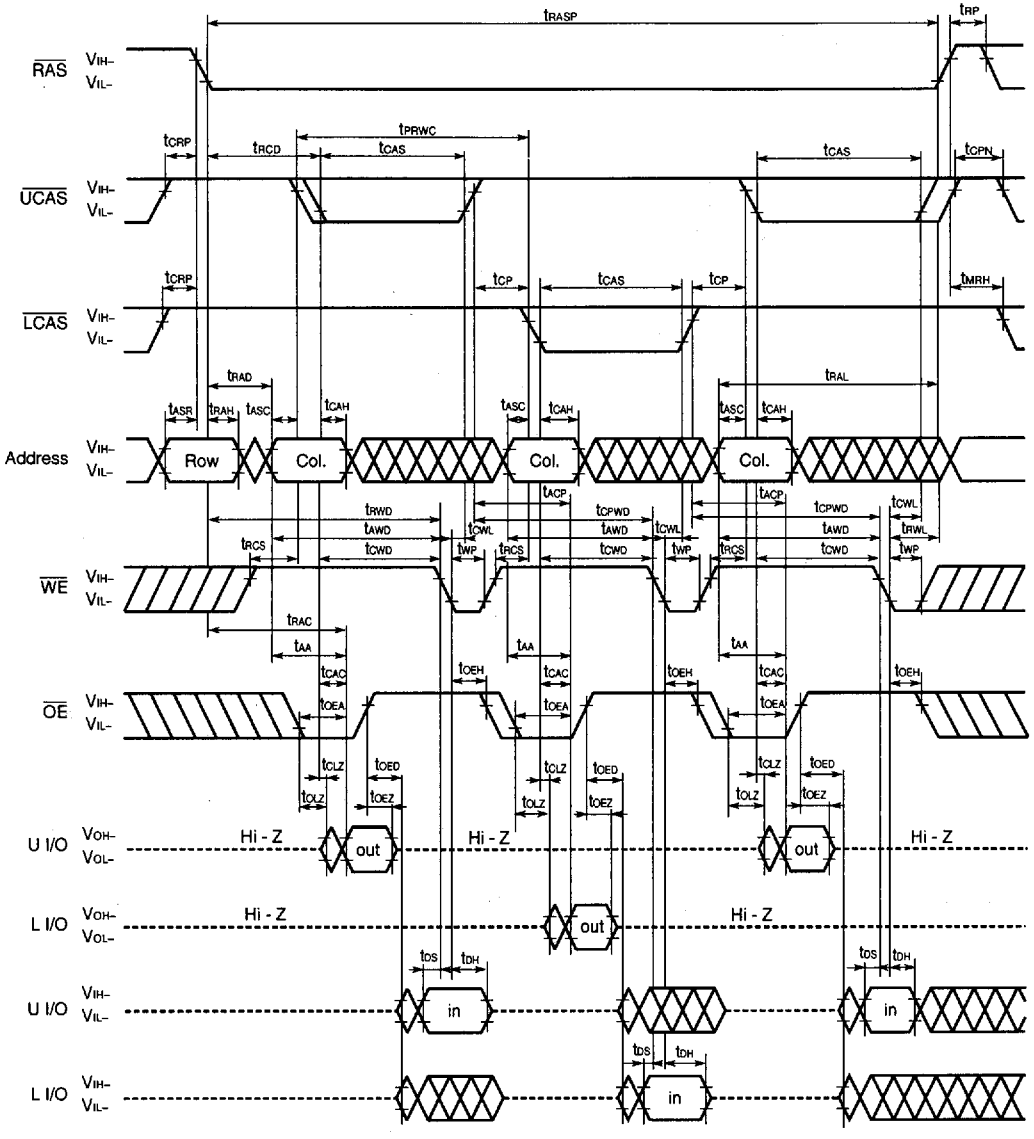
ITEM	MILLIMETERS	INCHES
A	23.2 MAX.	0.91 MAX.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.06
G	2.5 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.2 MAX.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01

Fast Page Mode Read Modify Write Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

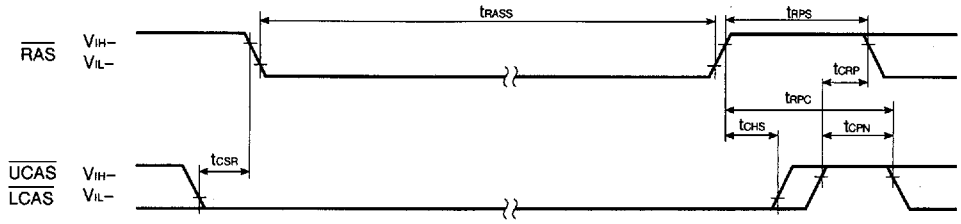
Fast Page Mode Byte Read Modify Write Cycle



Remarks 1. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

2. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

$\overline{CAS}$ Before $\overline{RAS}$ Self Refresh Cycle (Only for the μPD42S18160)



Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

Cautions on Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh

$\overline{CAS}$ before $\overline{RAS}$ self refresh can be used independently when used in combination with distributed $\overline{CAS}$ before $\overline{RAS}$ long refresh; However, when used in combination with burst $\overline{CAS}$ before $\overline{RAS}$ long refresh or with long $\overline{RAS}$ only refresh (both distributed and burst), the following cautions must be observed.

(1) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Burst $\overline{CAS}$ Before $\overline{RAS}$ Long Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and burst $\overline{CAS}$ before $\overline{RAS}$ long refresh are used in combination, please perform $\overline{CAS}$ before $\overline{RAS}$ refresh as follows just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

μPD42S18160: 1,024 times within a 16 ms interval

(2) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Long $\overline{RAS}$ Only Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and $\overline{RAS}$ only refresh are used in combination, please perform $\overline{RAS}$ only refresh as follows just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

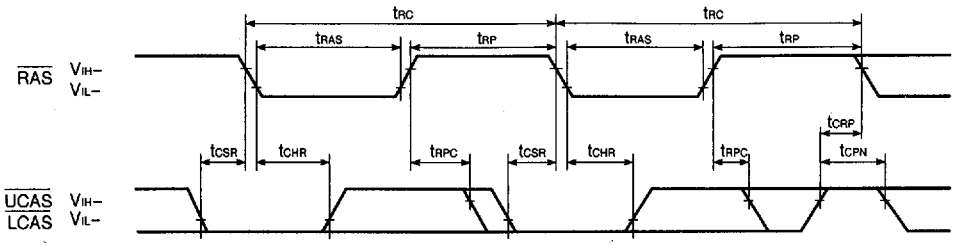
μPD42S18160: 1,024 times within a 16 ms interval

(3) If $t_{RASS\ (MIN.)}$ is not satisfied at the beginning of $\overline{CAS}$ before $\overline{RAS}$ self refresh cycles ($t_{RAS} < 100\ \mu s$), $\overline{CAS}$ before $\overline{RAS}$ refresh cycles will be executed one time.
If $10\ \mu s < t_{RAS} < 100\ \mu s$, $\overline{RAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ self refresh (t_{RPS}) is applied.
And refresh cycles as follows should be met.

μPD42S18160: 1,024 times within a 128 ms interval

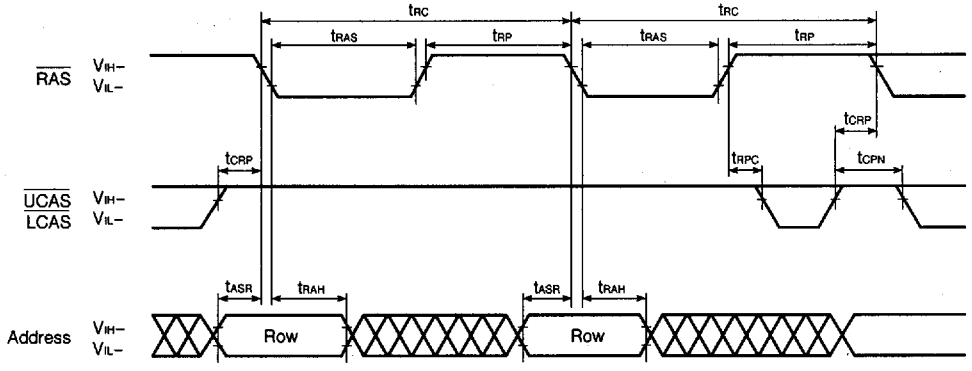
For details, please refer to **How to use DRAM** User's Manual.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

$\overline{RAS}$ Only Refresh Cycle



Remark $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

Hidden Refresh Cycle (Read)