μPD41101
910 x 8-BIT
LINE BUFFER FOR NTSC TV

Description

The μPD41101 is a 910-word by 8-bit line buffer fabricated with the N-channel silicon-gate process. The device helps to create an NTSC flicker-free television picture (noninterlaced scan conversion) by providing intermediate storage and very high-speed read and write operation.

The μPD41101 can also be used as a digital delay line. The delay length is variable from 10 bits (at maximum clock speed) to 910 bits.

Features

- ☐ 910-word x 8-bit organization
- ☐ Line buffer for NTSC, $4f_{SC}$ digital television systems
- ☐ Asynchronous and simultaneous read/write operation
- ☐ 1H (910-bit) delay line capability
- ☐ TTL-compatible inputs and outputs
- ☐ Three-state outputs
- ☐ Single 5-volt ±10% power supply
- ☐ 300-mil, 24-pin plastic DIP and 450-mil, 24-pin plastic miniflat packaging

Ordering Information

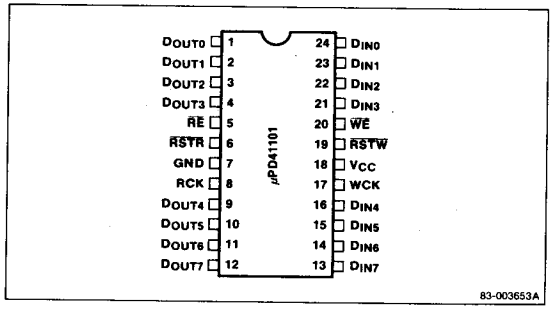
Part Number	Read Cycle Time (min)	Write Cycle Time (min)	Package
μPD41101C-3	34 ns	34 ns	24-pin plastic DIP
C-2	34 ns	69 ns	
C-1	69 ns	69 ns	
μPD41101G-3	34 ns	34 ns	24-pin plastic miniflat
G-2	34 ns	69 ns	
G-1	69 ns	69 ns	

Pin Identification

Symbol	Function
D_{IN0}-D_{IN7}	Write data inputs
D_{OUT0}-D_{OUT7}	Read data outputs
$\overline{RSTW}$	Write address reset input
$\overline{RSTR}$	Read address reset input
$\overline{WE}$	Write enable input
$\overline{RE}$	Read enable input
WCK	Write clock input
RCK	Read clock input
GND	Ground
V_{CC}	+5-volt power supply

Pin Configuration

24-Pin Plastic DIP or Miniflat



Pin Functions

D_{IN0}-D_{IN7} [Data Inputs]

In a digital television application, the digital composite signal, luminance, chrominance, etc., information is written into these inputs.

D_{OUT0}-D_{OUT7} [Data Outputs]

These tri-state outputs are used to access the stored information. In a simple digital delay line application, a delay of one-half write clock cycle plus a maximum of 300 ns is required to move data from the data inputs to the data outputs.

$\overline{RSTW}$ [Write Address Reset Input]

Bringing this signal to a low level resets the internal write address to 0 if $\overline{WE}$ is also at a low level. If $\overline{WE}$ is at a high level when the $\overline{RSTW}$ input is brought low, the internal write address is set to 909. The state of this input is strobed by the rising edge of WCK.

$\overline{RSTR}$ [Read Address Reset Input]

Strobed by the rising edge of RCK, this signal resets the internal read address to 0 if $\overline{RE}$ is also at a low level. If $\overline{RE}$ is at a high level when the $\overline{RSTR}$ input is brought low, the internal read address is set to 909.

$\overline{WE}$ [Write Enable Input]

This input controls write operation. If $\overline{WE}$ is at a low level, all write cycles proceed. If $\overline{WE}$ is at a high level, no data is written to storage cells and the write address stops increasing. The state of $\overline{WE}$ is strobed by the rising edge of WCK.

$\overline{RE}$ [Read Enable Input]

This signal is similar to $\overline{WE}$ but controls read operation. If $\overline{RE}$ is at a high level, the data outputs become high impedance and the internal read address stops increasing. The state of $\overline{RE}$ is strobed by the rising edge of RCK.

WCK [Write Clock Input]

All write cycles are executed synchronously with WCK. The states of both $\overline{RSTW}$ and $\overline{WE}$ are strobed by the rising edge of WCK at the beginning of a cycle, and the data inputs are strobed by the rising edge of WCK at the end of a cycle. The internal write address increases with each WCK cycle unless $\overline{WE}$ is at a high level to hold the write address constant. Unless inhibited by $\overline{WE}$, the internal write address will automatically wrap around from 909 to 0 and begin increasing again.

RCK [Read Clock Input]

All read cycles are executed synchronously with RCK. The states of both $\overline{RSTR}$ and $\overline{RE}$ are strobed by the rising edge of RCK at the beginning of a cycle. This same edge of RCK starts internal read operation, and access time is referenced to this edge. The internal read address increases with each RCK cycle unless $\overline{RE}$ is at a high level to hold the read address constant. Unless inhibited by $\overline{RE}$, the internal read address will automatically wrap around from 909 to 0 and begin increasing again.

Absolute Maximum Ratings

Supply voltage, V_{CC}	−1.5 to +7.0 V
Voltage on any input pin, V_I	−1.5 to +7.0 V
Voltage on any output pin, V_O	−1.5 to +7.0 V
Short-circuit output current, I_{OS}	20 mA
Operating temperature, T_{OPR}	−20 to +70°C
Storage temperature, T_{STG}	−55 to +125°C

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Block Diagram

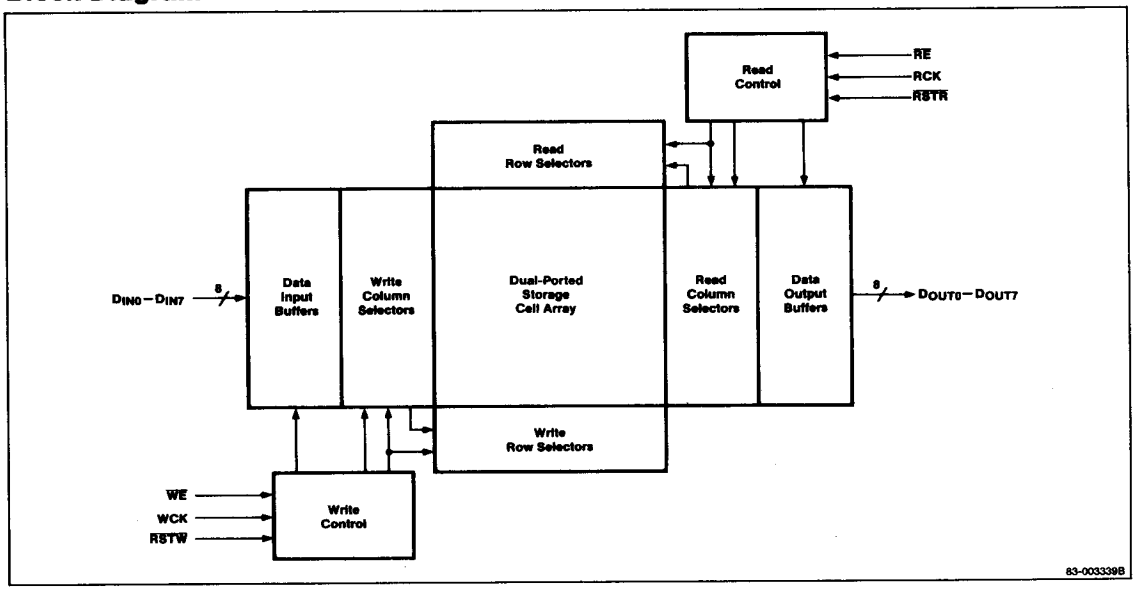
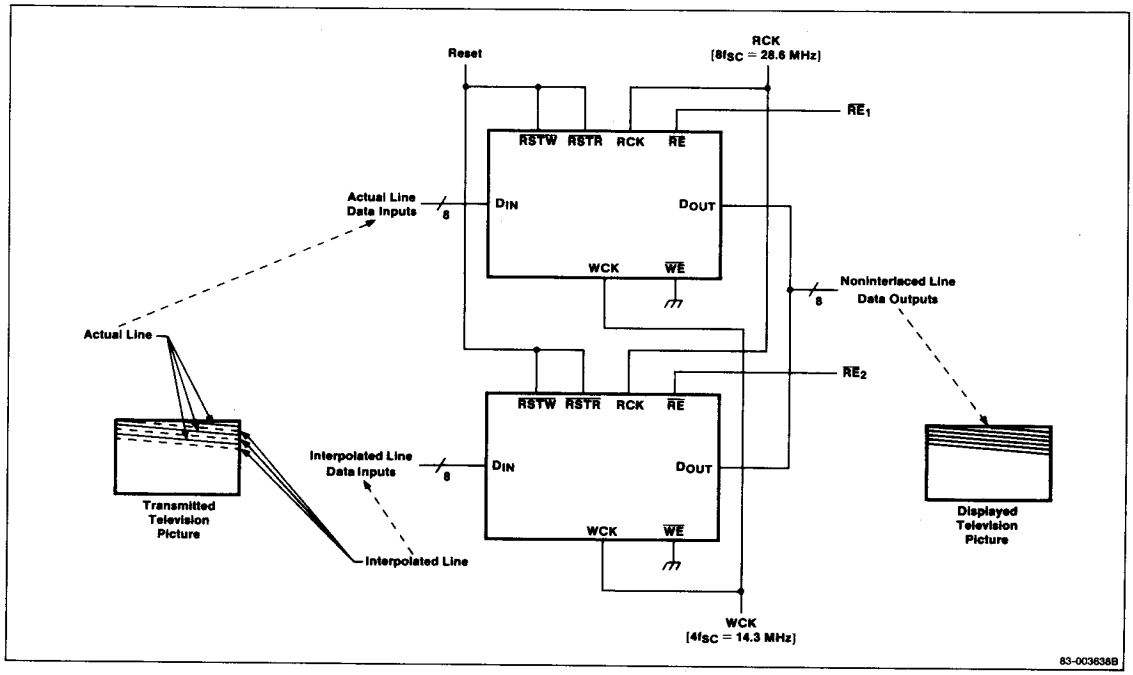


Figure 1. Connection for Noninterlaced Scan Conversion



Recommended DC Operating Conditions

T_A = −20 to +70°C; GND = 0 V

Parameter	Symbol	Limits Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.4		5.5	V
Input voltage, low	V_{IL}	−1.5		0.8	V

Capacitance

T_A = −20 to +70°C; V_{CC} = 5.0 V ±10%; f = 1 MHz

Parameter	Symbol	Limits Min	Typ	Max	Unit	Pins Under Test
Input capacitance	C_I			5	pF	$\overline{WE}$, $\overline{RE}$, WCK, RCK, $\overline{RSTW}$, $\overline{RSTR}$, D_{IN0}-D_{IN7}
Output capacitance	C_O			7	pF	D_{OUT0}-D_{OUT7}

Notes:

(1) These parameters are sampled and not 100% tested.

DC Characteristics

T_A = −20 to +70°C; V_{CC} = 5.0 V ±10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Write/read cycle operating current	I_{CC}			90	mA	
Input leakage current	I_I	−10		10	μA	V_I = 0 to V_{CC}; all other pins not under test = 0 V
Output leakage current	I_O	−10		10	μA	D_{OUT} disabled; V_O = 0 to 5.5 V
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −1 mA
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 2 mA

Notes:

(1) All voltages are referenced to ground.

AC Characteristics

$T_A = -20$ to $+70°C$; $V_{CC} = 5.0\ V \pm 10\%$

Parameter	Symbol	Limits μPD41101-3 Min	Max	μPD41101-2 Min	Max	μPD41101-1 Min	Max	Unit	Test Conditions
Write clock cycle time	t_{WCK}	34	1090	69	1090	69	1090	ns	
WCK pulse width	t_{WCW}	14		25		25		ns	
WCK precharge time	t_{WCP}	14		25		25		ns	
Read clock cycle time	t_{RCK}	34	1090	34	1090	69	1090	ns	
RCK pulse width	t_{RCW}	14		14		25		ns	
RCK precharge time	t_{RCP}	14		14		25		ns	
Access time	t_{AC}		27		27		49	ns	Figure 5
Access time after a reset cycle	t_{ACR}		27		27		49	ns	
Output hold time	t_{OH}	5		5		5		ns	
Output hold time after a reset cycle	t_{OHR}	5		5		5		ns	Figure 5 (Note 7)
Output active time	t_{LZ}	5	27	5	27	5	49	ns	(Note 4)
Output disable time	t_{HZ}	5	27	5	27	5	49	ns	
Data-in setup time	t_{DS}	14		18		18		ns	
Data-in hold time	t_{DH}	5		5		5		ns	
Reset active setup time	t_{RS}	14		14		20		ns	(Note 8)
Reset active hold time	t_{RH}	5		5		5		ns	
Reset inactive hold time	t_{RN1}	5		5		5		ns	(Note 9)
Reset inactive setup time	t_{RN2}	14		14		20		ns	
Write enable setup time	t_{WES}	14		20		20		ns	(Note 10)
Write enable hold time	t_{WEH}	5		5		5		ns	
Write enable high delay from WCK	t_{WEN1}	5		5		5		ns	(Note 11)
Write enable low delay to WCK	t_{WEN2}	14		20		20		ns	
Read enable setup time	t_{RES}	14		14		20		ns	(Note 10)
Read enable hold time	t_{REH}	5		5		5		ns	
Read enable high delay from RCK	t_{REN1}	5		5		5		ns	(Note 11)
Read enable low delay to RCK	t_{REN2}	14		14		20		ns	
Write disable pulse width	t_{WEW}	0	(Note 6)	0	(Note 6)	0	(Note 6)	ms	
Read disable pulse width	t_{REW}	0	(Note 6)	0	(Note 6)	0	(Note 6)	ms	
Write reset time	t_{RSTW}	0	(Note 6)	0	(Note 6)	0	(Note 6)	ms	
Read reset time	t_{RSTR}	0	(Note 6)	0	(Note 6)	0	(Note 6)	ms	
Transition time	t_T	3	35	3	35	3	35	ns	

Notes:

(1) All voltages are referenced to ground.

(2) Input pulse rise and fall times assume $t_T = 5$ ns. Input pulse levels = GND to 3 V. Transition times are measured between 3 V and 0 V. See figure 3.

(3) Output timing reference levels are 0.8 and 2.0 volts. See figure 4.

(4) This delay is measured at ±200 mV from the steady-state voltage with the load specified in figure 6. Under any conditions, $t_{LZ} \geq t_{HZ}$.

(5) Input timing reference levels = 1.5 V.

AC Characteristics (cont)

Notes [cont]:

(6) t_{WEW} (max) and t_{REW} (max) must be satisfied by the following equations in 1 line cycle operation:
$t_{WEW} + t_{RSTW} + 910\ (t_{WCK}) \leq 1$ ms
$t_{REW} + t_{RSTR} + 910\ (t_{RCK}) \leq 1$ ms

(7) This parameter has meaning when $t_{RCK} \geq t_{ACR}$ (max).

(8) If either t_{RS} or t_{RH} is less than the specified value, reset operations are not guaranteed.

(9) If either t_{RN1} or t_{RN2} is less than the specified value, internal reset operations may extend to cycles immediately preceding or following the period of desired reset operations.

(10) If either t_{WES} or t_{WEH} (t_{RES} or t_{REH}) is less than the specified value, write (read) disable operations are not guaranteed.

(11) If either t_{WEN1} or t_{WEN2} (t_{REN1} or t_{REN2}) is less than the specified value, internal write (read) disable operations may extend to cycles immediately preceding or following the period of desired disable operations.

Figure 2. Connection for a 1H (910-Bit) Delay Line

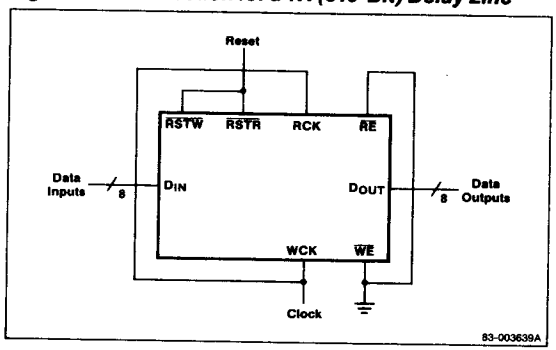


Figure 3. AC Input Timing Reference Waveform

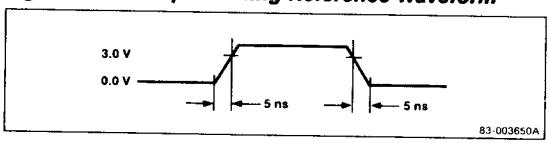


Figure 4. AC Output Timing Reference Waveform

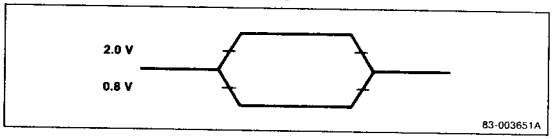


Figure 5. Output Load for t_{AC}, t_{ACR}, t_{OH}, and t_{OHR}

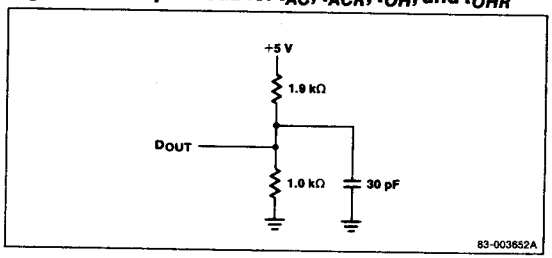
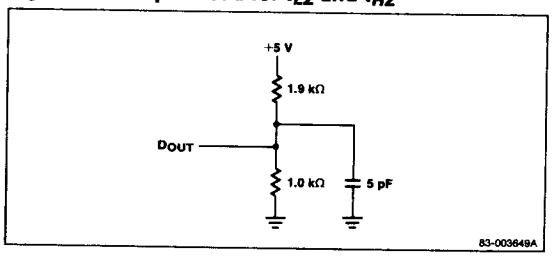
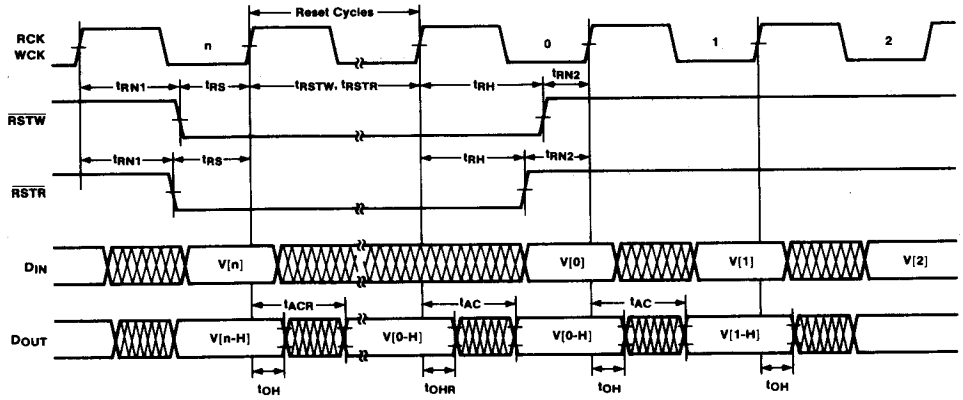


Figure 6. Output Load for t_{LZ} and t_{HZ}



Timing Waveforms

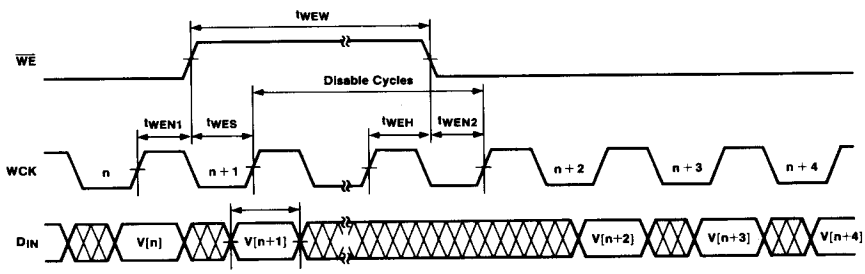
Read or Write Reset



Note:
[1] $\overline{WE} = \overline{RE} = V_{IL}$.
[2] V = Valid Data.
[3] Read operations commence from the rising edge of RCK at the beginning of a cycle. For the first cycle in a group of reset cycles, the read access time is defined as t_{ACR}. In all other cycles, t_{AC} defines the read access time.
[4] H = 910 cycles.
[5] Write data is strobed into the device on the rising edge of WCK at the end of a cycle.

83-003645B

Write Disable

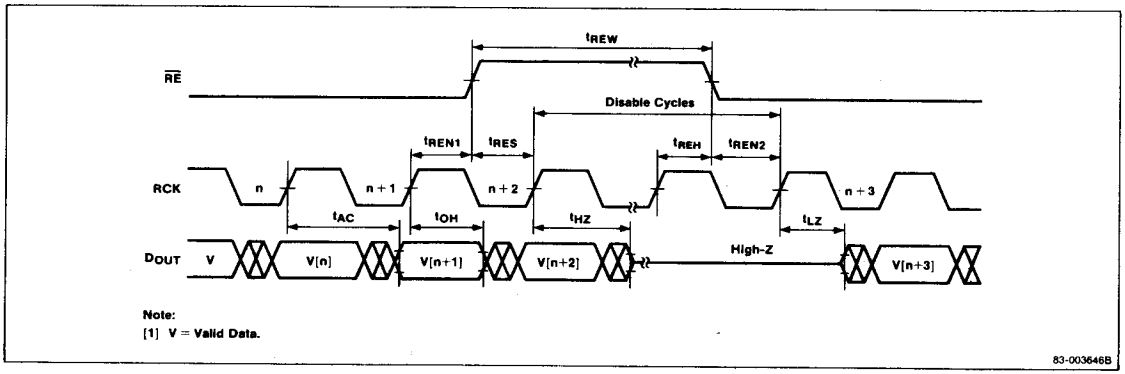


Note:
[1] V = Valid Data.

83-003723B

Timing Waveforms (cont)

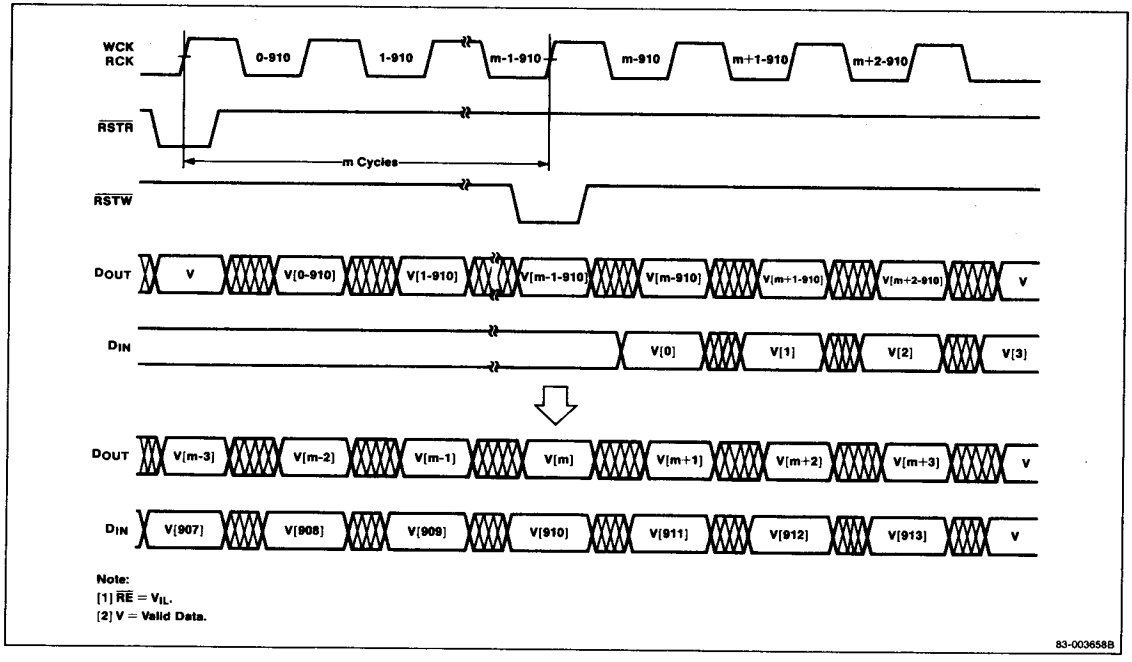
Read Disable



Note:
[1] V = Valid Data.

83-003646B

(910-m)-Bit Delay Line, No. 1

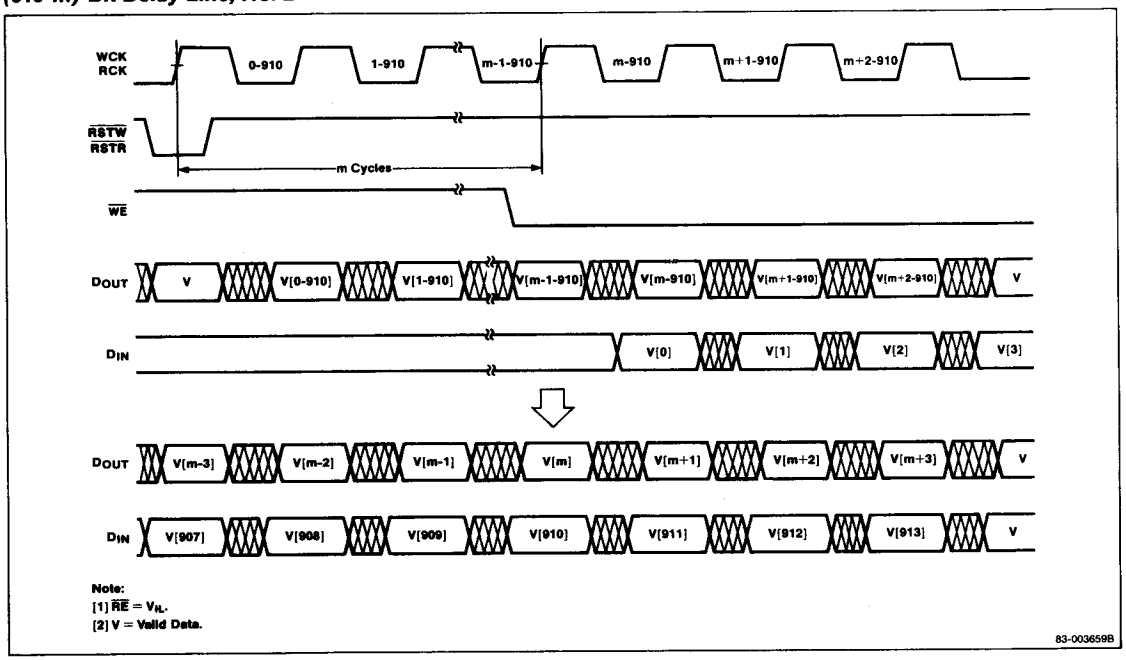


Note:
[1] $\overline{RE}$ = V_{IL}.
[2] V = Valid Data.

83-003658B

Timing Waveforms (cont)

(910-m)-Bit Delay Line, No. 2

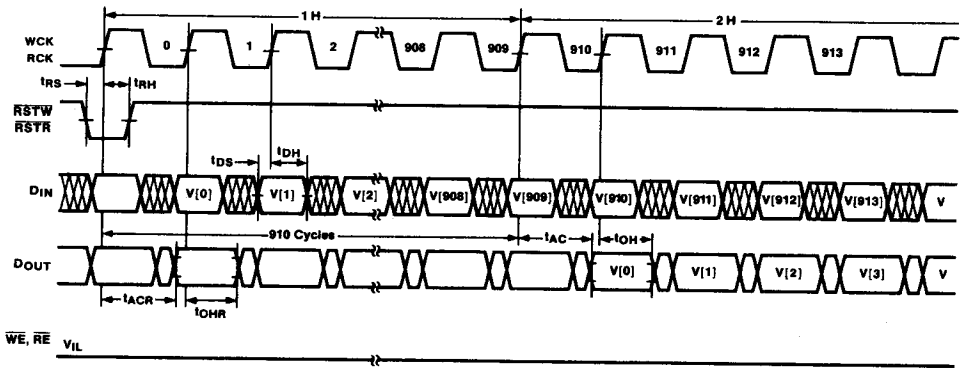


Note:
[1] $\overline{RE} = V_{IL}$.
[2] V = Valid Data.

83-003659B

Timing Waveforms (cont)

910-Bit Delay Line



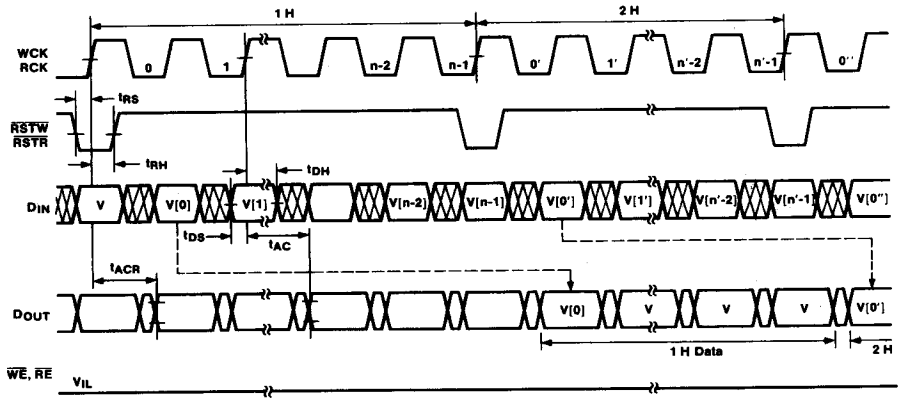
Note:
[1] V = Valid Data.
[2] 1H = the first group of 910 bits. 2H = the second group of 910 bits. See figure 2.

83-003657B

3

Timing Waveforms (cont)

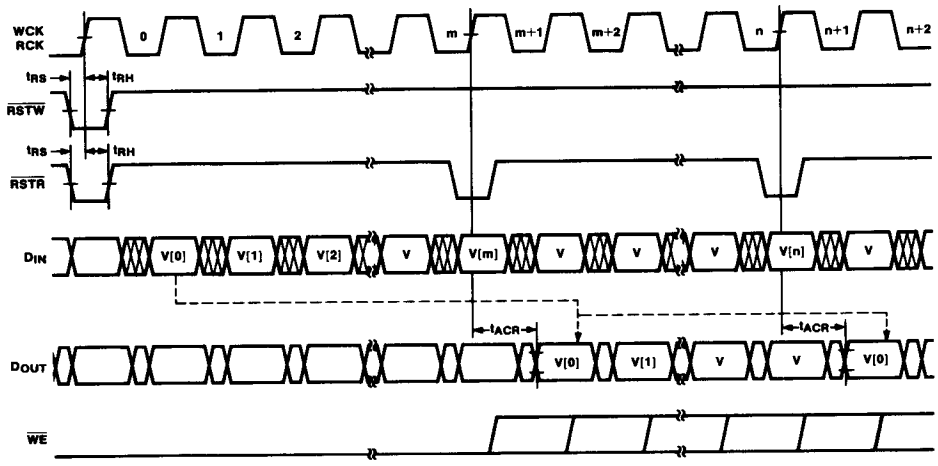
n-Bit Delay Line



Note:
[1] V = Valid Data.
[2] 1H = the first group of n bits. 2H = the second group of n'bits.

83-003643B

Re-Read Operation

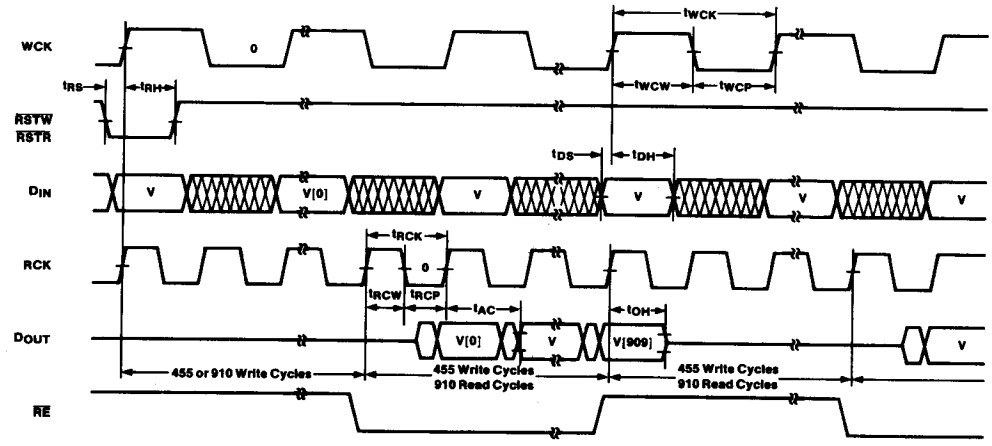


Note:
[1] $\overline{RE}$ = V_{IL}.
[2] V = Valid Data.
[3] The data stored in any location can be re-read as many times as desired within a period of 1 ms following the writing of data into that location provided that a second write operation has not re-written new data into that location.

83-003644B

Timing Waveforms (cont)

Basic Timing for Noninterlaced Scan Conversion



Note:
[1] $\overline{WE} = V_{IL}$.
[2] V = Valid Data.
[3] For compatibility with NTSC standards the WCK frequency is approximately 14.3 MHz. RCK cycles at twice this frequency, 28.6 MHz.

83-003655B

3

Timing Waveforms (cont)

Application Timing for Noninterlaced Scan Conversion