μPD41264
Dual-Port Graphics Buffer

Description

The μPD41264 is a dual-port graphics buffer equipped with a 64K x 4-bit random access port and a 256 x 4-bit serial read port. The serial read port is connected to an internal 1024-bit data register through a 256 x 4-bit serial read output circuit. The random access port is used by the host CPU to read or write data addressed in any desired order and has a write-per-bit option that allows each of the four data bits to be individually selected or masked for a write cycle.

The μPD41264 features fully asynchronous dual access, except when transferring stored graphics data from a selected row of the storage array to the data register. During a data transfer, the random access port requires a special timing cycle using a transfer clock, while the serial read port continues to operate normally. Following the clock transition of a data transfer, serial read output data changes from an old line to a new line and the starting location on the new line is addressable in the data transfer cycle.

The μPD41264 is fabricated with a double polylayer, N-channel, silicon gate process that provides high storage cell density, high performance, and high reliability. Refreshing is accomplished by means of $\overline{RAS}$-only refresh cycles or by normal read or write cycles on the 256 address combinations of A_0 through A_7 during a 4-ms period. Automatic internal refreshing, by means of either hidden refreshing or the $\overline{CAS}$ before $\overline{RAS}$ timing and on-chip refresh circuitry, is also available. The transfer of a row of data from the storage array to the data register also refreshes that row automatically.

All inputs and outputs, including clocks, are TTL-compatible. All address and data-in signals are latched on-chip to simplify system design. Data-out is unlatched to allow greater system flexibility. The μPD41264 is available in a 24-pin plastic DIP, or 24-pin plastic ZIP, and is guaranteed for operation at 0 to +70°C.

Features

- Three functional blocks
  - 64K x 4-bit random access storage array
  - 1024-bit data register
  - 256 x 4-bit serial read output circuit
- Two data ports: random access and serial read
- Dual-port accessibility except during data transfer
- Addressable start of serial read operation
- Real-time data transfer
- Single +5-volt ± 10% power supply
- On-chip substrate bias generator
- Random access port
  - Two main clocks: $\overline{RAS}$ and $\overline{CAS}$
  - Multiplexed address inputs
  - Direct connection of I/O and address lines allowed by $\overline{OE}$ to simplify system design
  - Refresh interval: 256 cycles/4 ms
  - Read, early write, late write, read-write/read-modify-write, $\overline{RAS}$-only refresh, and page mode capabilities
  - Automatic internal refreshing by means of the $\overline{CAS}$ before $\overline{RAS}$ on-chip address counter
  - Hidden refreshing by means of $\overline{CAS}$-controlled output
  - Write-per-bit capability
  - Write bit selection multiplexed on IO_0-IO_3
- $\overline{RAS}$-activated data transfer
  - Same cycle time as for random access
  - Row data transferred to data register as specified by row address inputs
  - Starting location of following serial read operation specified by column address inputs
  - Transfer of 1024 bits of data on one row to the data register, and the starting location of the serial read circuit, activated by a low-to-high transition of $\overline{DT}$
  - Data transfer during real-time operation or standby of serial port
- Fast serial read operation by means of SC pins
  - Serial data presented on SO_0-SO_3
  - Direct connection of multiple serial outputs for extension of data length
- Fully TTL-compatible inputs, outputs, and clocks
- Three-state outputs for random and serial access
- 24-pin plastic DIP and 24-pin plastic ZIP packaging

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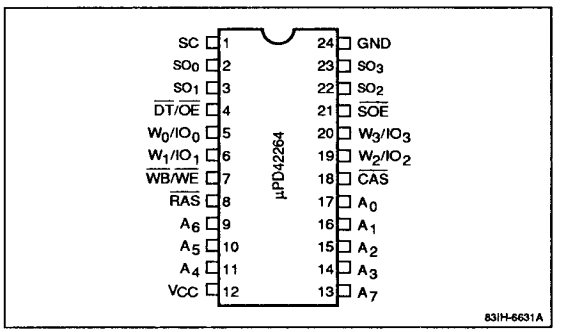
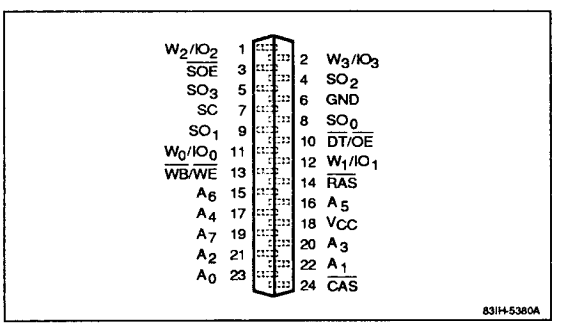
Pin Configurations

24-Pin Plastic DIP and SOJ



24-Pin Plastic ZIP



Ordering Information

Part Number	Row Access Time (max)	Serial Access Time (max)	Package
μPD41264C-12	120 ns	40 ns	24-pin plastic DIP
C-15	150 ns	60 ns	
μPD41264V-12	120 ns	40 ns	24-pin plastic ZIP
V-15	150 ns	60 ns	

Pin Identification

Symbol	Function
A_0 - A_7	Address inputs
$\overline{CAS}$	Column address strobe
$\overline{DT/OE}$	Data transfer/output enable
$\overline{RAS}$	Row address strobe
SC	Serial control
SO_0 - SO_3	Serial read outputs
$\overline{SOE}$	Serial output enable
W_0/IO_0 - W_3/IO_3	Write-per-bit inputs/data inputs and outputs
GND	Ground
$\overline{WB/WE}$	Write-per-bit/write enable
V_{CC}	+5-volt power supply

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.4		5.5	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Operating temperature	T_A	0		70	°C

Absolute Maximum Ratings

Voltage on any pin except V_{CC} relative to GND, V_{R1}	−1.0 to +7.0 V
Voltage on V_{CC} relative to GND, V_{R2}	−1.0 V to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.5 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	$C_{I(A)}$	5	pF	A_0 - A_7
	$C_{I(\overline{DT}/\overline{OE})}$	6	pF	$\overline{DT}/\overline{OE}$
	$C_{I(\overline{WB}/\overline{WE})}$	8	pF	$\overline{WB}/\overline{WE}$
	$C_{I(\overline{RAS})}$	8	pF	$\overline{RAS}$
	$C_{I(\overline{CAS})}$	8	pF	$\overline{CAS}$
	$C_{I(\overline{SOE})}$	8	pF	$\overline{SOE}$
	$C_{I(SC)}$	8	pF	SC
Input/output capacitance	$C_{IO(W/IO)}$	7	pF	W_0/IO_0 - W_3/IO_3
Output capacitance	$C_{O(SO)}$	7	pF	SO_0 - SO_3

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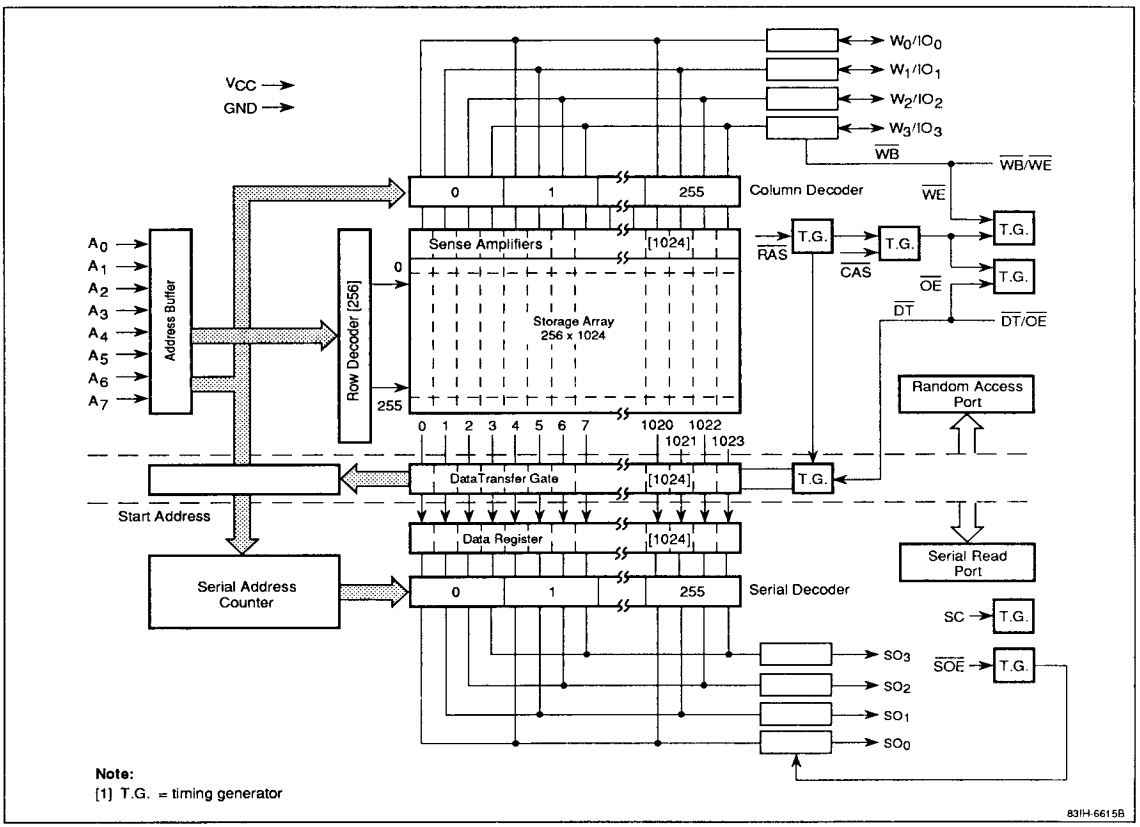
Block Diagram



Device Operation

The μPD41264 has a random access port and a serial read port. The random access port executes standard read/write cycles as well as data transfer cycles, all of which are based on conventional $\overline{RAS}$/$\overline{CAS}$ timing. In a data transfer, data in each storage cell on the selected row is transferred simultaneously through a transfer gate to the corresponding register location. The serial read port shows the contents of the data register in serial order. The random access and serial read ports can operate asynchronously, except when the transfer gate is turned on during the data transfer period.

Addressing

The storage array is a 256-row by 1024-column matrix. Each of 4 data bits in the random access port corresponds to 65,536 storage cells, and 16 address bits are required to decode one cell location. Eight row address bits are set up on pins A_0 through A_7 and latched onto the chip by $\overline{RAS}$. Eight column address bits then are set up on pins A_0 through A_7 and latched onto the chip by $\overline{CAS}$. All addresses must be stable, on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$.

$\overline{RAS}$ is similar to a chip enable signal; whenever it is activated, 1024 cells on the selected row are sensed simultaneously and the sense amplifiers automatically restore the data. $\overline{CAS}$ is a chip selection signal that activates the column decoder and input/output buffers.

Through 1 of 256 column decoders, 4 storage cells on a row are connected to 4 data buses, respectively. In a data transfer cycle, 8 row address bits are used to select 1 of the 256 possible rows involved in the transfer of data to the data register. Eight column address bits are then used to select the 1 of 256 possible serial decoders that corresponds to the starting location of the next serial read cycle. In the serial read port, when SC is activated, 4 data bits in the 1024-bit data register are transferred to 4 serial data buses and read out. Activating SC repeatedly causes a serial read cycle (starting from the location specified in the data transfer) to be executed within the 1024 bits in the data register.

Random Access Port

An operation in the random access port begins with a negative transition of $\overline{RAS}$. Both $\overline{RAS}$ and $\overline{CAS}$ have minimum pulse widths, as specified in the timing table, which must be maintained for proper device operation and data integrity. Once begun, a cycle must meet all specifications, including minimum cycle time. To reduce the number of pins, the following functions are multi-plexed in the random access port:

- $\overline{DT}/\overline{OE}$
- $\overline{WB}/\overline{WE}$
- W_i/IO_i (i = 0, 1, 2, 3)

The $\overline{OE}$, $\overline{WE}$ and IO_i functions represent standard operations while $\overline{DT}$, $\overline{WB}$, and W_i are special inputs to be applied in the same way as row address inputs, with setup and hold times referenced to the negative transition of $\overline{RAS}$. The $\overline{DT}$ level determines whether a cycle is a random access operation or a data transfer operation. $\overline{WB}$ affects only write cycles and determines whether or not the write-per-bit option is used. W_i defines data bits to be written with the write-per-bit capability. In the following discussions, these multiplexed pins are designated as $\overline{DT}(/\overline{OE})$, for example, depending on the function being described.

To use the μPD41264 for random access, $\overline{DT}(/\overline{OE})$ must be high as $\overline{RAS}$ falls. Holding $\overline{DT}(/\overline{OE})$ high disconnects the 1024-bit data register from the corresponding 1024-digit lines of the storage array. Conversely, to execute a data transfer, $\overline{DT}(/\overline{OE})$ must be low as $\overline{RAS}$ falls to open the 1024 data transfer gates and transfer data from one of the rows to the data register.

Read Cycle. A read cycle is executed by activating $\overline{RAS}$, $\overline{CAS}$, and $\overline{OE}$ and maintaining $(\overline{WB}/)\overline{WE}$ high while $\overline{CAS}$ is active. The $(W_i/)IO_i$ data pin (i = 0, 1, 2, 3) remains in high impedance until valid data appears at the output at access time. Device access time, t_{ACC}, is the longest of the following three calculated intervals:

- t_{RAC}
- $\overline{RAS}$ to $\overline{CAS}$ delay (t_{RCD}) + t_{CAC}
- $\overline{RAS}$ to $\overline{OE}$ delay + t_{OEA}

Access times from $\overline{RAS}$ (t_{RAC}), from $\overline{CAS}$ (t_{CAC}), and from $\overline{OE}$ (t_{OEA}) are device parameters. The $\overline{RAS}$ to $\overline{CAS}$ and $\overline{RAS}$ to $\overline{OE}$ delays are system-dependent timing parameters.

Output becomes valid after the access time has elapsed and it remains valid while both $\overline{CAS}$ and $\overline{OE}$ are low. $\overline{CAS}$ or $\overline{OE}$ high returns the output to high impedance.

Write Cycle. A write cycle is executed by bringing ($\overline{WB}$/)$\overline{WE}$ low during the $\overline{RAS}$/$\overline{CAS}$ cycle. The falling edge of $\overline{CAS}$ or ($\overline{WB}$/)$\overline{WE}$ strobes the data on (W_i/)IO_i into the on-chip data latch. To make use of the write-per-bit capability, $\overline{WB}$(/$\overline{WE}$) must be low as $\overline{RAS}$ falls. In this case, data bits targeted for write operation can be specified by keeping W_i(/IO_i) high, with setup and hold times referenced to the negative transition of $\overline{RAS}$.

For those data bits of W_i(/IO_i) that are kept low as $\overline{RAS}$ falls, write operation is inhibited on the chip. If $\overline{WB}$(/$\overline{WE}$) is high as $\overline{RAS}$ falls, the write-per-bit option is not used and a write cycle is executed for all four data bits.

Early Write Cycle. An early write cycle is executed by bringing ($\overline{WB}$/)$\overline{WE}$ low before $\overline{CAS}$. Data is strobed by $\overline{CAS}$, with setup and hold times referenced to this signal, and the output remains in high impedance for the entire cycle. As $\overline{RAS}$ falls, ($\overline{DT}$/)$\overline{OE}$ must meet the setup and hold times of a high $\overline{DT}$, but otherwise ($\overline{DT}$/)$\overline{OE}$ does not affect any circuit operation while $\overline{CAS}$ is active.

Read-Write/Read-Modify-Write Cycle. Bringing the ($\overline{WB}$/)$\overline{WE}$ signal low with $\overline{RAS}$ and $\overline{CAS}$ low executes this cycle. (W_i/)IO_i shows read data at access time. Afterward, in preparation for the upcoming write cycle, (W_i/)IO_i is returned to high impedance by a high ($\overline{DT}$/)$\overline{OE}$. The data to be written is strobed by ($\overline{WB}$/)$\overline{WE}$, with setup and hold times referenced to this signal.

Late Write Cycle. This cycle shows the timing flexibility of ($\overline{DT}$/)$\overline{OE}$, which can be activated just after ($\overline{WB}$/)$\overline{WE}$ falls, even when ($\overline{WB}$/)$\overline{WE}$ is brought low after $\overline{CAS}$.

Refresh Cycle. A cycle at each of the 256 row addresses (A_0 through A_7) will refresh all storage cells. Any cycle in the random access port (i.e., read, write, refresh, or data transfer) refreshes the 1024 bits selected by the $\overline{RAS}$ addresses or by the on-chip refresh address counter.

$\overline{RAS}$-only Refresh Cycle. A cycle having only $\overline{RAS}$ active refreshes one row of the storage array. A high $\overline{CAS}$ is maintained while $\overline{RAS}$ is active to keep (W_i/)IO_i in a state of high impedance. This cycle is preferred for refreshing, especially when the host system consists of multiple rows of random access devices. The data outputs may be OR-tied with no bus contention when $\overline{RAS}$-only refresh cycles are executed.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle. This cycle executes internal refreshing using the on-chip control circuitry. Whenever $\overline{CAS}$ is low as $\overline{RAS}$ falls, this circuitry automatically refreshes the row addresses specified by the internal address counter. In this cycle, the circuit operation based on $\overline{CAS}$ is maintained in a reset state. When internal refreshing is complete, the address counter automatically increments in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ cycle.

Hidden Refresh Cycle. This function performs hidden refreshing after a read cycle, without disturbing the read data output. Once valid, the data output is controlled by $\overline{CAS}$ and $\overline{OE}$. After the read cycle, $\overline{CAS}$ is held low while $\overline{RAS}$ goes high for precharging. A $\overline{RAS}$-only cycle is then executed (except that $\overline{CAS}$ is held low instead of high) and the data output remains valid. Since hidden refreshing is the same as $\overline{CAS}$ before $\overline{RAS}$ refreshing, the data output remains valid during either operation.

Fast-Page Cycle. This feature allows faster data access by keeping the same row address while successive column addresses are strobed onto the chip. By maintaining $\overline{RAS}$ low while successive $\overline{CAS}$ cycles are executed, data is transferred at a faster rate because $\overline{RAS}$ addresses are maintained internally and do not have to be reapplied. During this operation, it is also possible to execute read, write and read-write/read-modify-write cycles. Additionally, the write-per-bit control specified in the entry write cycle is maintained through the following fast-page write cycle.

Data Transfer Cycle. A data transfer cycle is executed by bringing $\overline{DT}(/\overline{OE})$ low as $\overline{RAS}$ falls. The specified 1 of the possible 256 rows involved in the data transfer, aswell as the starting location of the following serial read cycle in the serial read port, are defined by address inputs. $\overline{DT}(/\overline{OE})$ must be low for a specified time, measured from $\overline{RAS}$ and $\overline{CAS}$, so that the data transfer condition may be satisfied . The low-to-high transition of $\overline{DT}$ causes two transfer operations through the data transfer gates: column address buffer outputs are transferred to the serial address counters, and storage cell data amplified on digit lines is transferred to the data register. At least one SC cycle is required to hold the data in the register. Otherwise, the beginning of the next transfer cycle destroys the newly transferred data. $\overline{RAS}$ and $\overline{CAS}$ must be low during these operations to keep the transferred data in the random access port.

Serial Read Port

The serial read port is used only to read serially the contents of the data register starting from a specified location. The entire operation, therefore, follows a data transfer cycle. Data stored in the serial register remains valid for a minimum of 4 ms after the transfer cycle. The only condition under which the serial read port must synchronize with the random access port is when the positive transition of $\overline{DT}(/\overline{OE})$ must occur within a specified period in an SC cycle. Except for this SC cycle, the serial read port can operate asynchronously with the random access port. The output data appears at SO_i after an access time of t_{SCA}, measured from SC high, only when $\overline{SOE}$ is maintained low. The SC cycle that includes the positive transition of $\overline{DT}(/\overline{OE})$ shows old data in the data register; subsequent SC cycles show new data transferred to the data register serially and in a looped manner. The serial output is maintained until the next SC signal is activated. $\overline{SOE}$ controls the impedance of the serial output to allow multiplexing of more than one bank of μPD41264 graphics buffers into the same external circuitry. When $\overline{SOE}$ is low, SO_i is enabled and the proper data is read. When $\overline{SOE}$ is at a high logic level, SO_i is disabled and in a state of high impedance.

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DC Characteristics

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{IL}	−10		10	μA	V_{IN} = 0 to 5.5 V; all other pins not under test = 0 V
Output leakage current	I_{OL}	−10		10	μA	D_{OUT} (IO_i, SO_i) disabled; V_{OUT} = 0 to 5.5 V
Random access port output voltage, high	$V_{OH(R)}$	2.4			V	$I_{OH(R)}$ = −2 mA
Random access port output voltage, low	$V_{OL(R)}$			0.4	V	$I_{OL(R)}$ = 4.2 mA
Serial read port output voltage, high	$V_{OH(S)}$	2.4			V	$I_{OH(S)}$ = −2 mA
Serial read port output voltage, low	$V_{OL(S)}$			0.4	V	$I_{OL(S)}$ = 4.2 mA

Power Supply Current

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Random Access Port	Serial Read Port	Symbol	−12 Max	−15 Max	Unit	Test Conditions
Read/write cycle	Standby	I_{CC1}	95	85	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; t_{RC} = t_{RC} min; IO = 0 mA; SC = $\overline{SOE}$ = V_{IH} (Note 1)
Standby	Standby	I_{CC2}	12	12	mA	$\overline{RAS}$ = V_{IH}; D_{OUT} = high impedance; SC = $\overline{SOE}$ = V_{IH}
$\overline{RAS}$-only refresh cycle	Standby	I_{CC3}	75	65	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ = V_{IH}; t_{RC} = t_{RC} min; SC = $\overline{SOE}$ = V_{IH}
Page cycle	Standby	I_{CC4}	65	55	mA	$\overline{RAS}$ = V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; SC = $\overline{SOE}$ = V_{IH} (Note 1)
$\overline{CAS}$ before $\overline{RAS}$ refresh cycle	Standby	I_{CC5}	75	65	mA	$\overline{CAS}$ low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; SC = $\overline{SOE}$ = V_{IH} (Note 1)
Data transfer	Standby	I_{CC6}	120	100	mA	$\overline{DT}$ low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; SC = $\overline{SOE}$ = V_{IH}
Read/write cycle	Active	I_{CC7}	155	130	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; t_{RC} = t_{RC} min; $\overline{SOE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min (Note 1)
Standby	Active	I_{CC8}	60	45	mA	$\overline{RAS}$ = V_{IH}; D_{OUT} = high impedance; $\overline{SOE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min (Note 1)
$\overline{RAS}$-only refresh cycle	Active	I_{CC9}	135	110	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ = V_{IH}; t_{RC} = t_{RC} min; $\overline{SOE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min (Note 1)
Page cycle	Active	I_{CC10}	125	100	mA	$\overline{RAS}$ = V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; $\overline{SOE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min (Note 1)
$\overline{CAS}$ before $\overline{RAS}$ refresh cycle	Active	I_{CC11}	135	110	mA	$\overline{CAS}$ low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SOE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min (Note 1)
Data transfer	Active	I_{CC12}	180	145	mA	$\overline{DT}$ low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SOE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min (Note 1)

Notes:

(1) No load on IO_i or SO_i. Except for I_{CC2}, I_{CC3}, and I_{CC6}, real values depend on output loading and cycle rates.

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V±10%

Parameter	Symbol	μPD41264-12 Min	μPD41264-12 Max	μPD41264-15 Min	μPD41264-15 Max	Unit	Test Conditions
Column address hold time after $\overline{RAS}$ low	t_{AR}	80		100		ns	
Column address setup time	t_{ASC}	0		0		ns	
Row address setup time	t_{ASR}	0		0		ns	
Access time from $\overline{CAS}$	t_{CAC}		60		75	ns	(Notes 2, 5)
Column address hold time	t_{CAH}	20		25		ns	
$\overline{CAS}$ pulse width	t_{CAS}	60	10,000	75	10,000	ns	

AC Characteristics (cont)

Parameter	Symbol	μPD41264-12 Min	μPD41264-12 Max	μPD41264-15 Min	μPD41264-15 Max	Unit	Test Conditions
$\overline{DT}$ low hold time after $\overline{RAS}$ low	t_{CDH}	40		55		ns	(Note 12)
$\overline{CAS}$ before $\overline{RAS}$ refresh hold time	t_{CHR}	25		30		ns	
$\overline{CAS}$ precharge time (page cycle only)	t_{CP}	50		60		ns	
$\overline{CAS}$ precharge time (nonpage cycle)	t_{CPN}	25		30		ns	
$\overline{CAS}$ high to $\overline{RAS}$ low precharge time	t_{CRP}	10		10		ns	
$\overline{CAS}$ hold time	t_{CSH}	120		150		ns	
$\overline{CAS}$ before $\overline{RAS}$ refresh setup time	t_{CSR}	10		10		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	100		120		ns	(Note 10)
Write command to $\overline{CAS}$ lead time	t_{CWL}	40		45		ns	
Data-in hold time	t_{DH}	35		45		ns	(Note 11)
$\overline{DT}$ high hold time	t_{DHH}	20		25		ns	
Data-in hold time after $\overline{RAS}$ low	t_{DHR}	95		120		ns	
$\overline{DT}$ high setup time	t_{DHS}	0		0		ns	
$\overline{DT}$ low setup time	t_{DLS}	0		0		ns	
Data-in setup time	t_{DS}	0		0		ns	(Note 11)
$\overline{DT}$ high to $\overline{CAS}$ high delay	t_{DTC}	10		10		ns	
$\overline{DT}$ high hold time after $\overline{RAS}$ high	t_{DTH}	20		25		ns	
$\overline{DT}$ high to $\overline{RAS}$ high delay	t_{DTR}	10		10		ns	
$\overline{OE}$ pulse width	t_{OE}	35		40		ns	
Access time from $\overline{OE}$	t_{OEA}		30		40	ns	(Note 2)
$\overline{OE}$ to data-in setup delay	t_{OED}	35		40		ns	
$\overline{OE}$ hold time after $\overline{WE}$ low	t_{OEH}	30		40		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	10		10		ns	
Output disable time from $\overline{OE}$ high	t_{OEZ}	0	30	0	40	ns	(Note 6)
Output disable time from $\overline{CAS}$ high	t_{OFF}	0	30	0	40	ns	(Note 6)
Page cycle time	t_{PC}	120		145		ns	
Access time from $\overline{RAS}$	t_{RAC}		120		150	ns	(Notes 2, 4)
Row address hold time	t_{RAH}	15		20		ns	
$\overline{RAS}$ pulse width	t_{RAS}	120	10,000	150	10,000	ns	
Random read or write cycle time	t_{RC}	220		270		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	60	30	75	ns	(Note 4)
Read command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns	(Note 9)
Read command setup time	t_{RCS}	0		0		ns	
$\overline{DT}$ low hold time after $\overline{RAS}$ low (serial port active)	t_{RDH}	100		130		ns	
Refresh interval	t_{REF}		4		4	ms	
$\overline{RAS}$ precharge time	t_{RP}	90		100		ns	
$\overline{RAS}$ high to $\overline{CAS}$ low precharge time	t_{RPC}	0		0		ns	
Read command hold after $\overline{RAS}$ high	t_{RRH}	20		20		ns	(Note 9)
$\overline{RAS}$ hold time	t_{RSH}	60		75		ns	

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AC Characteristics (cont)

Parameter	Symbol	μPD41264-12 Min	μPD41264-12 Max	μPD41264-15 Min	μPD41264-15 Max	Unit	Test Conditions
Read-write/read-modify-write cycle time	t_{RWC}	300		355		ns	
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	160		195		ns	(Note 10)
Write command to $\overline{RAS}$ lead time	t_{RWL}	40		45		ns	
SC pulse width	t_{SCH}	10		20		ns	
Serial output access time from SC	t_{SCA}		40		60	ns	(Notes 2, 7)
Serial clock cycle time	t_{SCC}	40	50,000	60	50,000	ns	
SC precharge time	t_{SCL}	10		20		ns	
SC high to $\overline{DT}$ high delay	t_{SDD}	10		20		ns	
SC low hold time after $\overline{DT}$ high	t_{SDH}	10		20		ns	
Serial output access time from $\overline{SOE}$	t_{SOA}		35		50	ns	
$\overline{SOE}$ pulse width	t_{SOE}	15		20		ns	
Serial output hold time after SC high	t_{SOH}	10		10		ns	
$\overline{SOE}$ low to serial output setup delay	t_{SOO}	5		5		ns	
$\overline{SOE}$ precharge time	t_{SOP}	15		20		ns	
Serial output disable time from $\overline{SOE}$ high	t_{SOZ}	0	30	0	40	ns	(Note 6)
Rise and fall transition time	t_T	3	50	3	50	ns	
Write-per-bit hold time	t_{WBH}	20		25		ns	
Write-per-bit setup time	t_{WBS}	0		0		ns	
Write command hold time	t_{WCH}	35		45		ns	
Write command hold time after $\overline{RAS}$ low	t_{WCR}	95		120		ns	
Write command setup time	t_{WCS}	0		0		ns	(Note 10)
Write bit selection hold time	t_{WH}	20		25		ns	
Write command pulse width	t_{WP}	35		45		ns	
Write bit selection setup time	t_{WS}	0		0		ns	

Notes:

(1) See input/output timing waveforms for timing reference voltages.

(2) See figures 1 and 2 for output loads.

(3) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles (except $\overline{CAS}$-before-$\overline{RAS}$ cycles), before proper device operation is achieved.

(4) Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. The t_{RCD} (max) limit is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC}.

(5) Assumes that $t_{RCD} \geq t_{RCD}$ (max).

(6) An output disable time defines the time at which the output achieves the open-circuit condition and is not referenced to output voltage levels.

(7) Data in the serial output register remains valid for 4 ms (min) after a data transfer cycle.

(8) V_{IH} (min) and V_{IL} (min) are reference levels for measuring the timing of input signals. Additionally, transition times are measured between V_{IH} and V_{IL}.

(9) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(10) t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in read-write and read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(11) These parameters are referenced to the falling edge of $\overline{CAS}$ in early write cycles and to the falling edge of (WB/)$\overline{WE}$ in delayed write or read-modify-write cycles.

(12) Use t_{RDH} and t_{CDH} when the serial port is active and t_{RDH1}, t_{RSD}, t_{CSD} and t_{SSC} if it is in standby.

(13) $\overline{SOE}$ may be tied to GND if the output enable function of the serial port is not needed.

Figure 1. Input Timing

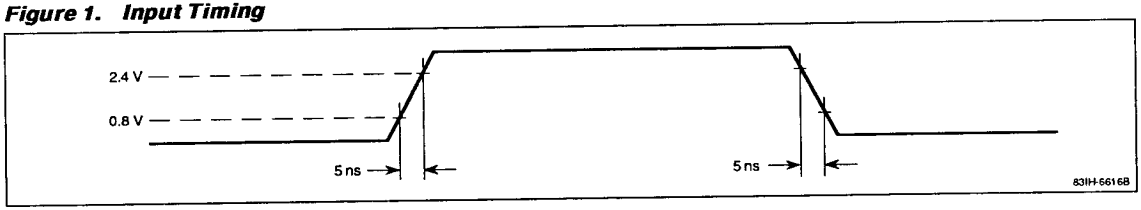

Figure 2. Output Timing

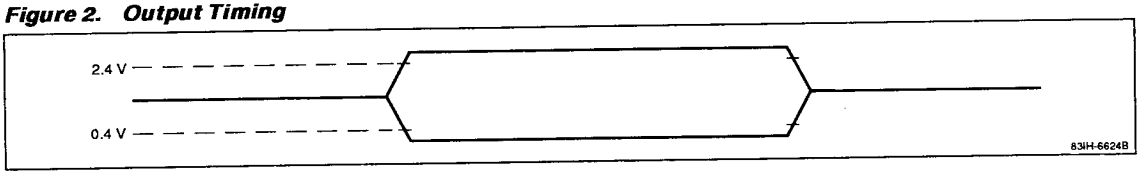

Figure 3. Output Loading in Random Access Port

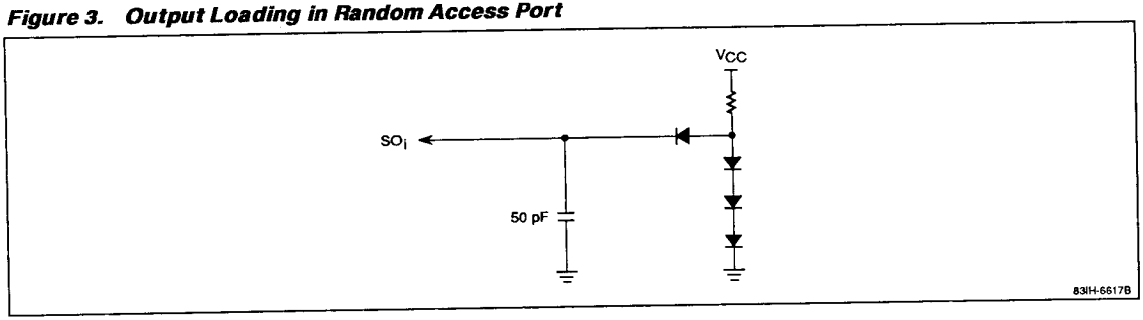

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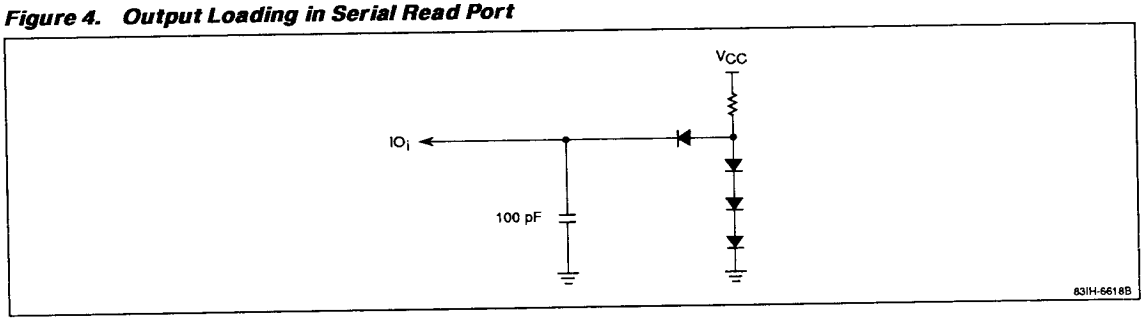
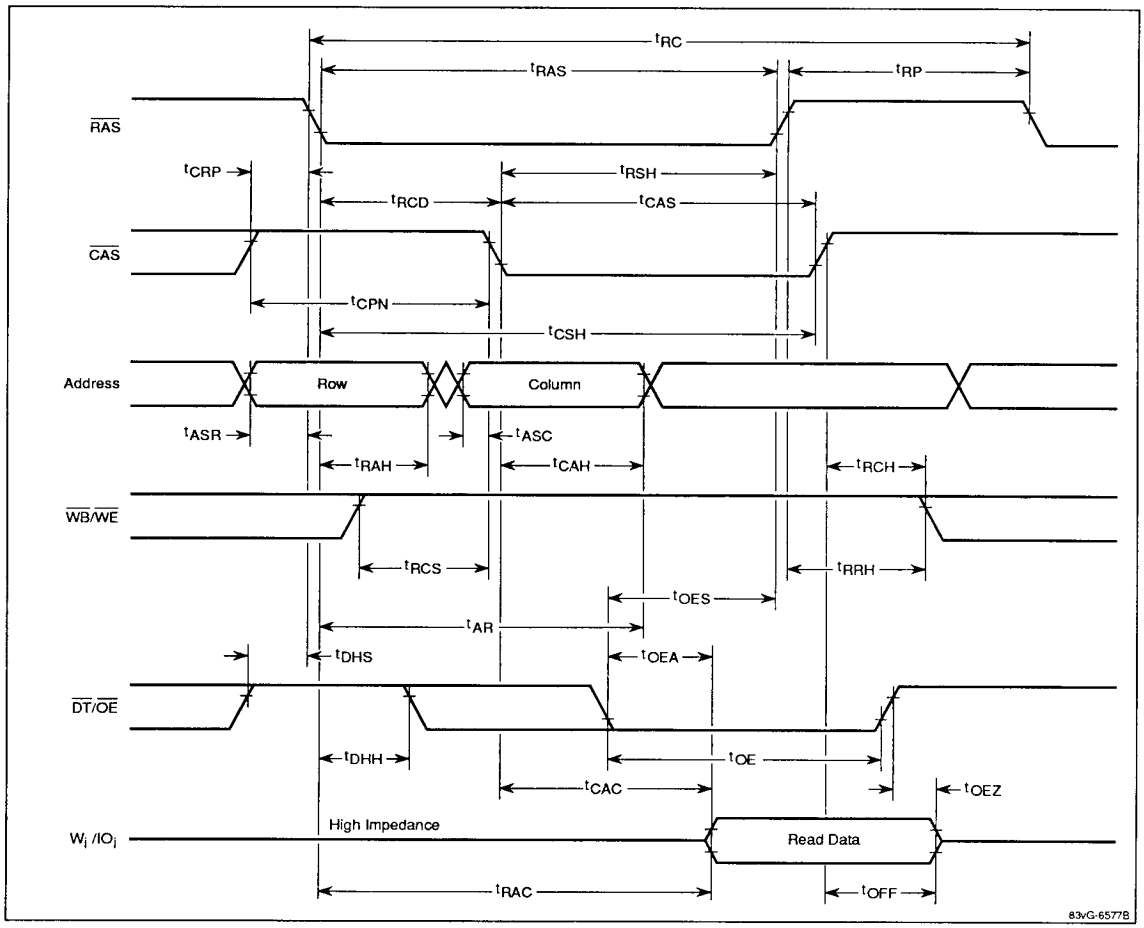
Figure 4. Output Loading in Serial Read Port



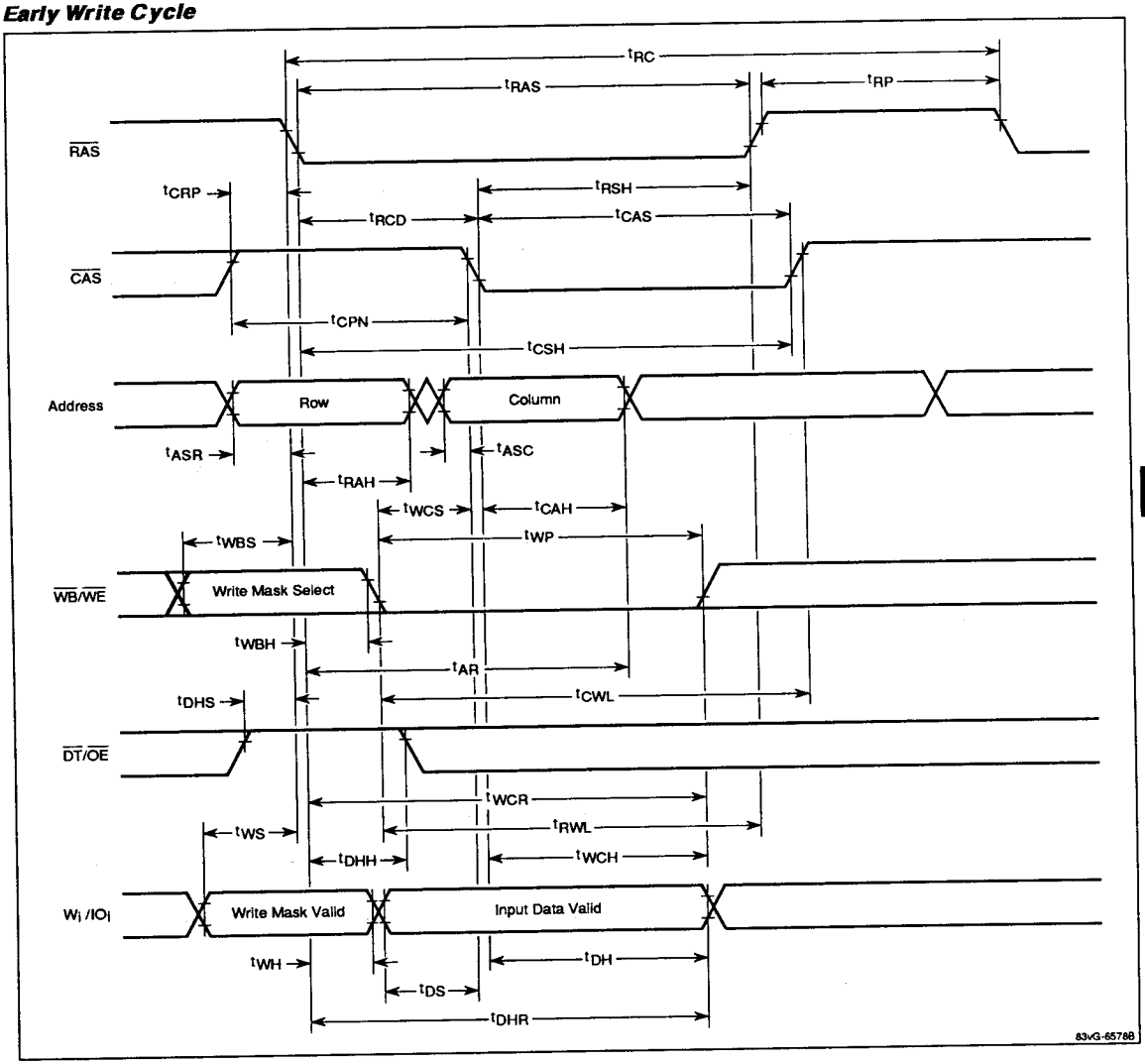
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

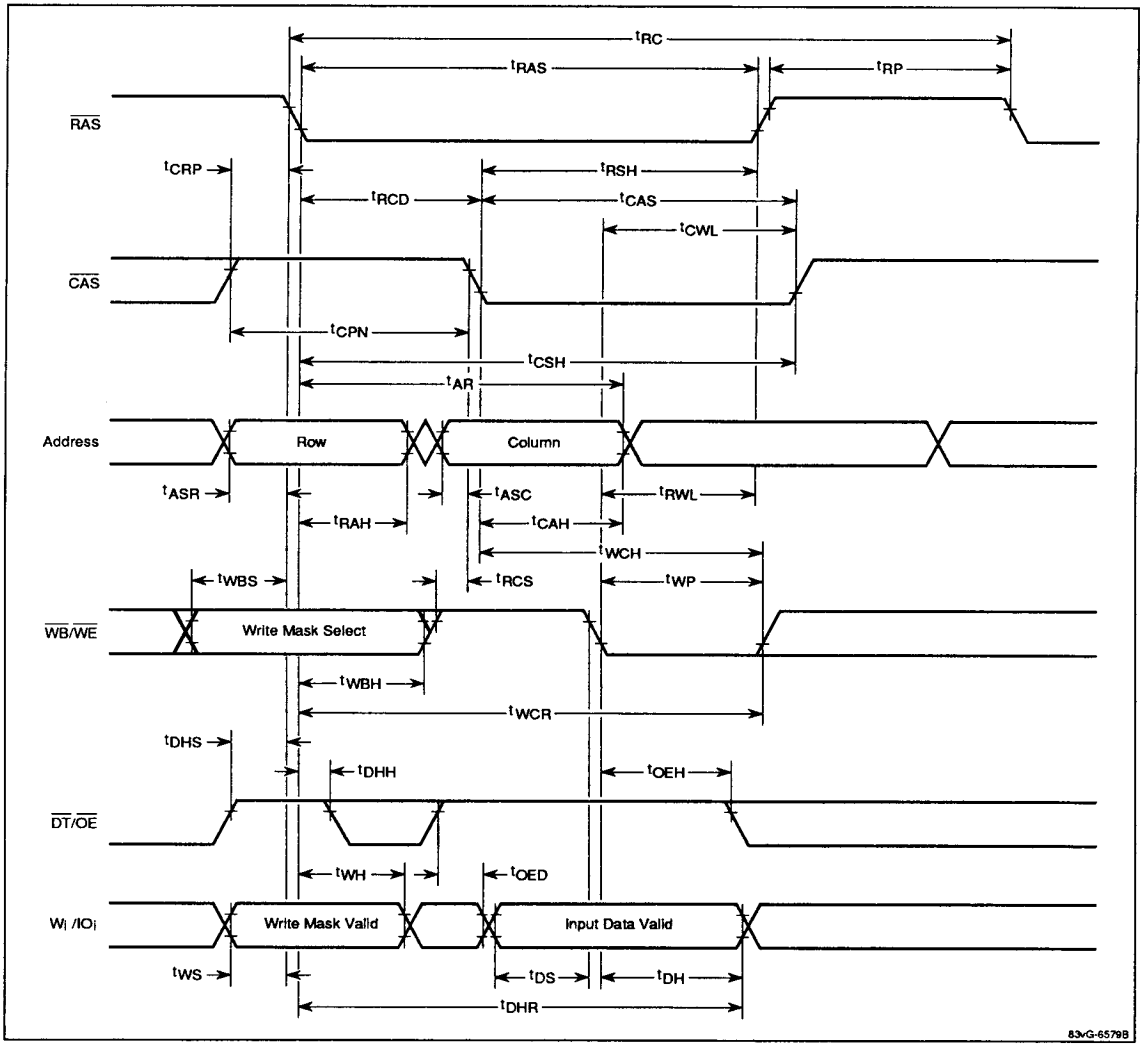
Early Write Cycle



12a

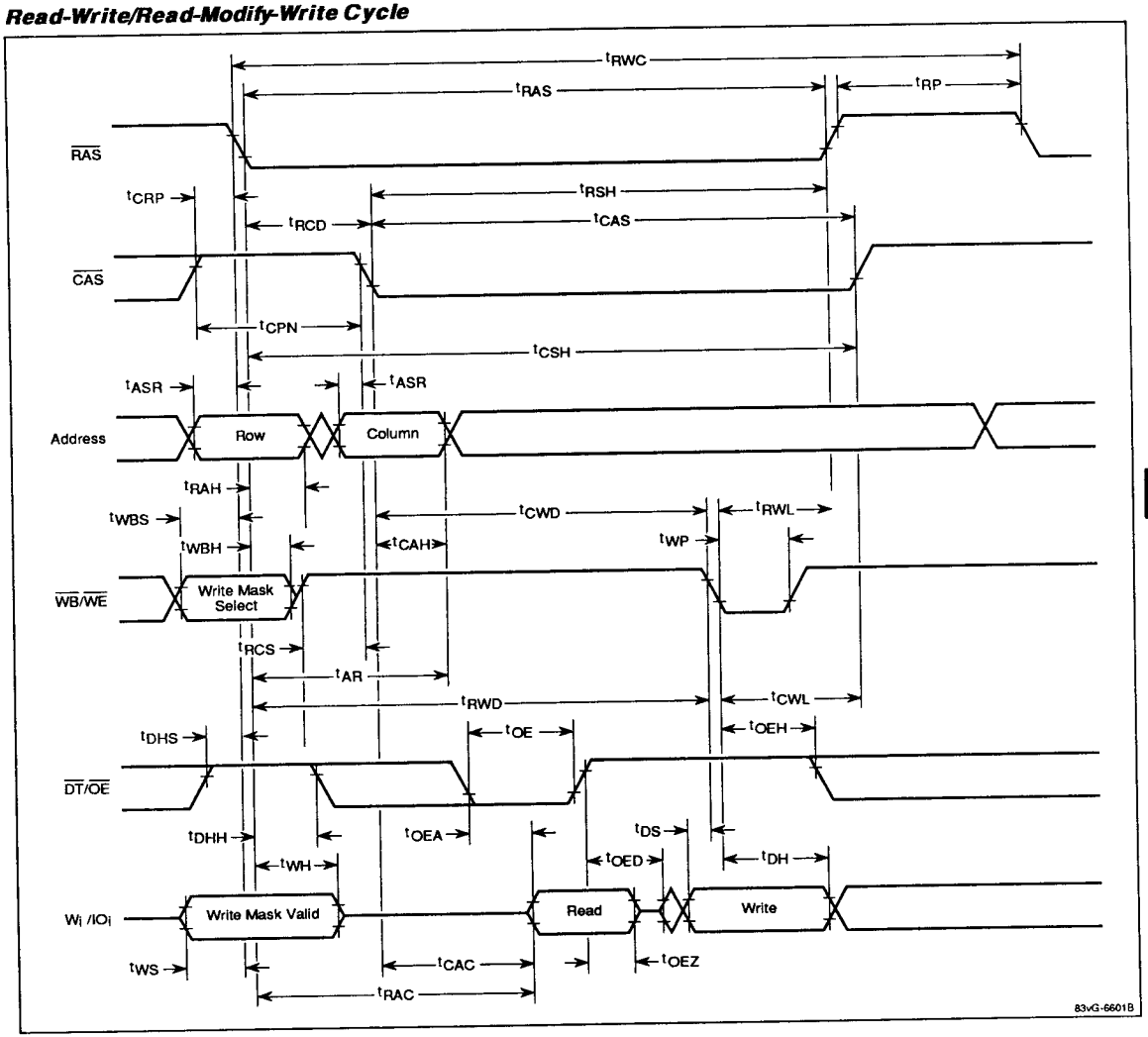
Timing Waveforms (cont)

Late Write Cycle



Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle



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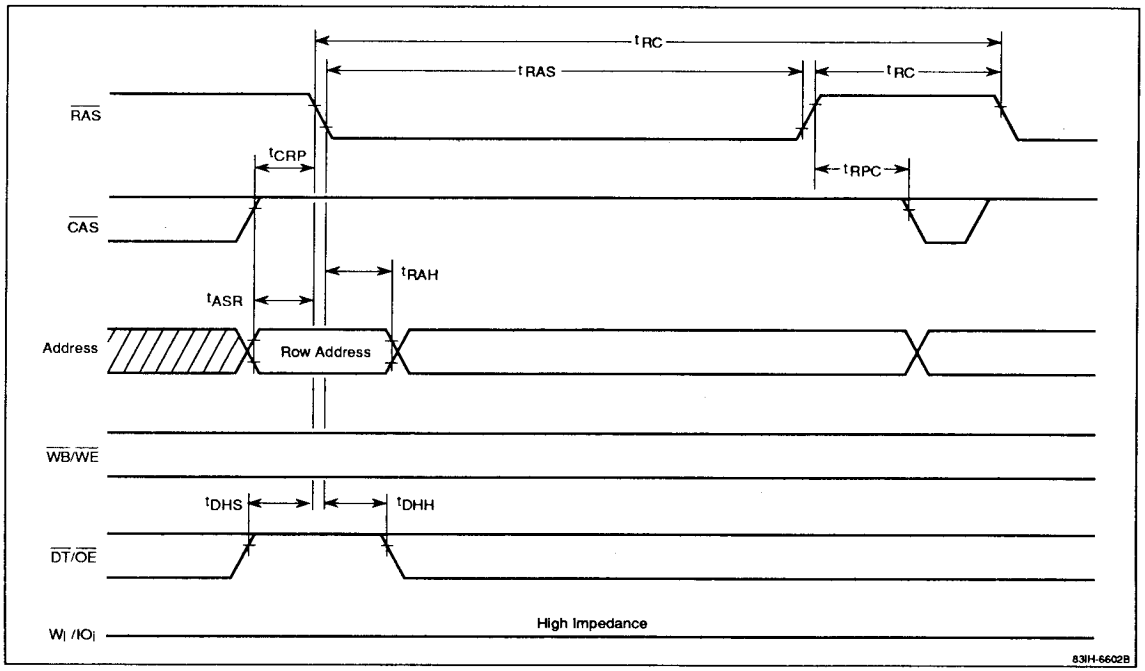
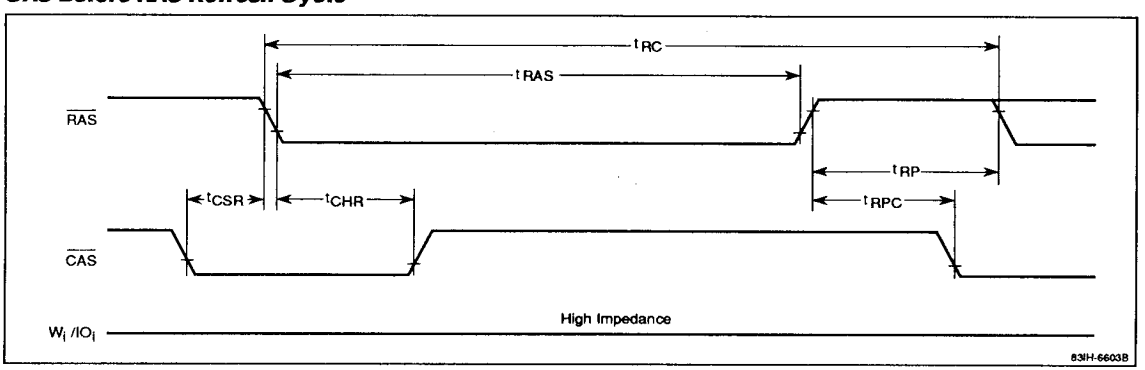
Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle

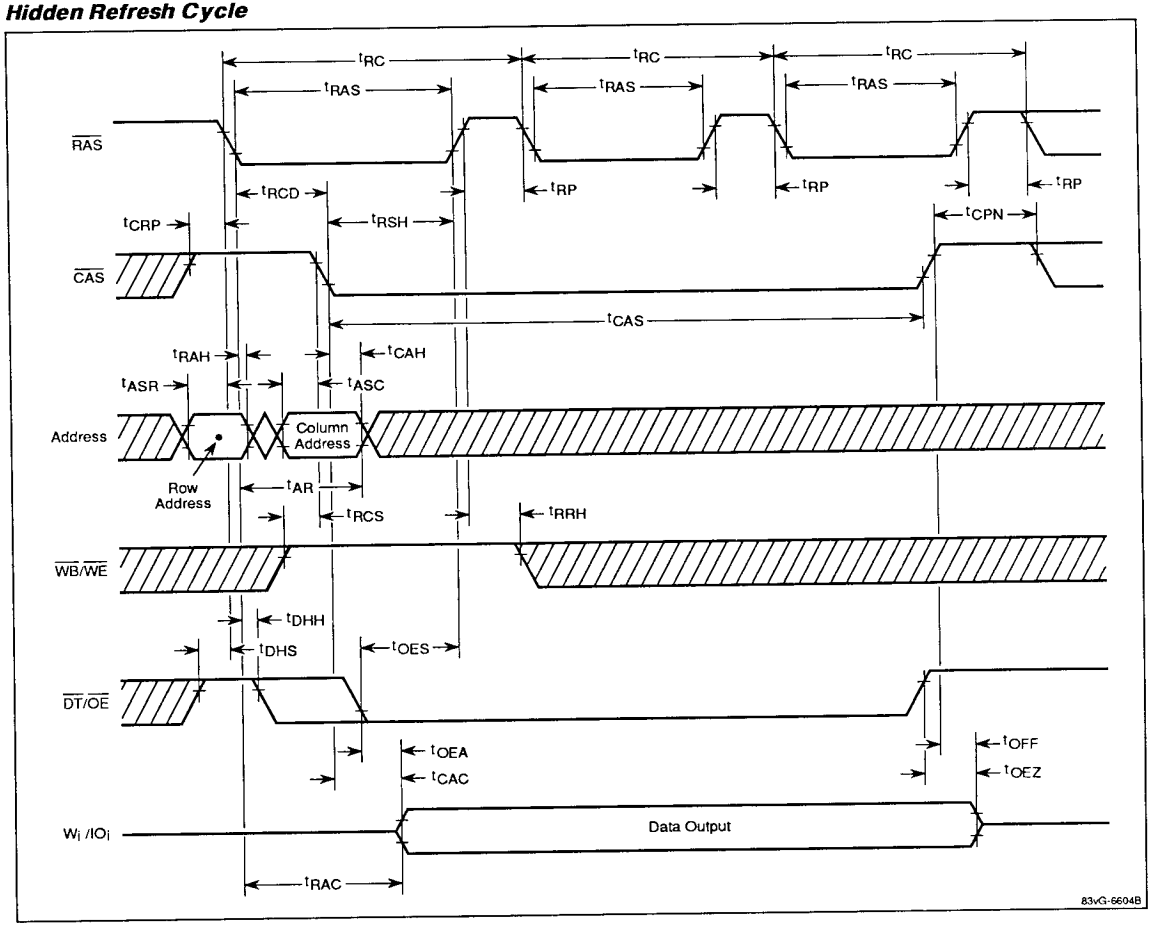


$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Timing Waveforms (cont)

Hidden Refresh Cycle



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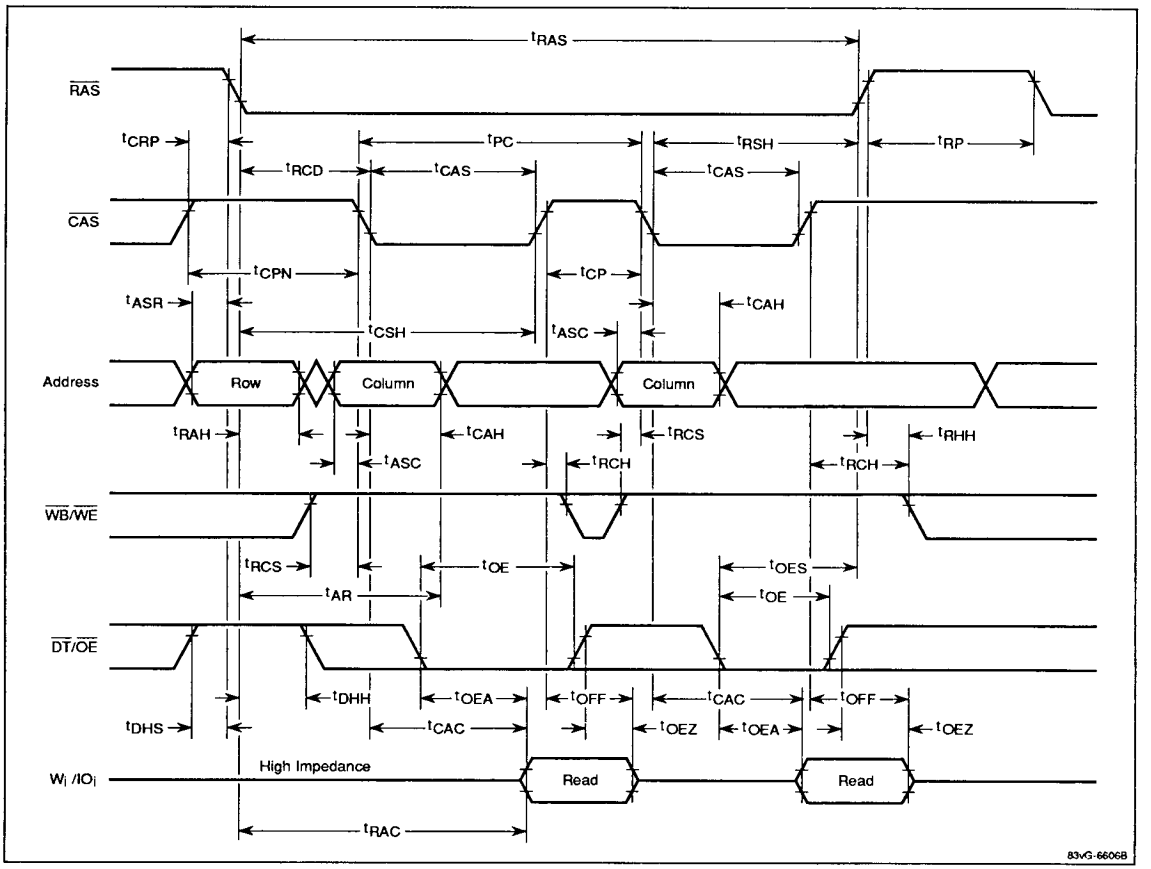
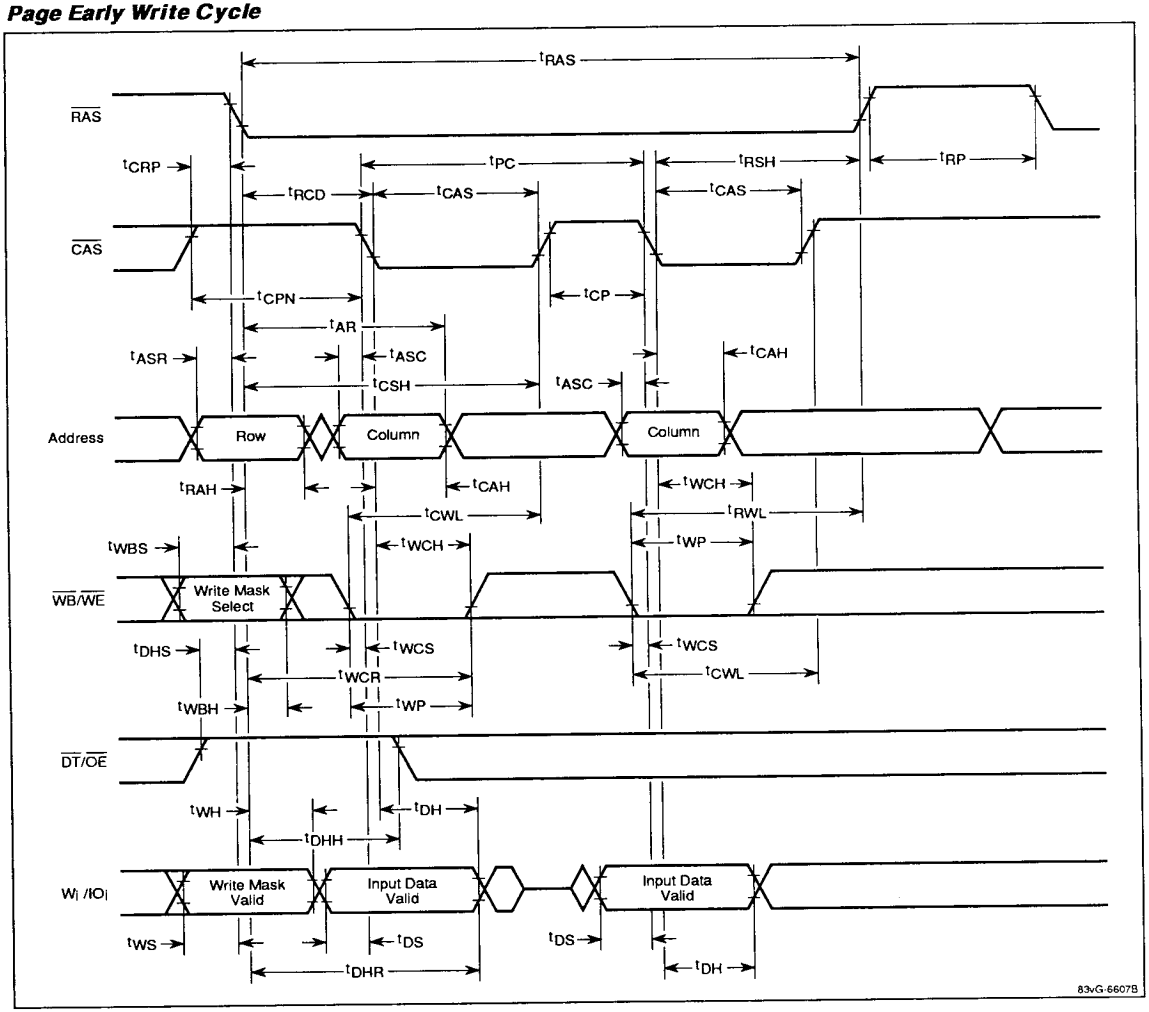
Timing Waveforms (cont)

Page Read Cycle



Timing Waveforms (cont)

Page Early Write Cycle



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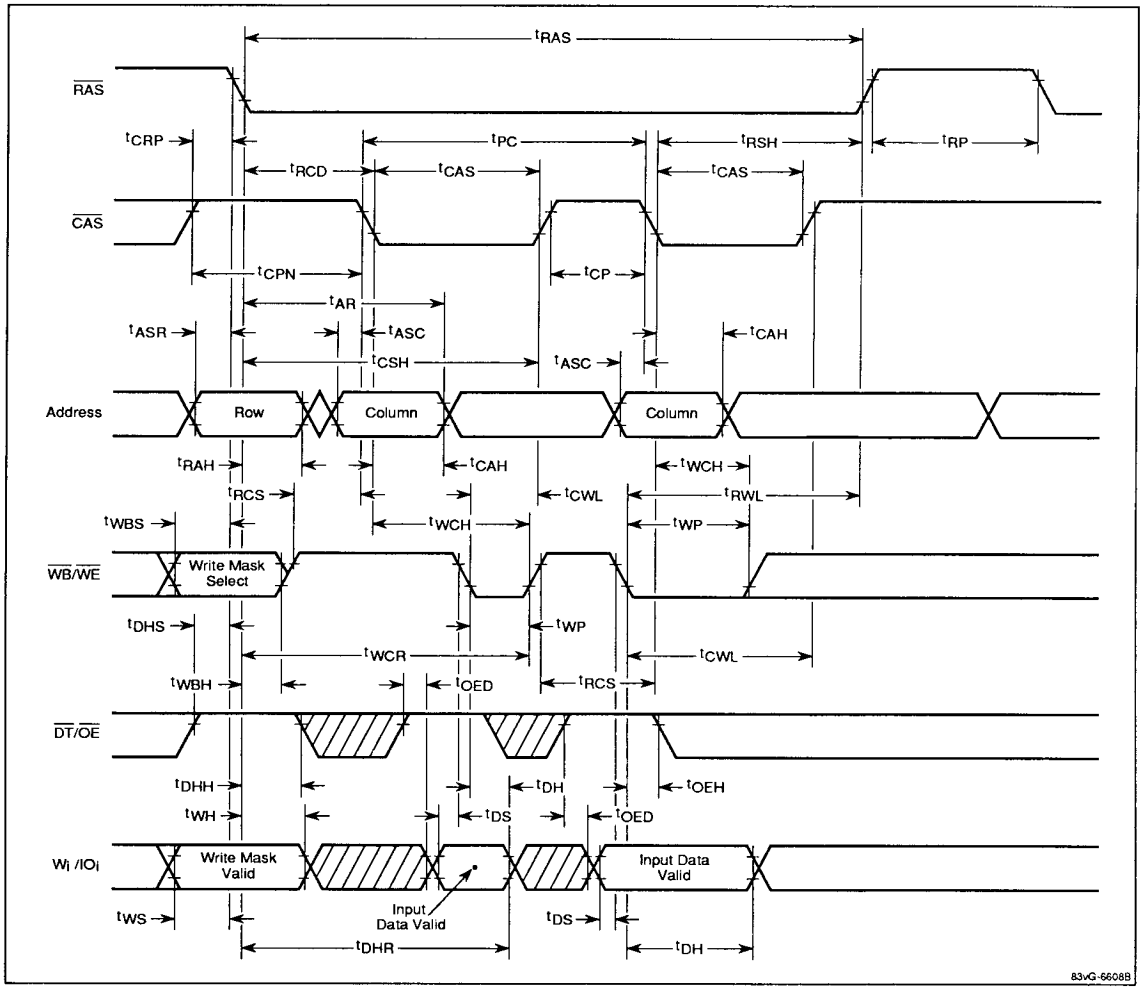
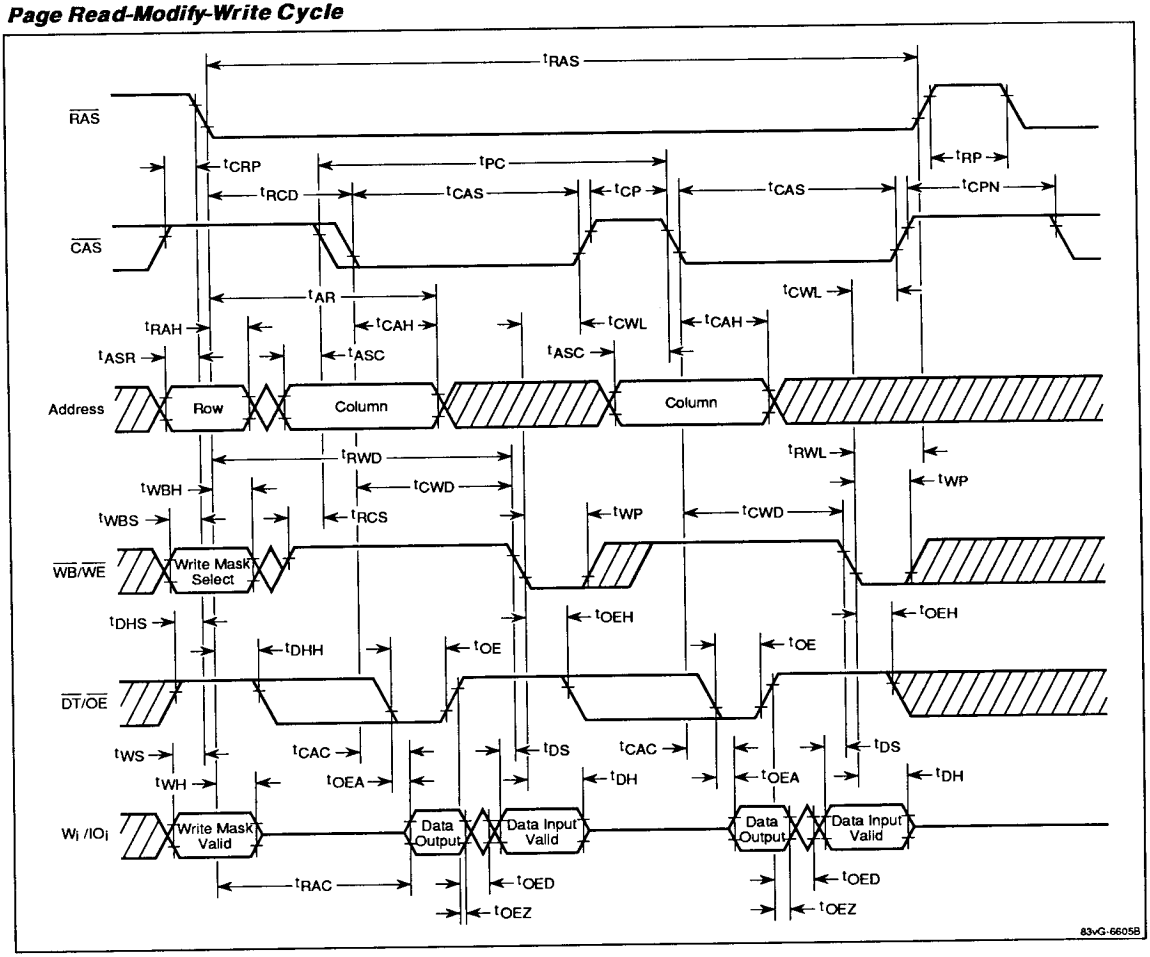
Timing Waveforms (cont)

Page Late Write Cycle



Timing Waveforms (cont)

Page Read-Modify-Write Cycle



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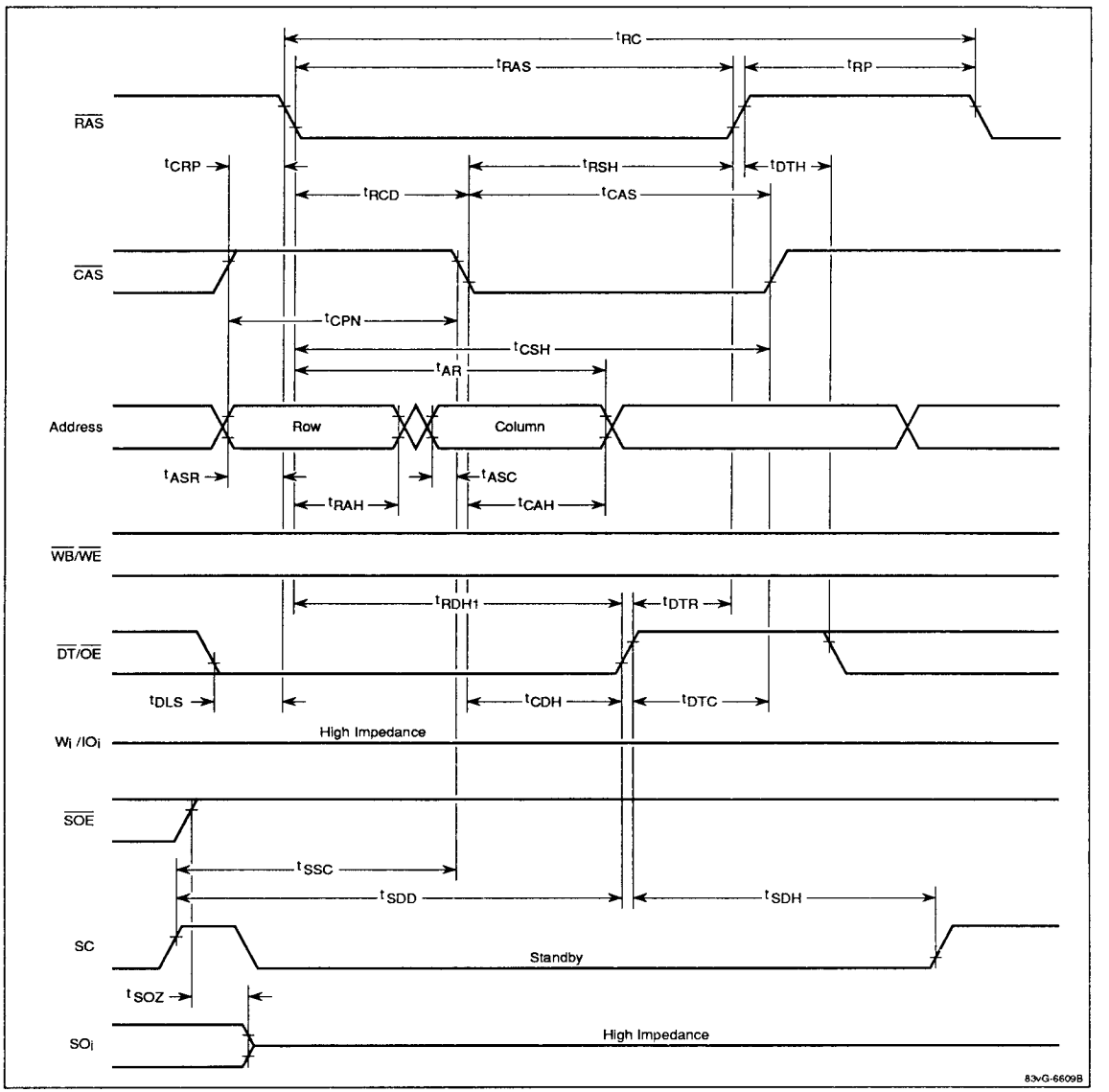
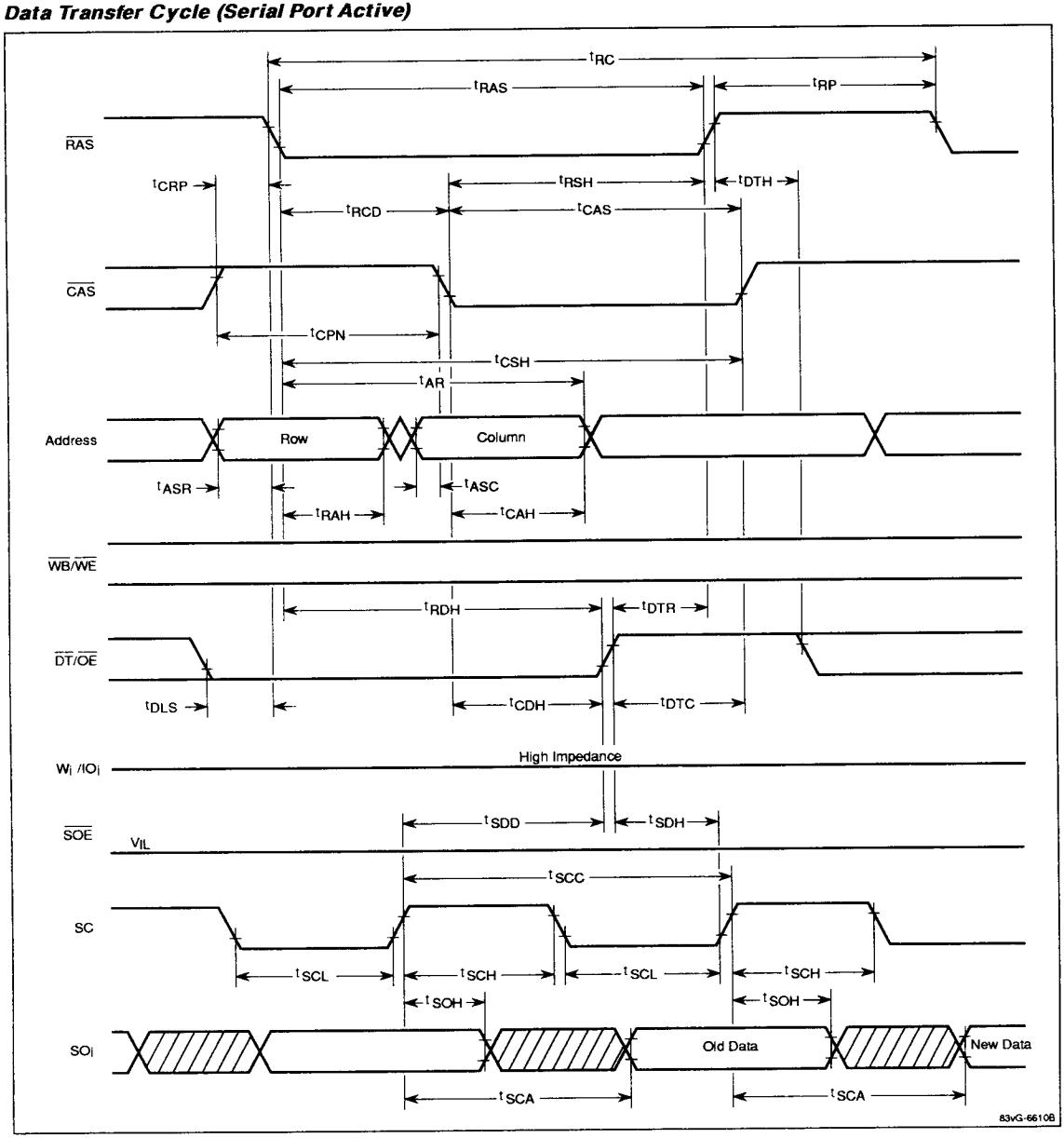
Timing Waveforms (cont)

Data Transfer Cycle (Serial Port in Standby)



Timing Waveforms (cont)

Data Transfer Cycle (Serial Port Active)



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Timing Waveforms (cont)

Serial Read Cycle