μPD421001
1,048,576 x 1-Bit
Dynamic CMOS RAM

Description

The μPD421001 is a 1,048,576-word by 1-bit dynamic RAM designed with a nibble mode and to operate from a single +5-volt power supply. Advanced polycide technology using trench capacitors minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and advanced CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit generates the negative-voltage substrate bias—automatically and transparently.

The three-state output is controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CAS}$ low. Data output is returned to high impedance by returning $\overline{CAS}$ high. The device is capable of executing nibble read and write cycles by cycling $\overline{CAS}$.

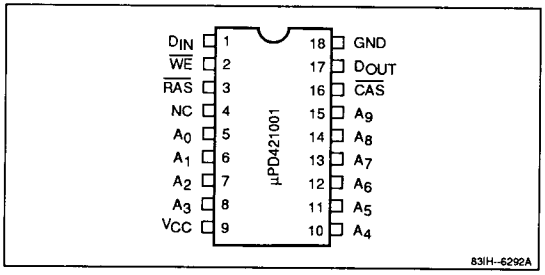
Refreshing may be accomplished by means of $\overline{CAS}$ before $\overline{RAS}$ cycles that internally generate the refresh address. Refreshing can also be accomplished by means of RAS-only refresh cycles or by normal read or write cycles on the 512 address combinations of A_0 through A_8 during an 8-ms period.

Features

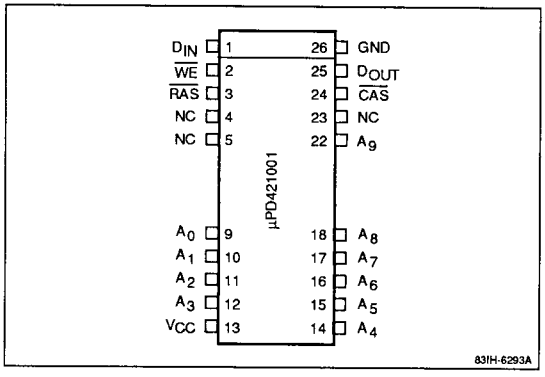
- 1,048,576-word by 1-bit organization
- Single +5-volt ±10% power supply
- Nibble option
- Low power dissipation
  - —90 mA max (active) for 60 ns version
  - —1 mA max (standby)
- $\overline{CAS}$ before $\overline{RAS}$ refresh cycles
- Multiplexed address inputs
- On-chip substrate bias generator
- Nonlatched, three-state outputs
- Low input capacitance
- TTL-compatible inputs and outputs
- 512 refresh cycles every 8 ms
- High-density 18-pin plastic DIP, 26/20-pin plastic SOJ, or 20-pin plastic ZIP packaging

Pin Configurations

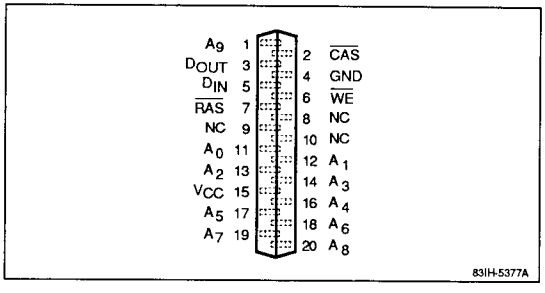
18-Pin Plastic DIP



26/20-Pin Plastic SOJ



20-Pin Plastic ZIP



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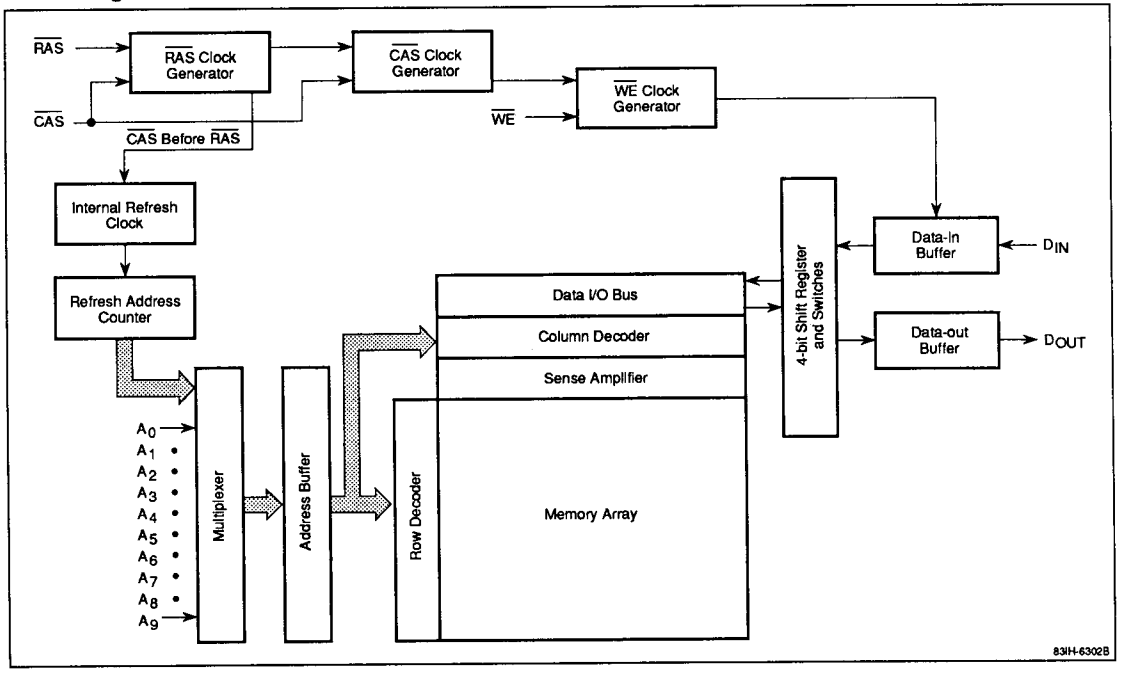
TSOP package will be available in 1991.

Block Diagram



Ordering Information

Part Number	RAS Access Time (max)	R/W Cycle Time (max)	Nibble Cycle (max)	Package
μPD421001C-60	60 ns	120 ns	40 ns	18-pin plastic DIP
C-70	70 ns	130 ns	40 ns	
C-80	80 ns	160 ns	40 ns	
C-10	100 ns	190 ns	45 ns	
μPD421001LA-60	60 ns	120 ns	40 ns	26/20-pin plastic SOJ
LA-70	70 ns	130 ns	40 ns	
LA-80	80 ns	160 ns	40 ns	
LA-10	100 ns	190 ns	45 ns	
μPD421001V-60	60 ns	120 ns	40 ns	20-pin plastic ZIP
V-70	70 ns	130 ns	40 ns	
V-80	80 ns	160 ns	40 ns	
V-10	100 ns	190 ns	45 ns	

Pin Identification

Name	Function
A_0 - A_9	Address inputs
D_{IN}	Data input
D_{OUT}	Data output
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Absolute Maximum Ratings

Voltage on any pin relative to GND, V_T	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 25 °C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	6	pF	Address, D_{IN}
	C_{I2}	8	pF	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$
Output capacitance	C_D	7	pF	D_{OUT}

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Ambient temperature	T_A	0		70	°C

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			2.0	mA	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}
				1.0	mA	$\overline{RAS}$ = $\overline{CAS}$ = V_{CC} − 0.2
Input leakage current	$I_{I(L)}$	−10		10	μA	V_{IN} = 0 to 5.5 V; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10		10	μA	D_{OUT} disabled; V_{OUT} = 0 to 5.5 V
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −5 mA

6

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		-60		-70		-80		-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Operating current, average	I_{CC1}		90		80		70		60	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} min (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		90		80		70		60	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ = V_{IH}; t_{RC} = t_{RC} min (Note 5)
Operating current, nibble cycle, average	I_{CC4}		80		70		60		50	mA	$\overline{RAS}$ = V_{IL}; $\overline{CAS}$ cycling; t_{NC} = t_{NC} min (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		90		80		70		60	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ before $\overline{RAS}$; t_{RC} = t_{RC} min (Note 5)
Access time from column address	t_{AA}		30		35		45		50	ns	(Notes 7, 10)
Column address hold time referenced to $\overline{RAS}$	t_{AR}	N/A		N/A		60		70		ns	(Note 18)
Column address setup time	t_{ASC}	0		0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	30		35		45		50		ns	(Note 17)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		20		20		25	ns	(Notes 7, 9, 10)
Column address hold time	t_{CAH}	15		17		20		20		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	20	10,000	25	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		15		15		20		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		10		ns	(Note 13)
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		100		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		10		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	20		20		20		25		ns	(Note 17)
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		15		15		20		ns	
Data-in hold time	t_{DH}	15		15		20		20		ns	(Note 16)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	N/A		N/A		60		70		ns	(Note 18)
Data-in setup time	t_{DS}	0		0		0		0		ns	(Note 16)
Nibble access time	t_{NAC}		20		20		20		25	ns	(Note 7)

AC Characteristics (cont)

Parameter	Symbol	-60		-70		-80		-10		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ pulse width (nibble cycle)	t_{NAS}	20	10,000	20	10,000	20	10,000	25	10,000	ns	
Nibble cycle time	t_{NC}	40		40		40		45		ns	(Note 6)
$\overline{CAS}$ to $\overline{WE}$ delay (nibble cycle)	t_{NCWD}	20		20		20		25		ns	(Note 17)
Write command to $\overline{CAS}$ lead time (nibble cycle)	t_{NCWL}	15		15		20		25		ns	
$\overline{CAS}$ precharge (nibble cycle)	t_{NP}	10		10		10		10		ns	
$\overline{RAS}$ hold time (nibble read cycle)	t_{NRRSH}	20		20		20		25		ns	
$\overline{RAS}$ hold time (nibble write cycle)	t_{NWRSH}	20		20		20		25		ns	
Output buffer turnoff delay	t_{OFF}	0	15	0	15	0	20	0	25	ns	(Note 11)
Access time from $\overline{RAS}$	t_{RAC}		60		70		80		100	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	17	35	17	50	ns	(Note 10)
Row address hold time	t_{RAH}	10		10		12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		45		50		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width, nibble cycle	t_{RASP}	60	100,000	70	100,000	80	100,000	100	100,000	ns	
Random read or write cycle time	t_{RC}	120		130		160		190		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	25	60	25	75	ns	(Note 12)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	(Note 14)
Read command setup time	t_{RCS}	0		0		0		0		ns	
Refresh period	t_{REF}		8		8		8		8	ms	Addresses A_0 - A_8
$\overline{RAS}$ precharge time	t_{RP}	50		50		70		80		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10		10		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		10		ns	(Note 14)
$\overline{RAS}$ hold time	t_{RSH}	20		20		20		25		ns	
Read-write cycle time	t_{RWC}	145		155		190		225		ns	(Note 6)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	60		70		80		100		ns	(Note 17)
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		30		ns	

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AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Rise and fall transition time	t_T	3	50	3	50	3	50	3	50	ns	(Note 4)
Write command hold time	t_{WCH}	15		15		15		20		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	N/A		N/A		55		70		ns	(Note 18)
Write command setup time	t_{WCS}	0		0		0		0		ns	(Note 17)
Write command pulse width	t_{WP}	15		15		15		20		ns	(Note 15)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved.

(3) AC measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each nibble cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF (V_{OH} = 2.0 V, V_{OL} = 0.8 V).

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).

(10) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(11) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(12) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), then access time is controlled exclusively by t_{CAC}.

(13) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(14) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(15) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

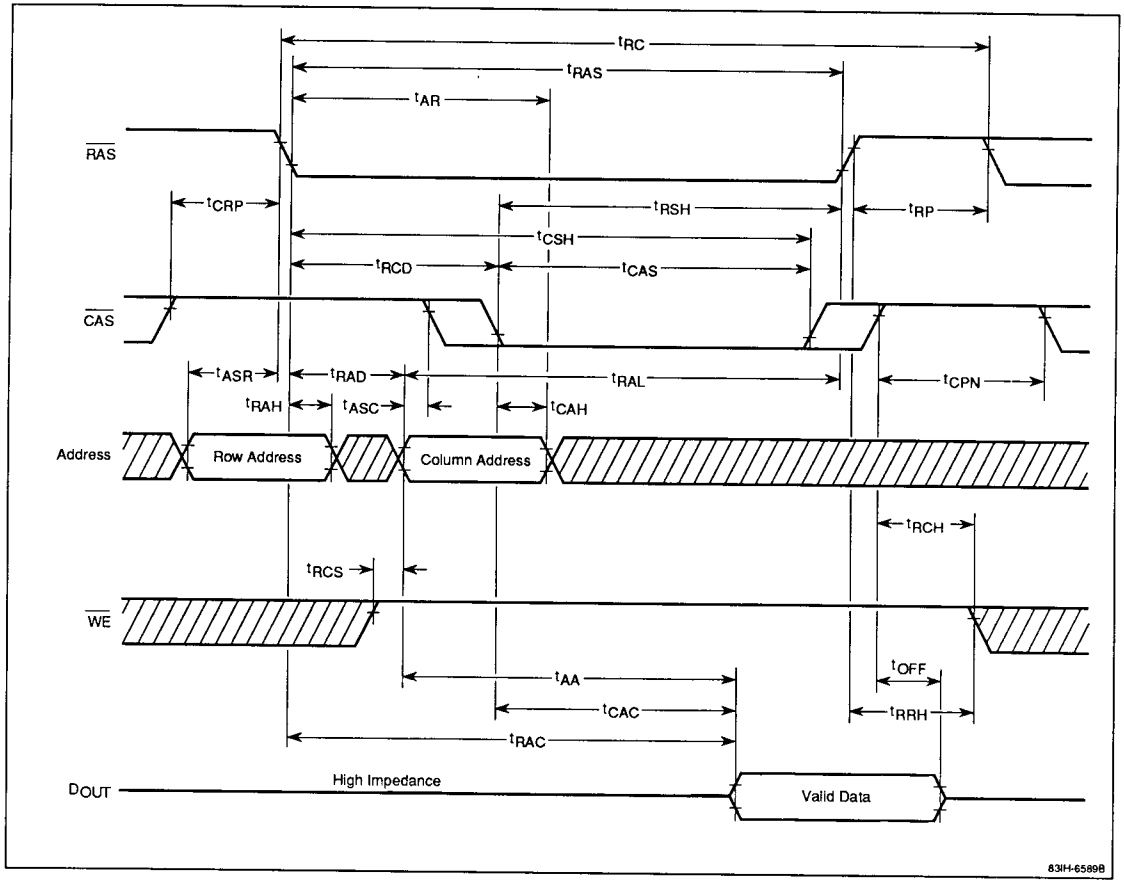
(16) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(17) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output pin (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(18) This parameter is not needed for the μPD421001-60 and μPD421001-70.

Timing Waveforms

Read Cycle



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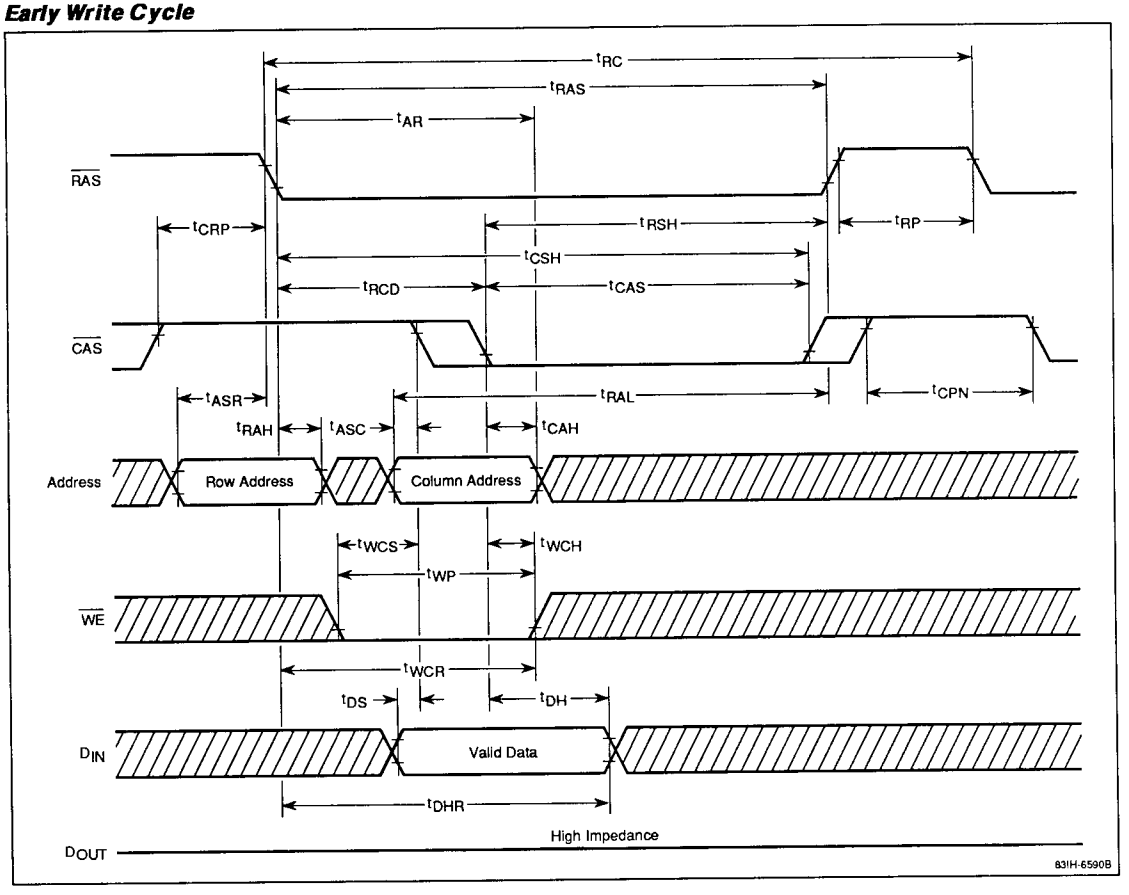
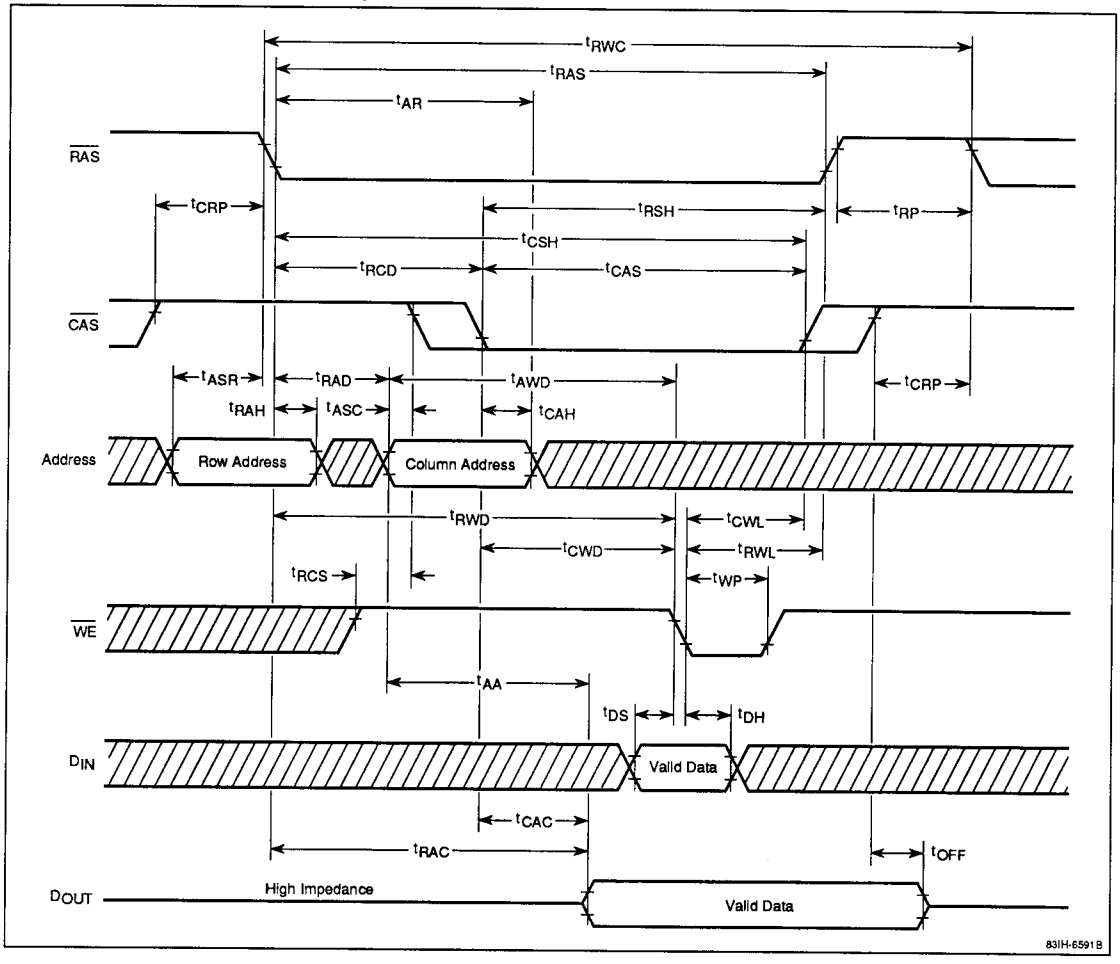
Timing Waveforms (cont)

Early Write Cycle



Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle



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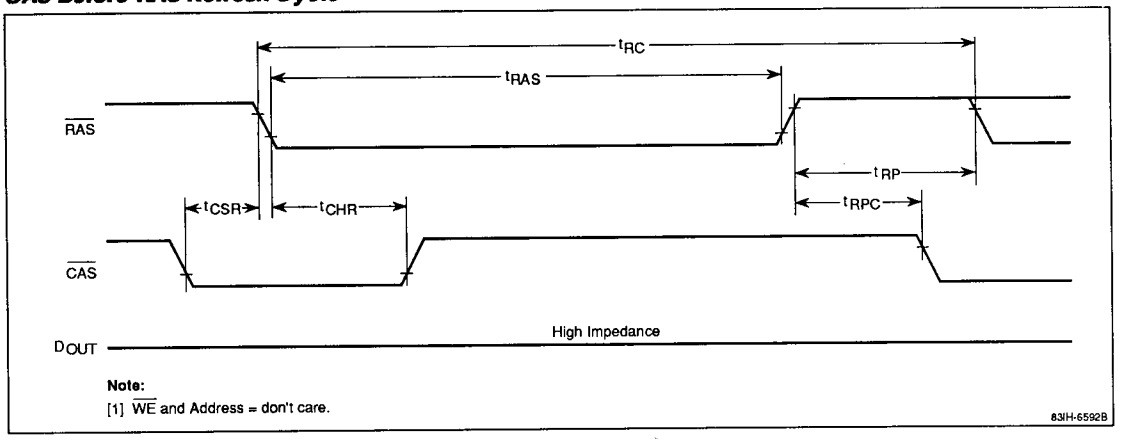
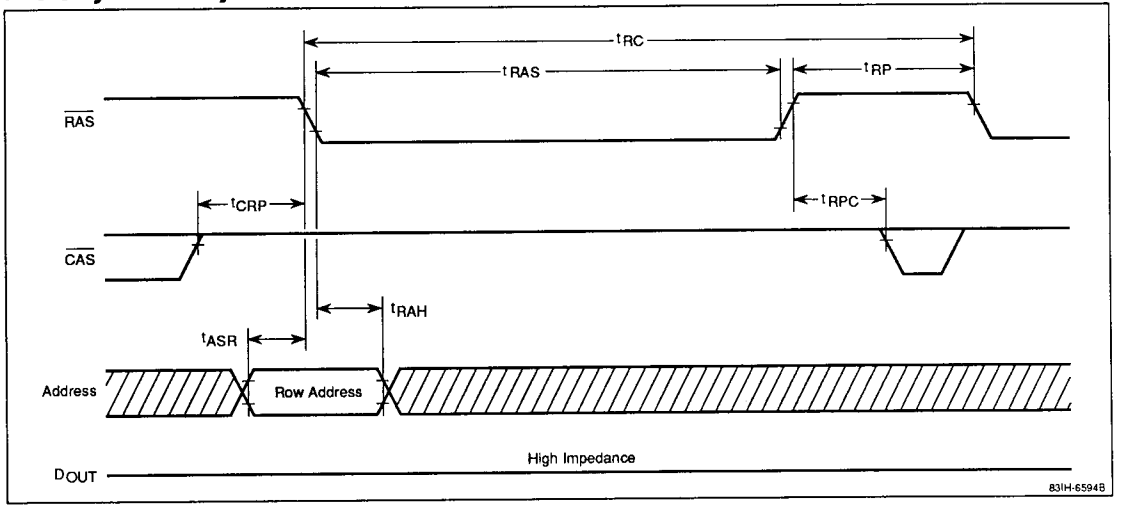
Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle

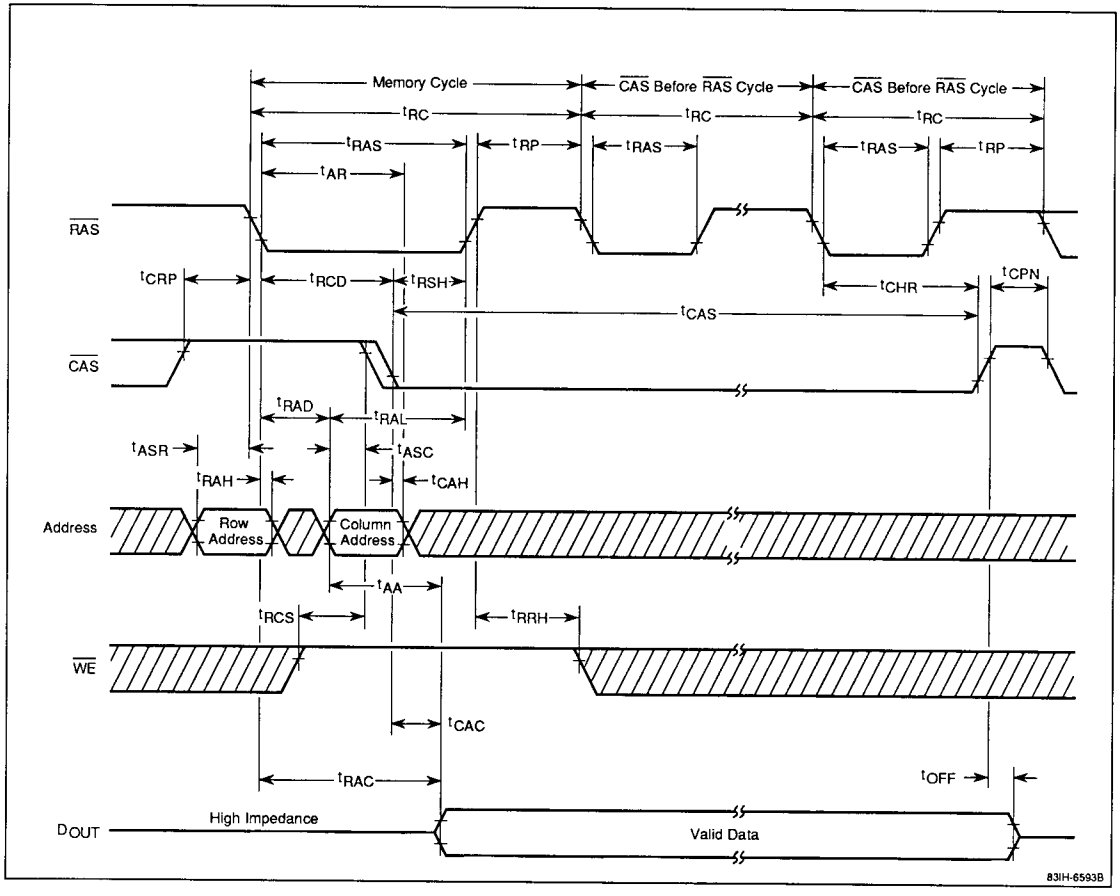


$\overline{RAS}$-Only Refresh Cycle



Timing Waveforms (cont)

Hidden Refresh Cycle



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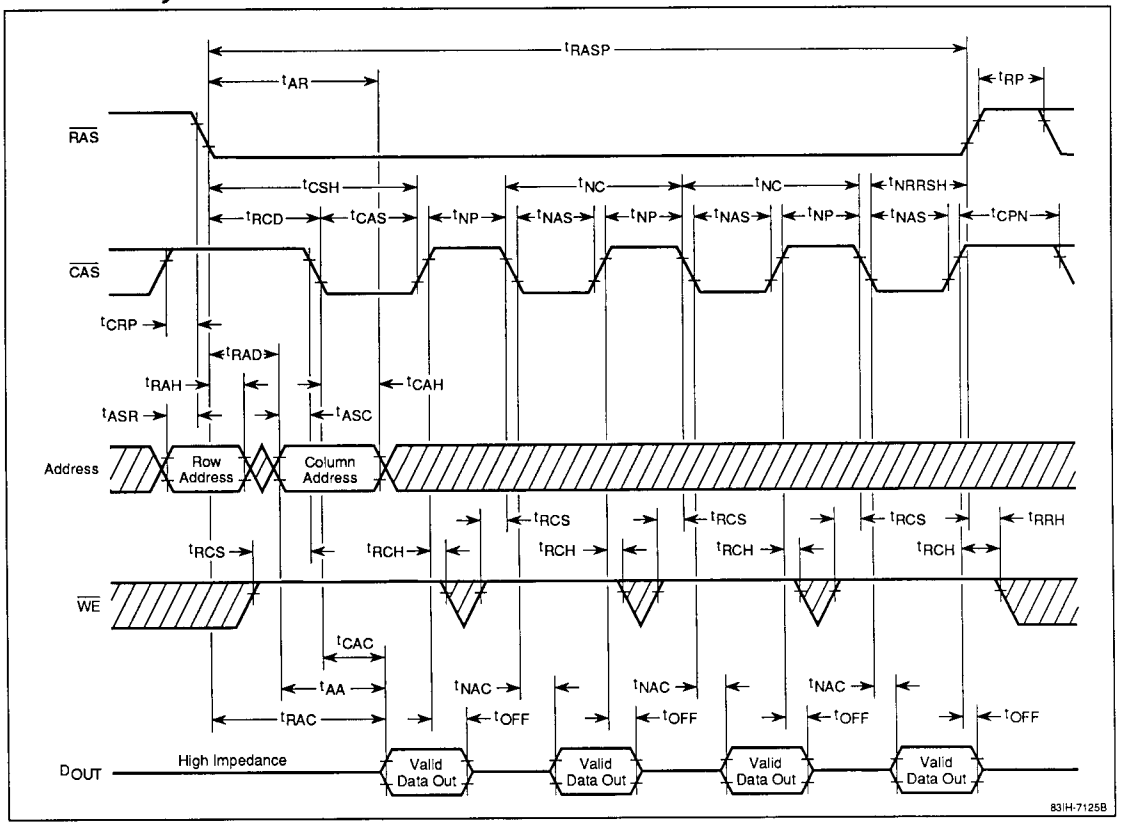
Timing Waveforms (cont)

Nibble Read Cycle

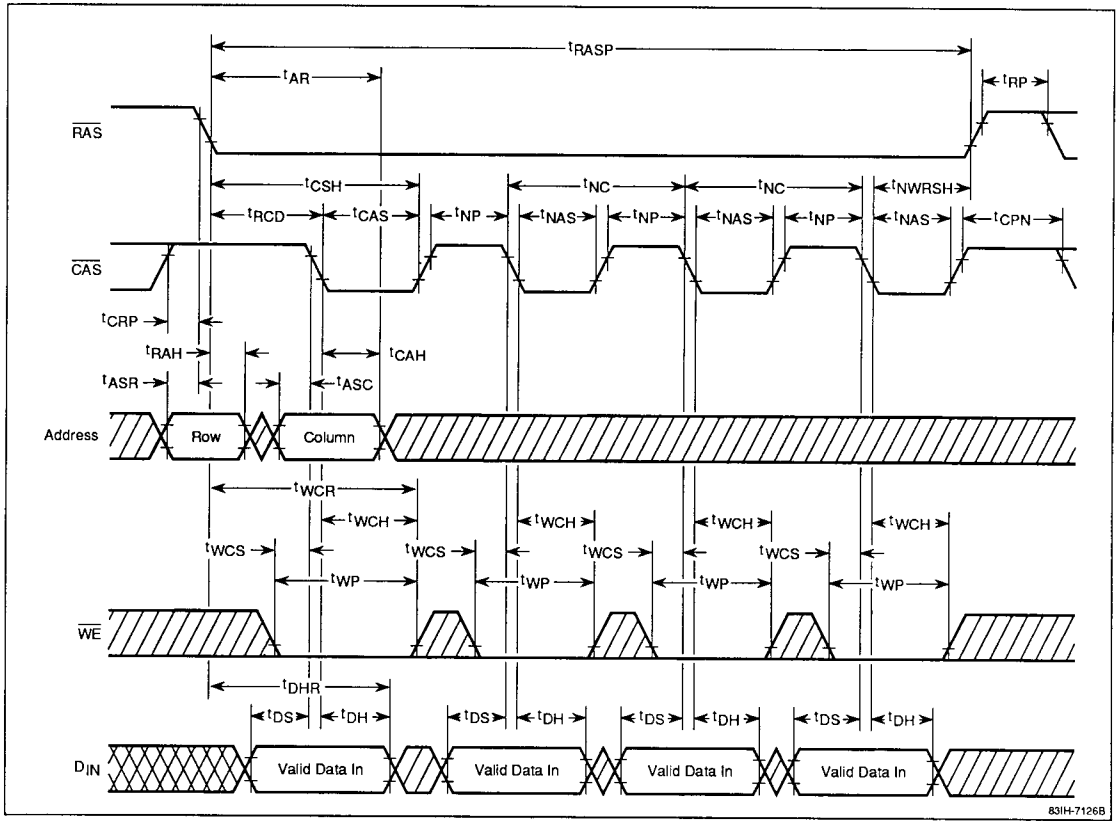


The μPD421001 is capable of executing nibble read, write, or read-modify-write cycles. Nibble mode allows high-speed serial access of maximum of 4 data bits. The first bit is determined by the row and column addresses, and the next bits are accessed automatically by cycling $\overline{CAS}$ while $\overline{RAS}$ is held low. The addresses of nibble bits are determined by the combination of row address A_9 and column address A_9 in the following sequence.

		Row Address										Column Address										
Sequence	**Nibble Bit**	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	**Comment**
$\overline{RAS}/\overline{CAS}$	1	0	0	1	0	0	0	1	0	1	0	0	1	1	0	1	0	1	0	0	0	Example: external address input
$\overline{CAS}$ cycling	2	1	0	1	0	0	0	1	0	1	0	0	1	1	0	1	0	1	0	0	0	Internal address generated
$\overline{CAS}$ cycling	3	0	0	1	0	0	0	1	0	1	0	1	1	1	0	1	0	1	0	0	0	
$\overline{CAS}$ cycling	4	1	0	1	0	0	0	1	0	1	0	1	1	1	0	1	0	1	0	0	0	
$\overline{CAS}$ cycling	1	0	0	1	0	0	0	1	0	1	0	0	1	1	0	1	0	1	0	0	0	Repeated sequence

Timing Waveforms (cont)

Nibble Early Write Cycle



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Timing Waveforms (cont)

Nibble Read-Write/Read-Modify-Write Cycle