

MOS INTEGRATED CIRCUIT

μ PD42S17805, 4217805

16 M-BIT DYNAMIC RAM
2 M-WORD BY 8-BIT, EDO

Description

The μ PD42S17805, 4217805 are 2,097,152 words by 8 bits CMOS dynamic RAMs with optional EDO.

EDO is a kind of the page mode and is useful for the read operation.

Besides, the μ PD42S17805 can execute $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh.

The μ PD42S17805, 4217805 are packaged in 28-pin plastic TSOP (II) and 28-pin plastic SOJ.

Features

- EDO (Hyper page mode)
- 2,097,152 words by 8 bits organization
- Single +5.0 V ± 10 % power supply
- Fast access and cycle time

Part number	Power consumption Active (MAX.)	Access time (MAX.)	R/W cycle time (MIN.)	EDO (Hyper page mode) cycle time (MIN.)
μ PD42S17805-50, 4217805-50	660 mW	50 ns	84 ns	20 ns
μ PD42S17805-60, 4217805-60	605 mW	60 ns	104 ns	25 ns
μ PD42S17805-70, 4217805-70	550 mW	70 ns	124 ns	30 ns

- The μ PD42S17805 can execute $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh

Part number	Refresh cycle	Refresh	Power consumption at standby (MAX.)
μ PD42S17805	2,048 cycles/128 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh	1.4 mW (CMOS level input)
μ PD4217805	2,048 cycles/32 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh	5.5 mW (CMOS level input)

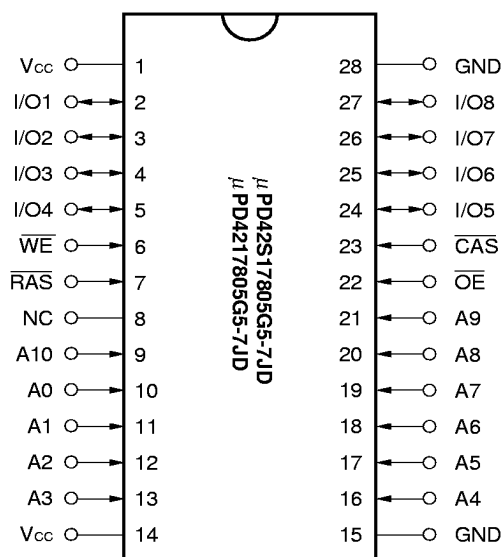
The information in this document is subject to change without notice.

Ordering Information

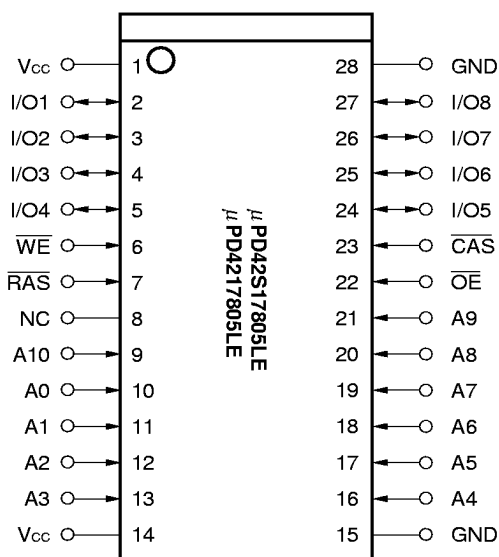
Part number	Access time (MAX.)	Package	Refresh
μ PD42S17805G5-50-7JD	50 ns	28-pin plastic TSOP (II) (400 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh
μ PD42S17805G5-60-7JD	60 ns		$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
μ PD42S17805G5-70-7JD	70 ns		$\overline{\text{RAS}}$ only refresh
μ PD42S17805LE-50	50 ns	28-pin plastic SOJ (400 mil)	Hidden refresh
μ PD42S17805LE-60	60 ns		
μ PD42S17805LE-70	70 ns		
μ PD4217805G5-50-7JD	50 ns	28-pin plastic TSOP (II) (400 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
μ PD4217805G5-60-7JD	60 ns		$\overline{\text{RAS}}$ only refresh
μ PD4217805G5-70-7JD	70 ns		Hidden refresh
μ PD4217805LE-50	50 ns	28-pin plastic SOJ (400 mil)	
μ PD4217805LE-60	60 ns		
μ PD4217805LE-70	70 ns		

Pin Configurations (Marking Side)

28-pin Plastic TSOP (II) (400 mil)

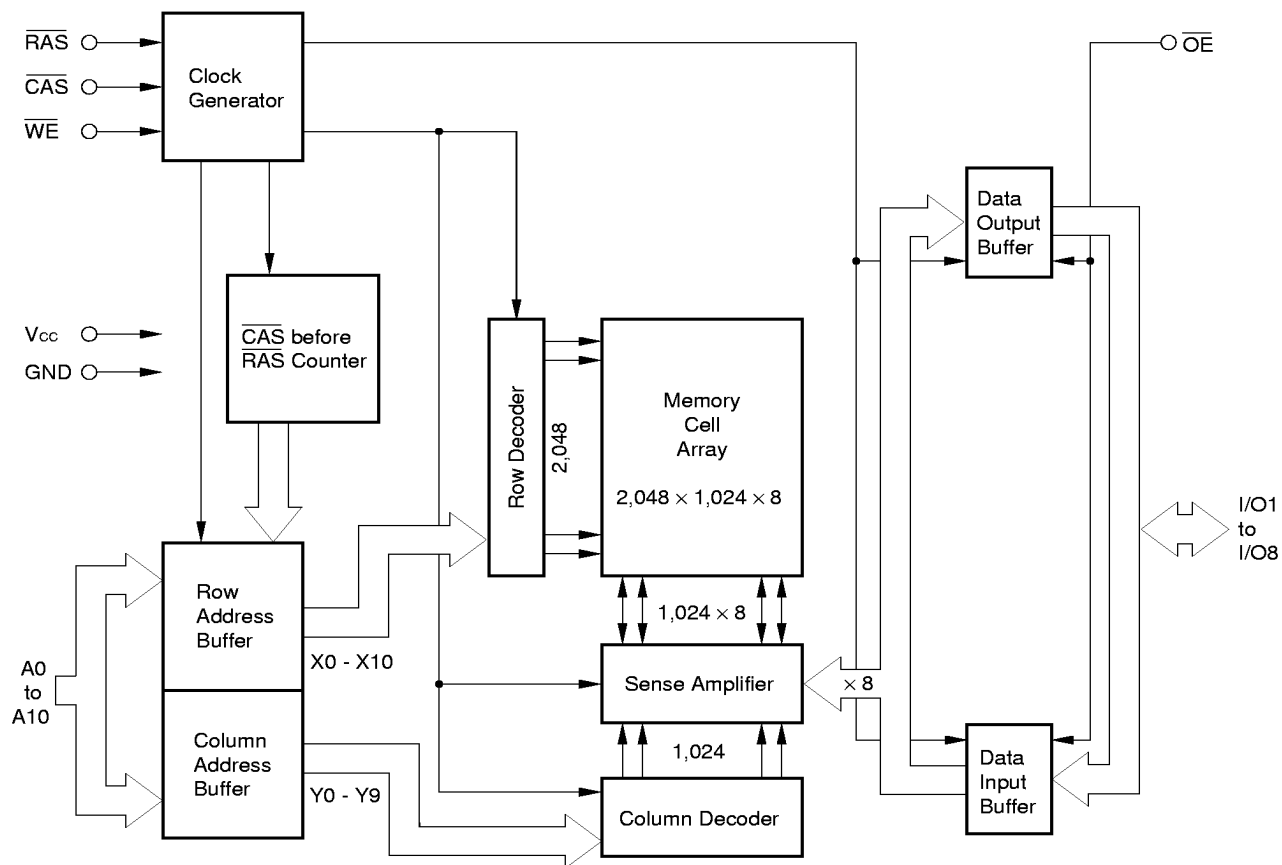


28-pin Plastic SOJ (400 mil)



A0 to A10 : Address Inputs
 I/O1 to I/O8: Data Inputs/Outputs
 $\overline{RAS}$: Row Address Strobe
 $\overline{CAS}$: Column Address Strobe
 $\overline{WE}$: Write Enable
 $\overline{OE}$: Output Enable
 V_{CC} : Power Supply
 GND : Ground
 NC : No Connection

Block Diagram



Input/Output Pin Functions

The μPD42S17805, 4217805 have input pins $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$, A0 to A10 and input/output pins I/O1 to I/O8.

Pin name	Input/Output	Function
$\overline{\text{RAS}}$ (Row address strobe)	Input	$\overline{\text{RAS}}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
$\overline{\text{CAS}}$ (Column address strobe)	Input	$\overline{\text{CAS}}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A10 (Address inputs)	Input	Address bus. Input total 21-bit of address signal, upper 11-bit and lower 10-bit in sequence (address multiplex method). Therefore, one word is selected from 2,097,152-word by 8-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{\text{RAS}}$. Then, switch the address bus to column address and activate $\overline{\text{CAS}}$. Each address is taken into the device when $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are activated. Therefore, the address input setup time (t_{ASR} , t_{ASC}) and hold time (t_{RAH} , t_{CAH}) are specified for the activation of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$.
$\overline{\text{WE}}$ (Write enable)	Input	Write control signal. Write operation is executed by activating $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$.
$\overline{\text{OE}}$ (Output enable)	Input	Read control signal. Read operation can be executed by activating $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{OE}}$. If $\overline{\text{WE}}$ is activated during read operation, $\overline{\text{OE}}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O8 (Data inputs/outputs)	Input/Output	8-bit data bus. I/O1 to I/O8 are used to input/output data.

★ Hyper Page Mode (EDO)

The hyper page mode (EDO) is a kind of page mode with enhanced features. The two major features of the hyper page mode (EDO) are as follows.

1. Data output time is extended.

In the hyper page mode (EDO), the output data is held to the next $\overline{\text{CAS}}$ cycle's falling edge, instead of the rising edge. For this reason, valid data output time in the hyper page mode (EDO) is extended compared with the fast page mode (= data extend function). In the fast page mode, the data output time becomes shorter as the $\overline{\text{CAS}}$ cycle time becomes shorter. Therefore, in the hyper page mode (EDO), the timing margin in read cycle is larger than that of the fast page mode even if the $\overline{\text{CAS}}$ cycle time becomes shorter.

2. The $\overline{\text{CAS}}$ cycle time in the hyper page mode (EDO) is shorter than that in the fast page mode.

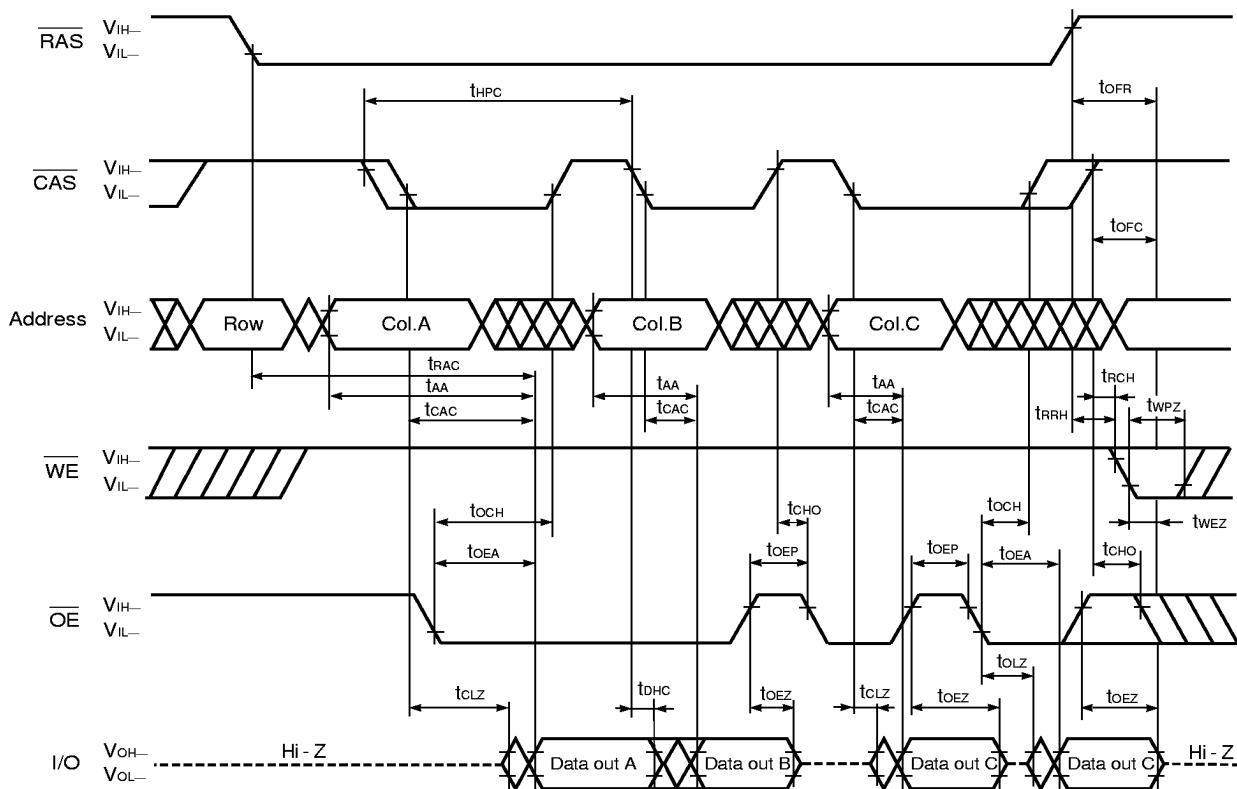
In the hyper page mode (EDO), due to the data extend function, the $\overline{\text{CAS}}$ cycle time can be shorter than in the fast page mode if the timing margin is the same.

Taking a device whose t_{RAC} is 60 ns as an example, the $\overline{\text{CAS}}$ cycle time in the fast page mode is 25 ns while that in the fast page mode is 40 ns.

In the hyper page mode (EDO), read (data out) and write (data in) cycles can be executed repeatedly during one $\overline{\text{RAS}}$ cycle. The hyper page mode (EDO) allows both read and write operations during one cycle.

The following shows a part of the hyper page mode (EDO) read cycle. Specifications to be observed are described in the next page.

Hyper Page Mode (EDO) Read Cycle



Cautions when using the hyper page mode (EDO)

1. $\overline{\text{CAS}}$ access should be used to operate t_{HPC} at the MIN. value.
2. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$ as follows. The effective specification depends on the state of each signal.
 - (1) Both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are inactive (at the end of read cycle)

$\overline{\text{WE}}$: inactive, $\overline{\text{OE}}$: active

t_{OFC} is effective when $\overline{\text{RAS}}$ is inactivated before $\overline{\text{CAS}}$ is inactivated.

t_{OFR} is effective when $\overline{\text{CAS}}$ is inactivated before $\overline{\text{RAS}}$ is inactivated.

The slower of t_{OFC} and t_{OFR} becomes effective.
 - (2) Both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are active or either $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ is active (in read cycle)

$\overline{\text{WE}}$, $\overline{\text{OE}}$: inactive t_{OEZ} is effective.

Both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are inactive or $\overline{\text{RAS}}$ is active and $\overline{\text{CAS}}$ is inactive (at the end of read cycle)

$\overline{\text{WE}}$, $\overline{\text{OE}}$: active and either t_{RRH} or t_{RCH} must be met t_{WEZ} and t_{WPZ} are effective.

The faster of t_{OEZ} and t_{WEZ} becomes effective.

The faster of (1) and (2) becomes effective.
3. In read cycle, the effective specification depends on the state of $\overline{\text{CAS}}$ signal when controlling data output with the $\overline{\text{OE}}$ signal.
 - (1) $\overline{\text{CAS}}$: inactive, $\overline{\text{OE}}$: active t_{CHO} is effective.
 - (2) $\overline{\text{CAS}}$, $\overline{\text{OE}}$: active t_{OCH} is effective.

Electrical Specifications

- All voltages are referenced to GND.
- After power up ($V_{CC} \geq V_{CC(MIN.)}$), wait more than 100 μ s ($\overline{RAS}$, $\overline{CAS}$ inactive) and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−1.0 to +7.0	V
Supply voltage	V_{CC}		−1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		1	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.5	5.0	5.5	V
High level input voltage	V_{IH}		2.4		$V_{CC} + 1.0$	V
Low level input voltage	V_{IL}		−1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance ($T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$			7	
Data input/output capacitance	$C_{I/O}$	I/O			7	pF

DC Characteristics (Recommended operating conditions unless otherwise noted)

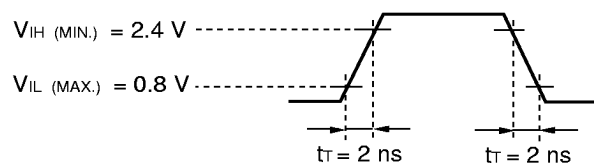
Parameter		Symbol	Test condition	MIN.	MAX.	Unit	Notes
Operating current		I _{CC1}	$\overline{\text{RAS}}, \overline{\text{CAS}}$ cycling	$t_{\text{RAC}} = 50 \text{ ns}$	120	mA	1, 2, 3
			$t_{\text{RC}} = t_{\text{RC (MIN.)}}, I_{\text{O}} = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$	110		
				$t_{\text{RAC}} = 70 \text{ ns}$	100		
Standby current	μ PD42S17805	I _{CC2}	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH (MIN.)}}, I_{\text{O}} = 0 \text{ mA}$		2.0	mA	
			$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}, I_{\text{O}} = 0 \text{ mA}$		0.25		
	μ PD4217805		$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH (MIN.)}}, I_{\text{O}} = 0 \text{ mA}$		2.0		
			$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}, I_{\text{O}} = 0 \text{ mA}$		1.0		
$\overline{\text{RAS}}$ only refresh current		I _{CC3}	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}} \geq V_{\text{IH (MIN.)}}$ $t_{\text{RC}} = t_{\text{RC (MIN.)}}, I_{\text{O}} = 0 \text{ mA}$	$t_{\text{RAC}} = 50 \text{ ns}$	120	mA	1, 2, 3, 4
				$t_{\text{RAC}} = 60 \text{ ns}$	110		
				$t_{\text{RAC}} = 70 \text{ ns}$	100		
Operating current (Hyper page mode (EDO))		I _{CC4}	$\overline{\text{RAS}} \leq V_{\text{IL (MAX.)}}, \overline{\text{CAS}}$ cycling $t_{\text{HPC}} = t_{\text{HPC (MIN.)}}, I_{\text{O}} = 0 \text{ mA}$	$t_{\text{RAC}} = 50 \text{ ns}$	100	mA	1, 2, 5
				$t_{\text{RAC}} = 60 \text{ ns}$	90		
				$t_{\text{RAC}} = 70 \text{ ns}$	80		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh current		I _{CC5}	$\overline{\text{RAS}}$ cycling $t_{\text{RC}} = t_{\text{RC (MIN.)}}, I_{\text{O}} = 0 \text{ mA}$	$t_{\text{RAC}} = 50 \text{ ns}$	120	mA	1, 2
				$t_{\text{RAC}} = 60 \text{ ns}$	110		
				$t_{\text{RAC}} = 70 \text{ ns}$	100		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ long refresh current (2,048 cycles / 128 ms, only for the μ PD42S17805)		I _{CC6}	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh: $t_{\text{RC}} = 62.5 \mu\text{s}$ $\overline{\text{RAS}}, \overline{\text{CAS}}:$ $V_{\text{CC}} - 0.2 \text{ V} \leq V_{\text{IH}} \leq V_{\text{IH (MAX.)}}$ $0 \text{ V} \leq V_{\text{IL}} \leq 0.2 \text{ V}$ Standby: $\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}$ Address: V_{IH} or V_{IL} $\overline{\text{WE}}, \overline{\text{OE}}: V_{\text{IH}}$ $I_{\text{O}} = 0 \text{ mA}$	$t_{\text{RAS}} \leq 300 \text{ ns}$	400	μA	1, 2
				$t_{\text{RAS}} \leq 1 \mu\text{s}$	500	μA	1, 2
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh current (only for the μ PD42S17805)		I _{CC7}	$\overline{\text{RAS}}, \overline{\text{CAS}}:$ $t_{\text{RAS}} = 5 \text{ ms}$ $V_{\text{CC}} - 0.2 \text{ V} \leq V_{\text{IH}} \leq V_{\text{IH (MAX.)}}$ $0 \text{ V} \leq V_{\text{IL}} \leq 0.2 \text{ V}$ $I_{\text{O}} = 0 \text{ mA}$		250	μA	2
Input leakage current		I _{I (L)}	$V_{\text{I}} = 0 \text{ to } 5.5 \text{ V}$ All other pins not under test = 0 V	-10	+10	μA	
Output leakage current		I _{O (L)}	$V_{\text{O}} = 0 \text{ to } 5.5 \text{ V}$ Output is disabled (Hi-Z)	-10	+10	μA	
High level output voltage		V _{OH}	$I_{\text{O}} = -5.0 \text{ mA}$	2.4		V	
Low level output voltage		V _{OL}	$I_{\text{O}} = +4.2 \text{ mA}$		0.4	V	

- Notes**
1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (t_{RC} and t_{HPC}).
 2. Specified values are obtained with outputs unloaded.
 3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{\text{RAS}} \leq V_{\text{IL (MAX.)}}$ and $\overline{\text{CAS}} \geq V_{\text{IH (MIN.)}}$.
 4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
 5. I_{CC4} is measured assuming that all column address inputs are switched only once during each hyper page (EDO) cycle.

AC Characteristics (Recommended Operating Conditions unless otherwise noted)

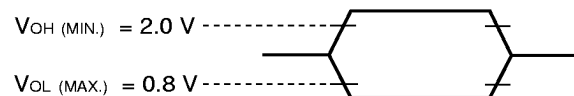
AC Characteristics Test Conditions

(1) Input timing specification



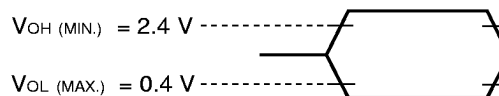
★ (2) Output timing specification

• μPD42S17805-50, 4217805-50

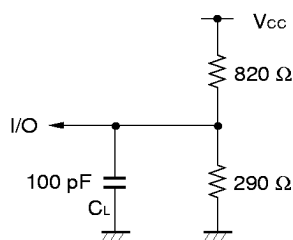


• μPD42S17805-60, 4217805-60

• μPD42S17805-70, 4217805-70



(3) Output load condition



Common to Read, Write, Read Modify Write Cycle

Parameter		Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Notes
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write cycle time		t _{RC}	84	—	104	—	124	—	ns	
RAS precharge time		t _{RP}	30	—	40	—	50	—	ns	
CAS precharge time		t _{CPN}	8	—	10	—	10	—	ns	
RAS pulse width		t _{RAS}	50	10,000	60	10,000	70	10,000	ns	1
CAS pulse width		t _{CAS}	8	10,000	10	10,000	12	10,000	ns	
RAS hold time		t _{RSH}	10	—	10	—	12	—	ns	
CAS hold time		t _{CSH}	38	—	40	—	50	—	ns	
RAS to CAS delay time		t _{RCD}	11	37	14	45	14	52	ns	2
RAS to column address delay time		t _{RAD}	9	25	12	30	12	35	ns	2
CAS to RAS precharge time		t _{CRP}	5	—	5	—	5	—	ns	3
Row address setup time		t _{ASR}	0	—	0	—	0	—	ns	
Row address hold time		t _{RAH}	7	—	10	—	10	—	ns	
Column address setup time		t _{ASC}	0	—	0	—	0	—	ns	
Column address hold time		t _{CAH}	7	—	10	—	12	—	ns	
OE lead time referenced to RAS		t _{OES}	0	—	0	—	0	—	ns	
CAS to data setup time		t _{CLZ}	0	—	0	—	0	—	ns	
OE to data setup time		t _{OLZ}	0	—	0	—	0	—	ns	
OE to data delay time		t _{OED}	10	—	13	—	15	—	ns	
Transition time (rise and fall)		t _T	1	50	1	50	1	50	ns	
Refresh time	μPD42S17805	t _{REF}	—	128	—	128	—	128	ms	4
	μPD4217805		—	32	—	32	—	32	ms	

Notes 1. In $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles, $t_{RAS(MAX.)}$ is 100 μ s.

If 10 μ s < t_{RAS} < 100 μ s, $\overline{\text{RAS}}$ precharge time for $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh (t_{RPS}) is applied.

2. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{\text{RAS}}$
$t_{RAD} \leq t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{RAC(MAX.)}$	$t_{RAC(MAX.)}$
$t_{RAD} > t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{AA(MAX.)}$	$t_{RAD} + t_{AA(MAX.)}$
$t_{RCD} > t_{RCD(MAX.)}$	$t_{CAC(MAX.)}$	$t_{RCD} + t_{CAC(MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC} , t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD(MAX.)}$ and $t_{RCD} \geq t_{RCD(MAX.)}$ will not cause any operation problems.

3. $t_{CRP(MIN.)}$ requirement is applied to $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycles.

4. This specification is applied only to the μ PD42S17805.

Read Cycle

Parameter	Symbol	$t_{RAC} = 50 \text{ ns}$		$t_{RAC} = 60 \text{ ns}$		$t_{RAC} = 70 \text{ ns}$		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Access time from $\overline{RAS}$	t_{RAC}	—	50	—	60	—	70	ns	1
Access time from $\overline{CAS}$	t_{CAC}	—	13	—	15	—	18	ns	1
Access time from column address	t_{AA}	—	25	—	30	—	35	ns	1
Access time from $\overline{OE}$	t_{OEA}	—	13	—	15	—	18	ns	
Column address lead time referenced to $\overline{RAS}$	t_{RAL}	25	—	30	—	35	—	ns	
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	ns	2
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	2
Output buffer turn-off delay time from $\overline{OE}$	t_{OEZ}	0	10	0	13	0	15	ns	3
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5	—	5	—	5	—	ns	4

Notes 1. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD}(\text{MAX.})$ and $t_{RCD} \leq t_{RCD}(\text{MAX.})$	$t_{RAC}(\text{MAX.})$	$t_{RAC}(\text{MAX.})$
$t_{RAD} > t_{RAD}(\text{MAX.})$ and $t_{RCD} \leq t_{RCD}(\text{MAX.})$	$t_{AA}(\text{MAX.})$	$t_{RAD} + t_{AA}(\text{MAX.})$
$t_{RCD} > t_{RCD}(\text{MAX.})$	$t_{CAC}(\text{MAX.})$	$t_{RCD} + t_{CAC}(\text{MAX.})$

$t_{RAD}(\text{MAX.})$ and $t_{RCD}(\text{MAX.})$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC} , t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD}(\text{MAX.})$ and $t_{RCD} \geq t_{RCD}(\text{MAX.})$ will not cause any operation problems.

2. Either $t_{RCH}(\text{MIN.})$ or $t_{RRH}(\text{MIN.})$ should be met in read cycles.
3. $t_{OEZ}(\text{MAX.})$ defines the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL} .
4. $\overline{WE}$: inactive (in read cycle)
 $\overline{CAS}$: inactive, $\overline{OE}$: active t_{CHO} is effective.
 $\overline{CAS}$, $\overline{OE}$: active t_{OCH} is effective.

Write Cycle

Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ hold time referenced to $\overline{CAS}$	t _{WCH}	7	—	10	—	10	—	ns	1
$\overline{WE}$ pulse width	t _{WP}	8	—	10	—	10	—	ns	1
$\overline{WE}$ lead time referenced to $\overline{RAS}$	t _{RWL}	10	—	10	—	12	—	ns	
$\overline{WE}$ lead time referenced to $\overline{CAS}$	t _{CWL}	8	—	10	—	12	—	ns	
$\overline{WE}$ setup time	t _{WCS}	0	—	0	—	0	—	ns	2
$\overline{OE}$ hold time	t _{OEH}	0	—	0	—	0	—	ns	
Data-in setup time	t _{DS}	0	—	0	—	0	—	ns	3
Data-in hold time	t _{DH}	7	—	10	—	10	—	ns	3

- Notes**
1. t_{WP} (MIN.) is applied to late write cycles or read modify write cycles. In early write cycles, t_{WCH} (MIN.) should be met.
 2. If t_{WCS} ≥ t_{WCS} (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.
 3. t_{DS} (MIN.) and t_{DH} (MIN.) are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{WE}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read modify write cycle time	t _{RWC}	107	—	133	—	157	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t _{RWD}	64	—	77	—	89	—	ns	1
$\overline{CAS}$ to $\overline{WE}$ delay time	t _{CWD}	27	—	32	—	37	—	ns	1
Column address to $\overline{WE}$ delay time	t _{AWD}	39	—	47	—	54	—	ns	1

- Note**
1. If t_{WCS} ≥ t_{WCS} (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If t_{RWD} ≥ t_{RWD} (MIN.), t_{CWD} ≥ t_{CWD} (MIN.), t_{AWD} ≥ t_{AWD} (MIN.) and t_{CPWD} ≥ t_{CPWD} (MIN.), the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Hyper Page Mode (EDO)

Parameter	Symbol	$t_{RAC} = 50 \text{ ns}$		$t_{RAC} = 60 \text{ ns}$		$t_{RAC} = 70 \text{ ns}$		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write cycle time	t_{HPC}	20	—	25	—	30	—	ns	1
$\overline{RAS}$ pulse width	t_{RASP}	50	125,000	60	125,000	70	125,000	ns	
★ $\overline{CAS}$ pulse width	t_{HCAS}	8	10,000	10	10,000	12	10,000	ns	
★ $\overline{CAS}$ precharge time	t_{CP}	8	—	10	—	10	—	ns	
Access time from $\overline{CAS}$ precharge	t_{ACP}	—	30	—	35	—	40	ns	
$\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPWD}	41	—	52	—	59	—	ns	2
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30	—	35	—	40	—	ns	
Read modify write cycle time	t_{HPRWC}	52	—	66	—	75	—	ns	
Data output hold time	t_{DHC}	5	—	5	—	5	—	ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5	—	5	—	5	—	ns	3
$\overline{OE}$ precharge time	t_{OEP}	5	—	5	—	5	—	ns	
Output buffer turn-off delay from $\overline{WE}$	t_{WEZ}	0	10	0	13	0	15	ns	4,5
★ $\overline{WE}$ pulse width	t_{WPZ}	8	—	10	—	10	—	ns	5
Output buffer turn-off delay from $\overline{RAS}$	t_{OFR}	0	10	0	13	0	15	ns	4,5
Output buffer turn-off delay from $\overline{CAS}$	t_{OFC}	0	10	0	13	0	15	ns	4,5

Notes 1. t_{HPC} (MIN.) is applied to $\overline{CAS}$ access.

2. If $t_{WCS} \geq t_{WCS}(\text{MIN.})$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD}(\text{MIN.})$, $t_{CWD} \geq t_{CWD}(\text{MIN.})$, $t_{AWD} \geq t_{AWD}(\text{MIN.})$ and $t_{CPWD} \geq t_{CPWD}(\text{MIN.})$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

3. $\overline{WE}$: inactive (in read cycle)

$\overline{CAS}$: inactive, $\overline{OE}$: active t_{CHO} is effective.

$\overline{CAS}$, $\overline{OE}$: active t_{OCH} is effective.

4. $t_{OFC}(\text{MAX.})$, $t_{OFR}(\text{MAX.})$ and $t_{WEZ}(\text{MAX.})$ define the time when the output achieves the conditions of Hi-Z and is not referenced to V_{OH} or V_{OL} .

5. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on state of each signal.

(1) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive (at the end of the read cycle)

$\overline{WE}$: inactive, $\overline{OE}$: active

t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.

t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.

The slower of t_{OFC} and t_{OFR} becomes effective.

(2) Both $\overline{RAS}$ and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)

$\overline{WE}$, $\overline{OE}$: inactive t_{OEZ} is effective.

Both $\overline{RAS}$ and $\overline{CAS}$ are inactive or $\overline{RAS}$ is active and $\overline{CAS}$ is inactive (at the end of read cycle)

$\overline{WE}$, $\overline{OE}$: active and either t_{RRH} or t_{RCH} must be met t_{WEZ} and t_{WPZ} are effective.

The faster of t_{OEZ} and t_{WEZ} becomes effective.

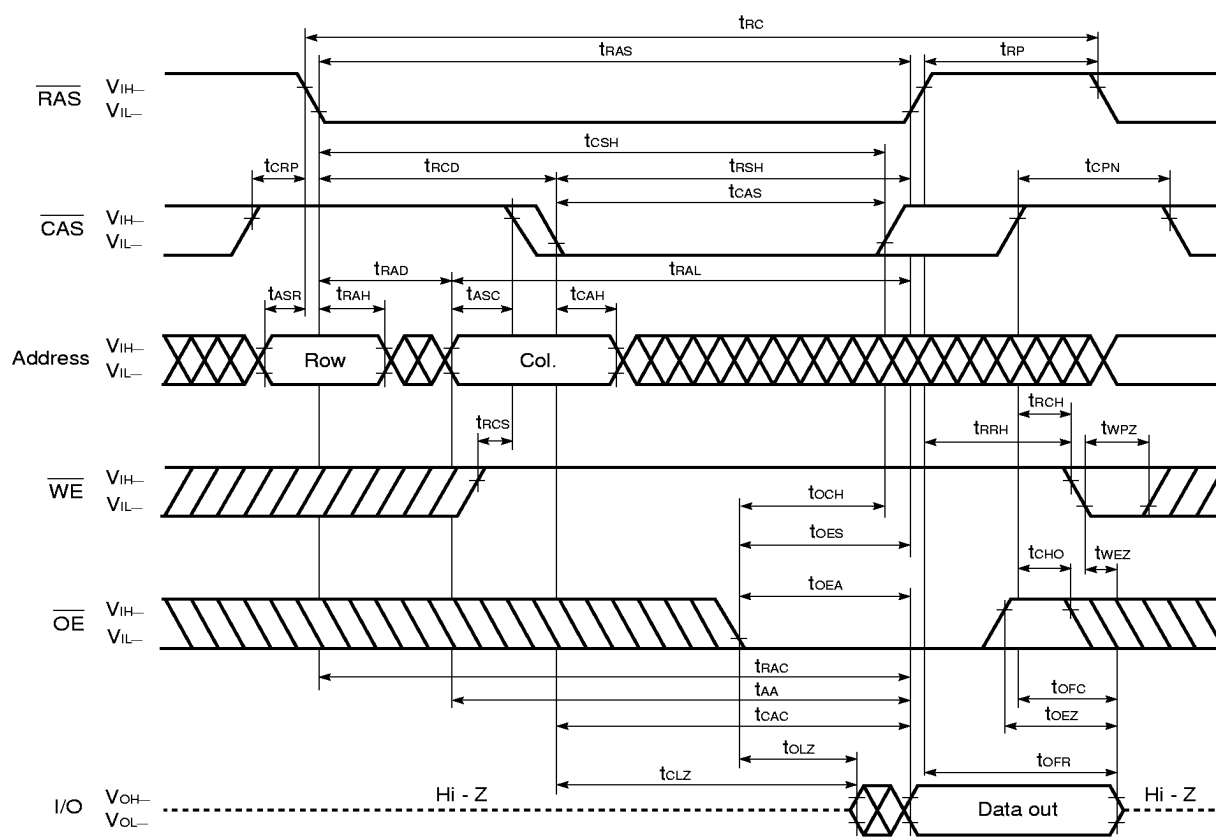
The faster of (1) and (2) becomes effective.

Refresh Cycle

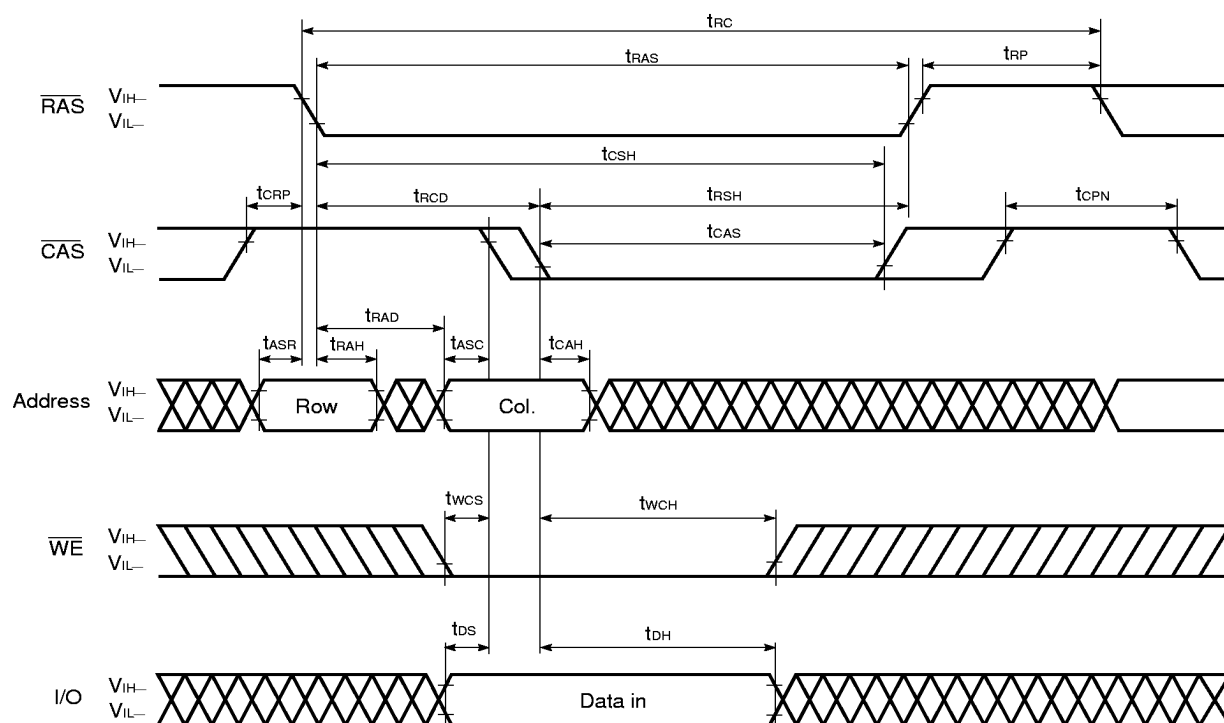
Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{\text{CAS}}$ setup time	t _{CSR}	5	—	5	—	5	—	ns	
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh)	t _{CHR}	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ precharge $\overline{\text{CAS}}$ hold time	t _{RPC}	5	—	5	—	5	—	ns	
$\overline{\text{RAS}}$ pulse width ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh)	t _{RASS}	100	—	100	—	100	—	μs	1
$\overline{\text{RAS}}$ precharge time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh)	t _{RPS}	90	—	110	—	130	—	ns	1
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh)	t _{CHS}	−50	—	−50	—	−50	—	ns	1
$\overline{\text{WE}}$ setup time	t _{WSR}	10	—	10	—	10	—	ns	
$\overline{\text{WE}}$ hold time	t _{WHR}	15	—	15	—	15	—	ns	

Note 1. This specification is applied only to the μPD42S17805.

Read Cycle

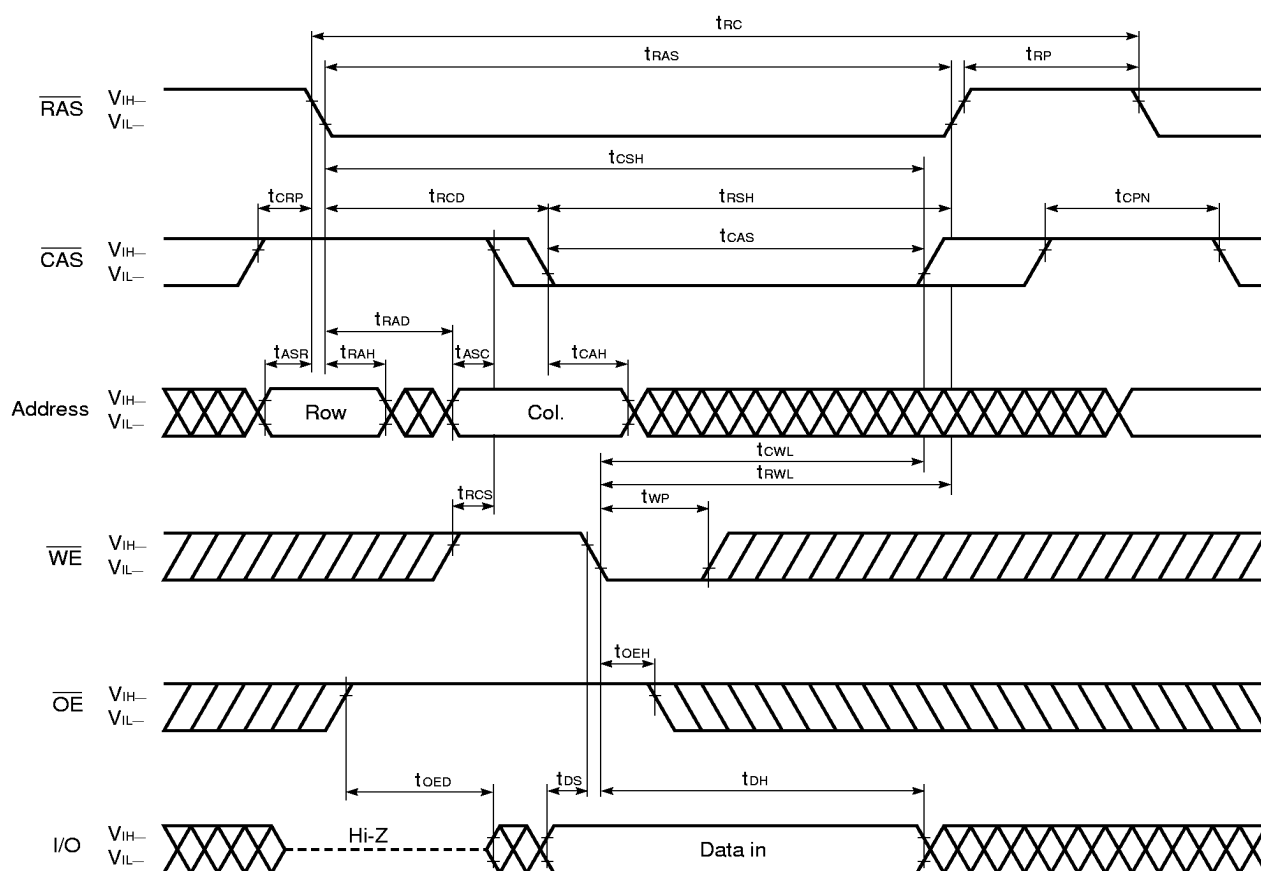


Early Write Cycle

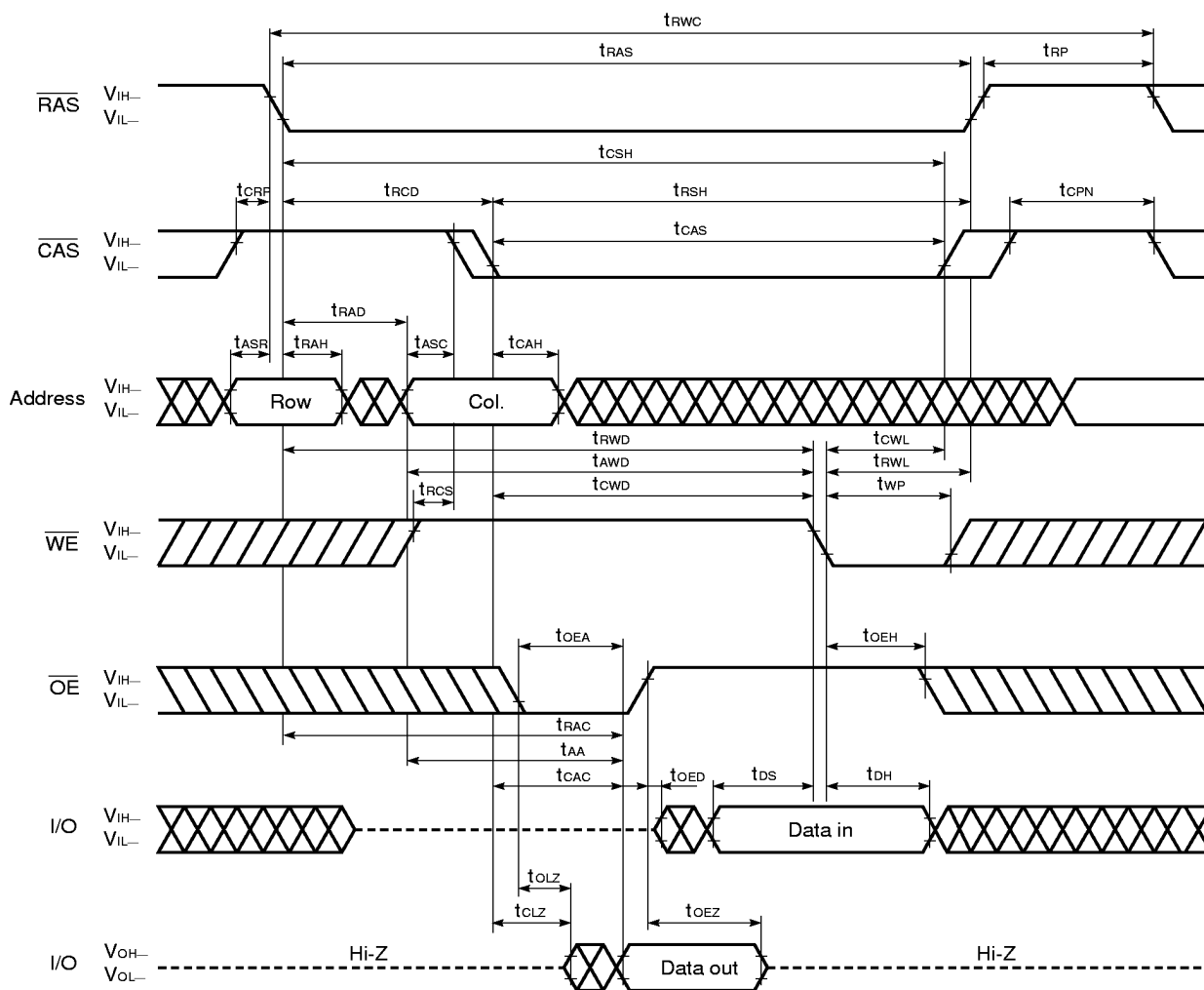


Remark $\overline{OE}$: Don't care

Late Write Cycle



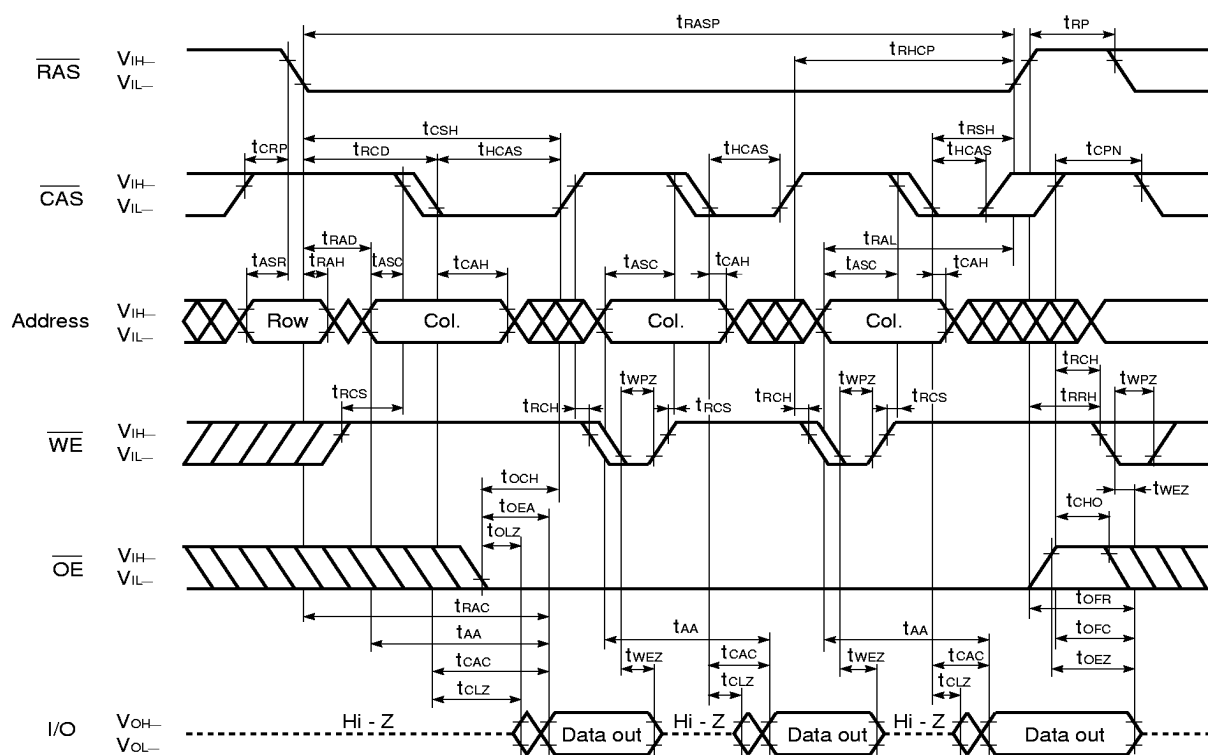
Read Modify Write Cycle



[illegible]

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Hyper Page Mode (EDO) Read Cycle ($\overline{\text{WE}}$ Control)



Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

The timing diagram illustrates the sequence of signals for the 64K1602 LCD module. The signals and their timing parameters are as follows:

- RAS:** $\overline{\text{RAS}}$ signal. Timing parameters: t_{RASP} (RAS pulse width), t_{RHCP} (RAS hold time), t_{RSH} (RAS setup time), t_{RCP} (RAS to CAS delay).
- CAS:** $\overline{\text{CAS}}$ signal. Timing parameters: t_{RCD} (RAS to CAS delay), t_{HCAS} (CAS hold time), t_{CP} (CAS to RAS delay), t_{CAS} (CAS pulse width), t_{CPN} (CAS to next pulse delay).
- Address:** Signal for Row, Col.A, Col.B, and Col.C. Timing parameters: t_{ASR} (Address setup time), t_{RAH} (Address hold time), t_{ASC} (Address to RAS delay), t_{CAH} (Address to CAS hold time), t_{ASC} (Address to RAS delay), t_{CAH} (Address to CAS hold time), t_{ASC} (Address to RAS delay), t_{CAH} (Address to CAS hold time).
- WE:** $\overline{\text{WE}}$ signal. Timing parameters: t_{RAD} (Write Enable to RAS delay), t_{ASC} (Write Enable to Address delay), t_{CAH} (Write Enable to CAS hold time), t_{ASC} (Write Enable to RAS delay), t_{CAH} (Write Enable to CAS hold time), t_{ASC} (Write Enable to RAS delay), t_{CAH} (Write Enable to CAS hold time).
- OE:** $\overline{\text{OE}}$ signal. Timing parameters: t_{ASC} (Output Enable to Address delay), t_{CAH} (Output Enable to CAS hold time), t_{ASC} (Output Enable to RAS delay), t_{CAH} (Output Enable to CAS hold time), t_{ASC} (Output Enable to RAS delay), t_{CAH} (Output Enable to CAS hold time).
- I/O:** Signal for Data out A, Data out B, and Data out C. Timing parameters: t_{ASR} (I/O setup time), t_{RAH} (I/O hold time), t_{ASC} (I/O to RAS delay), t_{CAH} (I/O to CAS hold time), t_{ASC} (I/O to RAS delay), t_{CAH} (I/O to CAS hold time), t_{ASC} (I/O to RAS delay), t_{CAH} (I/O to CAS hold time).

Powered by ICminer.com Electronic-Library Service Copyright 2003

The diagram illustrates the timing relationships for the 16M1602 LCD module. It includes the following signals and parameters:

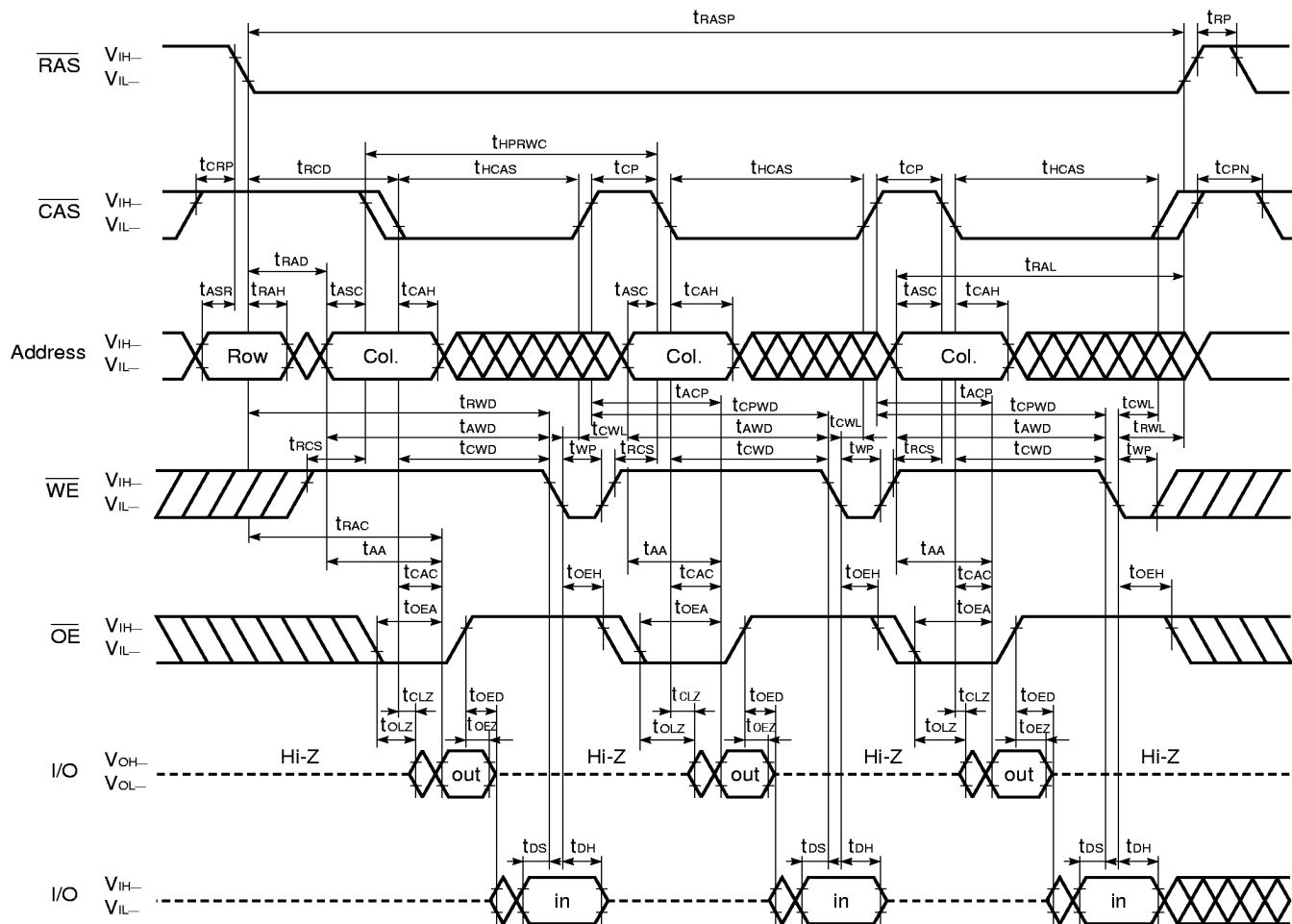
- RAS:** Row Address Strobe. Parameters shown include t_{RAS} (pulse width), t_{RHP} (hold time), t_{CRP} (setup time), t_{RSH} (setup time), and t_{RCP} (hold time).
- CAS:** Column Address Strobe. Parameters shown include t_{CSP} (setup time), t_{CSD} (setup time), t_{CHP} (hold time), t_{CHD} (hold time), t_{CSP} (setup time), t_{CHP} (hold time), t_{CSD} (setup time), t_{CHD} (hold time), and t_{CPN} (hold time).
- Address:** Data bus for Row and Column addresses. Parameters shown include t_{ASR} (setup time), t_{RAH} (hold time), t_{ASC} (setup time), t_{CAH} (hold time), t_{ASC} (setup time), t_{CAH} (hold time), t_{ASC} (setup time), t_{CAH} (hold time), and t_{RAL} (hold time).
- WE:** Write Enable. Parameters shown include t_{WCS} (setup time), t_{WCH} (hold time), t_{WCS} (setup time), t_{WCH} (hold time), t_{WCS} (setup time), t_{WCH} (hold time), and t_{WCS} (setup time).
- I/O:** Data bus for data in/out. Parameters shown include t_{DS} (setup time), t_{DH} (hold time), t_{DS} (setup time), t_{DH} (hold time), t_{DS} (setup time), t_{DH} (hold time), and t_{DS} (setup time).

- Remarks**
1. $\overline{\text{OE}}$: Don't care
 2. In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

The diagram illustrates the timing relationships for a 256K16 DRAM. The signals shown are $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, Address, $\overline{\text{WE}}$, $\overline{\text{OE}}$, and I/O. The I/O signal is shown as a bus with data in and Hi-Z states. The diagram includes various timing parameters such as t_{RASP} , t_{RHCP} , t_{RP} , t_{CRP} , t_{RCD} , t_{HCAS} , t_{CP} , t_{HPCAS} , t_{RSH} , t_{CPN} , t_{RAD} , t_{ASR} , t_{RAH} , t_{ASC} , t_{CAH} , t_{CS} , t_{CWL} , t_{RCS} , t_{WP} , t_{TOEH} , t_{TOED} , t_{DS} , and t_{DH} .

Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

Hyper Page Mode (EDO) Read Modify Write Cycle

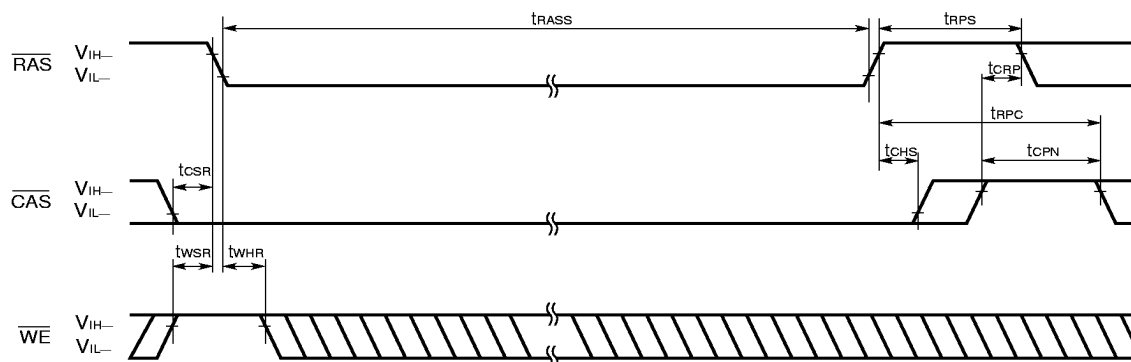


Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

[illegible]

Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

CAS Before RAS Self Refresh Cycle (Only for the μPD42S17805)



Remark Address, $\overline{OE}$: Don't care I/O : Hi-Z

Cautions on Use of CAS Before RAS Self Refresh

CAS before RAS self refresh can be used independently when used in combination with distributed CAS before RAS long refresh; However, when used in combination with burst CAS before RAS long refresh or with long RAS only refresh (both distributed and burst), the following cautions must be observed.

(1) Normal Combined Use of CAS Before RAS Self Refresh and Burst CAS Before RAS Long Refresh

When CAS before RAS self refresh and burst CAS before RAS long refresh are used in combination, please perform CAS before RAS refresh 2,048 times within a 32 ms interval just before and after setting CAS before RAS self refresh.

(2) Normal Combined Use of CAS Before RAS Self Refresh and Long RAS Only Refresh

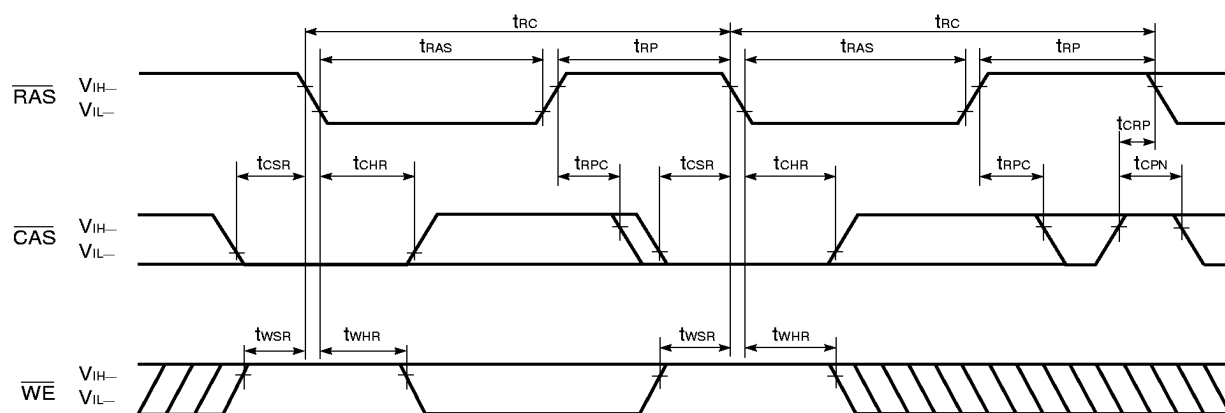
When CAS before RAS self refresh and RAS only refresh are used in combination, please perform RAS only refresh 2,048 times within a 32 ms interval just before and after setting CAS before RAS self refresh.

(3) If $t_{RASS(MIN.)}$ is not satisfied at the beginning of CAS before RAS self refresh cycles ($t_{RAS} < 100 \mu s$), CAS before RAS refresh cycles will be executed one time.

If $10 \mu s < t_{RAS} < 100 \mu s$, RAS precharge time for CAS before RAS self refresh (t_{RPS}) is applied. And refresh cycles (2,048/128 ms) should be met.

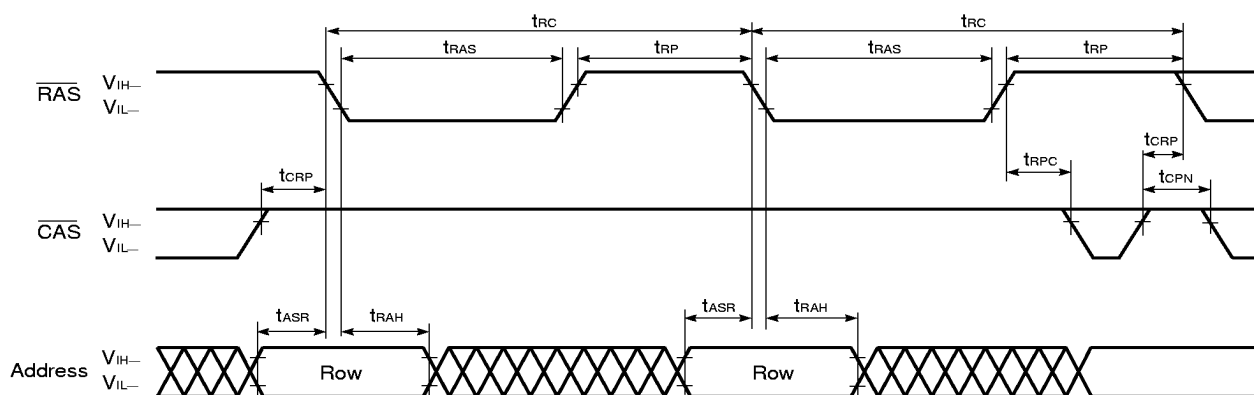
For details, please refer to **How to use DRAM User's Manual**.

CAS Before RAS Refresh Cycle



Remark Address, $\overline{\text{OE}}$: Don't care I/O: Hi-Z

RAS Only Refresh Cycle



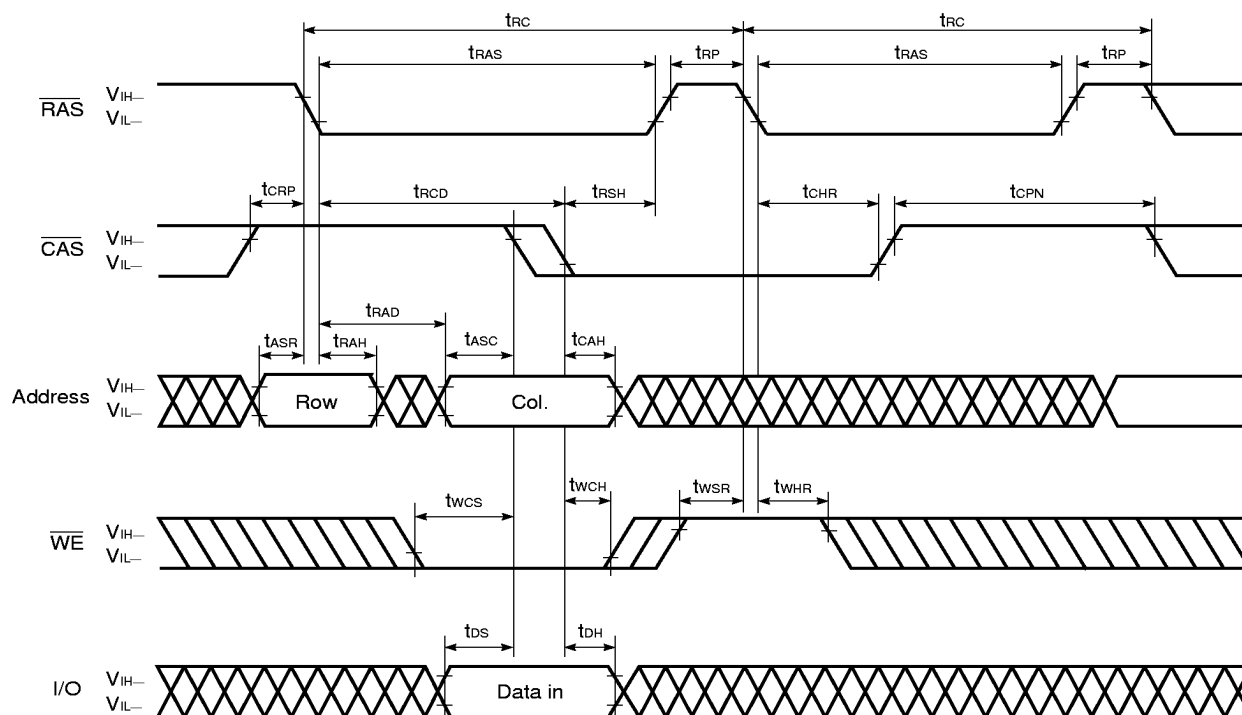
Remark $\overline{\text{WE}}$, $\overline{\text{OE}}$: Don't care I/O: Hi-Z

The diagram illustrates the timing relationships for a 256Kbit DRAM. The signals shown are:

- RAS**: Row Address Strobe, active low. Timing parameters include t_{RC} (total row cycle), t_{RAS} (RAS pulse width), and t_{RP} (RAS precharge time).
- CAS**: Column Address Strobe, active low. Timing parameters include t_{CRP} (CAS precharge time), t_{RCD} (RAS to CAS delay), t_{RSH} (RAS to CAS setup time), t_{CHR} (CAS to RAS delay), and t_{CPN} (CAS precharge time).
- Address**: Row and Column addresses. Timing parameters include t_{ASR} (address setup time), t_{RAH} (address hold time), t_{AD} (address delay), t_{AL} (address latency), t_{AS} (address setup time), t_{AH} (address hold time), t_{SC} (sense amplifiers), and t_{CH} (column hit time).
- WE**: Write Enable, active low. Timing parameters include t_{WHR} (write enable hold time), t_{WPZ} (write enable pulse width), t_{WEZ} (write enable delay), and t_{WEZ} (write enable delay).
- OE**: Output Enable, active low. Timing parameters include t_{OES} (output enable setup time), t_{OEA} (output enable delay), t_{OFC} (output enable delay), t_{OFR} (output enable delay), t_{OES} (output enable setup time), t_{OEA} (output enable delay), t_{OFC} (output enable delay), t_{OFR} (output enable delay).
- I/O**: Data bus. Timing parameters include t_{OLZ} (output load time), t_{CLZ} (column load time), t_{CHQ} (column hit time), t_{FC} (first column delay), t_{FR} (first row delay), t_{EZ} (output enable delay), t_{OZ} (output enable delay), t_{OFC} (output enable delay), t_{OFR} (output enable delay).

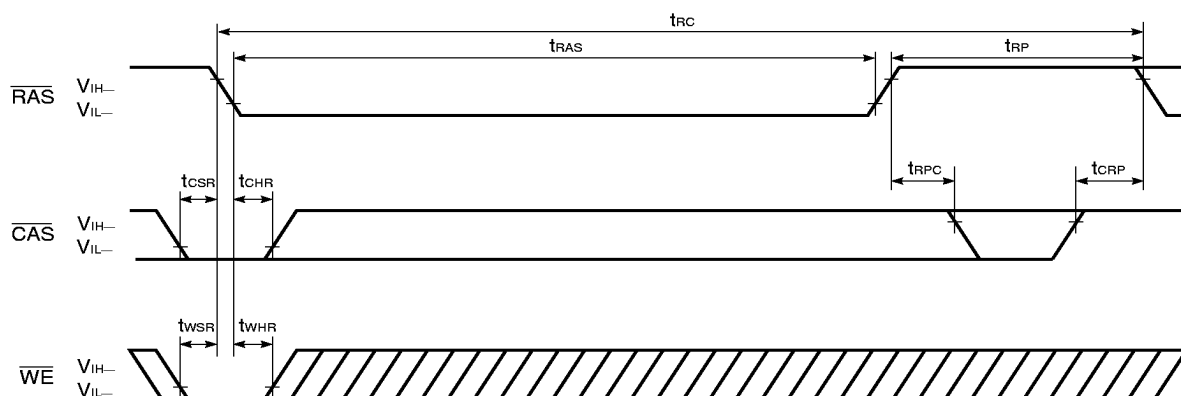
The diagram also shows the data bus state, with "Hi - Z" indicating high impedance and "Data out" indicating data output.

Hidden Refresh Cycle (Write)



Remark $\overline{\text{OE}}$: Don't care

Test Mode Set Cycle ($\overline{\text{WE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle)



Remark Address, $\overline{\text{OE}}$: Don't care I/O: Hi-Z

Test Mode

By using the test mode, the test time can be reduced. The reason for this is that, the memory emulates the $\times 16$ -bit organization during test mode. Don't care about the input levels of the $\overline{\text{CAS}}$ input A0.

(1) Setting the mode

Executing the test mode cycle ($\overline{\text{WE}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle) sets the test mode.

(2) Write/read operation

When either a "0" or a "1" is written to the input pin in test mode, this data is written to 16 bits of memory cell.

Next, when the data is read from the output pin at the same address, the cell can be checked.

Output = "1": Normal write (all memory cells)

Output = "0": Abnormal write

(3) Refresh

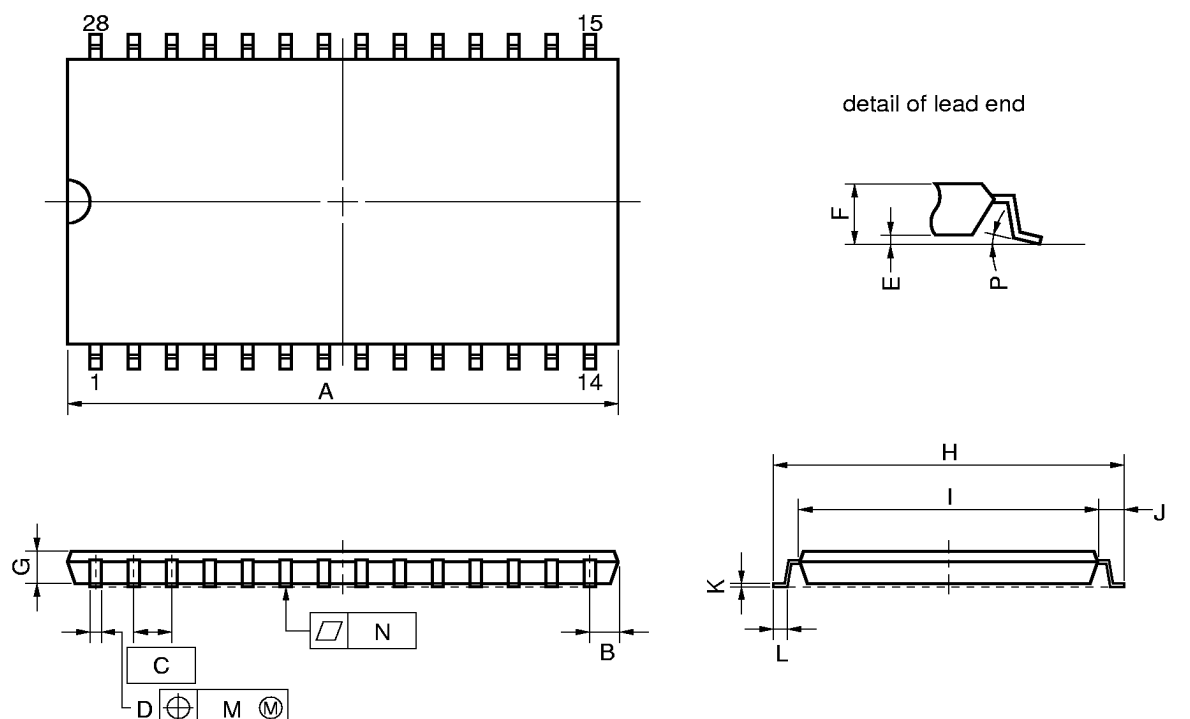
Refresh in the test mode must be performed with the $\overline{\text{RAS}}$ / $\overline{\text{CAS}}$ cycle or with the $\overline{\text{WE}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle. The $\overline{\text{WE}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle use the same counter as the $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh's internal counter.

(4) Mode Cancellation

The test mode is cancelled by executing one cycle of $\overline{\text{RAS}}$ only refresh cycle or $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle.

Package Drawings

28PIN PLASTIC TSOP(II) (400 mil)



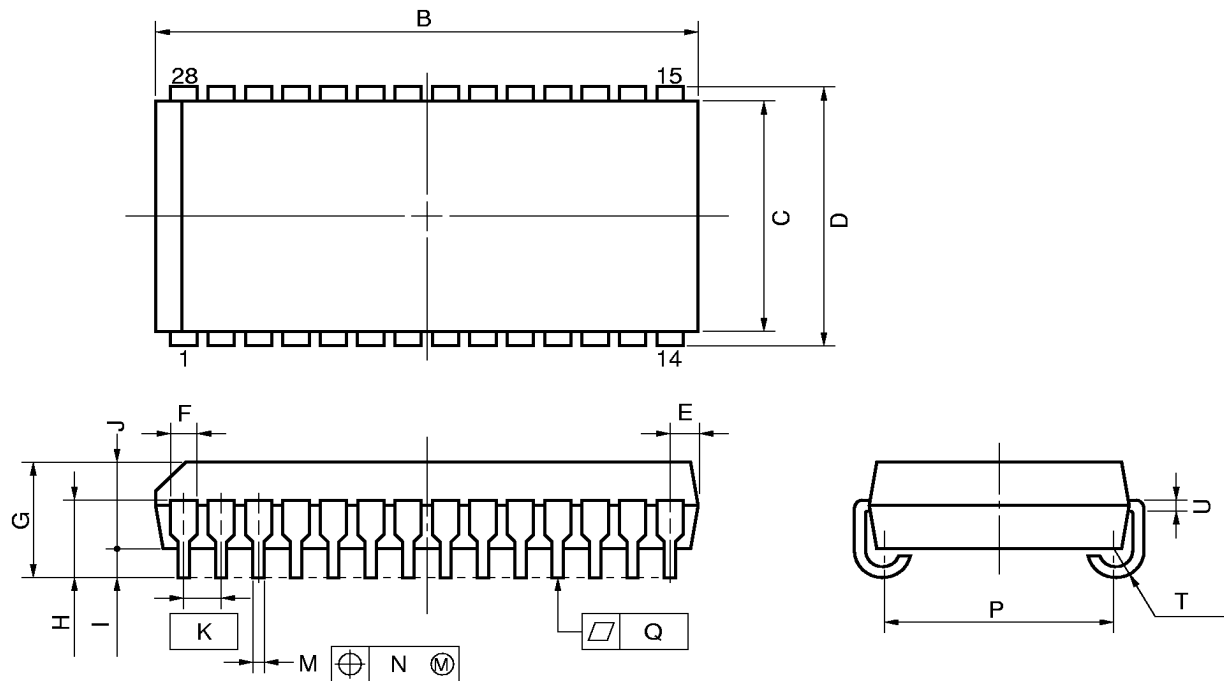
NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	18.63 MAX.	0.734 MAX.
B	1.075 MAX.	0.043 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.42^{+0.08}_{-0.07}$	0.017 ± 0.003
E	0.1 ± 0.05	0.004 ± 0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	11.76 ± 0.2	0.463 ± 0.008
I	10.16 ± 0.1	0.400 ± 0.004
J	0.8 ± 0.2	$0.031^{+0.009}_{-0.008}$
K	$0.145^{+0.025}_{-0.015}$	0.006 ± 0.001
L	0.5 ± 0.1	$0.020^{+0.004}_{-0.005}$
M	0.21	0.009
N	0.10	0.004
P	$3^{\circ} +7^{\circ}_{-3^{\circ}}$	$3^{\circ} +7^{\circ}_{-3^{\circ}}$

S28G5-50-7JD3

28 PIN PLASTIC SOJ (400 mil)



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

P28LE-400A1

ITEM	MILLIMETERS	INCHES
B	18.67 ^{+0.2} _{-0.35}	0.735 ^{+0.008} _{-0.013}
C	10.16	0.400
D	11.18±0.2	0.440 ^{+0.008} _{-0.007}
E	1.08±0.15	0.043 ^{+0.006} _{-0.007}
F	0.74	0.029
G	3.5±0.2	0.138 ^{+0.008} _{-0.007}
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	0.016 ^{+0.004} _{-0.005}
N	0.12	0.005
P	9.40±0.20	0.370 ^{+0.008} _{-0.007}
Q	0.10	0.004
T	R 0.85	R 0.033
U	0.20 ^{+0.10} _{-0.05}	0.008 ^{+0.004} _{-0.002}

★ Recommended Soldering Conditions

The following conditions (see tables below and next page) must be met for soldering conditions of the μPD42S17805, 4217805.

For more details, refer to our document “SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL” (C10535E).

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

Types of Surface Mount Device

μPD42S17805G5-7JD, 4217805G5-7JD: 28-pin plastic TSOP (II) (400 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface: 235 °C or lower, Reflow time: 30 seconds or less (210 °C or higher), Number of reflow processes: MAX. 3 Exposure limit: 7 days ^{Note} (10 hours pre-baking is required at 125 °C afterwards)	IR35-107-3
VPS	Peak temperature of package: 215 °C or lower, Reflow time: 40 seconds or less (200 °C or higher), Number of reflow processes: MAX. 3 Exposure limit: 7 days ^{Note} (10 hours pre-baking is required at 125 °C afterwards)	VP15-107-3
Partial heating method	Terminal temperature: 300 °C or lower, Time: 3 seconds or lower (Per side of the package).	—

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for “Partial heating method”.

μPD42S17805LE, 4217805LE: 28-pin plastic SOJ (400 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface: 235 °C or lower, Reflow time: 30 seconds or less (210 °C or higher), Number of reflow processes: MAX. 3 Exposure limit: 7 days ^{Note} (20 hours pre-baking is required at 125 °C afterwards)	IR35-207-3
VPS	Peak temperature of package: 215 °C or lower, Reflow time: 40 seconds or less (200 °C or higher), Number of reflow processes: MAX. 3 Exposure limit: 7 days ^{Note} (20 hours pre-baking is required at 125 °C afterwards)	VP15-207-3
Partial heating method	Terminal temperature: 300 °C or lower, Time: 3 seconds or less (Per side of the package).	—

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for “Partial heating method”.