

MOS INTEGRATED CIRCUIT
μPD42S4170, 424170, 42S4270, 424270

4 M-BIT DYNAMIC RAM
256K-WORD BY 16-BIT, FAST PAGE MODE, BYTE WRITE MODE

DESCRIPTION

The μPD42S4170, 424170, 42S4270, 424270 are 262 144 words by 16 bits dynamic CMOS RAMs. The fast page mode and byte write mode capability realize high speed access and low power consumption.

Besides, the μPD42S4170, 42S4270 can execute $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh. Refresh cycles are 1 024 cycles on the μPD42S4170, 424170 and 512 cycles on the μPD42S4270, 424270.

These are packaged in 44-pin plastic TSOP, 40-pin plastic SOJ and 40-pin plastic ZIP (only for μPD42S4170, 424170).

FEATURES

- 262 144 words by 16 bits organization
- Single +5.0 V ± 10 % power supply
- Fast access and cycle time

Part number	Power consumption Active (MAX.)	Access time (MAX.)	R/W cycle time (MIN.)	Fast page mode cycle time (MIN.)
μPD42S4170-70	660.0 mW	70 ns	130 ns	45 ns
μPD424170-70				
μPD42S4170-80	577.5 mW	80 ns	150 ns	50 ns
μPD424170-80				
μPD42S4270-70	880.0 mW	70 ns	130 ns	45 ns
μPD424270-70				
μPD42S4270-80	797.5 mW	80 ns	150 ns	50 ns
μPD424270-80				
μPD42S4270-10	660.0 mW	100 ns	190 ns	65 ns
μPD424270-10				

- μPD42S4170, 42S4270 can execute $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh

Part number	Refresh cycle	Refresh	Power consumption at standby (MAX.)
μPD42S4170	1 024 cycles/128 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh	1.1 mW (CMOS level input)
μPD42S4270	512 cycles/128 ms		
μPD424170	1 024 cycles/ 16 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh	5.5 mW (CMOS level input)
μPD424270	512 cycles/ 8 ms		

The information in this document is subject to change without notice.

The mark ★ shows revised points.

- Multiplexed address inputs

Part number	Row address	Column address
μPD42S4170, 424170	A0 to A9	A0 to A7
μPD42S4270, 424270	A0 to A8	A0 to A8

ORDERING INFORMATION

Part number	Access time (MAX.)	Package	Refresh
μPD42S4170G5-70-7JF	70 ns	44-pin Plastic TSOP	CAS before RAS self refresh RAS only refresh CAS before RAS refresh Hidden refresh
μPD42S4270G5-70-7JF			
μPD42S4170G5-80-7JF	80 ns		
μPD42S4270G5-80-7JF			
μPD42S4270G5-10-7JF	100 ns		
μPD42S4170G5-70-7KF	70 ns	44-pin Plastic TSOP (Reverse bent)	
μPD42S4270G5-70-7KF			
μPD42S4170G5-80-7KF	80 ns		
μPD42S4270G5-80-7KF			
μPD42S4270G5-10-7KF	100 ns		
μPD42S4170LE-70	70 ns	40-pin Plastic SOJ	
μPD42S4270LE-70			
μPD42S4170LE-80	80 ns		
μPD42S4270LE-80			
μPD42S4270LE-10	100 ns		
μPD42S4170V-70	70 ns	40-pin Plastic ZIP	
μPD42S4170V-80	80 ns		
μPD424170G5-70-7JF	70 ns	44-pin Plastic TSOP	RAS only refresh CAS before RAS refresh Hidden refresh
μPD424270G5-70-7JF			
μPD424170G5-80-7JF	80 ns		
μPD424270G5-80-7JF			
μPD424270G5-10-7JF	100 ns		
μPD424170G5-70-7KF	70 ns	44-pin Plastic TSOP (Reverse bent)	
μPD424270G5-70-7KF			
μPD424170G5-80-7KF	80 ns		
μPD424270G5-80-7KF			
μPD424270G5-10-7KF	100 ns		
μPD424170LE-70	70 ns	40-pin Plastic SOJ	
μPD424270LE-70			
μPD424170LE-80	80 ns		
μPD424270LE-80			
μPD424270LE-10	100 ns		
μPD424170V-70	70 ns	40-pin Plastic ZIP	
μPD424170V-80	80 ns		

QUALITY GRADE

STANDARD

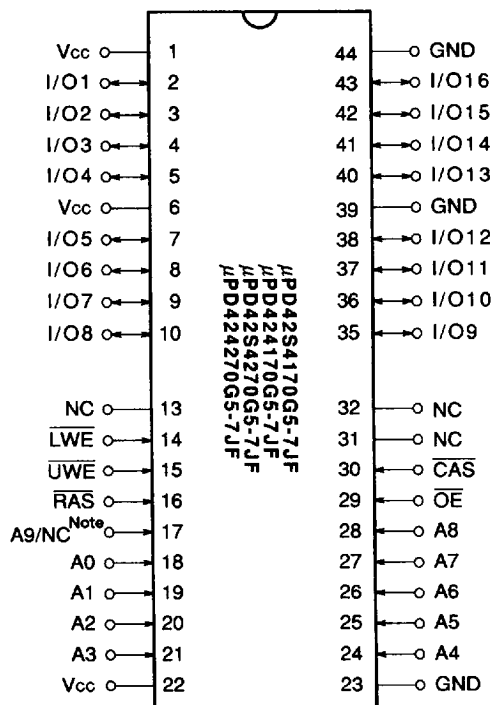
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

PIN CONFIGURATIONS



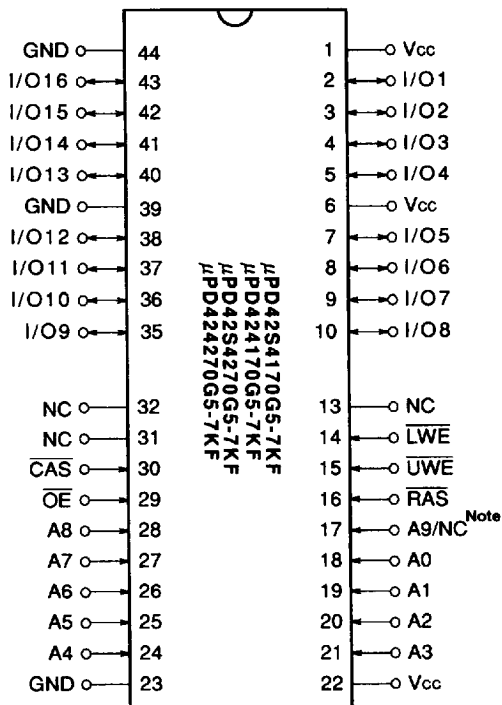
44-pin Plastic TSOP

(Marking Side)



44-pin Plastic TSOP (Reverse bent)

(Marking Side)



Note A9 ... μPD42S4170, 424170

NC ... μPD42S4270, 424270 (No connection)

A0 to A9 : Address Inputs

I/O1 to I/O16 : Data Inputs/Outputs

$\overline{\text{RAS}}$: Row Address Strobe

$\overline{\text{CAS}}$: Column Address Strobe

$\overline{\text{UWE}}$: Upper Byte Write Enable

$\overline{\text{LWE}}$: Lower Byte Write Enable

$\overline{\text{OE}}$: Output Enable

Vcc : Power Supply (+5.0 V $\pm$ 10 %)

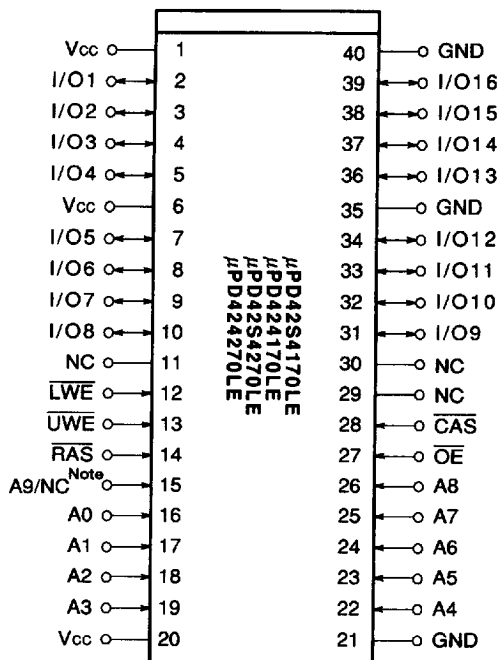
GND : Ground

NC : No Connection

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40-pin Plastic SOJ

(Top View)

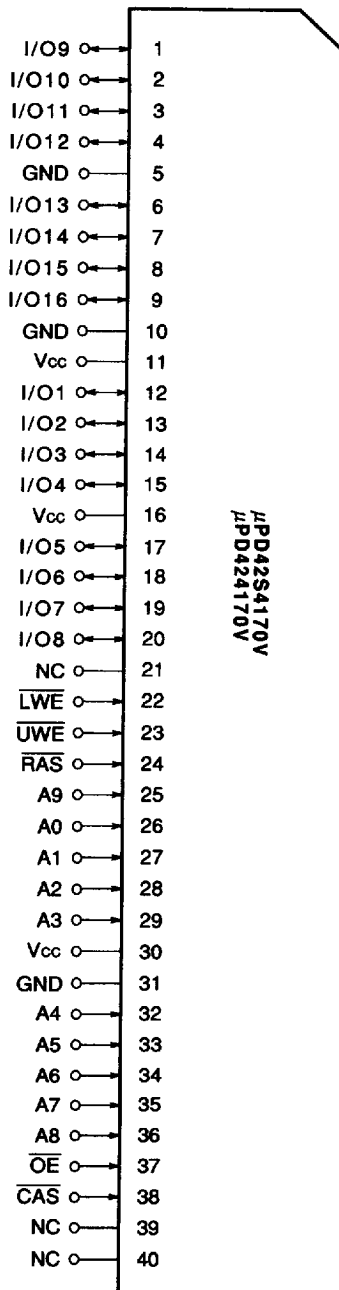


Note A9 ... μPD42S4170, 424170

NC ... μPD42S4270, 424270 (No connection)

40-pin Plastic ZIP (Only for μPD42S4170, 424170)

(Front View)



A0 to A9 : Address Inputs

I/O1 to I/O16 : Data Inputs/Outputs

RAS : Row Address Strobe

CAS : Column Address Strobe

UWE : Upper Byte Write Enable

LWE : Lower Byte Write Enable

OE : Output Enable

Vcc : Power Supply (+5.0 V ± 10 %)

GND : Ground

NC : No Connection

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ELECTRICAL SPECIFICATIONS NOTE 1

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	CONDITION	RATING	UNIT
Voltage on Any Pin Relative to GND	V_T		-1.0 to +7.0	V
Supply Voltage	V_{CC}		-1.0 to +7.0	V
Output Current	I_O		50	mA
Power Dissipation	P_D		1	W
Operating Temperature	T_{opt}		0 to +70	°C
Storage Temperature	T_{stg}		-55 to +125	°C

Remark Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS NOTE 2, 3

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
High Level Input Voltage	V_{IH}		2.4		$V_{CC} + 1.0$	V
Low Level Input Voltage	V_{IL}		-0.3		+0.8	V
Ambient Temperature	T_a		0		70	°C

CAPACITANCE ($T_a = +25\text{ °C}$, $f = 1\text{ MHz}$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$			7	pF
Data Input/Output Capacitance	C_D	I/O1 to I/O16			7	pF

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★ DC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted)

[μPD42S4170, 424170]

PARAMETER		SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT	NOTE
Operating current		I _{CC1}	RAS, CAS Cycling t _{RC} = t _{RC(MIN)} , I _O = 0 mA	t _{RAC} = 70 ns	120	mA	4, 5
				t _{RAC} = 80 ns	105		
Standby current	μPD42S4170	I _{CC2}	V _{IH(MIN)} ≤ RAS, CAS I _O = 0 mA		2	mA	
			V _{CC-0.2 V} ≤ RAS, CAS I _O = 0 mA		0.2		
	μPD424170		V _{IH(MIN)} ≤ RAS, CAS I _O = 0 mA		2		
			V _{CC-0.2 V} ≤ RAS, CAS I _O = 0 mA		1		
RAS only refresh current		I _{CC3}	RAS Cycling, V _{IH(MIN)} ≤ CAS t _{RC} = t _{RC(MIN)} , I _O = 0 mA	t _{RAC} = 70 ns	120	mA	4, 5
				t _{RAC} = 80 ns	105		
Operating current (Fast page mode)		I _{CC4}	RAS ≤ V _{IL(MAX)} CAS Cycling, t _{PC} = t _{PC(MIN)} , I _O = 0 mA	t _{RAC} = 70 ns	100	mA	4, 5
				t _{RAC} = 80 ns	90		
CAS before RAS refresh current		I _{CC5}	RAS Cycling, t _{RC} = t _{RC(MIN)} , I _O = 0 mA	t _{RAC} = 70 ns	120	mA	4, 5
				t _{RAC} = 80 ns	105		
CAS before RAS long refresh current (1 024 cycles/128 ms, only for μPD42S4170)		I _{CC6}	Standby : V _{CC-0.2 V} ≤ RAS, CAS ≤ V _{IH(MAX)} CAS before RAS refresh : 1 024 cycles/128 ms RAS, CAS : 0 V ≤ V _{IL} ≤ 0.2 V V _{CC-0.2 V} ≤ V _{IH} ≤ V _{IH(MAX)} WE, OE: V _{IH} Address input : V _{IH} or V _{IL} Output : Hi-Z	t _{RAS} ≤ 200 ns	200	μA	4, 5
				t _{RAS} ≤ 1 μs	300		
Self refresh current (CAS before RAS self refresh, only for μPD42S4170)		I _{CC7}	I _O = 0 mA RAS, CAS : 0 V ≤ V _{IL} ≤ 0.2 V V _{CC-0.2 V} ≤ V _{IH} ≤ V _{IH(MAX)}		150	μA	
Input leakage current		I _{I(L)}	V _I = 0 to 5.5 V all other pins except for testing pin = 0 V	-10	+10	μA	
Output leakage current		I _{O(L)}	Output is disabled (Hi-Z) V _O = 0 to 5.5 V	-10	+10	μA	
High level output voltage		V _{OH}	I _O = -2.5 mA	2.4		V	
Low level output voltage		V _{OL}	I _O = 2.1 mA		0.4	V	

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[μ PD42S4270, 424270]

PARAMETER		SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT	NOTE
Operating current		I _{CC1}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ Cycling $t_{\text{RC}} = t_{\text{RC}}(\text{MIN})$, $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 70 \text{ ns}$	160	mA	4, 5
				$t_{\text{RAC}} = 80 \text{ ns}$	145		
				$t_{\text{RAC}} = 100 \text{ ns}$	120		
Standby current	μ PD42S4270	I _{CC2}	$V_{\text{IH}}(\text{MIN}) \leq \overline{\text{RAS}}, \overline{\text{CAS}}$ $I_o = 0 \text{ mA}$		2	mA	
			$V_{\text{CC}} - 0.2 \text{ V} \leq \overline{\text{RAS}}, \overline{\text{CAS}}$ $I_o = 0 \text{ mA}$		0.2		
	μ PD424270		$V_{\text{IH}}(\text{MIN}) \leq \overline{\text{RAS}}, \overline{\text{CAS}}$ $I_o = 0 \text{ mA}$		2		
			$V_{\text{CC}} - 0.2 \text{ V} \leq \overline{\text{RAS}}, \overline{\text{CAS}}$ $I_o = 0 \text{ mA}$		1		
$\overline{\text{RAS}}$ only refresh current		I _{CC3}	$\overline{\text{RAS}}$ Cycling, $V_{\text{IH}}(\text{MIN}) \leq \overline{\text{CAS}}$ $t_{\text{RC}} = t_{\text{RC}}(\text{MIN})$, $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 70 \text{ ns}$	160	mA	4, 5
				$t_{\text{RAC}} = 80 \text{ ns}$	145		
				$t_{\text{RAC}} = 100 \text{ ns}$	120		
Operating current (Fast page mode)		I _{CC4}	$\overline{\text{RAS}} \leq V_{\text{IL}}(\text{MAX})$ $\overline{\text{CAS}}$ Cycling, $t_{\text{PC}} = t_{\text{PC}}(\text{MIN})$, $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 70 \text{ ns}$	140	mA	4, 5
				$t_{\text{RAC}} = 80 \text{ ns}$	130		
				$t_{\text{RAC}} = 100 \text{ ns}$	100		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh current		I _{CC5}	$\overline{\text{RAS}}$ Cycling, $t_{\text{RC}} = t_{\text{RC}}(\text{MIN})$, $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 70 \text{ ns}$	160	mA	4, 5
				$t_{\text{RAC}} = 80 \text{ ns}$	145		
				$t_{\text{RAC}} = 100 \text{ ns}$	120		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ long refresh current (512 cycles/128 ms, only for μ PD42S4270)		I _{CC6}	Standby : $V_{\text{CC}} - 0.2 \text{ V} \leq \overline{\text{RAS}}, \overline{\text{CAS}} \leq V_{\text{IH}}(\text{MAX})$ $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh : 512 cycles/128 ms $\overline{\text{RAS}}, \overline{\text{CAS}} : 0 \text{ V} \leq V_{\text{IL}} \leq 0.2 \text{ V}$ $V_{\text{CC}} - 0.2 \text{ V} \leq V_{\text{IH}} \leq V_{\text{IH}}(\text{MAX})$ $\overline{\text{WE}}, \overline{\text{OE}} : V_{\text{IH}}$ Address input : V_{IH} or V_{IL} Output : Hi-Z	$t_{\text{RAS}} \leq 200 \text{ ns}$	200	μA	4, 5
				$t_{\text{RAS}} \leq 1 \mu\text{s}$	300		
Self refresh current ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh, only for μ PD42S4270)		I _{CC7}	$I_o = 0 \text{ mA}$ $\overline{\text{RAS}}, \overline{\text{CAS}} : 0 \text{ V} \leq V_{\text{IL}} \leq 0.2 \text{ V}$ $V_{\text{CC}} - 0.2 \text{ V} \leq V_{\text{IH}} \leq V_{\text{IH}}(\text{MAX})$		150	μA	
Input leakage current		I _{I(L)}	$V_i = 0 \text{ to } 5.5 \text{ V}$ all other pins except for testing pin = 0 V	-10	+10	μA	
Output leakage current		I _{O(L)}	Output is disabled (Hi-Z) $V_o = 0 \text{ to } 5.5 \text{ V}$	-10	+10	μA	
High level output voltage		V _{OH}	$I_o = -2.5 \text{ mA}$	2.4		V	
Low level output voltage		V _{OL}	$I_o = 2.1 \text{ mA}$		0.4	V	

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AC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted) NOTE 6, 7

[μ PD42S4170, 424170]

(1/2)

PARAMETER	SYMBOL	t _{RAC} = 70 ns		t _{RAC} = 80 ns		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Random Read or Write Cycle Time	t _{RC}	130		150		ns	8
Read Modify Write Cycle Time	t _{RWC}	175		200		ns	8
Fast Page Mode Cycle Time	t _{PC}	45		50		ns	8
Read Modify Write Cycle Time (Fast Page Mode)	t _{PRWC}	90		105		ns	8
Access Time from $\overline{\text{RAS}}$	t _{RAC}		70		80	ns	9, 10
Access Time from $\overline{\text{CAS}}$	t _{CAC}		20		20	ns	9, 10
Access Time from Column Address	t _{AA}		35		40	ns	9, 10
Access Time from $\overline{\text{CAS}}$ Precharge	t _{ACP}		40		45	ns	10
$\overline{\text{CAS}}$ to Output Data Setup Time	t _{CLZ}	0		0		ns	10
Output Buffer Turn-off Delay Time ($\overline{\text{CAS}}$)	t _{OFF}	0	15	0	20	ns	11
Transition Time (rise and fall)	t _T	3	50	3	50	ns	
$\overline{\text{RAS}}$ Precharge Time	t _{RP}	50		60		ns	
$\overline{\text{RAS}}$ Pulse Width	t _{RAS}	70	10 000	80	10 000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t _{RASP}	70	125 000	80	125 000	ns	
$\overline{\text{RAS}}$ Hold Time	t _{RSH}	20		20		ns	
$\overline{\text{CAS}}$ Hold Time	t _{CSH}	70		80		ns	
$\overline{\text{CAS}}$ Pulse Width	t _{CAS}	20	10 000	20	10 000	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t _{RCD}	20	50	20	60	ns	9
$\overline{\text{RAS}}$ to Column Address Delay Time	t _{RAD}	15	35	15	40	ns	9
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t _{CRP}	10		10		ns	12
$\overline{\text{CAS}}$ Precharge Time (Fast Page Mode)	t _{CP}	10		10		ns	
Row Address Setup Time	t _{ASR}	0		0		ns	
Row Address Hold Time	t _{RAH}	10		10		ns	
Column Address Setup Time	t _{ASC}	0		0		ns	
Column Address Hold Time	t _{CAH}	15		15		ns	
$\overline{\text{CAS}}$ Precharge Time	t _{CPN}	10		10		ns	
Column Address Lead Time Referenced to $\overline{\text{RAS}}$	t _{RAL}	35		40		ns	
Read Command Setup Time	t _{RCS}	0		0		ns	
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t _{RCH}	0		0		ns	13
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t _{RRH}	0		0		ns	13
Write Command Hold Time Referenced to $\overline{\text{CAS}}$	t _{WCH}	15		15		ns	14
Write Command Pulse Width	t _{Wp}	15		15		ns	14
Write Command Lead Time Referenced to $\overline{\text{RAS}}$	t _{RWL}	20		25		ns	
Write Command Lead Time Referenced to $\overline{\text{CAS}}$	t _{CWL}	15		20		ns	
Data-in Setup Time	t _{DS}	0		0		ns	15
Data-in Hold Time	t _{DH}	15		20		ns	15

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(2/2)

PARAMETER		SYMBOL	t _{RAC} = 70 ns		t _{RAC} = 80 ns		UNIT	NOTE
			MIN.	MAX.	MIN.	MAX.		
Refresh Time	μ PD42S4170	t _{REF}		128		128	ms	17
	μ PD424170			16		16	ms	
Write Command Setup Time		t _{WCS}	0		0		ns	16
CAS to WE Delay Time		t _{CWD}	40		45		ns	16
RAS to WE Delay Time		t _{RWD}	90		105		ns	16
CAS Precharge Delay Time Referenced to WE (Fast Page Mode)		t _{CPWD}	60		70		ns	16
Column Address Delay Time Referenced to WE		t _{AWD}	55		65		ns	16
CAS Setup Time (CAS before RAS Refresh)		t _{CSR}	10		10		ns	
CAS Hold Time (CAS before RAS Refresh)		t _{CHR}	15		15		ns	
RAS Precharge CAS Hold Time		t _{RPC}	10		10		ns	
OE to RAS inactive Setup Time		t _{OES}	0		0		ns	
Access Time from OE		t _{OEA}		20		20	ns	
OE Data Delay Time		t _{OED}	15		20		ns	
Output Buffer Turn-off Delay Time (OE)		t _{OEZ}	0	15	0	20	ns	11
OE Output Data Setup Time		t _{OLZ}	0		0		ns	
OE Hold Time		t _{OEH}	0		0		ns	
Masked Byte Write Setup Time		t _{MCS}	0		0		ns	
Masked Byte Write Hold Time Referenced to RAS		t _{MRH}	0		0		ns	
Masked Byte Write Hold Time Referenced to CAS		t _{MCH}	0		0		ns	
RAS Hold Time Referenced to CAS Precharge		t _{RHCP}	40		45		ns	
RAS Pulse Width (CAS before RAS Self Refresh)		t _{RASS}	100		100		μ s	17
RAS Precharge Time (CAS before RAS Self Refresh)		t _{RPS}	130		150		ns	17
CAS Hold Time (CAS before RAS Self Refresh)		t _{CHS}	-50		-50		ns	17

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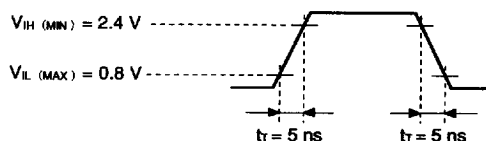
[μPD42S4270, 424270]

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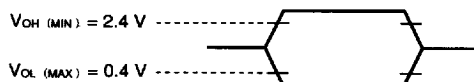
PARAMETER	SYMBOL	t _{RAC} = 70 ns		t _{RAC} = 80 ns		t _{RAC} = 100 ns		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Random Read or Write Cycle Time	t _{RC}	130		150		190		ns	8
Read Modify Write Cycle Time	t _{RWC}	175		200		255		ns	8
Fast Page Mode Cycle Time	t _{PC}	45		50		65		ns	8
Read Modify Write Cycle Time (Fast Page Mode)	t _{PRWC}	90		105		125		ns	8
Access Time from $\overline{\text{RAS}}$	t _{RAC}		70		80		100	ns	9, 10
Access Time from $\overline{\text{CAS}}$	t _{CAC}		20		20		25	ns	9, 10
Access Time from Column Address	t _{AA}		35		40		50	ns	9, 10
Access Time from $\overline{\text{CAS}}$ Precharge	t _{ACP}		40		45		55	ns	10
$\overline{\text{CAS}}$ to Output Data Setup Time	t _{CLZ}	0		0		0		ns	10
Output Buffer Turn-off Delay Time ($\overline{\text{CAS}}$)	t _{OFF}	0	15	0	20	0	20	ns	11
Transition Time (rise and fall)	t _T	3	50	3	50	3	50	ns	
$\overline{\text{RAS}}$ Precharge Time	t _{RP}	50		60		80		ns	
$\overline{\text{RAS}}$ Pulse Width	t _{RAS}	70	10 000	80	10 000	100	10 000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t _{RASP}	70	125 000	80	125 000	100	125 000	ns	
$\overline{\text{RAS}}$ Hold Time	t _{RS}	20		20		30		ns	
$\overline{\text{CAS}}$ Hold Time	t _{CS}	70		80		100		ns	
$\overline{\text{CAS}}$ Pulse Width	t _{CAS}	20	10 000	20	10 000	30	10 000	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t _{RC}	20	50	20	60	25	75	ns	9
$\overline{\text{RAS}}$ to Column Address Delay Time	t _{RAD}	15	35	15	40	20	50	ns	9
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t _{CRP}	10		10		10		ns	12
$\overline{\text{CAS}}$ Precharge Time (Fast Page Mode)	t _{CP}	10		10		10		ns	
Row Address Setup Time	t _{ASR}	0		0		0		ns	
Row Address Hold Time	t _{RAH}	10		10		15		ns	
Column Address Setup Time	t _{ASC}	0		0		0		ns	
Column Address Hold Time	t _{CAH}	15		15		20		ns	
$\overline{\text{CAS}}$ Precharge Time	t _{CPN}	10		10		10		ns	
Column Address Lead Time Referenced to $\overline{\text{RAS}}$	t _{RAL}	35		40		50		ns	
Read Command Setup Time	t _{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t _{RCH}	0		0		0		ns	13
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t _{RRH}	0		0		0		ns	13
Write Command Hold Time Referenced to $\overline{\text{CAS}}$	t _{WCH}	15		15		20		ns	14
Write Command Pulse Width	t _{WP}	15		15		20		ns	14
Write Command Lead Time Referenced to $\overline{\text{RAS}}$	t _{RWL}	20		25		25		ns	
Write Command Lead Time Referenced to $\overline{\text{CAS}}$	t _{CWL}	15		20		25		ns	
Data-in Setup Time	t _{DS}	0		0		0		ns	15
Data-in Hold Time	t _{DH}	15		20		20		ns	15

PARAMETER		SYMBOL	t _{RAC} = 70 ns		t _{RAC} = 80 ns		t _{RAC} = 100 ns		UNIT	NOTE
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Refresh Time	μPD42S4270	t _{REF}		128		128		128	ms	17
	μPD424270			8		8		8	ms	
Write Command Setup Time		t _{WCS}	0		0		0		ns	16
CAS to WE Delay Time		t _{CWD}	40		45		60		ns	16
RAS to WE Delay Time		t _{RWD}	90		105		135		ns	16
CAS Precharge Delay Time Referenced to WE (Fast Page Mode)		t _{CPWD}	60		70		85		ns	16
Column Address Delay Time Referenced to WE		t _{AWD}	55		65		90		ns	16
CAS Setup Time (CAS before RAS Refresh)		t _{CSR}	10		10		10		ns	
CAS Hold Time (CAS before RAS Refresh)		t _{CHR}	15		15		20		ns	
RAS Precharge CAS Hold Time		t _{RPC}	10		10		10		ns	
OE to RAS inactive Setup Time		t _{OES}	0		0		0		ns	
Access Time from OE		t _{OEA}		20		25		25	ns	
OE Data Delay Time		t _{OED}	15		20		25		ns	
Output Buffer Turn-off Delay Time (OE)		t _{OEZ}	0	15	0	20	0	20	ns	11
OE Output Data Setup Time		t _{OLZ}	0		0		0		ns	
OE Hold Time		t _{OEH}	0		0		0		ns	
Masked Write Setup Time		t _{MCS}	0		0		0		ns	
Masked Byte Write Hold Time Referenced to RAS		t _{MRH}	0		0		0		ns	
Masked Byte Write Hold Time Referenced to CAS		t _{MCH}	0		0		0		ns	
RAS Hold Time Referenced to CAS Precharge		t _{RHCP}	40		45		55		ns	
RAS Pulse Width (CAS before RAS Self Refresh)		t _{RASS}	100		100		100		μs	17
RAS Precharge Time (CAS before RAS Self Refresh)		t _{RPS}	130		150		190		ns	17
CAS Hold Time (CAS before RAS Self Refresh)		t _{CHS}	-50		-50		-50		ns	17

- ★ **NOTE**
1. $\overline{WE}$ means $\overline{UWE}$ and $\overline{LWE}$.
 2. All voltages are referenced to GND.
 3. An initial pause of 100 μs is required after power up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal address refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.
 4. I_{CC1} , I_{CC3} , I_{CC4} , I_{CC5} and I_{CC6} depend on t_{RC} and t_{EC} . Specified values are obtained with outputs open.
 5. Address can be changed once or less while $\overline{RAS} = V_{IL}$ and $\overline{CAS} = V_{IH}$.
 6. AC measurements assume $t_r = 5$ ns.
 7. AC Characteristics test condition
 - (1) Input timing specification



(2) Output timing specification



8. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($T_a = 0$ to 70 °C) is assured.
9. In random read cycle, the access time is changed by the conditions of t_{RAD} and t_{RCD} as follows.

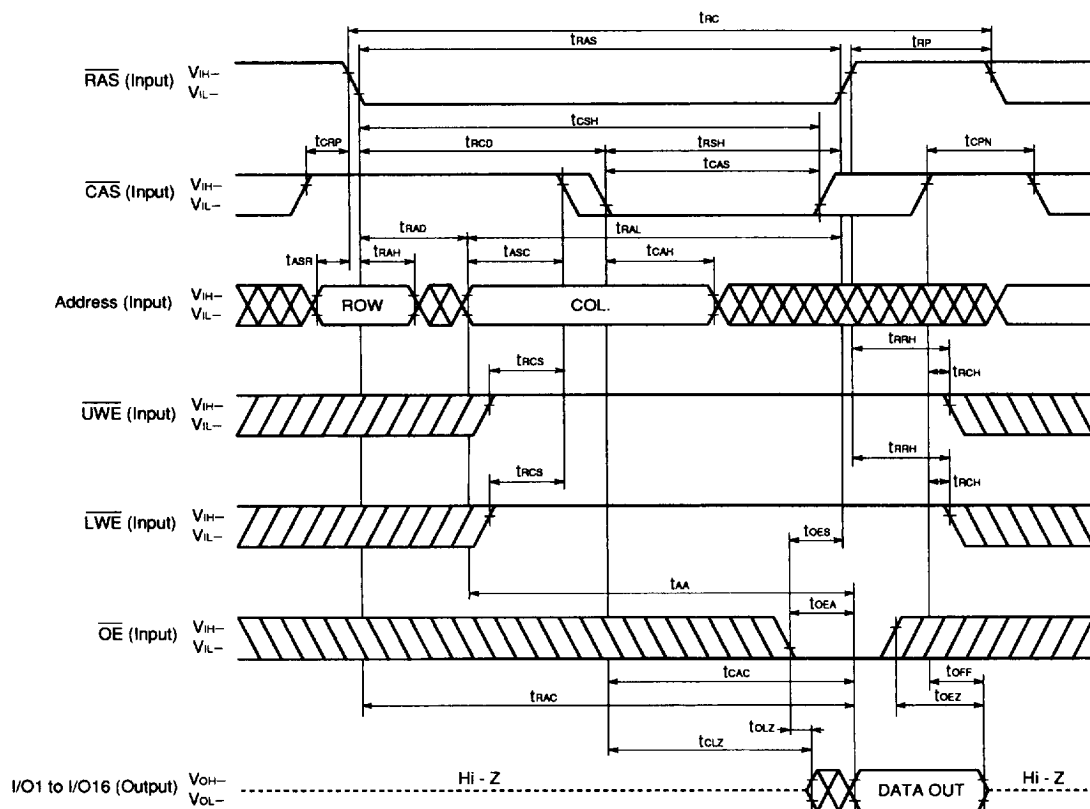
CONDITION	ACCESS TIME
$t_{RAD} \leq t_{RAD} (MAX.)$ and $t_{RCD} \leq t_{RCD} (MAX.)$	$t_{RAC} (MAX.)$
$t_{RAD} (MAX.) \leq t_{RAD}$ and $t_{RCD} \leq t_{RCD} (MAX.)$	$t_{AA} (MAX.)$
$t_{RCD} (MAX.) \leq t_{RCD}$	$t_{CAC} (MAX.)$

$t_{RAD} (MAX.)$ and $t_{RCD} (MAX.)$ indicate the points which the access time changes and are not the limits of operation.

10. Loading conditions are 1TTL and 100 pF.
11. $t_{OFF} (MAX.)$ and $t_{OEZ} (MAX.)$ define the time at which the output achieves the open circuit condition and are not referenced to V_{OH} or V_{OL} .
12. $t_{CRP} (MIN.)$ requirement should be applicable for $\overline{RAS}/\overline{CAS}$ cycles preceded by any cycles.
13. Either $t_{RCH} (MIN.)$ or $t_{RRH} (MIN.)$ must be satisfied for a read cycle.
14. $t_{WP} (MIN.)$ is applicable for late write cycle or read modify write cycle. In early write cycles, $t_{WCH} (MIN.)$ should be satisfied.
15. This specification is referenced to $\overline{CAS}$ falling edge in early write cycles and to $\overline{WE}$ falling edge in late write or read modify write cycles.
16. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} (MIN.) \leq t_{WCS}$, the cycle is an early write cycle and the data out pins will remain Hi-Z through the entire cycle. If $t_{RWD} (MIN.) \leq t_{RWD}$, $t_{CWD} (MIN.) \leq t_{CWD}$, $t_{AWD} (MIN.) \leq t_{AWD}$, and $t_{CPWD} (MIN.) \leq t_{CPWD}$, the cycle is a read modify write cycle and condition of the data out (at access time) is indeterminate.
17. This specification is applicable only for μPD42S4170, 42S4270.

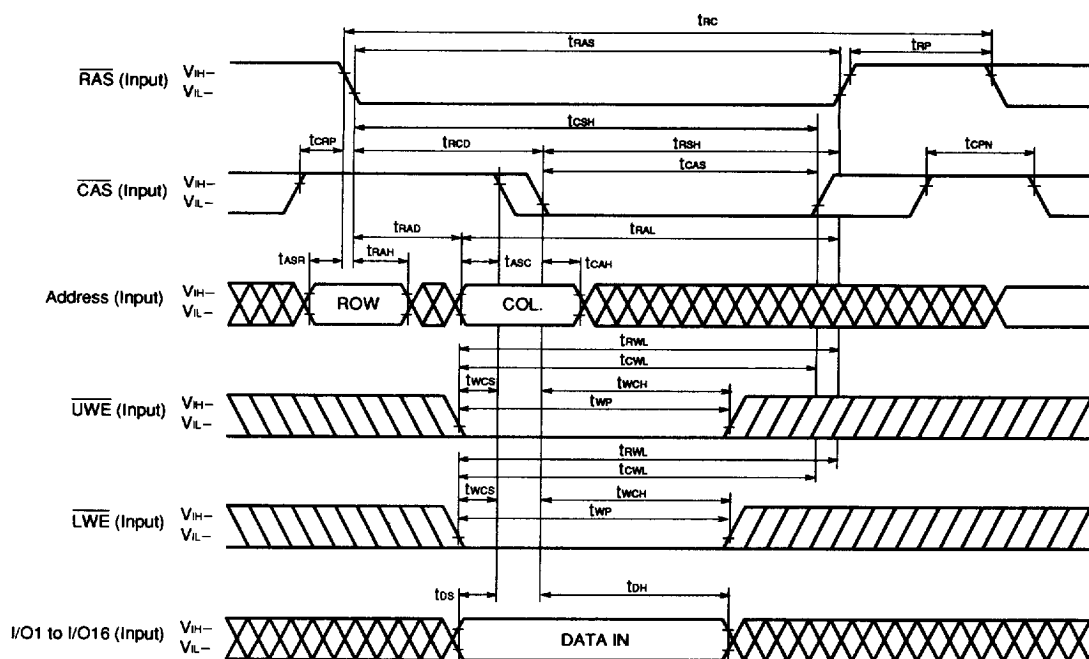
■ 6427525 0041966 959 ■ NECE

READ CYCLE



6427525 0041967 895 ■ NECE

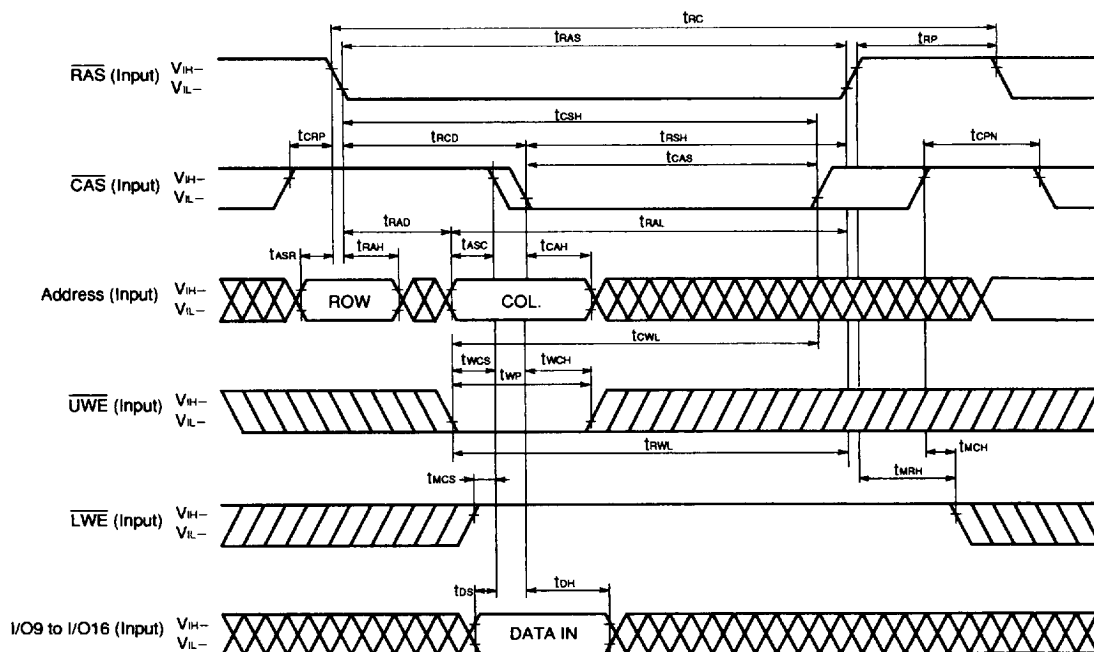
EARLY WRITE CYCLE



Remark $\overline{\text{OE}}$ = Don't care

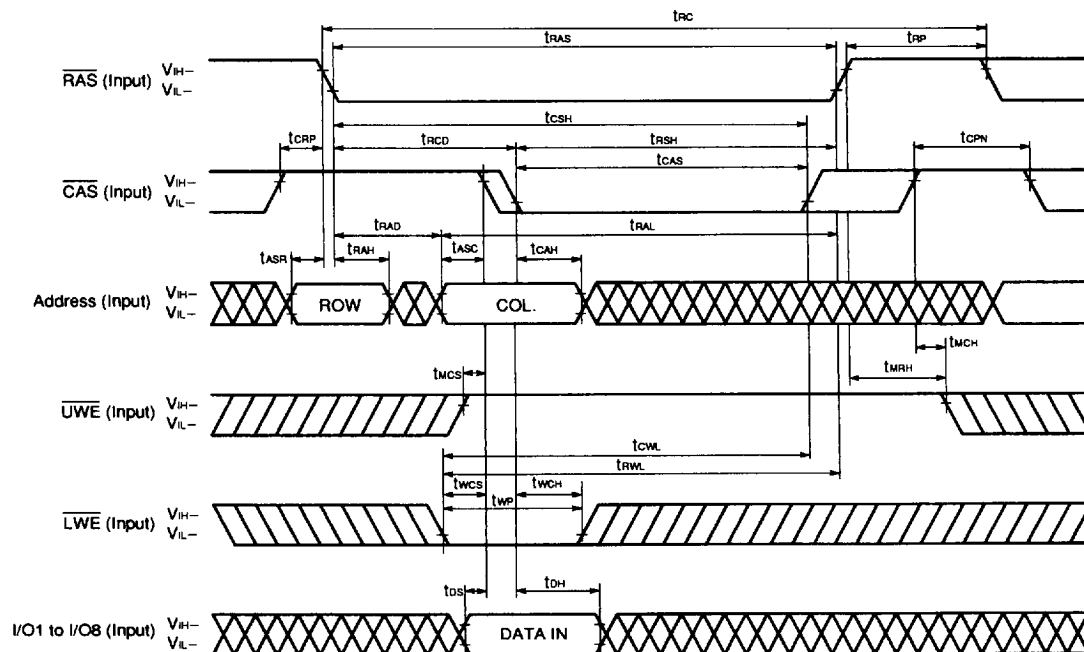
■ 6427525 0041968 721 ■ NECE

UPPER BYTE EARLY WRITE CYCLE



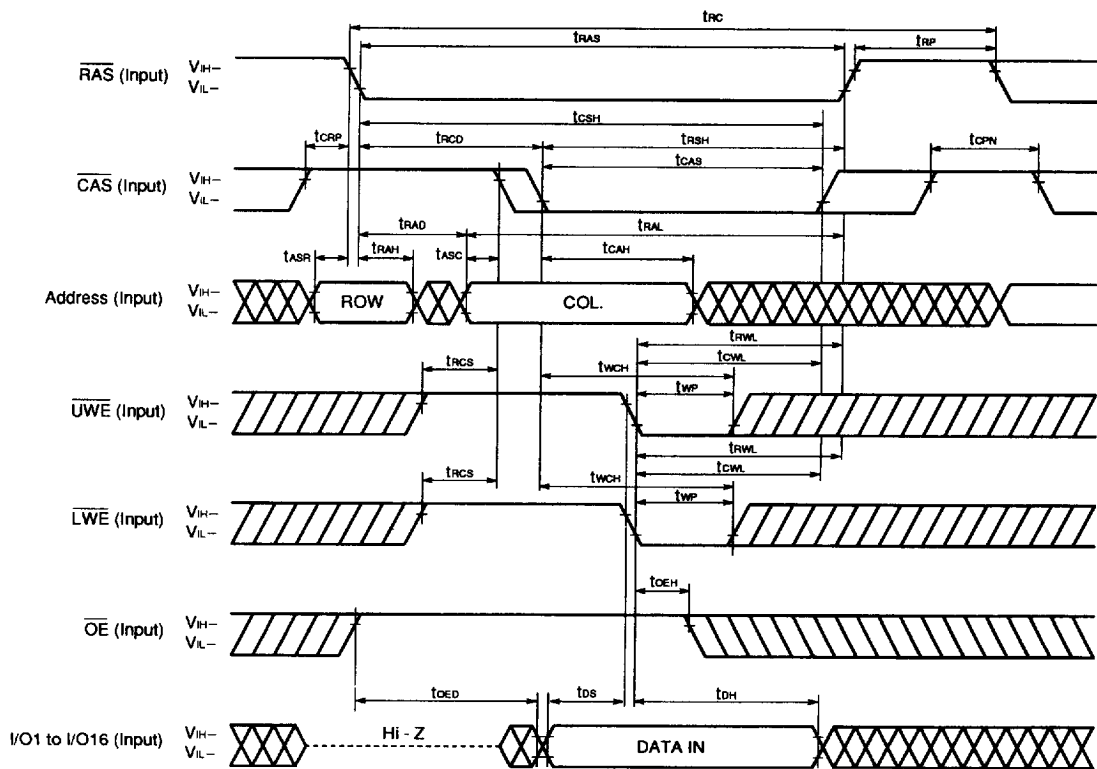
Remark $\overline{OE}$, I/O1 to I/O8 = Don't care

LOWER BYTE EARLY WRITE CYCLE



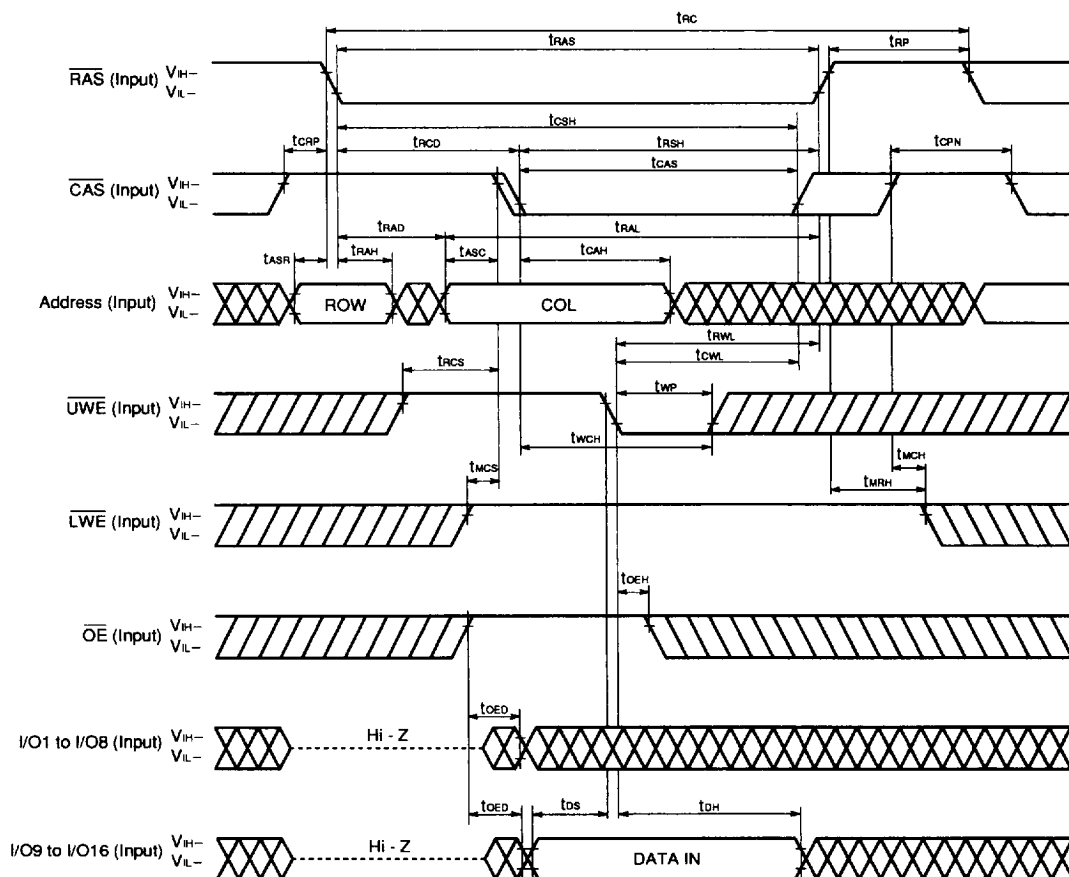
Remark $\overline{OE}$, I/O9 to I/O16 = Don't care

LATE WRITE CYCLE



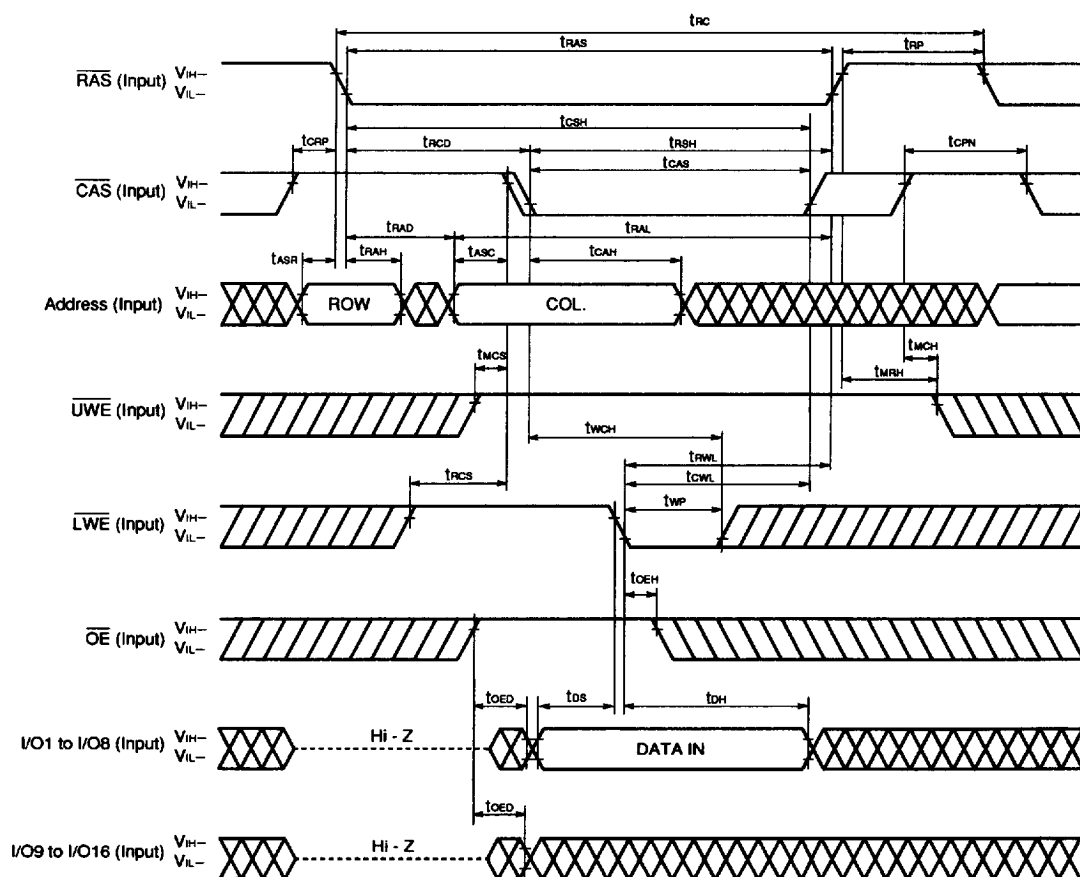
■ 6427525 0041970 38T ■ NECE

UPPER BYTE LATE WRITE CYCLE



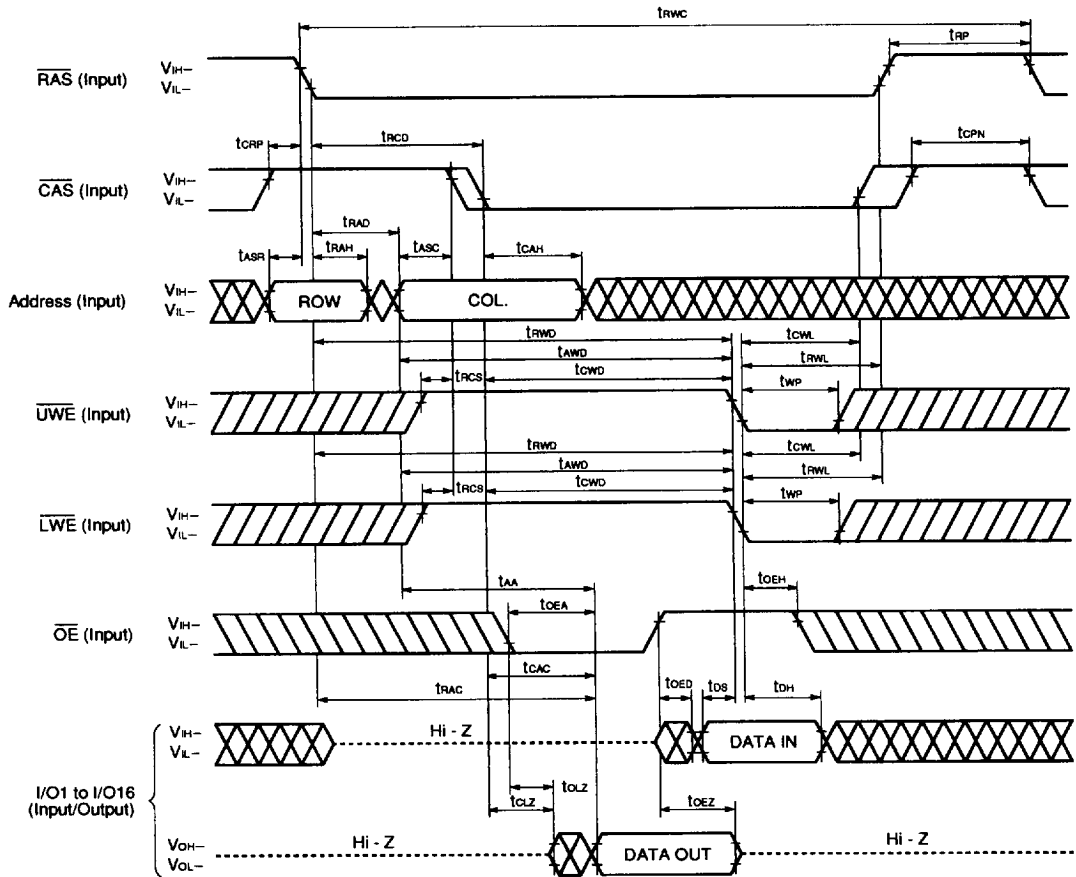
6427525 0041971 216 ■ NECE

LOWER BYTE LATE WRITE CYCLE



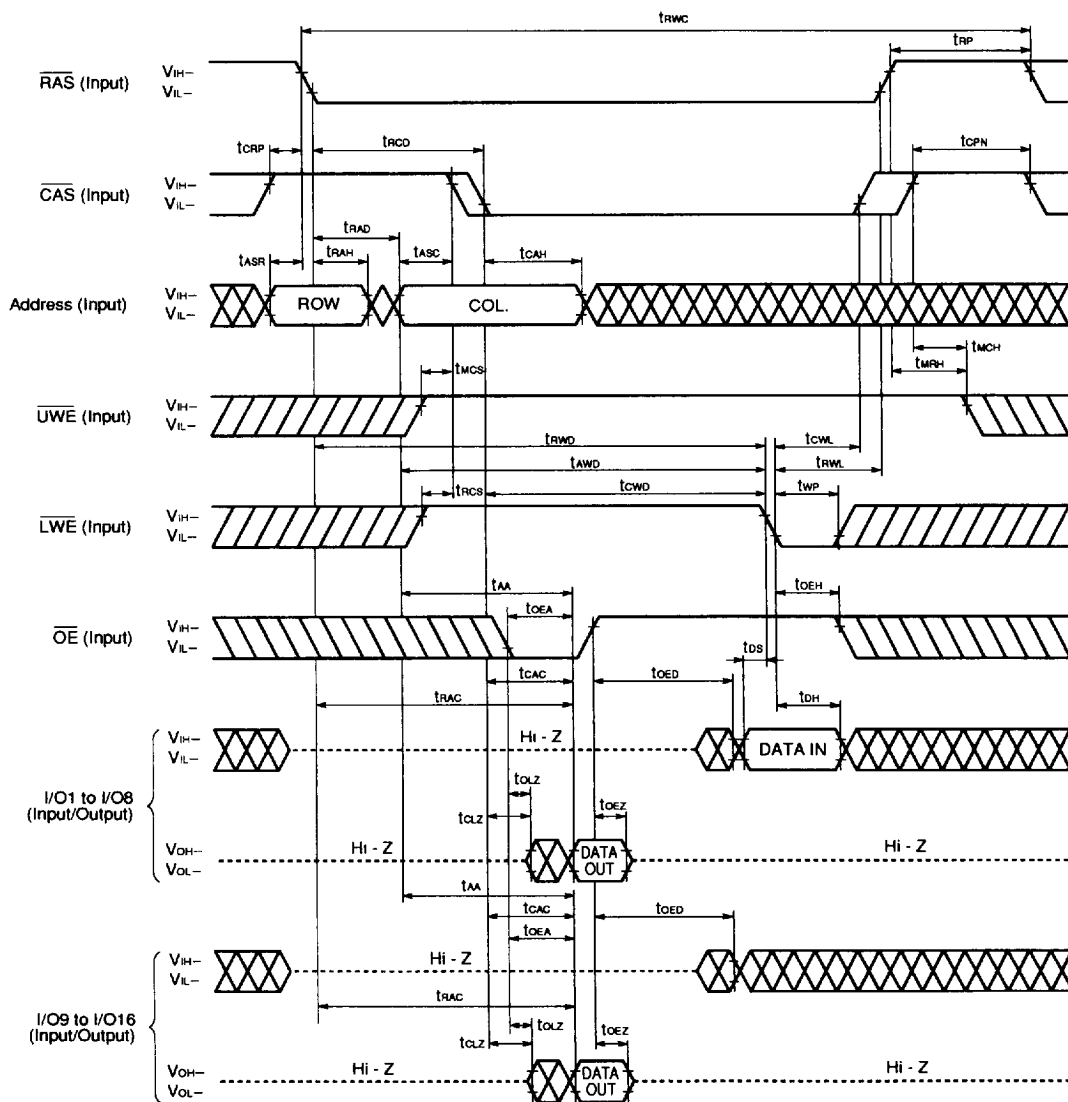
■ 6427525 0041972 152 ■ NECE

READ MODIFY WRITE CYCLE

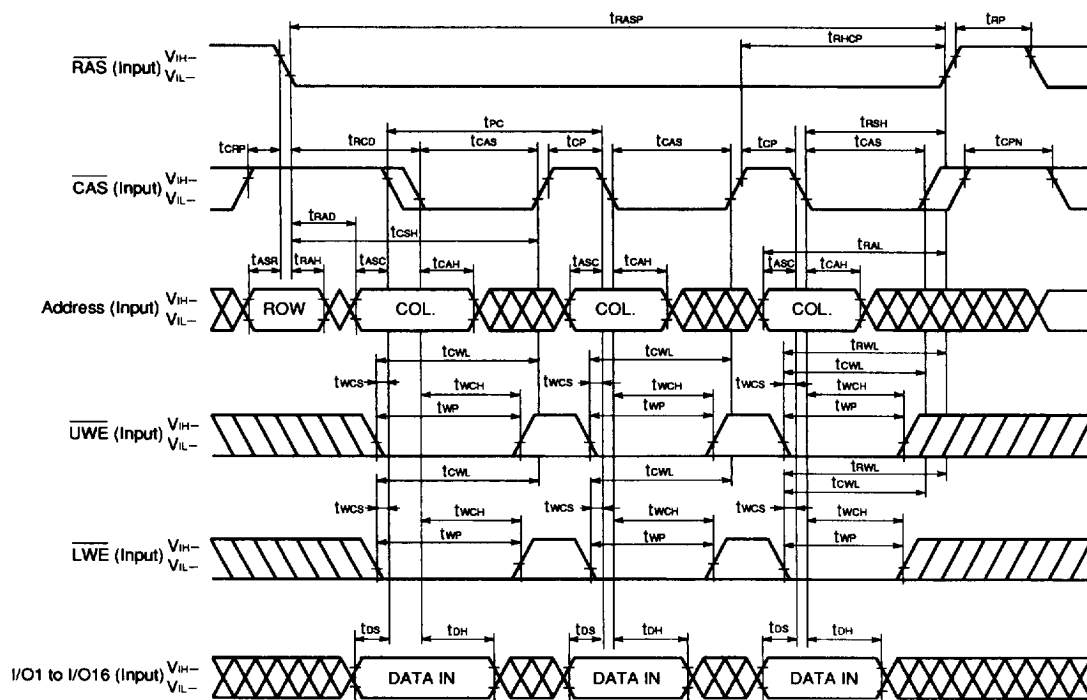


6427525 0041974 T25 NECE

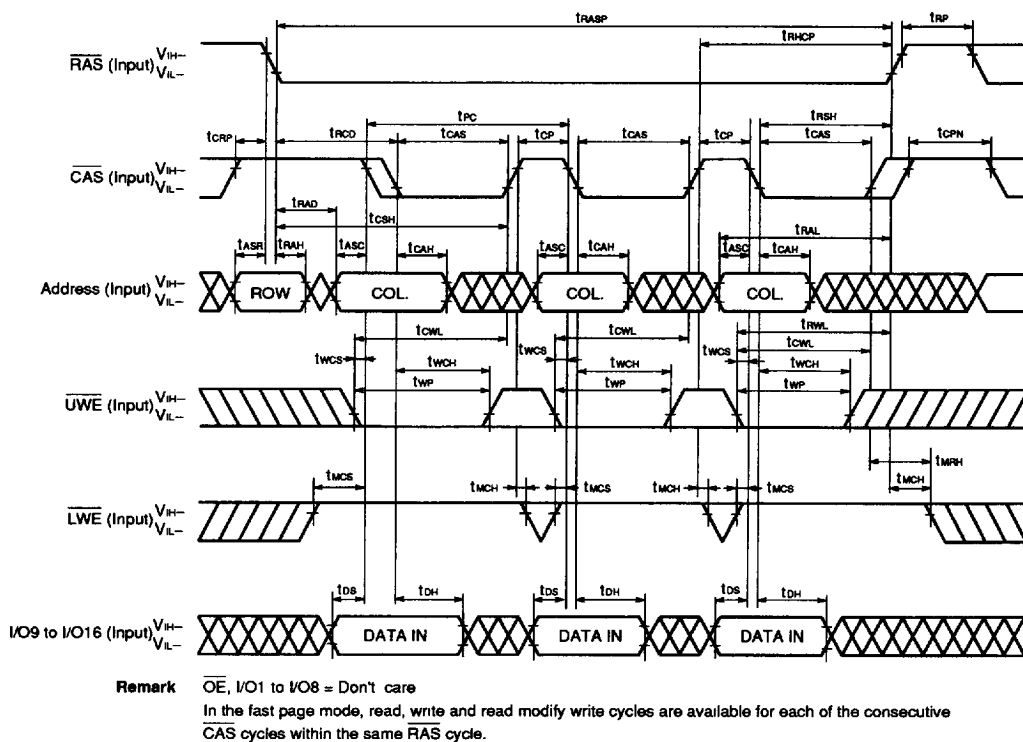
LOWER BYTE READ MODIFY WRITE CYCLE



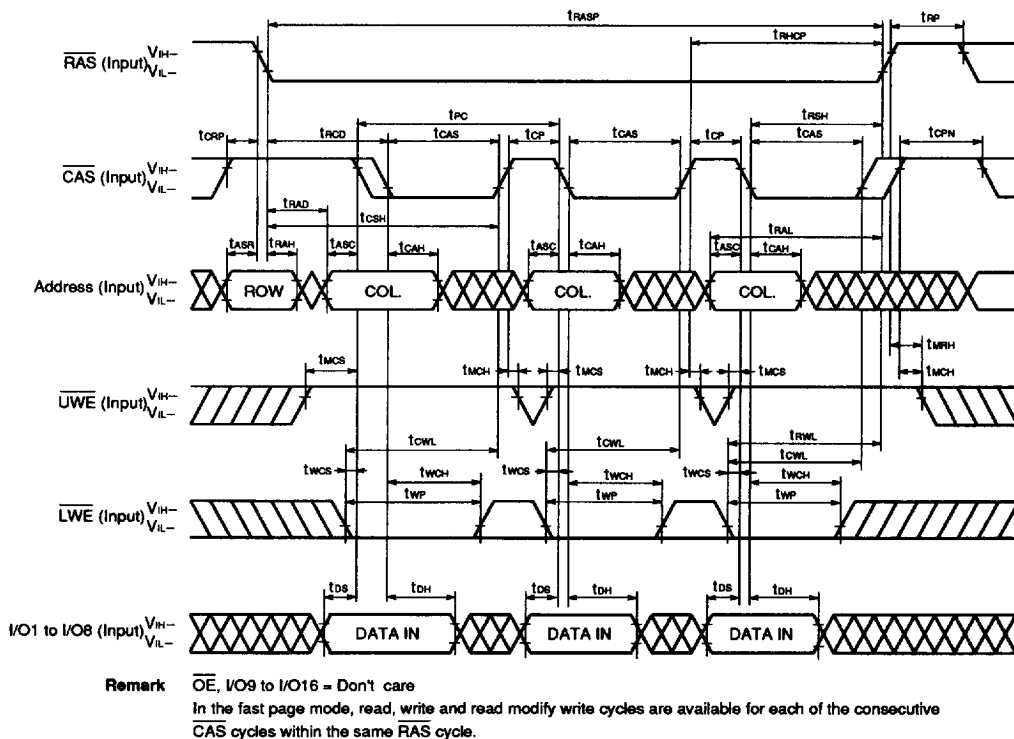
FAST PAGE MODE EARLY WRITE CYCLE



FAST PAGE MODE UPPER BYTE EARLY WRITE CYCLE

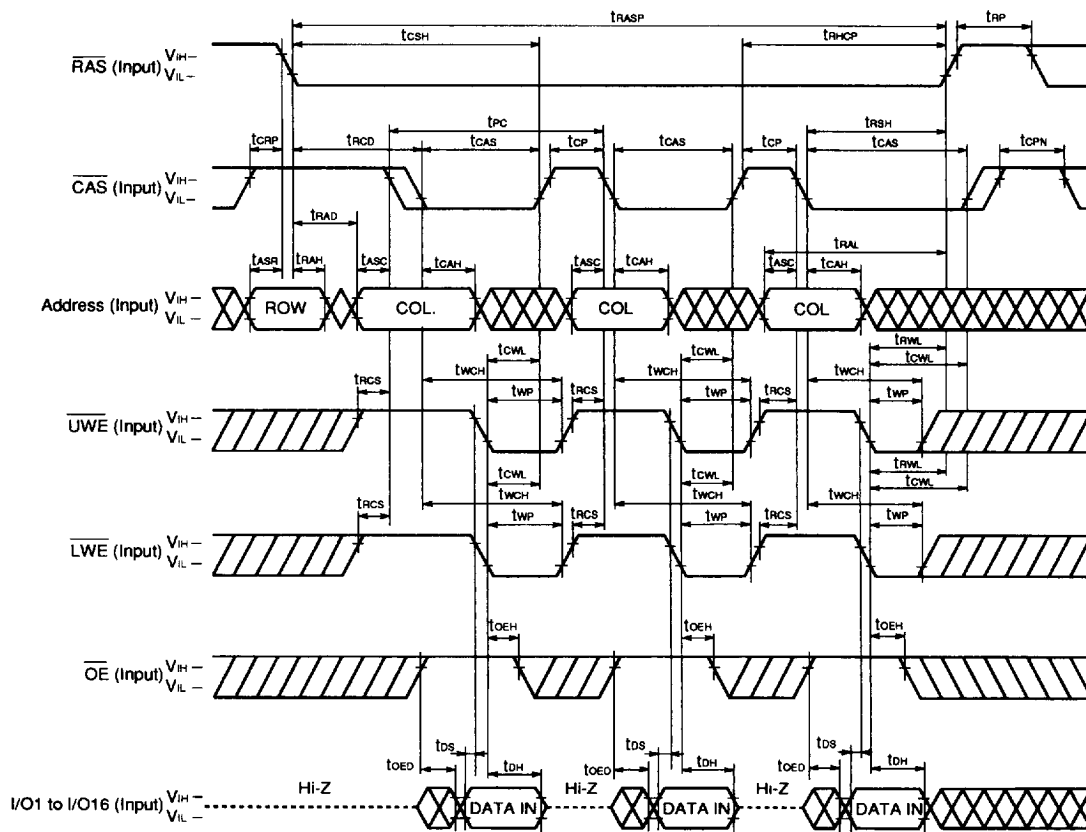


FAST PAGE MODE LOWER BYTE EARLY WRITE CYCLE



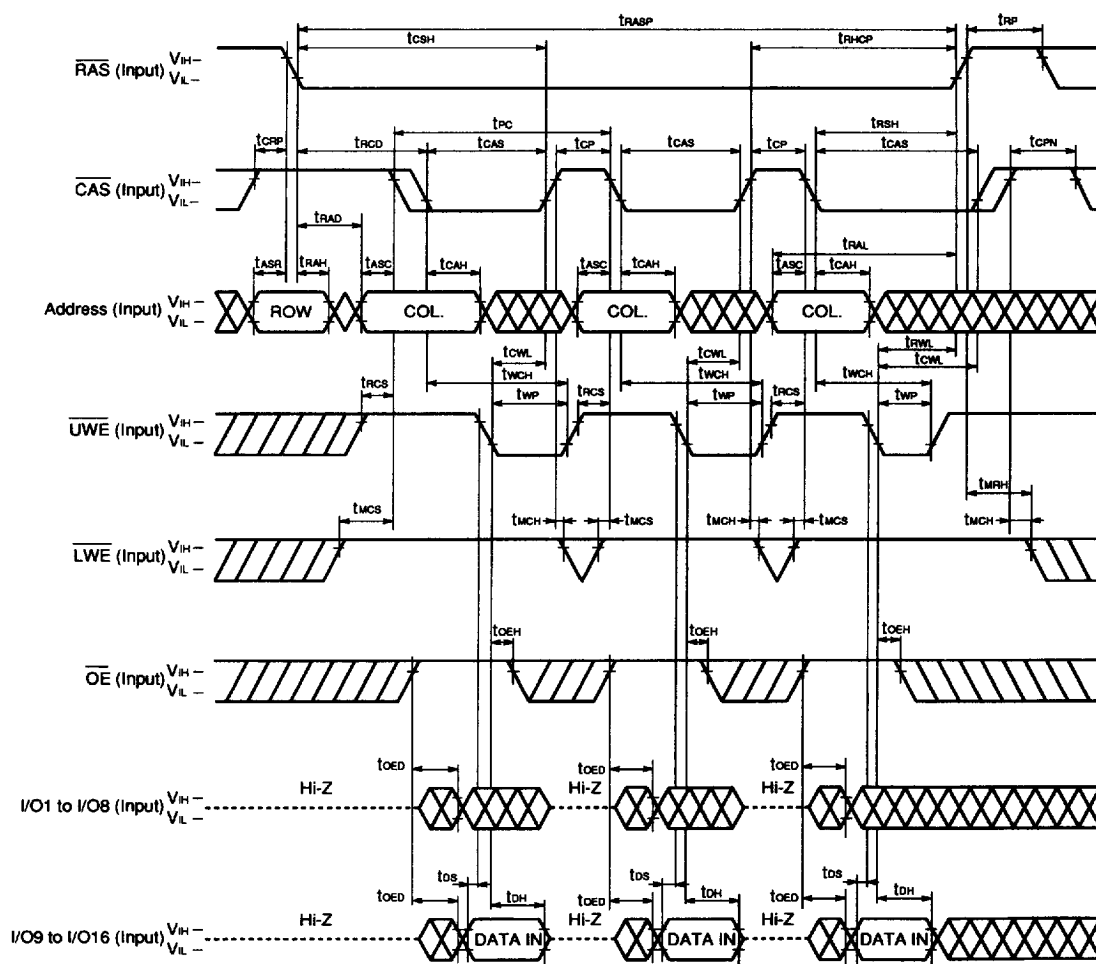
6427525 0041978 670 NECE

FAST PAGE MODE LATE WRITE CYCLE



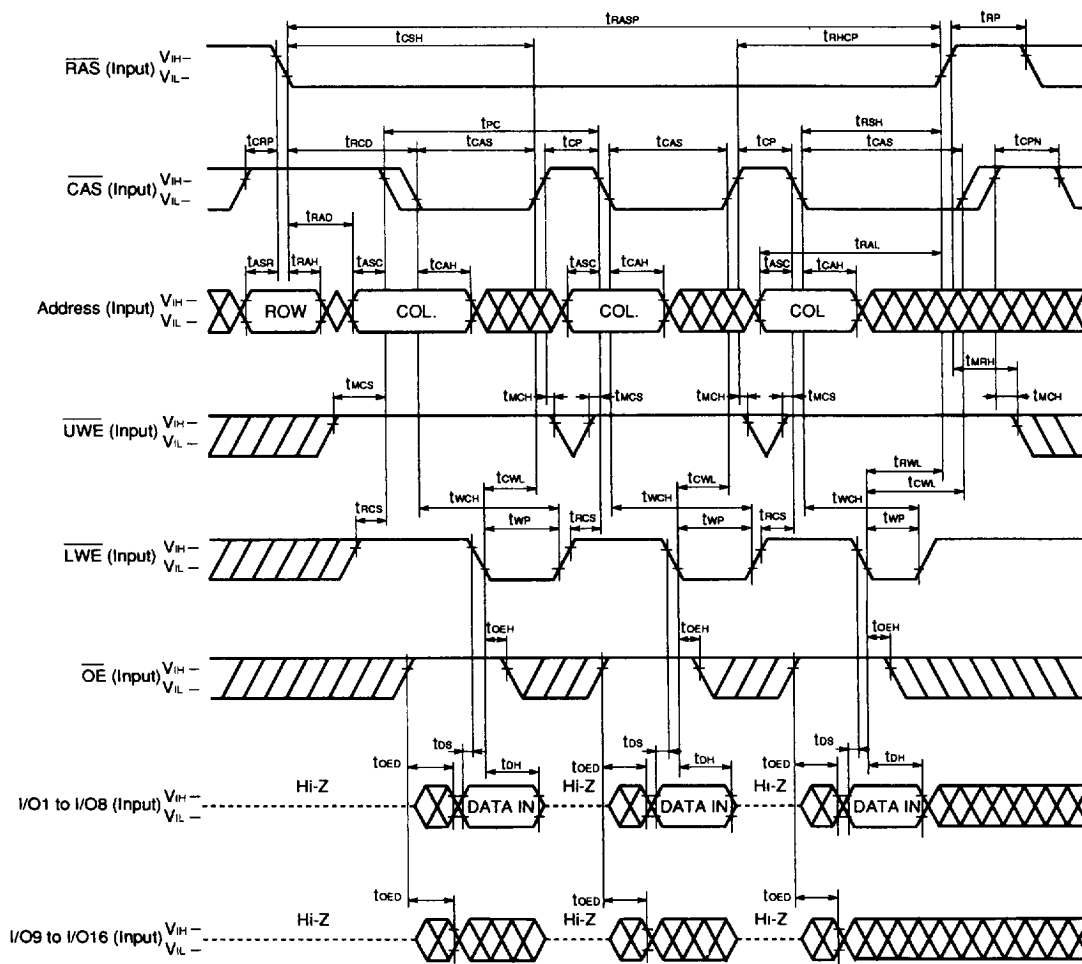
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

FAST PAGE MODE UPPER BYTE LATE WRITE CYCLE



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

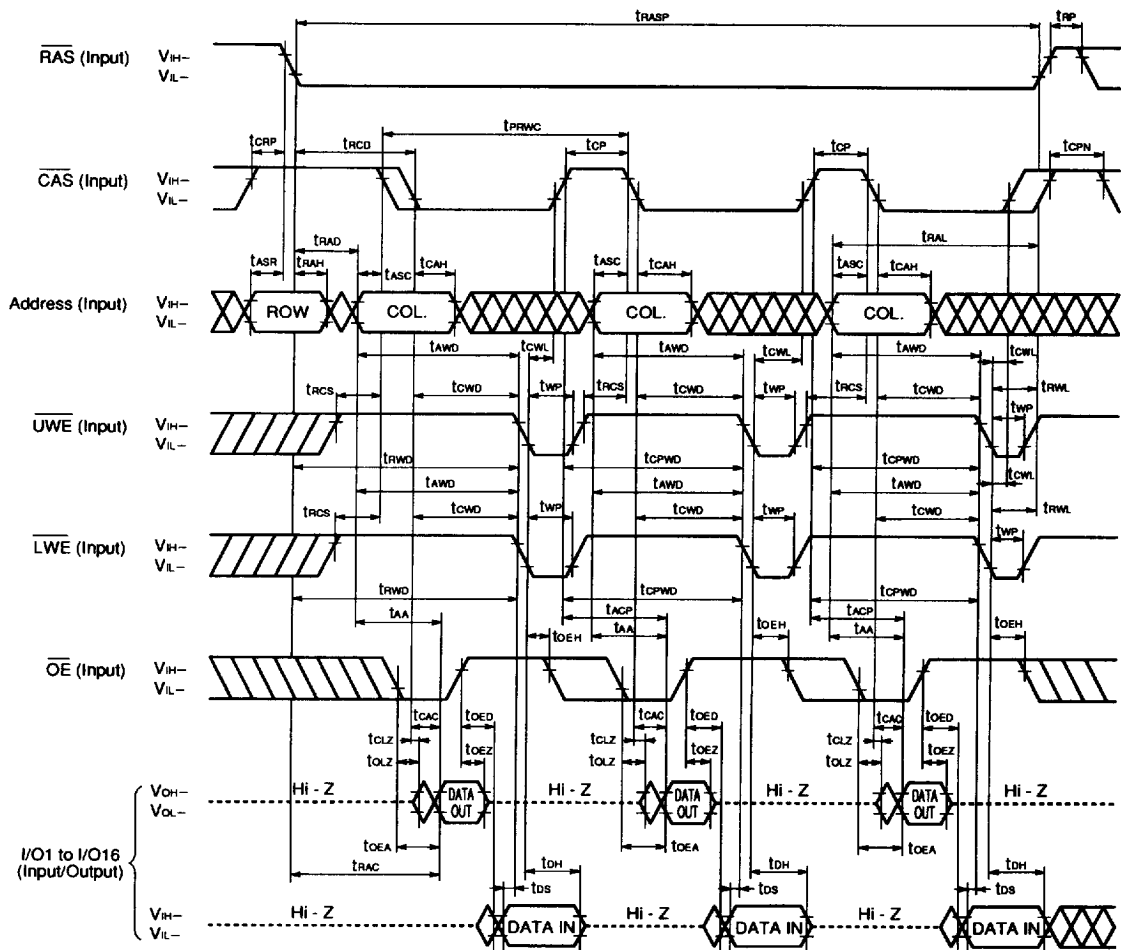
FAST PAGE MODE LOWER BYTE LATE WRITE CYCLE



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

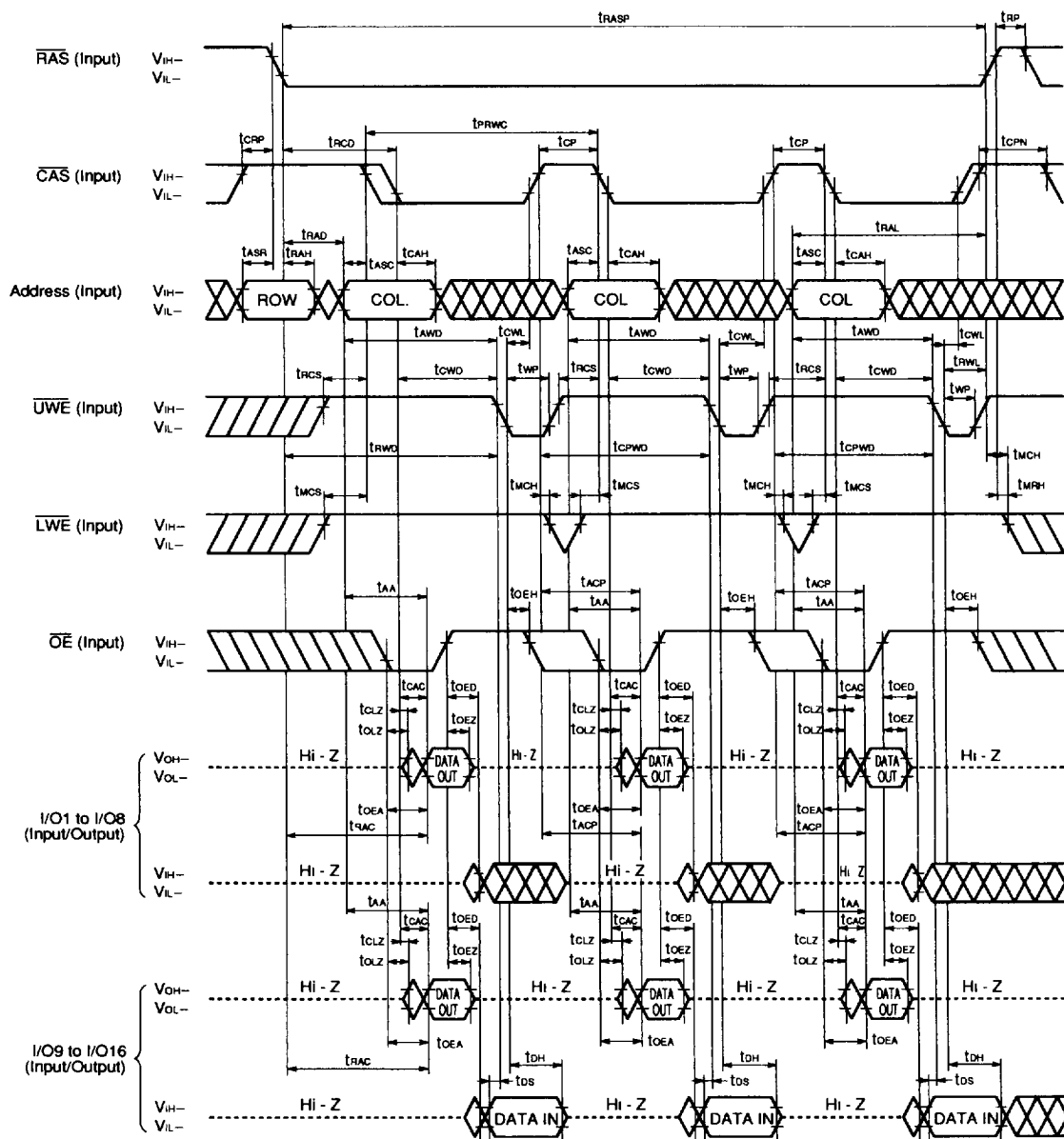
■ 6427525 0041981 165 ■ NECE

FAST PAGE MODE READ MODIFY WRITE CYCLE



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

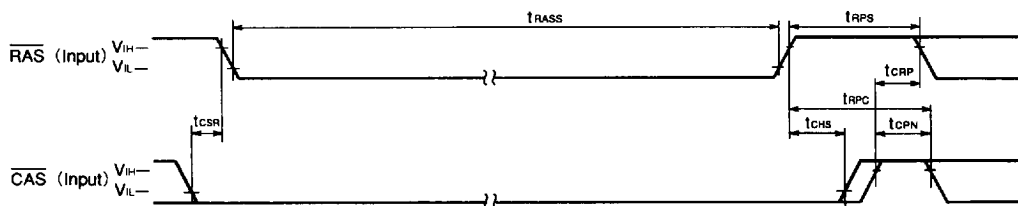
FAST PAGE MODE UPPER BYTE READ MODIFY WRITE CYCLE



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle

6427525 0041984 974 NECE

CAS BEFORE RAS SELF REFRESH CYCLE (Only for μ PD42S4170, 42S4270)



Remark Address, $\overline{UWE}$, $\overline{LWE}$, $\overline{OE}$ = Don't care I/O1 to I/O16 = Hi-Z

How to use the CAS before RAS self refresh mode.

CAS before RAS self refresh mode can't be used by itself. It must be used with performing one of 3 refreshes below.

• **When using distributed CAS before RAS refresh**

Refresh 1 024 times (μ PD42S4170) or 512 times (μ PD42S4270) during 128 ms before set into the CAS before RAS self refresh mode and after reset.

• **When using burst CAS before RAS refresh**

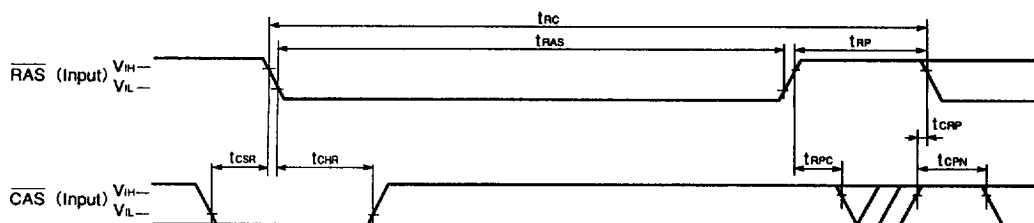
Refresh 1 024 times (μ PD42S4170) during 16 ms or 512 times (μ PD42S4270) during 8 ms before set into the CAS before RAS self refresh mode and after reset.

• **When using RAS only refresh**

Refresh all refresh addresses during 16 ms (μ PD42S4170) or 8 ms (μ PD42S4270) before set into the CAS before RAS self refresh mode and after reset.

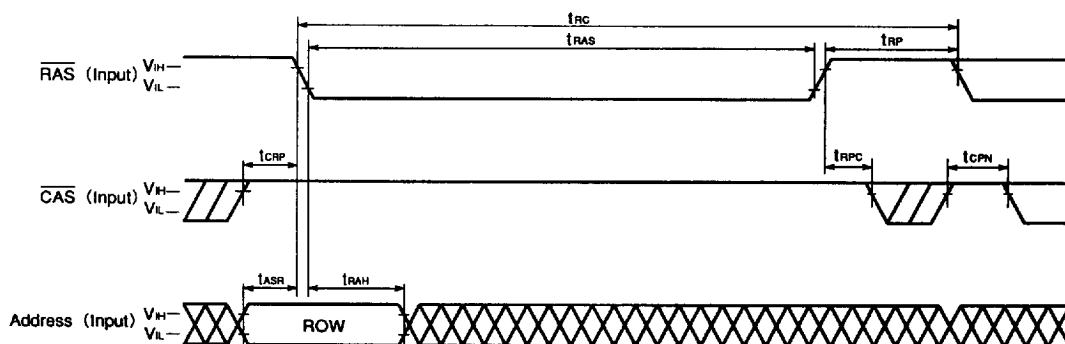
6427525 0041985 800 NECE

CAS BEFORE RAS REFRESH CYCLE



Remark Address, $\overline{UWE}$, $\overline{LWE}$, $\overline{OE}$ = Don't care I/O1 to I/O16 = Hi-Z

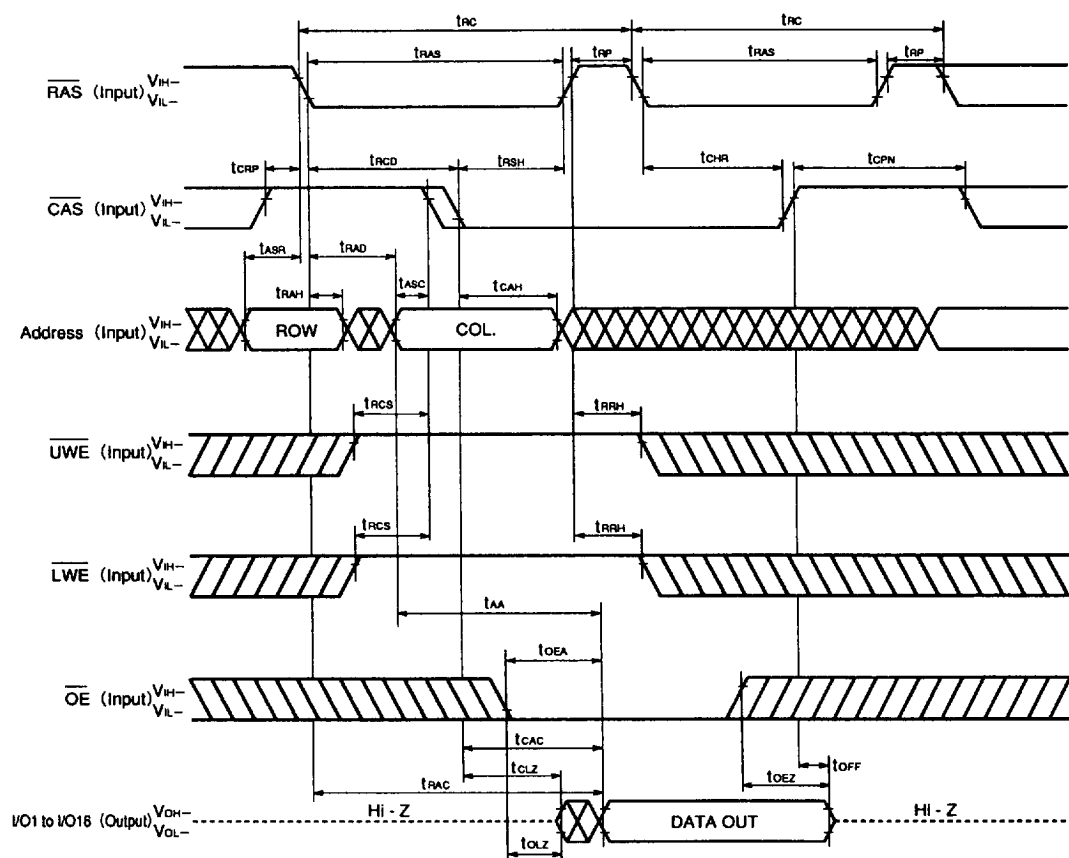
RAS ONLY REFRESH CYCLE



Remark $\overline{UWE}$, $\overline{LWE}$, $\overline{OE}$ = Don't care
I/O1 to I/O16 = Hi-Z

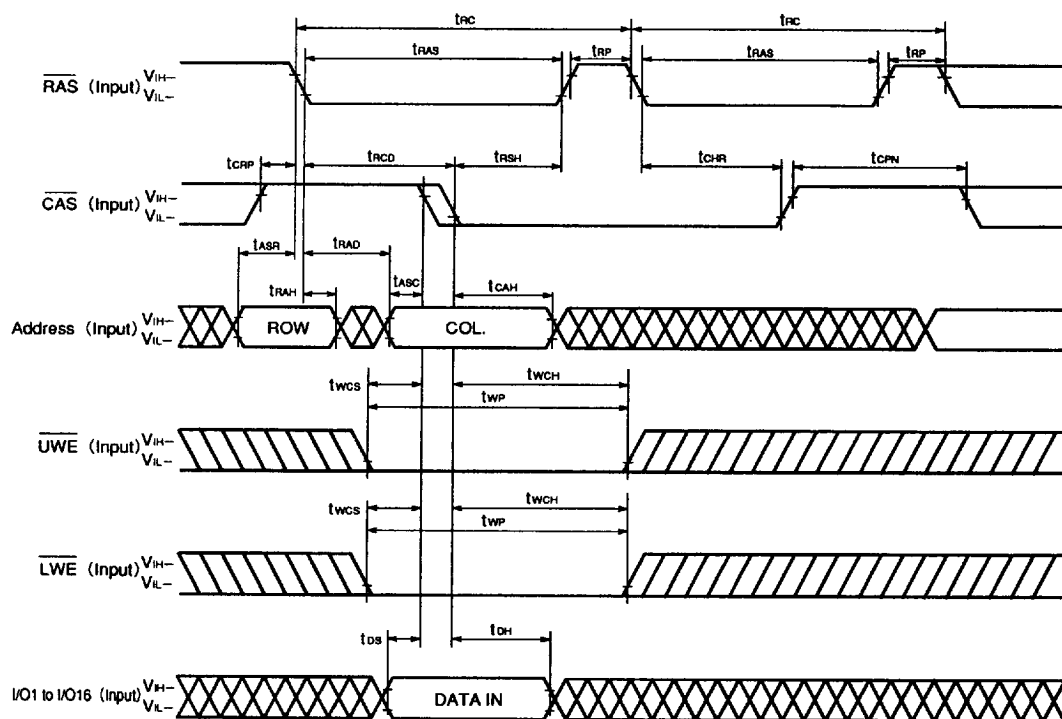
6427525 0041986 747 NECE

HIDDEN REFRESH CYCLE (READ)

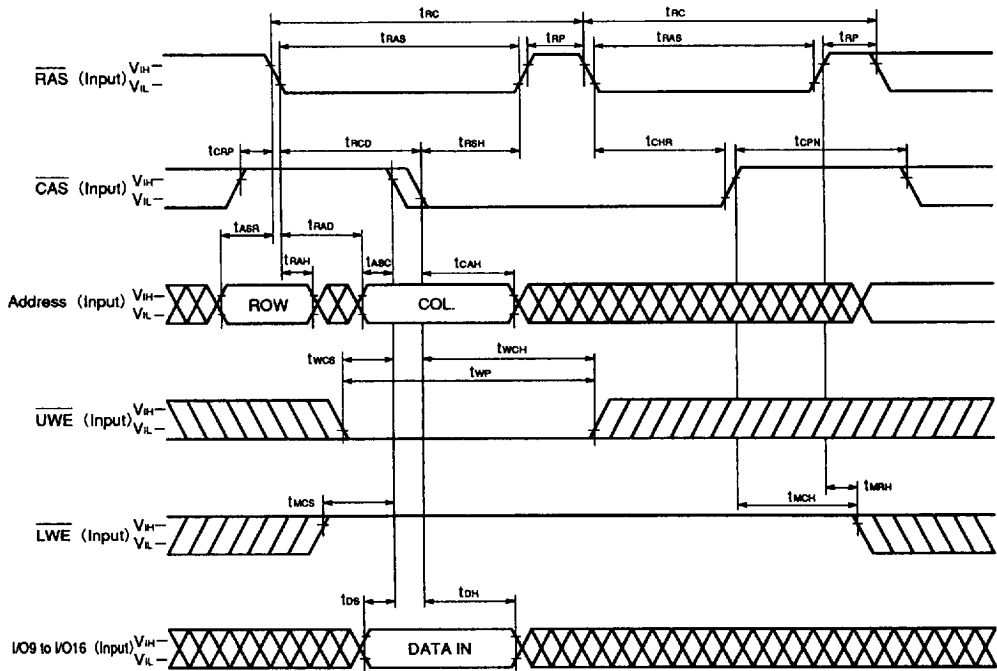


6427525 0041987 683 NECE

HIDDEN REFRESH CYCLE (WRITE)

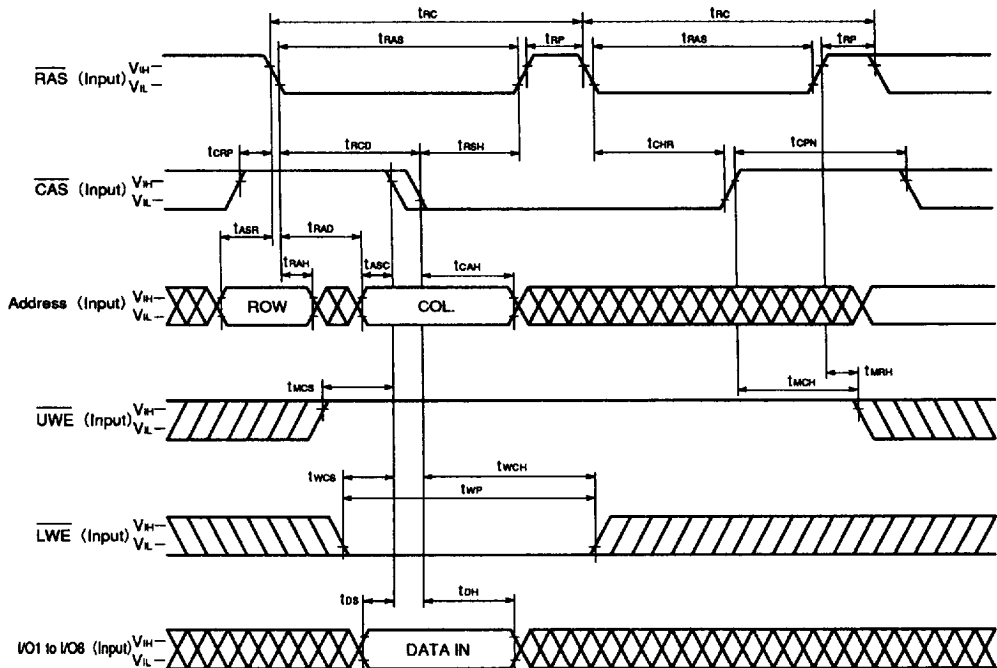
Remark $\overline{OE}$ = Don't care

6427525 0041988 51T NECE
HIDDEN REFRESH CYCLE (UPPER BYTE WRITE)



Remark $\overline{OE}$, I/O1 to I/O8 = Don't care

HIDDEN REFRESH CYCLE (LOWER BYTE WRITE)

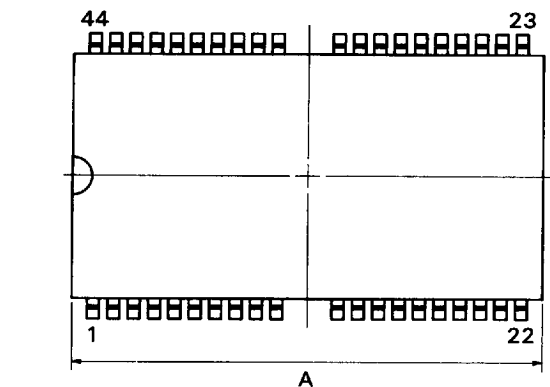


Remark $\overline{OE}$, I/O9 to I/O16 = Don't care

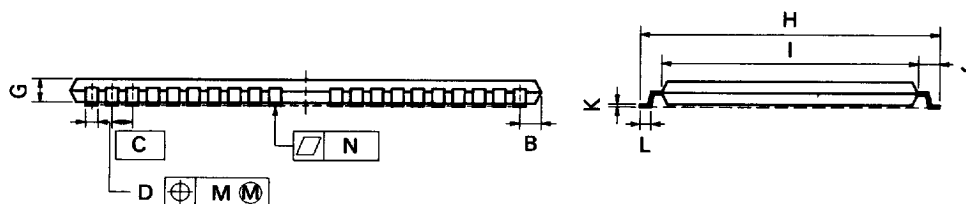
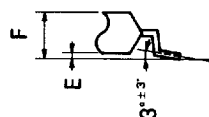
■ 6427525 0041989 456 ■ NECE

PACKAGE INFORMATION

44 PIN PLASTIC TSOP (400mil)



detail of lead end



NOTE

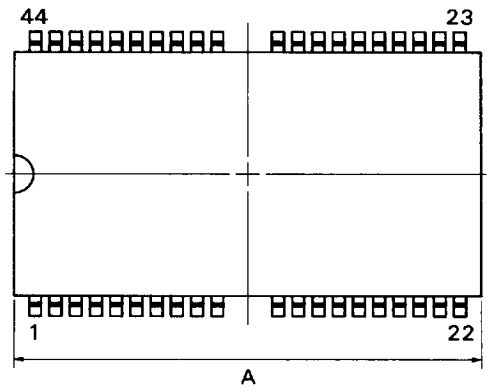
Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

S44G5-80-7JF

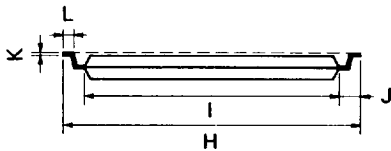
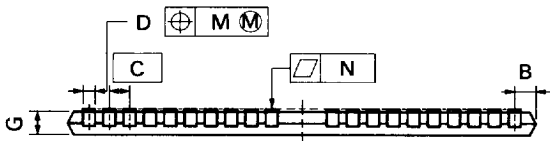
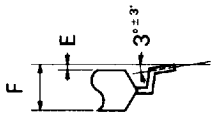
ITEM	MILLIMETERS	INCHES
A	18.81 MAX.	0.741 MAX.
B	1.0 MAX.	0.040 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	0.30 $\pm$ 0.10	0.012 $\pm$ 0.004
E	0.05 $\pm$ 0.05	0.002 $\pm$ 0.002
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	11.76 $\pm$ 0.2	0.463 $\pm$ 0.008
I	10.16 $\pm$ 0.1	0.400 $\pm$ 0.004
J	0.8 $\pm$ 0.2	0.031 $\pm$ 0.008
K	0.125 $\pm$ 0.10	0.005 $\pm$ 0.004
L	0.5 $\pm$ 0.1	0.020 $\pm$ 0.004
M	0.13	0.005
N	0.10	0.004

6427525 0041990 178 NECE

44 PIN PLASTIC TSOP (400mil)



detail of lead end



S44G5-80-7KF

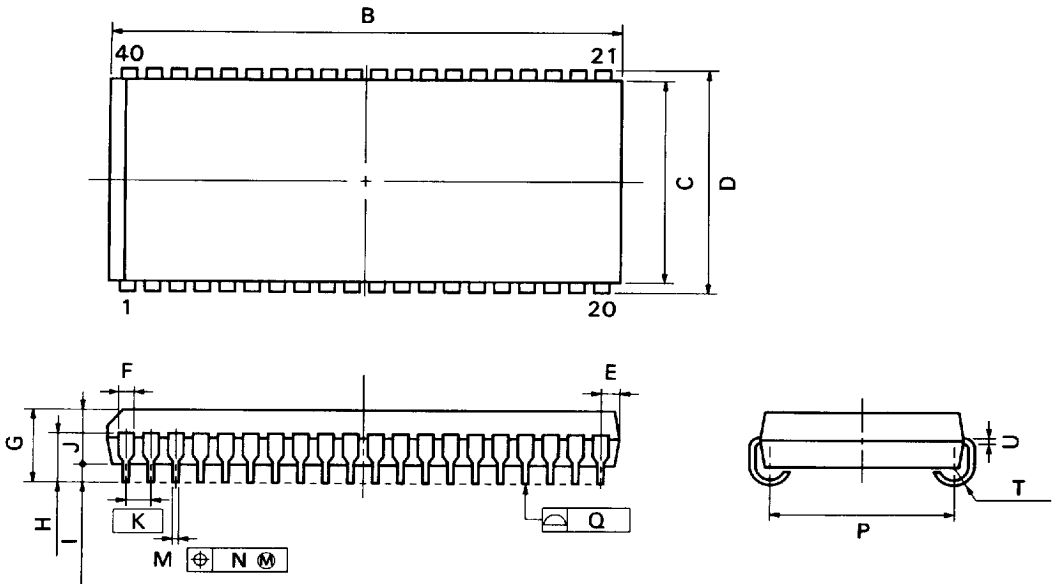
NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition

ITEM	MILLIMETERS	INCHES
A	18.81 MAX.	0.741 MAX.
B	1.0 MAX.	0.040 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	0.30 ^{+0.10} ₀	0.012 ^{+0.004} ₀
E	0.05 ^{+0.05} ₀	0.002 ^{±0.002}
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	11.76 ^{±0.2}	0.463 ^{±0.008}
I	10.16 ^{±0.1}	0.400 ^{±0.004}
J	0.8 ^{±0.2}	0.031 ^{+0.008} ₀
K	0.125 ^{+0.018} ₀	0.005 ^{+0.002} ₀
L	0.5 ^{±0.1}	0.020 ^{+0.004} ₀
M	0.13	0.005
N	0.10	0.004

■ 6427525 0041991 004 ■ NECE

40PIN PLASTIC SOJ (400 mil)



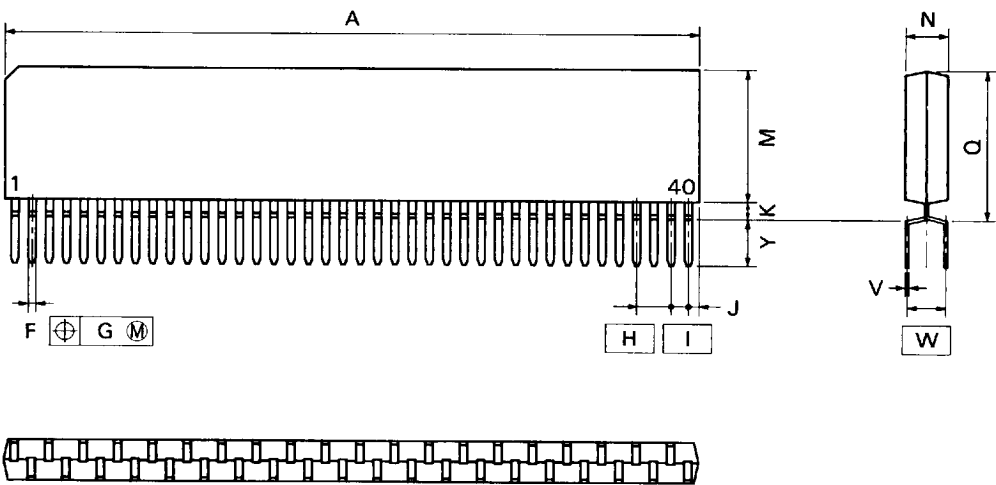
NOTE
Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

P40LE-400A-1

ITEM	MILLIMETERS	INCHES
B	26.29 ^{+0.2} _{-0.35}	1.035 ^{+0.008} _{-0.014}
C	10.16	0.400
D	11.18 ^{±0.2}	0.440 ^{±0.008}
E	1.08 ^{±0.15}	0.043 ^{+0.006} _{-0.007}
F	0.7	0.028
G	3.5 ^{±0.2}	0.138 ^{±0.008}
H	2.4 ^{±0.2}	0.094 ^{+0.009} _{-0.008}
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27(T.P.)	0.050(T.P.)
M	0.40 ^{±0.10}	0.016 ^{+0.004} _{-0.005}
N	0.12	0.005
P	9.4 ^{±0.20}	0.370 ^{±0.008}
Q	0.15	0.006
T	R 0.85	R 0.033
U	0.20 ^{+0.10} _{-0.06}	0.008 ^{+0.004} _{-0.002}

■ 6427525 0041992 T40 ■ NECE

40 PIN PLASTIC ZIP(475mil)



P40V 100-475A

NOTE
Each lead centerline is located within 0.25 mm (0.010 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	51.23 MAX.	2.017 MAX.
F	0.50 ^{+0.10} ₀	0.020 ^{+0.004} ₀
G	0.25	0.010
H	2.54 (T.P.)	0.100 (T.P.)
I	1.27 (T.P.)	0.050 (T.P.)
J	0.85 MAX.	0.034 MAX.
K	0.9 MIN.	0.035 MIN.
M	10.5 MAX.	0.414 MAX.
N	2.8 ^{+0.2} ₀	0.110 ^{+0.008} ₀
Q	12.07 MAX.	0.476 MAX.
V	0.25 ^{+0.10} ₀	0.010 ^{+0.004} ₀
W	2.54 (T.P.)	0.100 (T.P.)
Y	3.25 ^{+0.2} ₀	0.128 ^{+0.008} ₀

■ 6427525 0041993 987 ■ NECE

RECOMMENDED SOLDERING CONDITIONS

Please consult with our sales offices when soldering μPD42S4170, 424170, 42S4270, 424270.

TYPE OF SURFACE MOUNT DEVICE

μPD42S4170G5, 424170G5, 42S4270G5, 424270G5 (44-pin Plastic TSOP)

μPD42S4170LE, 424170LE, 42S4270LE, 424270LE (40-pin Plastic SOJ)

TYPE OF THROUGH HOLE MOUNT DEVICE

μPD42S4170V, 424170V (40-pin Plastic ZIP)