

CAT64LC10/CAT64LC10I

1K-Bit SERIAL E²PROM

FEATURES

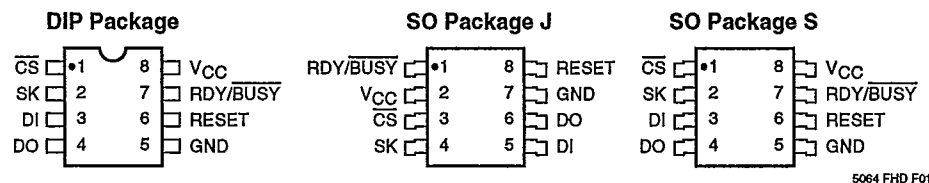
- SPI Bus Compatible
- Low Power CMOS Technology
- 2.5V to 5.5V Operation
- Self-Timed Write Cycle with Auto-Clear
- Hardware Reset Pin
- Hardware and Software Write Protection
- Power-Up Inadvertant Write Protection
- RDY/BUSY Pin for End-of-Write Protection
- 100,000 Program/Erase Cycles
- 100 Year Data Retention
- ZERO Power™ (CAT64LC10Z) Version Available
- Optional High Endurance Device Available

DESCRIPTION

The CAT64LC10 and CAT64LC10I are 1K bit Serial E²PROM memory devices which are configured as 64 registers by 16 bits. Each register can be written (or read) serially by using the DI (or DO) pin. The CAT64LC10/CAT64LC10I is manufactured using

Catalyst's advanced CMOS E²PROM floating gate technology. It is designed to endure 100,000 program/erase cycles and has a data retention of 100 years. The device is available in 8 pin DIP or SO packages.

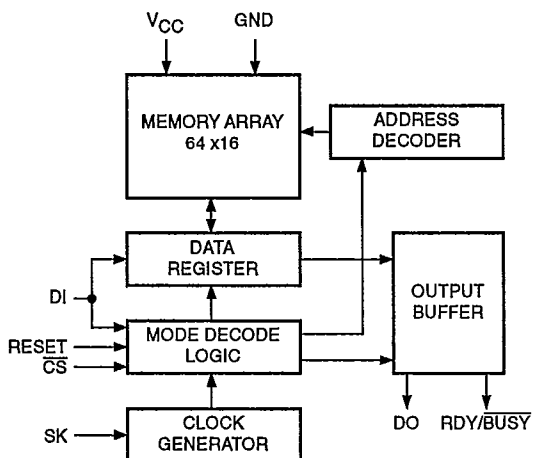
PIN CONFIGURATION



PIN FUNCTIONS

Pin Name	Function
CS	Chip Select
SK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
Vcc	+2.5V to +5.5V Power Supply
GND	Ground
RESET	Reset
RDY/BUSY	Ready/BUSY Status

BLOCK DIAGRAM



TD 5064

CATALYST SEMICONDUCTOR

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on any Pin with Respect to Ground ⁽¹⁾	-2.0V to +V _{CC} +2.0V
V _{CC} with Respect to Ground	-2.0V to +7.0V
Package Power Dissipation Capability (T _A = 25°C)	1.0W
Lead Soldering Temperature (10 secs)	300°C
Output Short Circuit Current ⁽²⁾	100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N _{END} ⁽³⁾	Endurance	100,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T _{DR} ⁽³⁾	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V _{ZAP} ⁽³⁾	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I _{LTH} ⁽³⁾⁽⁴⁾	Latch-Up	100		mA	JEDEC Standard 17

CAPACITANCE (T_A = 25°C, f = 1.0 MHz, V_{CC} = 5.5V)

Symbol	Test	Max.	Units	Conditions
C _{I/O} ⁽³⁾	Input/Output Capacitance (DO, RDY/BUSY)	8	pF	V _{I/O} = 0V
C _{IN} ⁽³⁾	Input Capacitance (CS, SK, DI, RESET)	6	pF	V _{IN} = 0V

Note:

- (1) The minimum DC input voltage is -0.5V. During transitions, inputs may undershoot to -2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} + 0.5V, which may overshoot to V_{CC} + 2.0V for periods of less than 20 ns.
- (2) Output shorted for no more than one second. No more than one output shorted at a time.
- (3) This parameter is tested initially and after a design or process change that affects the parameter.
- (4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from -1V to V_{CC} + 1V.

D.C. OPERATING CHARACTERISTICS

CAT64LC10 $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = +2.5\text{V}$ to $+5.5\text{V}$, unless otherwise specified.

CAT64LC10I $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = +2.5\text{V}$ to $+5.5\text{V}$, unless otherwise specified.

Sym.	Parameter		Limits			Units	Test Conditions
			Min.	Typ.	Max.		
I _{CC}	Operating Current	2.5V			0.4	mA	f _{SK} = 250 kHz
	EWEN, EWDS, READ	5.5V			1.0		f _{SK} = 1 MHz
I _{CCP}	Program Current	2.5V			2.0	mA	
		5.5V			3.0		
I _{SB}	Standby Current	Standard			3.0	μA	V _{IN} = GND or V _{CC}
I _{SBZ} ⁽⁵⁾		ZERO Pwr™			0		$\overline{\text{CS}} = V_{CC}$
I _{LI}	Input Leakage Current				2.0	μA	V _{IN} = GND to V _{CC}
I _{LO}	Output Leakage Current				10	μA	V _{OUT} = GND to V _{CC}
V _{IL}	Low Level Input Voltage, DI		-0.1		V _{CC} x 0.3	V	
V _{IH}	High Level Input Voltage, DI		V _{CC} x 0.7		V _{CC} + 0.5	V	
V _{IL}	Low Level Input Voltage, $\overline{\text{CS}}$, SK, RESET		-0.1		V _{CC} x 0.2	V	
V _{IH}	High Level Input Voltage, $\overline{\text{CS}}$, SK, RESET		V _{CC} x 0.8		V _{CC} + 0.5	V	
V _{OH}	High Level Output Voltage	2.5V	V _{CC} - 0.3			V	I _{OH} = -10μA
		4.5V	V _{CC} - 0.3				I _{OH} = -10μA
			2.4				I _{OH} = -400μA
V _{OL}	Low Level Output Voltage	2.5V			0.4	V	I _{OL} = 10μA
		4.5V					I _{OL} = 2.1mA

Note:

(5) Standby Current (I_{SBZ}) = 0μA (<900nA)

A.C. OPERATING CHARACTERISTICSCAT64LC10 $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = +2.5\text{V}$ to $+5.5\text{V}$, unless otherwise specified.CAT64LC10I $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = +2.5\text{V}$ to $+5.5\text{V}$, unless otherwise specified.

Symbol	Parameter		Limits			Units
			Min.	Typ.	Max.	
t _{CSS}	CS Setup Time		100			ns
t _{CSH}	CS Hold Time		100			ns
t _{DIS}	DI Setup Time		200			ns
t _{DIH}	DI Hold Time		200			ns
t _{PD1}	Output Delay to 1				300	ns
t _{PD0}	Output Delay to 0				300	ns
t _{HZ} ⁽⁶⁾	Output Delay to High Impedance				500	ns
t _{CSMIN}	Minimum CS High Time		250			ns
t _{SKHI}	Minimum SK High Time	2.5V	1000			ns
		4.5V–5.5V	400			
t _{SKLOW}	Minimum SK Low Time	2.5V	1000			ns
		4.5V–5.5V	400			
t _{SV}	Output Delay to Status Valid				500	ns
f _{SK}	Maximum Clock Frequency	2.5V	250			kHz
		4.5V–5.5V	1000			
t _{RESS}	Reset to CS Setup Time		0			ns
t _{RESMIN}	Minimum RESET High Time		250			ns
t _{RESH}	RESET to READY Hold Time		0			ns
t _{RC}	Write Recovery		100			ns

POWER-UP TIMING⁽³⁾⁽⁷⁾

Symbol	Parameter	Min.	Max.	Units
t _{PUR}	Power-Up to Read Operation		10	μs
t _{PUW}	Power-Up to Program Operation		1	ms

WRITE CYCLE LIMITS

Symbol	Parameter		Min.	Max.	Units
t _{WR}	Program Cycle Time	2.5V		10	ms
		4.5V–5.5V		5	

Note:

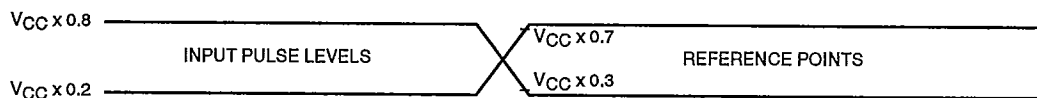
(3) This parameter is tested initially and after a design or process change that affects the parameter.

(6) This parameter is sampled but not 100% tested.

(7) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.

INSTRUCTION SET

Instruction	Opcode	Address	Data
Read	10101000	A5 A4 A3 A2 A1 A0 0 0	D15-D0
Write	10100100	A5 A4 A3 A2 A1 A0 0 0	D15-D0
Write Enable	10100011	X X X X X X X X	
Write Disable	10100000	X X X X X X X X	
[Write All Locations] ⁽⁸⁾	10100001	X X X X X X X X	D15-D0

Figure 1. A.C. Testing Input/Output Waveform ⁽⁹⁾(¹⁰)(¹¹) ($C_L = 100$ pF)

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Note:

(8) (Write All Locations) is a test mode operation and is therefore not included in the A.C./D.C. Operations specifications.

(9) Input Rise and Fall Times (10% to 90%) < 10 ns.

(10) Input Pulse Levels = $V_{CC} \times 0.2$ and $V_{CC} \times 0.8$.(11) Input and Output Timing Reference = $V_{CC} \times 0.3$ and $V_{CC} \times 0.7$.

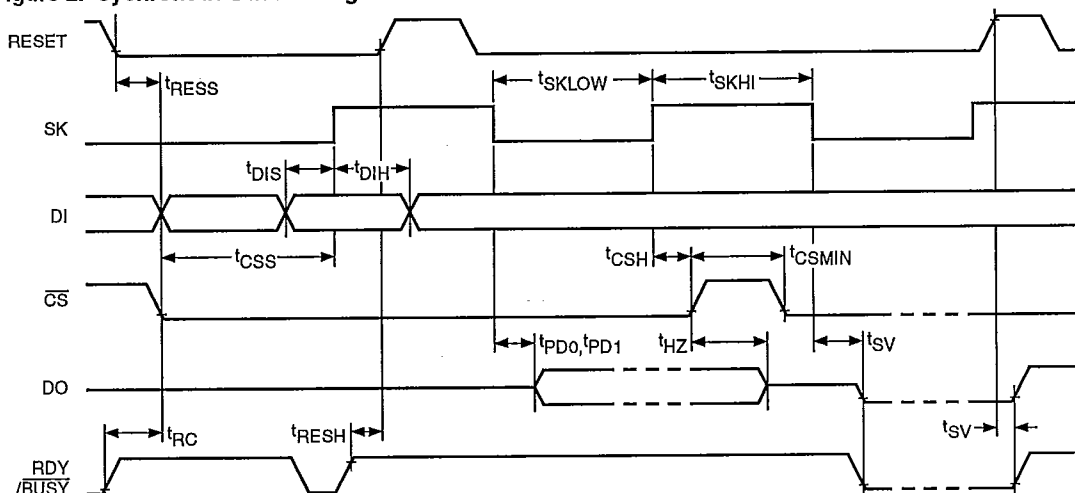
DEVICE OPERATION

The CAT64LC10/CAT64LC10I is a 1K bit nonvolatile memory intended for use with all standard controllers. The CAT64LC10/CAT64LC10I is organized in a 64 x 16 format. All instructions are based on an 8 bit format. There are four 16 bit instructions: READ, WRITE, EWEN, and EWDS. The CAT64LC10/CAT64LC10I operates on a single power supply ranging from 2.5V to 5.5V and it has an on-chip voltage generator to provide the high voltage needed during a programming operation. In-

structions, addresses and data to be written are clocked into the DI pin on the rising edge of the SK clock. The DO pin is normally in a high impedance state except when outputting data in a READ operation or outputting RDY/BUSY status when polled during a WRITE operation.

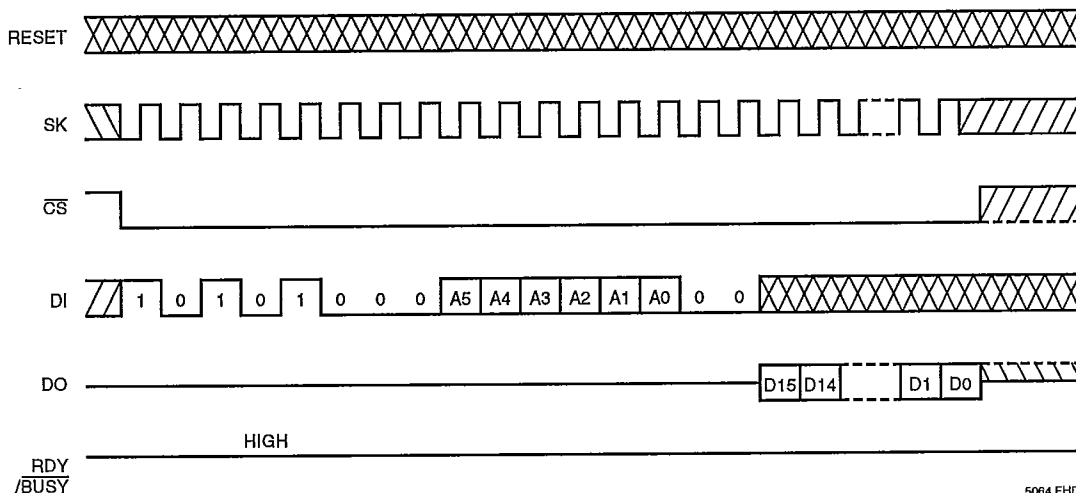
The format for all instructions sent to this device includes a 4 bit start sequence, 1010, a 4 bit op code and an 8 bit address field or dummy bits. For a WRITE operation, a

Figure 2. Synchronous Data Timing



5064 FHD F04

Figure 3. Read Instruction Timing



5064 FHD F05

16 bit data field is also required following the 8 bit address field.

The CAT64LC10/CAT64LC10I requires an active LOW $\overline{CS}$ in order to be selected. Each instruction must be preceded by a HIGH-to-LOW transition of $\overline{CS}$ before the input of the 4 bit start sequence. Prior to the 4 bit start sequence (1010), the device will ignore inputs of all other logical sequence.

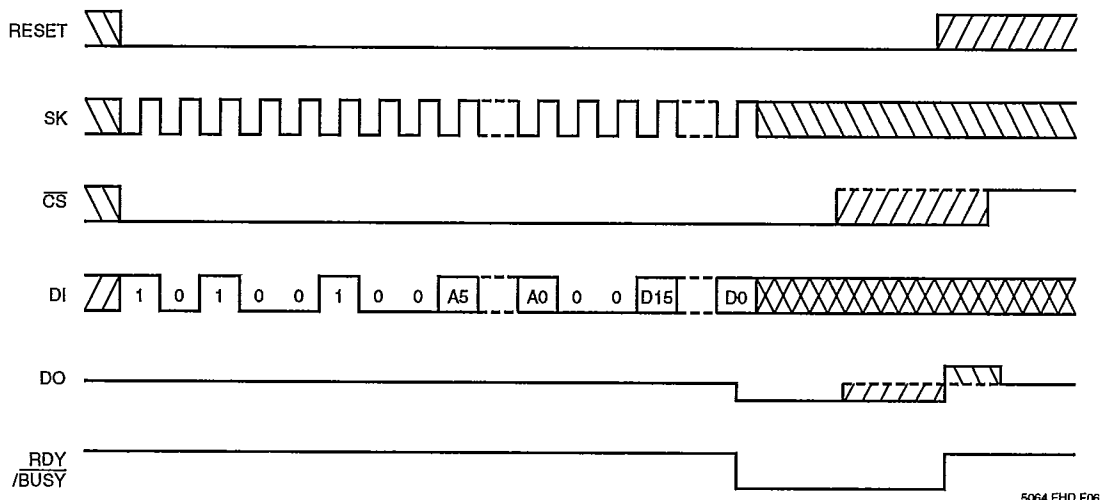
Read

Upon receiving a READ command and address (clocked into the DI pin), the DO pin will output data one t_{PD} after the falling edge of the 16th clock (the last bit of the address field). The READ operation is not affected by the RESET input.

Write

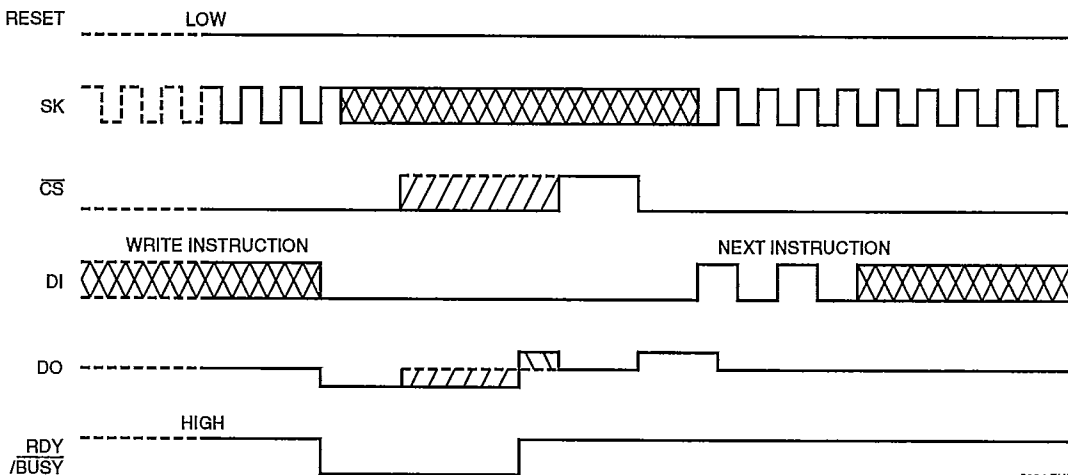
After receiving a WRITE op code, address and data, the device goes into the AUTO-Clear cycle and then the

Figure 4. Write Instruction Timing



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Figure 5. Ready/BUSY Status Instruction Timing



WRITE cycle. The RDY/BUSY pin will output the BUSY status (LOW) one t_{sv} after the rising edge of the 32nd clock (the last data bit) and will stay LOW until the write cycle is complete. Then it will output a logical "1" until the next WRITE cycle. The RDY/BUSY output is not affected by the input of $\overline{CS}$.

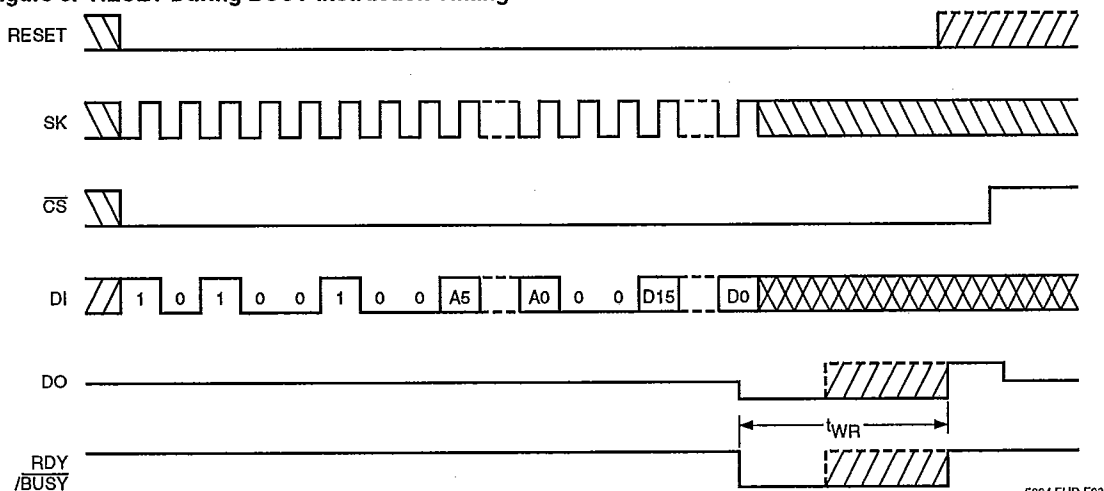
An alternative to get RDY/BUSY status is from the DO pin. During a write cycle, asserting a LOW input to the $\overline{CS}$ pin will cause the DO pin to output the RDY/BUSY status. Bringing $\overline{CS}$ HIGH will bring the DO pin back to a high impedance state again. After the device has completed a WRITE cycle, the DO pin will output a

logical "1" when the device is deselected. The rising edge of the first "1" input on the DI pin will reset DO back to the high impedance state again.

The WRITE operation can be halted anywhere in the operation by the RESET input. If a RESET pulse occurs during a WRITE operation, the device will abort the operation and output a READY status.

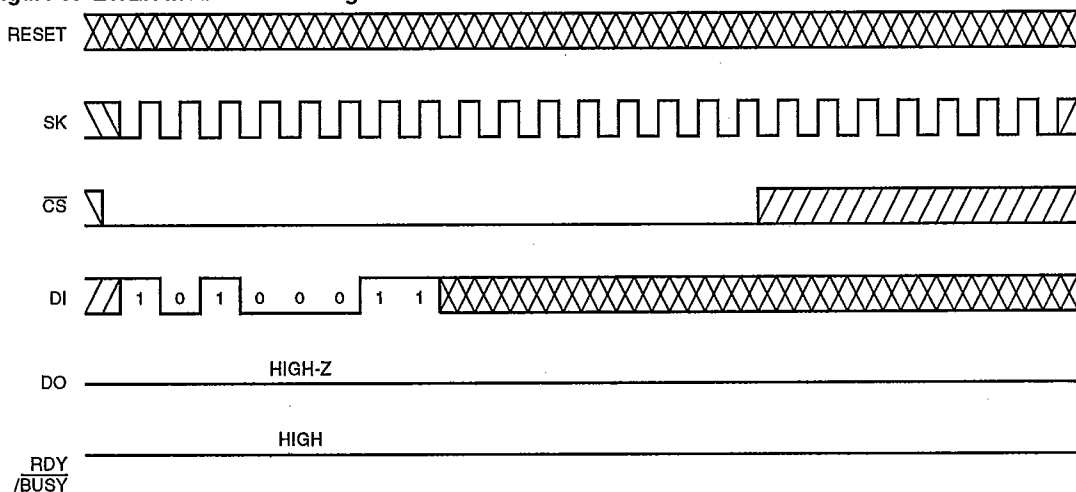
NOTE: Data may be corrupted if a RESET occurs while the device is BUSY. If the reset occurs before the BUSY period, no writing will be initiated. However, if RESET occurs after the BUSY period, new data will have been written over the old data.

Figure 6. RESET During BUSY Instruction Timing



5064 FHD F08

Figure 7. EWEN Instruction Timing



5064 FHD F09

RESET

The RESET pin, when set to HIGH, will reset or abort a WRITE operation. When RESET is set to HIGH while the WRITE instruction is being entered, the device will not execute the WRITE instruction and will keep DO in High-Z condition.

When RESET is set to HIGH, while the device is in a clear/write cycle, the device will abort the operation and will display READY status on the RDY/BUSY pin and on the DO pin if $\overline{CS}$ is low.

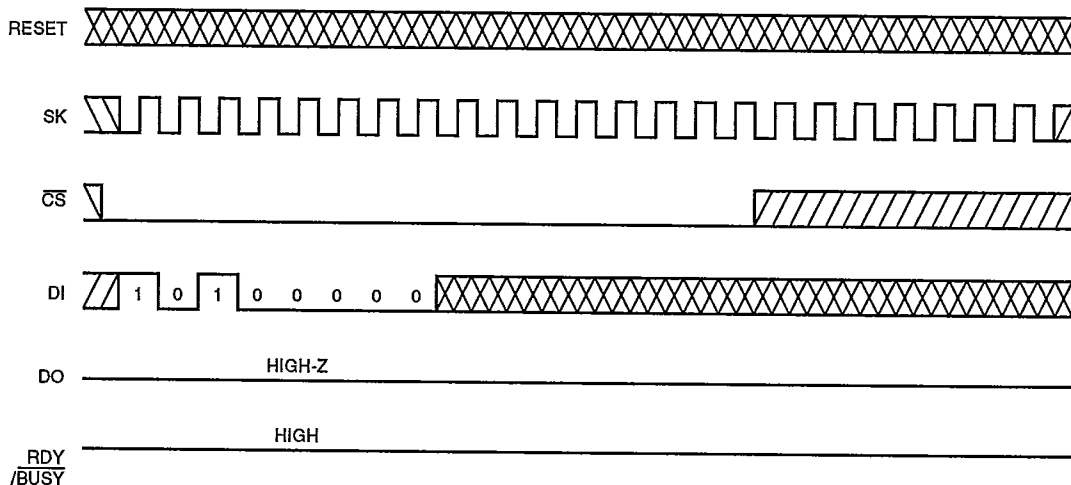
The RESET input affects only the WRITE and WRITE ALL operations. It does not reset any other operations

such as READ, EWEN and EWDS.

ERASE/WRITE ENABLE and DISABLE

The CAT64LC10/CAT64LC10I powers up in the erase/write disabled state. After power-up or while the device is in an erase/write disabled state, any write operation must be preceded by an execution of the EWEN instruction. Once enabled, the device will stay enabled until an EWDS has been executed or a power-down has occurred. The EWDS is used to prevent any inadvertent overwriting of the data. The EWEN and EWDS instructions have no effect on the READ operation and are not affected by the RESET input.

Figure 8. EWDS Instruction Timing



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