NEC

MOS INTEGRATED CIRCUIT

μPD42S16800L, 4216800L, 42S17800L, 4217800L

3.3 V OPERATION 16 M-BIT DYNAMIC RAM 2 M-WORD BY 8-BIT, FAST PAGE MODE

DESCRIPTION ★

The μPD42S16800L, 4216800L, 42S17800L, 4217800L are 2 097 152 words by 8 bits dynamic CMOS RAMs.

These differ in refresh cycle and the μPD42S16800L, 42S17800L can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh (see the table below).

These are packed in 28-pin plastic TSOP(II) (400 mil) and 28-pin plastic SOJ (400 mil).

b

FEATURES ★

- 2 097 152 words by 8 bits organization
- Single +3.3 V±0.3 V power supply
- Fast page mode
- The μPD42S16800L, μPD42S17800L can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh.

Part number	Refresh cycle	Refresh	Power consumption at standby (MAX.)
μPD42S16800L	4 096 cycles/128 ms	$\overline{CAS}$ before $\overline{RAS}$ self refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh	0.54 mW (CMOS level input)
μPD42S17800L	2 048 cycles/128 ms		
μPD4216800L	4 096 cycles/64 ms	$\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh	1.8 mW (CMOS level input)
μPD4217800L	2 048 cycles/32 ms		

- Fast access and cycle time

Part number	Power consumption Active (MAX.)	Access time (MAX.)	R/W cycle time (MIN.)	Fast page mode cycle time (MIN.)
μPD42S16800L-A60, 4216800L-A60	288 mW	60 ns	110 ns	40 ns
μPD42S17800L-A60, 4217800L-A60	360 mW			
μPD42S16800L-A70, 4216800L-A70	252 mW	70 ns	130 ns	45 ns
μPD42S17800L-A70, 4217800L-A70	324 mW			
μPD42S16800L-A80, 4216800L-A80	216 mW	80 ns	150 ns	50 ns
μPD42S17800L-A80, 4217800L-A80	288 mW			

The information in this document is subject to change without notice.

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The mark ★ shows revised points.

★ ORDERING INFORMATION

Part number	Access time (MAX.)	Package	Refresh
μPD42S16800LG5-A60	60 ns	28-pin plastic TSOP (II) (400 mil) Normal pinout	$\overline{CAS}$ before $\overline{RAS}$ self refresh $\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD42S17800LG5-A60			
μPD42S16800LG5-A70	70 ns		
μPD42S17800LG5-A70			
μPD42S16800LG5-A80	80 ns		
μPD42S17800LG5-A80			
μPD42S16800LG5M-A60	60 ns	28-pin plastic TSOP (II) (400 mil) Reverse pinout	
μPD42S17800LG5M-A60			
μPD42S16800LG5M-A70	70 ns		
μPD42S17800LG5M-A70			
μPD42S16800LG5M-A80	80 ns		
μPD42S17800LG5M-A80			
μPD42S16800LLE-A60	60 ns	28-pin plastic SOJ (400 mil)	
μPD42S17800LLE-A60			
μPD42S16800LLE-A70	70 ns		
μPD42S17800LLE-A70			
μPD42S16800LLE-A80	80 ns		
μPD42S17800LLE-A80			
μPD4216800LG5-A60	60 ns	28-pin plastic TSOP (II) (400 mil) Normal pinout	$\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD4217800LG5-A60			
μPD4216800LG5-A70	70 ns		
μPD4217800LG5-A70			
μPD4216800LG5-A80	80 ns		
μPD4217800LG5-A80			
μPD4216800LG5M-A60	60 ns	28-pin plastic TSOP (II) (400 mil) Reverse pinout	
μPD4217800LG5M-A60			
μPD4216800LG5M-A70	70 ns		
μPD4217800LG5M-A70			
μPD4216800LG5M-A80	80 ns		
μPD4217800LG5M-A80			
μPD4216800LLE-A60	60 ns	28-pin plastic SOJ (400 mil)	
μPD4217800LLE-A60			
μPD4216800LLE-A70	70 ns		
μPD4217800LLE-A70			
μPD4216800LLE-A80	80 ns		
μPD4217800LLE-A80			

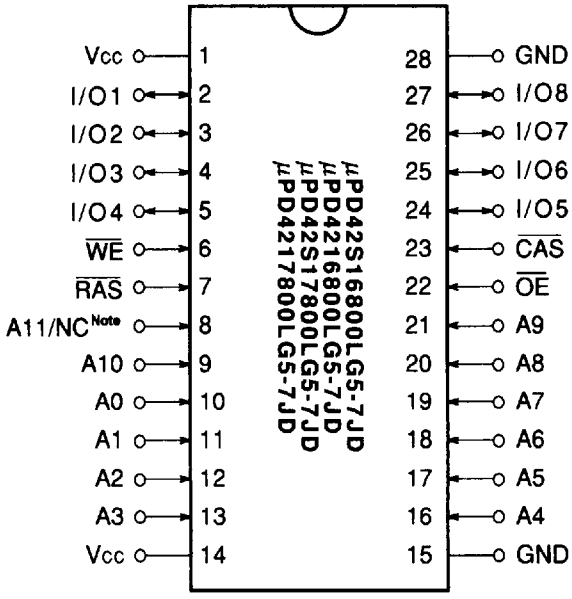
QUALITY GRADE

STANDARD

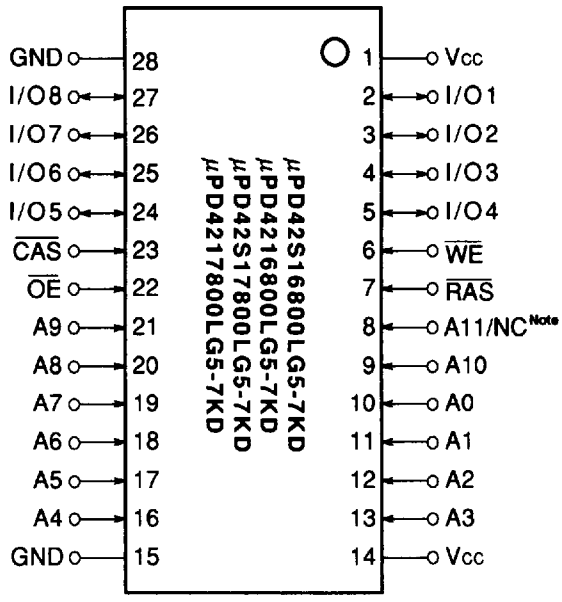
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

PIN CONFIGURATIONS (Marking Side) ★

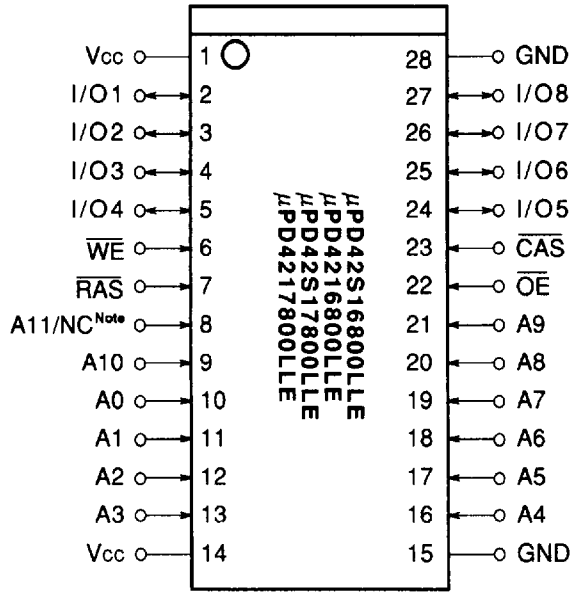
28-pin Plastic TSOP (II)



Reverse bent



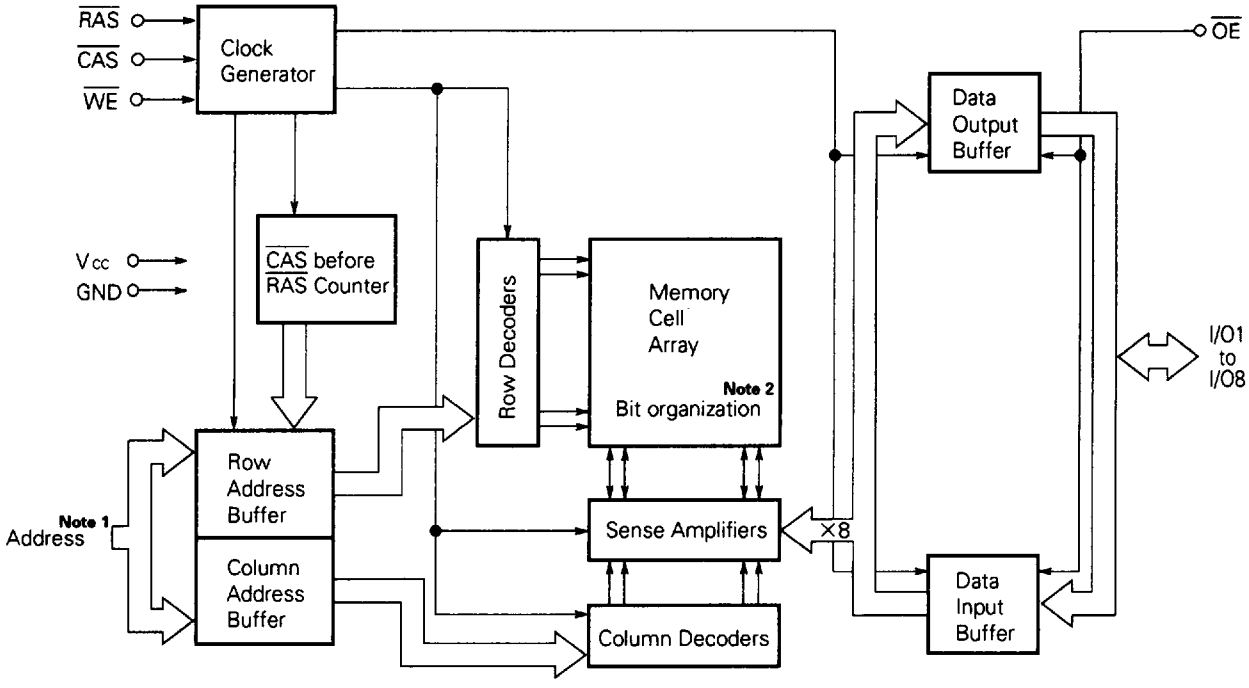
28-pin Plastic SOJ



A0 to A11	: Address inputs
I/O1 to I/O8	: Data Inputs/Outputs
$\overline{RAS}$	: Row address strobe
$\overline{CAS}$	: Column address strobe
$\overline{WE}$	: Write enable
$\overline{OE}$	: Output enable
Vcc	: Supply voltage
GND	: Ground
NC	: No connection

Note A11 ···μPD42S16800L, 4216800L
NC ···μPD42S17800L, 4217800L (No connection)

BLOCK DIAGRAM



Notes 1.

Part number	Row address	Column address
μPD42S16800L, 4216800L	A0 to A11	A0 to A8
μPD42S17800L, 4217800L	A0 to A10	A0 to A9

2. μPD42S16800L, 4216800L...4 096×512×8 μPD42S17800L, 4217800L...2 048×1 024×8

INPUT/OUTPUT PIN FUNCTIONS ★

The μPD42S16800L, 4216800L, 42S17800L, 4217800L have input pins $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$, A0 to A11/A10 [Note1] and input/output pins I/O1 to I/O8.

Pin name	Input/ Output	Function
$\overline{RAS}$ (Row address strobe)	Input	$\overline{RAS}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{CAS}$ before $\overline{RAS}$ refresh.
$\overline{CAS}$ (Column address strobe)		$\overline{CAS}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A11/A10 [Note1] (Address input)		Address bus. Input total 21-bit of address signal, upper 12/11 [Note2]-bit and lower 9/10 [Note3]-bit in sequence (address multiplex method). Therefore, one word is selected from 2 097 152-word by 8-bit memory cell array. In actual operation, latch row address by spacifying row address and activating $\overline{RAS}$. Then, switch the address bus to column address and activate $\overline{CAS}$. Each address is taken into the device when $\overline{RAS}$ and $\overline{CAS}$ are activated. Therefore, the address input setup time (t_{ASR}, t_{ASC}) and hold time (t_{RAH}, t_{CAH}) are specified for the activation of $\overline{RAS}$ and $\overline{CAS}$.
$\overline{WE}$ (Write enable)		Write control signal. Write operation is executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$.
$\overline{OE}$ (Output enable)		Read control signal. Read operation can be executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{OE}$. If $\overline{WE}$ is activated during read operation, $\overline{OE}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O8 (Data input/output)	Input/ Output	8-bit data bus. I/O1 to I/O8 are used to input/output data.

Notes 1. A11···μPD42S16800L, 4216800L A10···μPD42S17800L, 4217800L
2. 12···μPD42S16800L, 4216800L 11···μPD42S17800L, 4217800L
3. 9···μPD42S16800L, 4216800L 10···μPD42S17800L, 4217800L

ELECTRICAL SPECIFICATIONS Notes1, 2

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−0.5 to +4.6	V
Supply voltage	V_{CC}		−0.5 to +4.6	V
Output current	I_O		20	mA
Power dissipation	P_D		1	W
Operating temperature	T_{opt}		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Remark Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		V_{CC} +0.3	V
Low level input voltage	V_{IL}		−0.3		+0.8	V
Ambient temperature	T_a		0		70	°C

CAPACITANCE (T_a = +25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 to A11			5	pF
	C_{I2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$			7	pF
Data Input/Output capacitance	$C_{I/O}$	I/O1 to I/O8			7	pF

DC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted)

[μPD42S16800L, 4216800L]

Parameter		Symbol	Test condition		MIN.	MAX.	Unit	Notes	
Operating current		I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		80	mA	3,4	
				t_{RAC} = 70 ns		70			
				t_{RAC} = 80 ns		60			
Standby current	μPD42S16800L	I_{CC2}	$V_{IH(MIN.)} \leqq \overline{RAS}, \overline{CAS}$	I_O = 0 mA		0.5	mA		
			V_{CC}−0.2 V $\leqq \overline{RAS}, \overline{CAS}$	I_O = 0 mA		0.15			★
	μPD4216800L		$V_{IH(MIN.)} \leqq \overline{RAS}, \overline{CAS}$	I_O = 0 mA		2			
			V_{CC}−0.2 V $\leqq \overline{RAS}, \overline{CAS}$	I_O = 0 mA		0.5			
$\overline{RAS}$ only refresh current		I_{CC3}	$\overline{RAS}$ Cycling $V_{IH(MIN.)} \leqq \overline{CAS}$ $t_{RC} = t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		80	mA	3,4	
				t_{RAC} = 70 ns		70			
				t_{RAC} = 80 ns		60			
Operating current (Fast page mode)		I_{CC4}	$\overline{CAS}$ Cycling $\overline{RAS} \leqq V_{IL(MAX.)}$ $t_{PC} = t_{PC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		70	mA	3,4	
				t_{RAC} = 70 ns		60			
				t_{RAC} = 80 ns		50			
$\overline{CAS}$ before $\overline{RAS}$ refresh current		I_{CC5}	$\overline{RAS}$ Cycling, $t_{RC} = t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		80	mA	3,4	
				t_{RAC} = 70 ns		70			
				t_{RAC} = 80 ns		60			
$\overline{CAS}$ before $\overline{RAS}$ long refresh current (4 096 cycles/128 ms, only for μPD42S16800L)		I_{CC6}	Standby : V_{CC}−0.2 V $\leqq \overline{RAS}$ $\overline{CAS}$ before $\overline{RAS}$ Refresh : 4 096 cycles/128 ms $\overline{RAS}$, $\overline{CAS}$: 0 V $\leqq V_{IL} \leqq$ 0.2 V V_{CC}−0.2 V $\leqq V_{IH} \leqq V_{IH(MAX.)}$ $\overline{WE}$, $\overline{OE}$: V_{IH} Address input : Don't care Output : Open	$t_{RAS} \leqq 1\ \mu s$		220	μA	3,4	★
Self refresh current ($\overline{CAS}$ before $\overline{RAS}$ self refresh, only for μPD42S16800L)		I_{CC7}	I_O = 0 mA $\overline{RAS}$, $\overline{CAS}$: 0 V $\leqq V_{IL} \leqq$ 0.2 V V_{CC}−0.2 V $\leqq V_{IH} \leqq V_{IH(MAX.)}$			150	μA		★
Input leakage current		$I_{I(L)}$	V_I = 0 to 3.6 V all other pins not under test = 0 V		−5	+5	μA		
Output leakage current		$I_{O(L)}$	Outputs are disabled (Hi-Z) V_O = 0 to 3.6 V		−5	+5	μA		
High level output voltage		V_{OH}	I_O = −2.0 mA		2.4		V		
Low level output voltage		V_{OL}	I_O = +2.0 mA			0.4	V		

[μPD42S17800L, 4217800L]

Parameter		Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current		I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		100	mA	3,4
				t_{RAC} = 70 ns		90		
				t_{RAC} = 80 ns		80		
★ Standby current	μPD42S17800L	I_{CC2}	$V_{IH(MIN.)} \leqq \overline{RAS}, \overline{CAS}$	I_O = 0 mA		0.5	mA	
			V_{CC}−0.2 V $\leqq \overline{RAS}, \overline{CAS}$	I_O = 0 mA		0.15		
	μPD4217800L		$V_{IH(MIN.)} \leqq \overline{RAS}, \overline{CAS}$	I_O = 0 mA		2		
			V_{CC}−0.2 V $\leqq \overline{RAS}, \overline{CAS}$	I_O = 0 mA		0.5		
$\overline{RAS}$ only refresh current		I_{CC3}	$\overline{RAS}$ Cycling $V_{IH(MIN.)} \leqq \overline{CAS}$ $t_{RC} = t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		100	mA	3,4
				t_{RAC} = 70 ns		90		
				t_{RAC} = 80 ns		80		
Operating current (Fast page mode)		I_{CC4}	$\overline{CAS}$ Cycling $\overline{RAS} \leqq V_{IL(MAX.)}$ $t_{PC} = t_{PC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		70	mA	3,4
				t_{RAC} = 70 ns		60		
				t_{RAC} = 80 ns		50		
$\overline{CAS}$ before $\overline{RAS}$ refresh current		I_{CC5}	$\overline{RAS}$ Cycling, $t_{RC} = t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		100	mA	3,4
				t_{RAC} = 70 ns		90		
				t_{RAC} = 80 ns		80		
★ $\overline{CAS}$ before $\overline{RAS}$ long refresh current (2 048 cycles/128 ms, only for μPD42S17800L)		I_{CC6}	Standby : V_{CC}−0.2 V $\leqq \overline{RAS}$ $\overline{CAS}$ before $\overline{RAS}$ Refresh : 2 048 cycles/128 ms $\overline{RAS}$, $\overline{CAS}$: 0 V $\leqq V_{IL} \leqq$ 0.2 V V_{CC}−0.2 V $\leqq V_{IH} \leqq V_{IH(MAX.)}$ $\overline{WE}$, $\overline{OE}$: V_{IH} Address input : Don't care Output : Open	$t_{RAS} \leqq 1\ \mu s$		200	μA	3,4
★ Self refresh current ($\overline{CAS}$ before $\overline{RAS}$ self refresh, only for μPD42S17800L)		I_{CC7}	I_O = 0 mA $\overline{RAS}$, $\overline{CAS}$: 0 V $\leqq V_{IL} \leqq$ 0.2 V V_{CC}−0.2 V $\leqq V_{IH} \leqq V_{IH(MAX.)}$			150	μA	
Input leakage current		$I_{I(L)}$	V_I = 0 to 3.6 V all other pins not under test = 0 V		−5	+5	μA	
Output leakage current		$I_{O(L)}$	Outputs are disabled (Hi-Z) V_O = 0 to 3.6 V		−5	+5	μA	
High level output voltage		V_{OH}	I_O = −2.0 mA		2.4		V	
Low level output voltage		V_{OL}	I_O = +2.0 mA			0.4	V	

AC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted) Notes 5, 6 (1/2)

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Random Read or Write Cycle Time	t_{RC}	110		130		150		ns	7
Read Write Cycle Time	t_{RWC}	160		180		200		ns	7
Fast Page Mode Cycle Time (Read or Write)	t_{PC}	40		45		50		ns	7
Read Modify Write Cycle Time (Fast Page Mode)	t_{PRWC}	85		90		100		ns	7
Access Time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	8, 9
Access Time from $\overline{CAS}$ (Falling Edge)	t_{CAC}		15		18		20	ns	8, 9
Access Time from Column Address	t_{AA}		30		35		40	ns	8, 9
Access Time from $\overline{CAS}$ Precharge	t_{ACP}		35		40		45	ns	9
Access Time from $\overline{OE}$	t_{OEA}		15		18		20	ns	9
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	ns	8
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0		0		0		ns	9
$\overline{OE}$ to Data Setup Time	t_{OLZ}	0		0		0		ns	9
Output Buffer Turn-off Delay Time ($\overline{CAS}$)	t_{OFF}	0	13	0	15	0	15	ns	10
$\overline{OE}$ to Data Delay Time	t_{OED}	13		15		15		ns	
Output Buffer Turn-off Delay Time ($\overline{OE}$)	t_{OEZ}	0	13	0	15	0	15	ns	10
$\overline{OE}$ Command Hold Time	t_{OEH}	0		0		0		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive Setup Time	t_{OES}	0		0		0		ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ Pulse Width (Random Read, Write Cycle)	t_{RAS}	60	10 000	70	10 000	80	10 000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	125 000	70	125 000	80	125 000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15		18		20		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10 000	18	10 000	20	10 000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60		70		80		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	45	20	50	25	60	ns	8
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5		5		5		ns	11
$\overline{CAS}$ Precharge Time	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5		5		5		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35		40		45		ns	
Row Address Setup Time	t_{ASR}	0		0		0		ns	
Row Address Hold Time	t_{RAH}	10		10		12		ns	

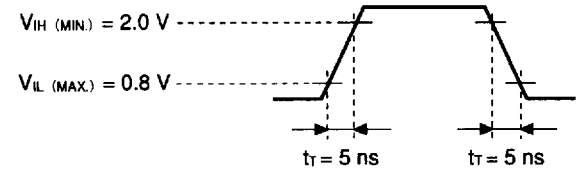
(2/2)

Parameter		Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Column Address Setup Time		t_{ASC}	0		0		0		ns	
Column Address Hold Time		t_{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to $\overline{RAS}$		t_{RAL}	30		35		40		ns	
Read Command Setup Time		t_{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$		t_{RRH}	0		0		0		ns	12
Read Command Hold Time Referenced to $\overline{CAS}$		t_{RCH}	0		0		0		ns	12
Write Command Hold Time Referenced to $\overline{CAS}$		t_{WCH}	10		10		15		ns	13
Write Command Pulse Width		t_{WP}	10		10		15		ns	13
Data-in Setup Time		t_{DS}	0		0		0		ns	14
Data-in Hold Time		t_{DH}	10		15		15		ns	14
$\overline{WE}$ Command Setup Time		t_{WCS}	0		0		0		ns	15
$\overline{CAS}$ to $\overline{WE}$ Delay Time		t_{CWD}	38		43		45		ns	15
$\overline{RAS}$ to $\overline{WE}$ Delay Time		t_{RWD}	83		95		105		ns	15
$\overline{CAS}$ Precharge Delay Time Referenced to $\overline{WE}$ (Fast Page Mode)		t_{CPWD}	58		65		70		ns	15
Column Address Delay Time Referenced to $\overline{WE}$		t_{AWD}	53		60		65		ns	15
Write Command Lead Time Referenced to $\overline{RAS}$		t_{RWL}	20		20		20		ns	
Write Command Lead Time Referenced to $\overline{CAS}$		t_{CWL}	15		15		15		ns	
$\overline{CAS}$ Setup Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh		t_{CSR}	5		5		5		ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh		t_{CHR}	10		10		10		ns	
$\overline{RAS}$ Pulse Width ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh Cycle)		t_{RASS}	100		100		100		μs	16
$\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh Cycle)		t_{RPS}	110		130		150		ns	16
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh Cycle)		t_{CHS}	−50		−50		−50		ns	16
$\overline{WE}$ Setup Time		t_{WSR}	10		10		10		ns	
$\overline{WE}$ Hold Time		t_{WHR}	15		15		15		ns	
★ Refresh Time	μPD42S16800L, 42S17800L	t_{REF}		128		128		128	ms	16
	μPD4216800L			64		64		64		
	μPD4217800L			32		32		32		

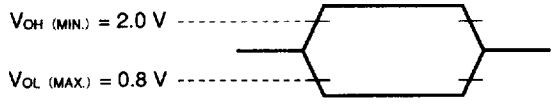
Notes

1. All voltages are referenced to GND.
2. After power-up, wait more than 100 μs and then, execute 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles or 8 $\overline{RAS}$ only refresh cycles to initialize the internal circuit.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5}, and I_{CC6} depend on t_{RC} and t_{PC}. Specified values are obtained with outputs open.
4. Address can be changed once or less while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
5. AC measurements assume t_T = 5 ns.
6. AC Characteristics test condition

   (1) Input timing specification



   (2) Output timing specification

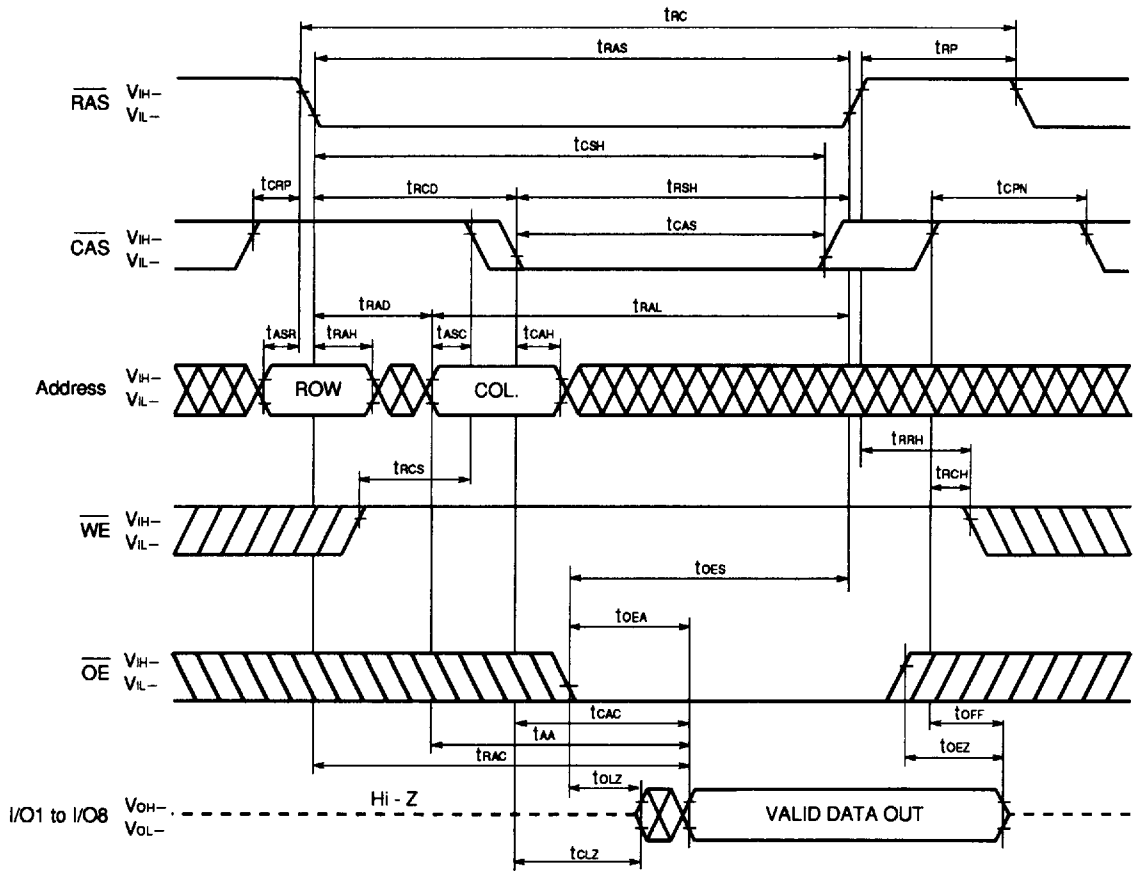


7. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (T_a = 0 to 70 °C) is assured.
8. In random read cycle, the access time is changed by the conditions of t_{RAD} and t_{RCD} as follows.

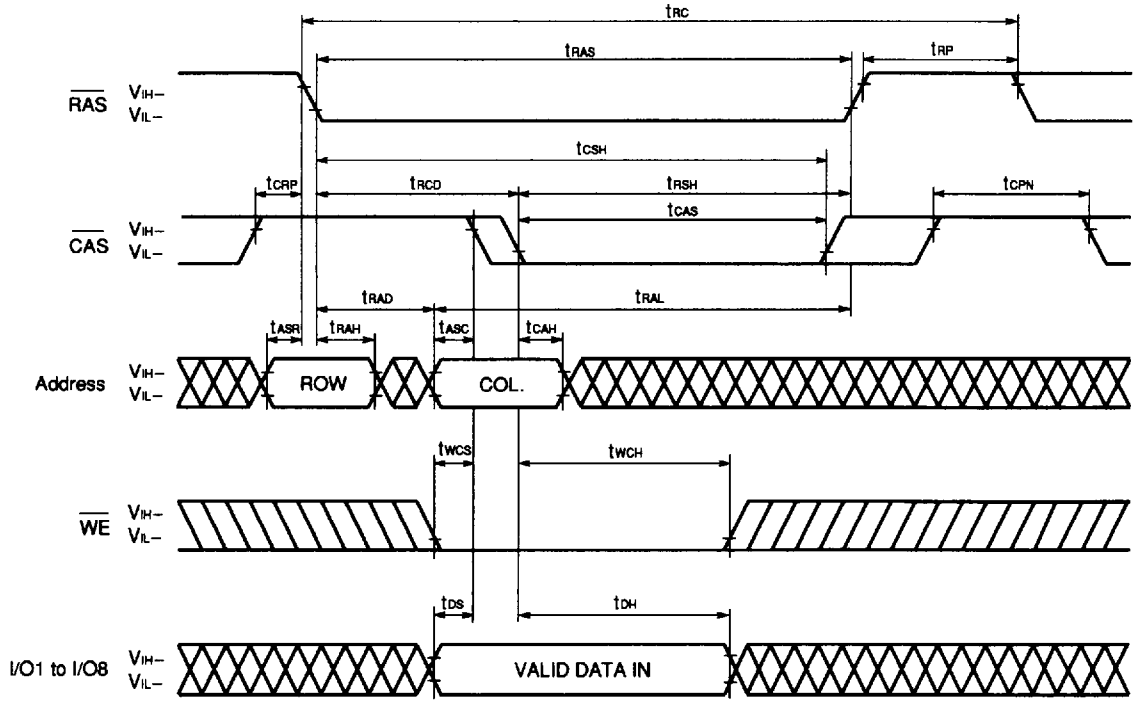
CONDITION	ACCESS TIME
$t_{RAD} \leqq t_{RAD\ (MAX.)}$ and $t_{RCD} \leqq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD\ (MAX.)} < t_{RAD}$ and $t_{RCD} \leqq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$
$t_{RCD\ (MAX.)} < t_{RCD}$	$t_{CAC\ (MAX.)}$

   $t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ indicate the points which the access time changes and are not the limits of operation.
9. Loading conditions are 1 TTL and 100 pF.
10. $t_{OFF\ (MAX.)}$ and $t_{OEZ\ (MAX.)}$ define the time at which the output achieves the open circuit condition and are not referenced to V_{OH} or V_{OL}.
11. $t_{CRP\ (MIN.)}$ requirement should be applicable for $\overline{RAS}$ / $\overline{CAS}$ cycles preceded by any cycles.
12. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN.)}$ must be satisfied for a read cycle.
13. $t_{WP\ (MIN.)}$ is applicable for late write cycle or read modify write cycle. In early write cycles, $t_{WCH\ (MIN.)}$ should be satisfied.
14. This specification is referenced to $\overline{CAS}$ falling edge in early write cycles and to $\overline{WE}$ falling edge in late write or read modify write cycles.
15. If $t_{WCS} \geqq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geqq t_{RWD\ (MIN.)}$, $t_{CWD} \geqq t_{CWD\ (MIN.)}$, $t_{AWD} \geqq t_{AWD\ (MIN.)}$, $t_{CPWD} \geqq t_{CPWD\ (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data out is indeterminate.
16. This specification is applicable only for μPD42S16800L and μPD42S17800L.

READ CYCLE

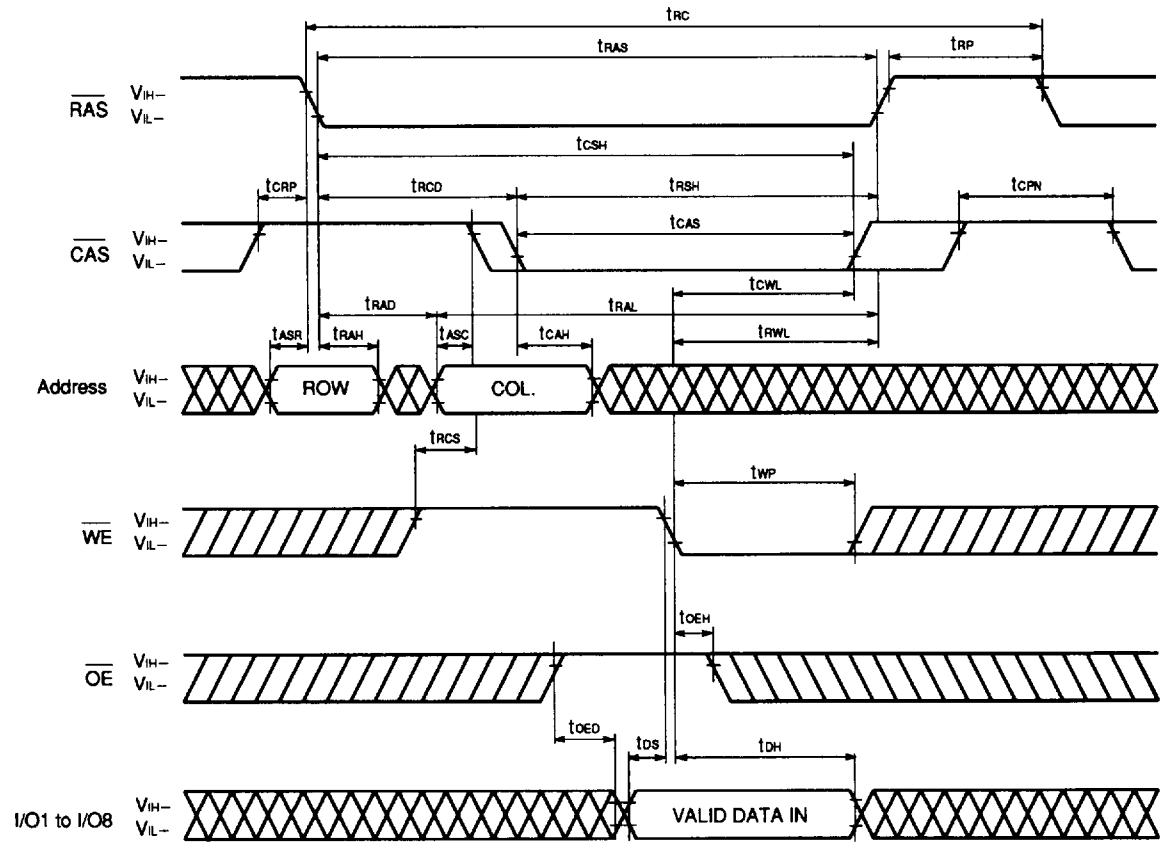


EARLY WRITE CYCLE

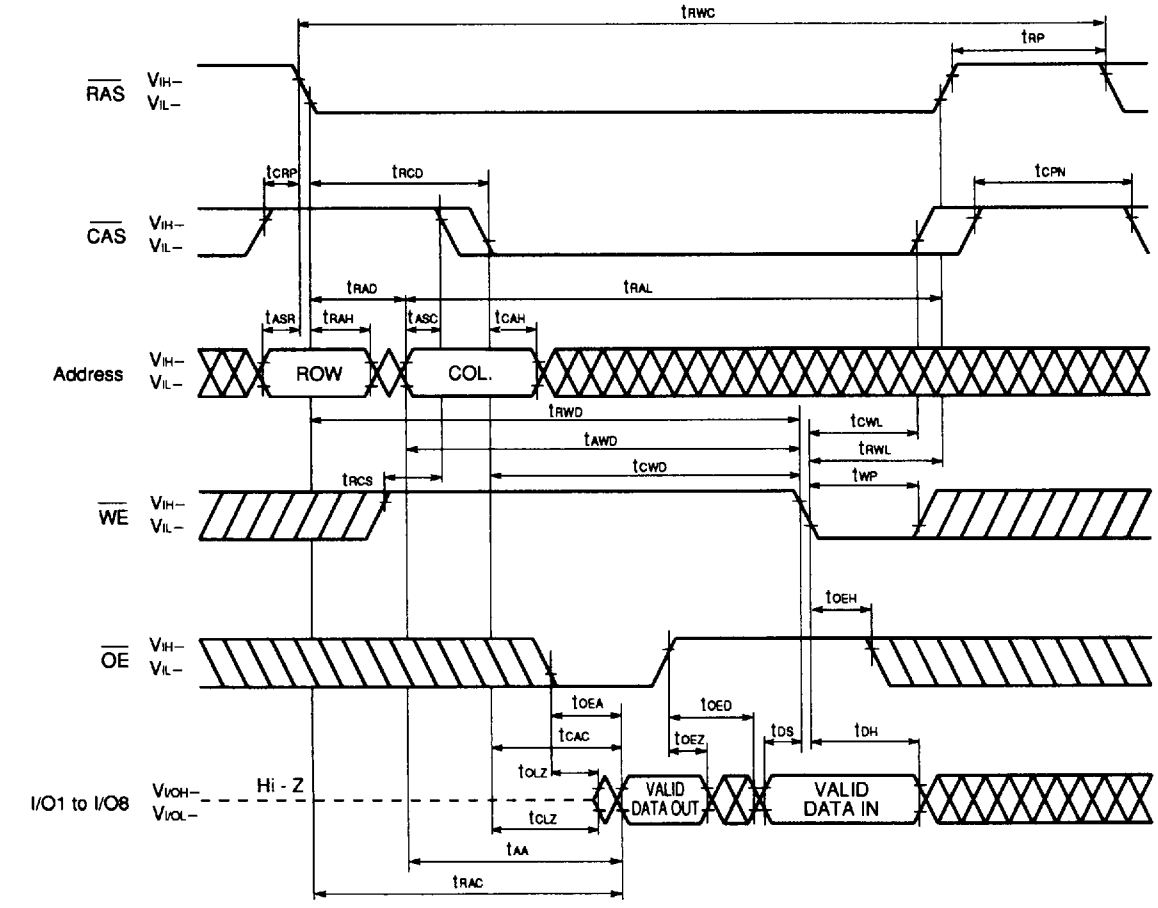


Remark $\overline{OE}$ = Don't Care

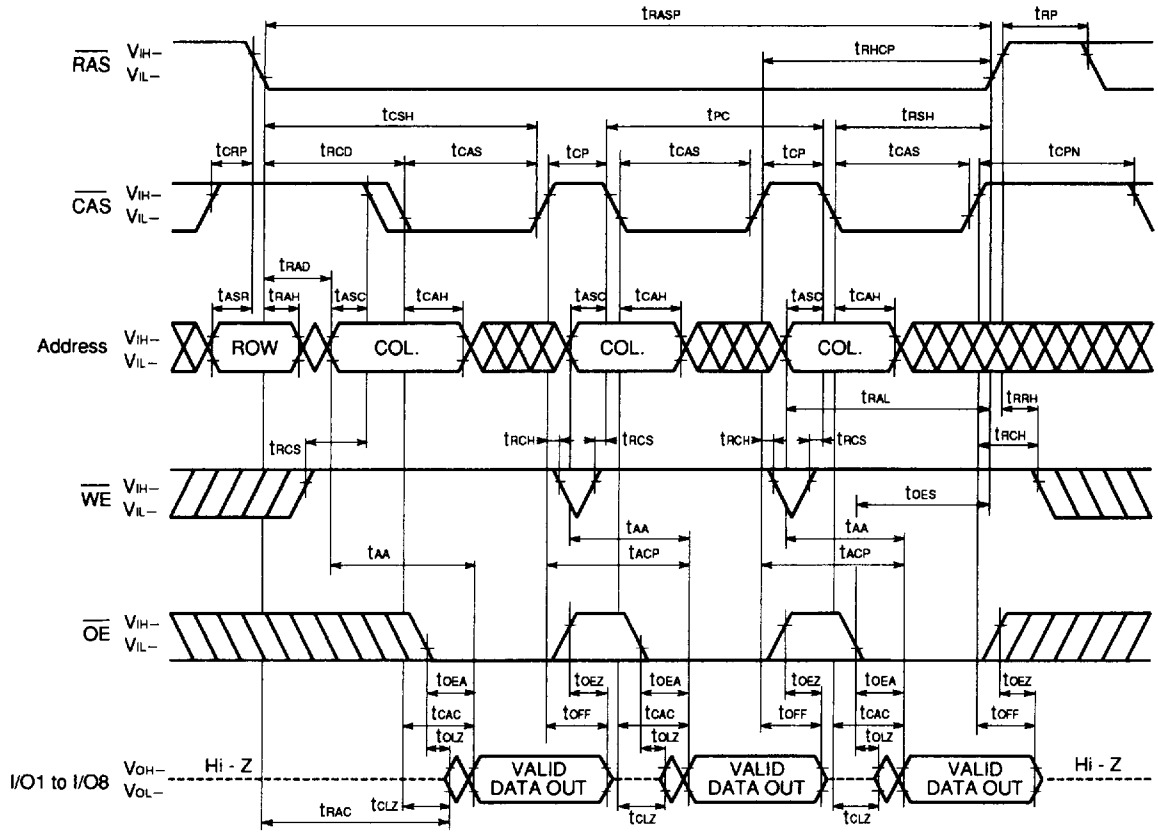
LATE WRITE CYCLE



READ MODIFY WRITE CYCLE

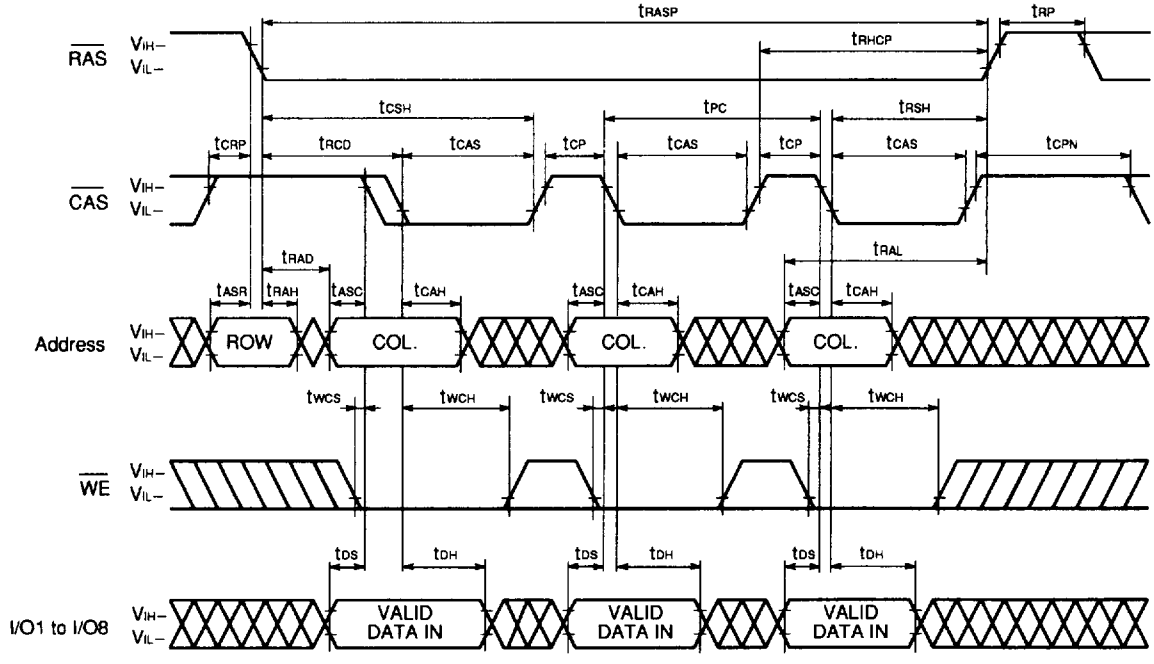


FAST PAGE MODE READ CYCLE



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

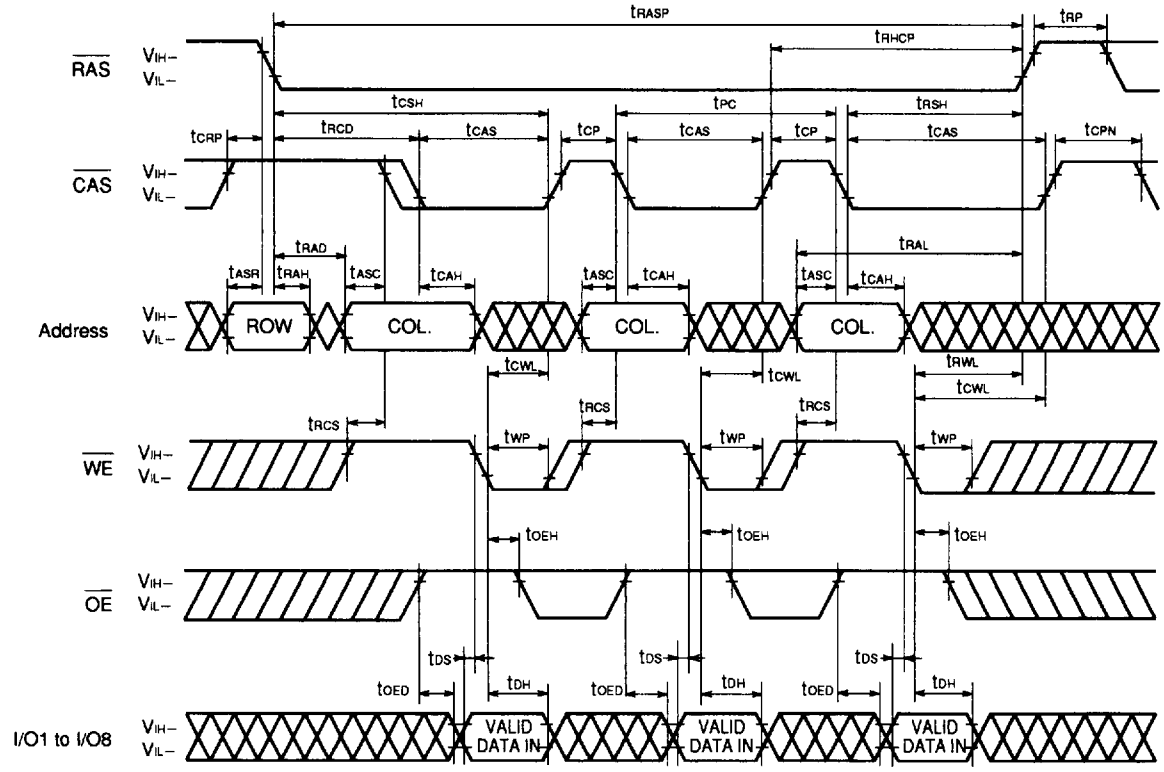
FAST PAGE MODE EARLY WRITE CYCLE



Remark $\overline{OE}$ = Don't Care

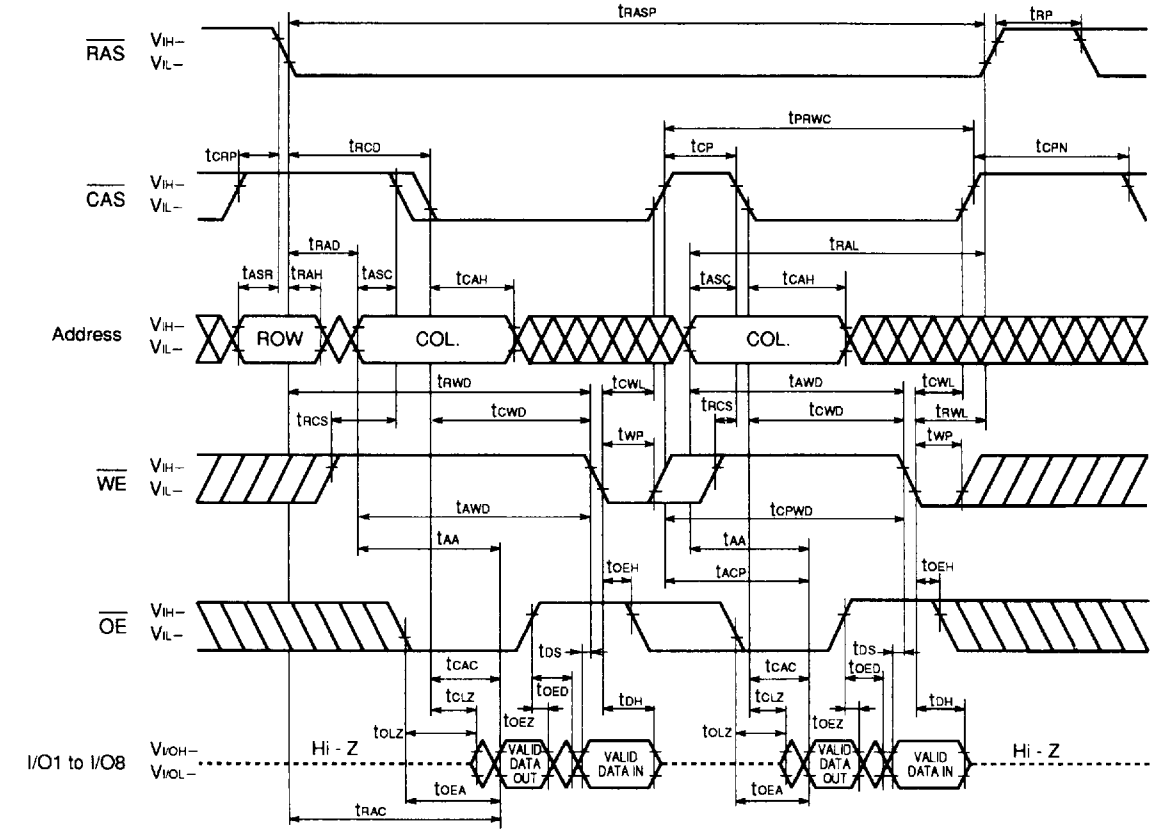
In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

FAST PAGE MODE LATE WRITE CYCLE



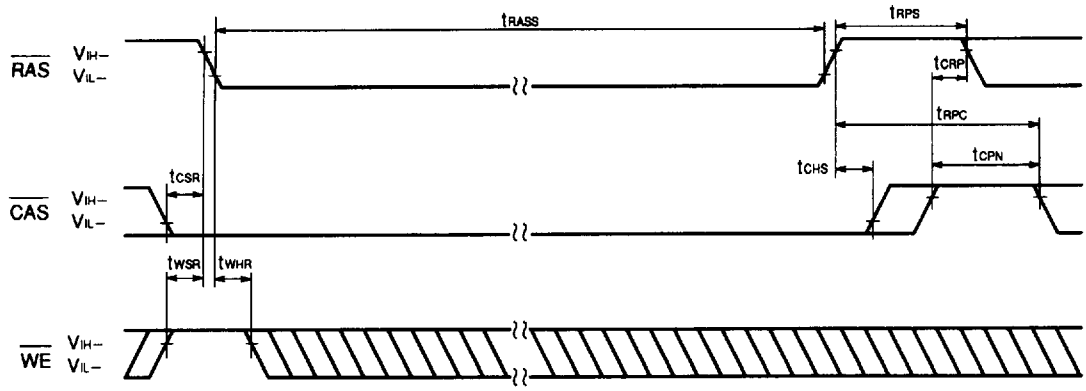
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

FAST PAGE MODE READ MODIFY WRITE CYCLE



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

$\overline{CAS}$ BEFORE $\overline{RAS}$ SELF REFRESH CYCLE (Only for μPD42S16800L, 42S17800L)



Remark Address, $\overline{OE}$ = Don't care I/O1 to I/O8 = Hi - Z

How to use $\overline{CAS}$ before $\overline{RAS}$ self refresh mode

$\overline{CAS}$ before $\overline{RAS}$ self refresh mode can't be used by itself. It must be used with perfoming one of 3 refreshes below.

- **When using distributed $\overline{CAS}$ before $\overline{RAS}$ refresh**

★ Refresh 4 096 times (μPD42S16800L) or 2 048 times (μPD42S17800L) during 128 ms before set into the $\overline{CAS}$ before $\overline{RAS}$ self refresh mode and after reset.

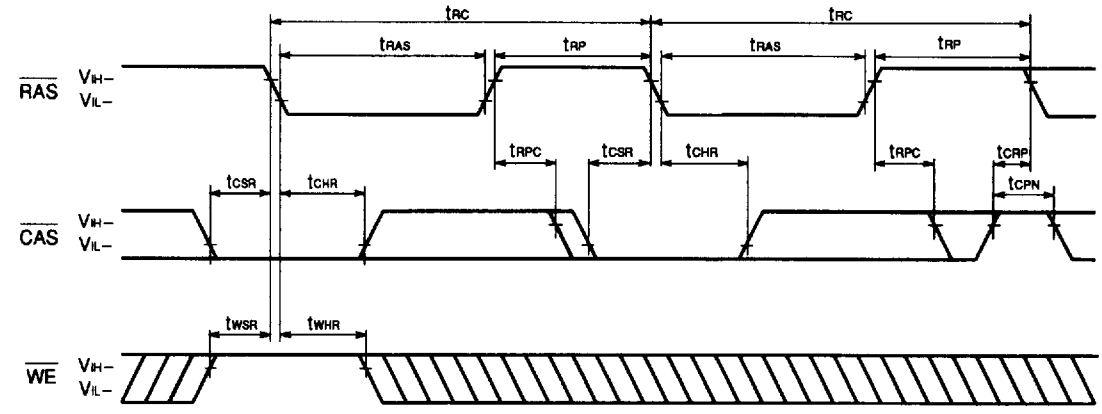
- **When using burst $\overline{CAS}$ before $\overline{RAS}$ refresh**

Refresh 4 096 times during 64 ms (μPD42S16800L) or 2 048 times during 32 ms (μPD42S17800L) before set into the $\overline{CAS}$ before $\overline{RAS}$ self refresh mode and after reset.

- **When using $\overline{RAS}$ only refresh**

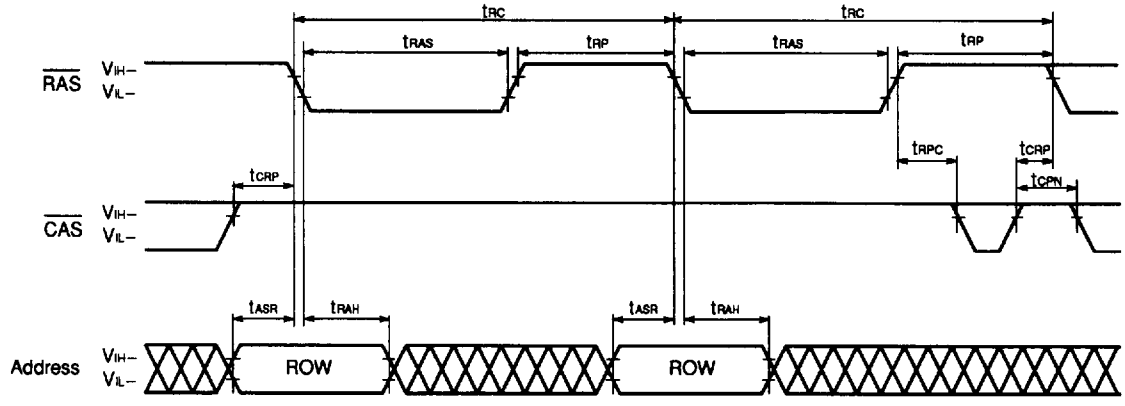
Refresh against all refresh addresses during 64 ms (μPD42S16800L) or during 32 ms (μPD42S17800L) before set into the $\overline{CAS}$ before $\overline{RAS}$ self refresh mode and after reset.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE ★



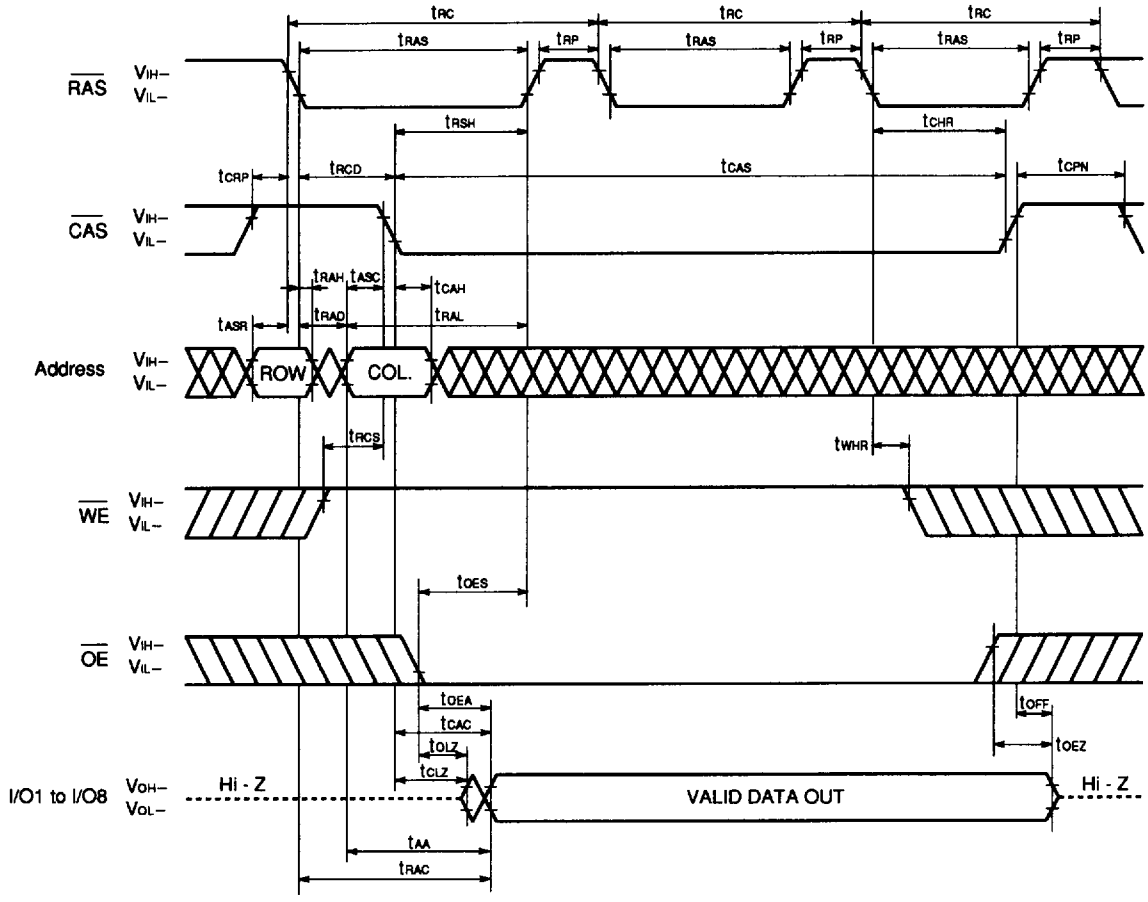
Remark Address, $\overline{OE}$ = Don't care I/O1 to I/O8 = Hi - Z

$\overline{RAS}$ ONLY REFRESH CYCLE ★

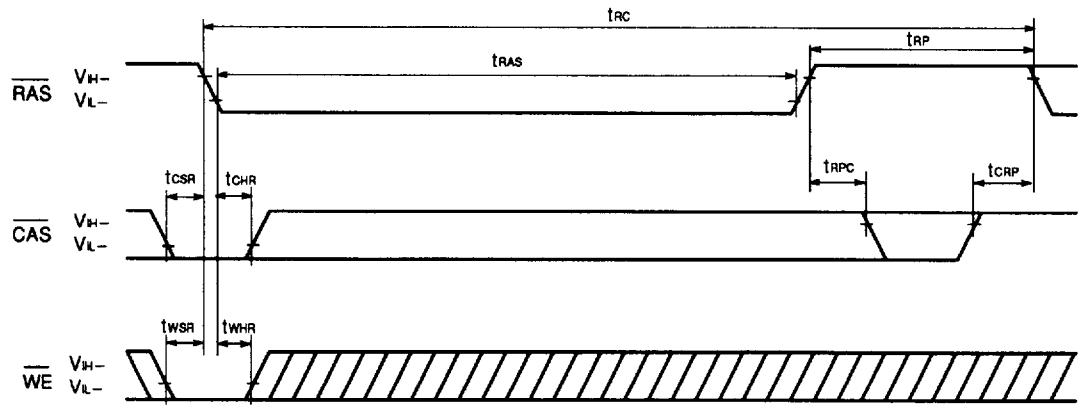


Remark $\overline{WE}$, $\overline{OE}$ = Don't care I/O1 to I/O8 = Hi - Z

HIDDEN REFRESH CYCLE



TEST MODE SET CYCLE ($\overline{WE}$ AND $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE)



Remark Address, $\overline{OE}$ = Don't care I/O1 to I/O8 = Hi - Z

TEST MODE

TEST MODE is fast test function. On using this mode, test time is reduced to 1/2. In this TEST MODE, internal organization is 1 M words by 16 bits apparently. Don't care about the input levels of the $\overline{CAS}$ input A0.

1. How to enter TEST MODE

Through TEST MODE SET CYCLE ($\overline{WE}$ and $\overline{CAS}$ before $\overline{RAS}$ refresh cycle), the device enters TEST MODE.

2. Write / Read in TEST MODE

Write data of "1" or "0" through I/O1 to I/O8 by controlling address except for above-mentioned address. Each input data through each I/O write 2 bits at once. And read through I/O1 to I/O8 to check written data. In case of writing each 2 bits rightly, each I/O data is "1". But wrong, the data is "0".

3. Refresh in TEST MODE

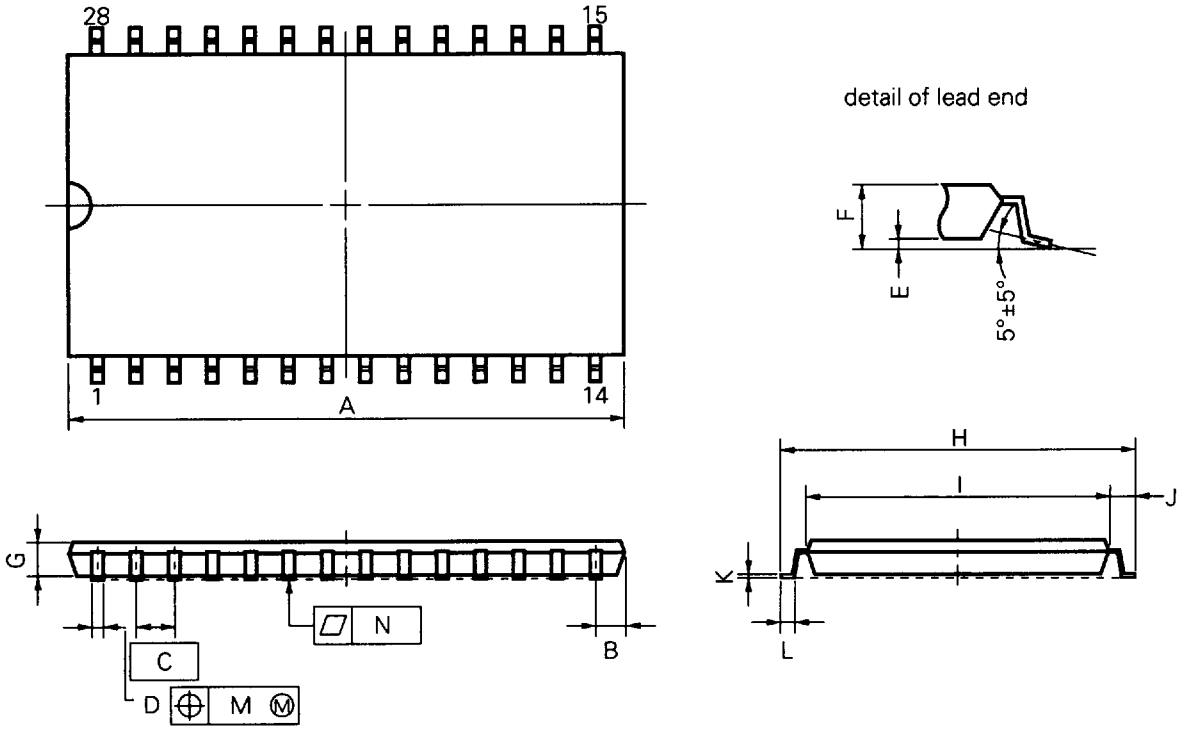
Use normal read cycle or $\overline{WE}$ and $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.

4. How to exit from TEST MODE

Through $\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, the device exits from TEST MODE.

PACKAGE DRAWINGS

28 PIN PLASTIC TSOP(II) (400 mil)



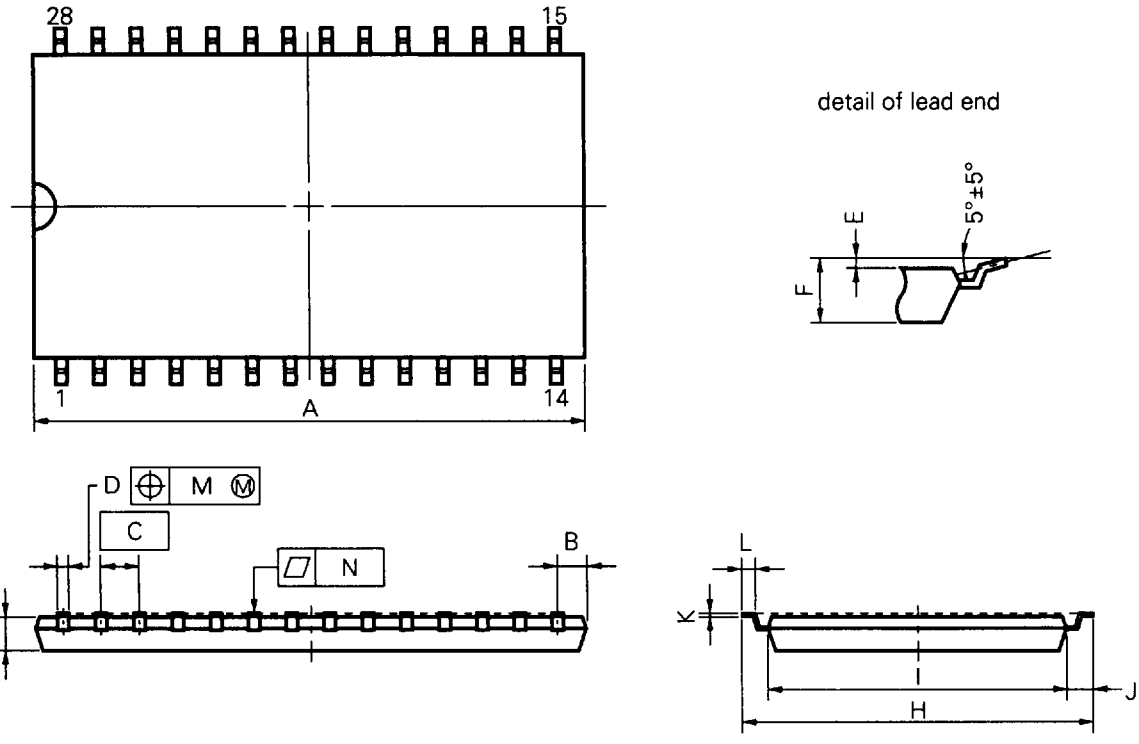
S28G5-50-7JD2-1

NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	18.81 MAX.	0.741 MAX.
B	1.15 MAX.	0.046 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40 ± 0.10	$0.016^{+0.004}_{-0.005}$
E	0.05 ± 0.05	0.002 ± 0.002
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	11.76 ± 0.2	0.463 ± 0.008
I	10.16 ± 0.1	0.400 ± 0.004
J	0.8 ± 0.2	$0.031^{+0.009}_{-0.008}$
K	$0.125^{+0.10}_{-0.05}$	$0.005^{+0.004}_{-0.002}$
L	0.5 ± 0.1	$0.020^{+0.004}_{-0.005}$
M	0.21	0.009
N	0.10	0.004

28 PIN PLASTIC TSOP(III) (400 mil)



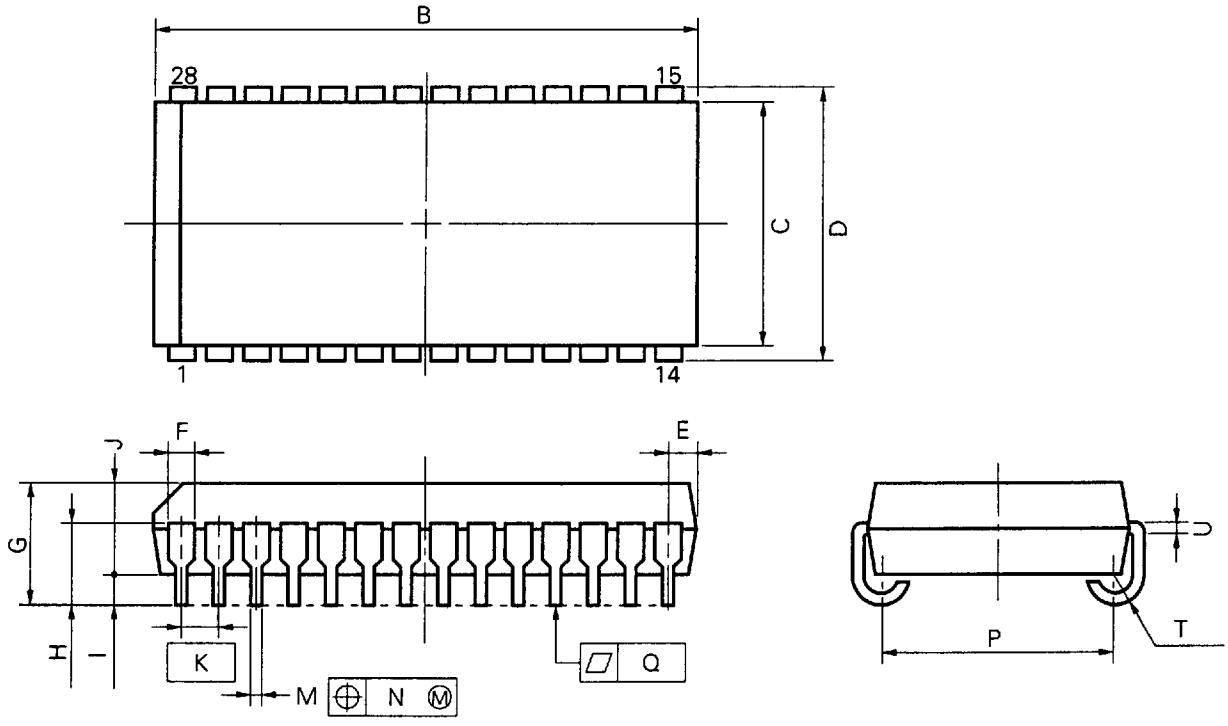
S28G5-50-7KD2-1

NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	18.81 MAX.	0.741 MAX.
B	1.15 MAX.	0.046 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40 ± 0.10	$0.016^{+0.004}_{-0.005}$
E	0.05 ± 0.05	0.002 ± 0.002
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	11.76 ± 0.2	0.463 ± 0.008
I	10.16 ± 0.1	0.400 ± 0.004
J	0.8 ± 0.2	$0.031^{+0.009}_{-0.008}$
K	$0.125^{+0.10}_{-0.05}$	$0.005^{+0.004}_{-0.002}$
L	0.5 ± 0.1	$0.020^{+0.004}_{-0.005}$
M	0.21	0.009
N	0.10	0.004

28 PIN PLASTIC SOJ (400 mil)



P28LE-400A1

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	$18.67^{+0.2}_{-0.35}$	$0.735^{+0.008}_{-0.013}$
C	10.16	0.400
D	11.18±0.2	$0.440^{+0.008}_{-0.007}$
E	1.08±0.15	$0.043^{+0.006}_{-0.007}$
F	0.74	0.029
G	3.5±0.2	$0.138^{+0.008}_{-0.007}$
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	9.40±0.20	$0.370^{+0.008}_{-0.007}$
Q	0.10	0.004
T	R 0.85	R 0.033
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

RECOMMENDED SOLDERING CONDITIONS

Please consult with our sales offices for soldering conditions of the μPD42S16800L, 4216800L, 42S17800L, 4217800L.

TYPE OF SURFACE MOUNT DEVICE

μPD42S16800LG5, 4216800LG5, 42S17800LG5, 4217800LG5 : 28-pin Plastic TSOP (II) (400 mil)
μPD42S16800LLE, 4216800LLE, 42S17800LLE, 4217800LLE : 28-pin Plastic SOJ (400 mil)

3. PACKAGE DRAWINGS

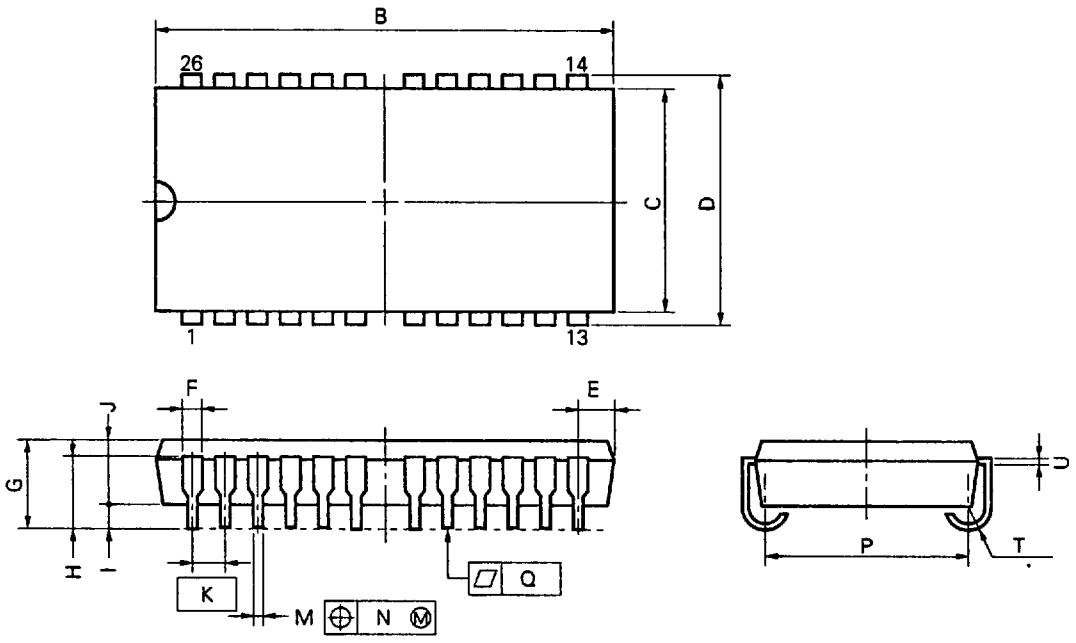
* : under development

PAGE(S) INTENTIONALLY BLANK

26 PIN PLASTIC SOJ (300mil)

24 Leads

NEC Cord:S26LA-300A



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

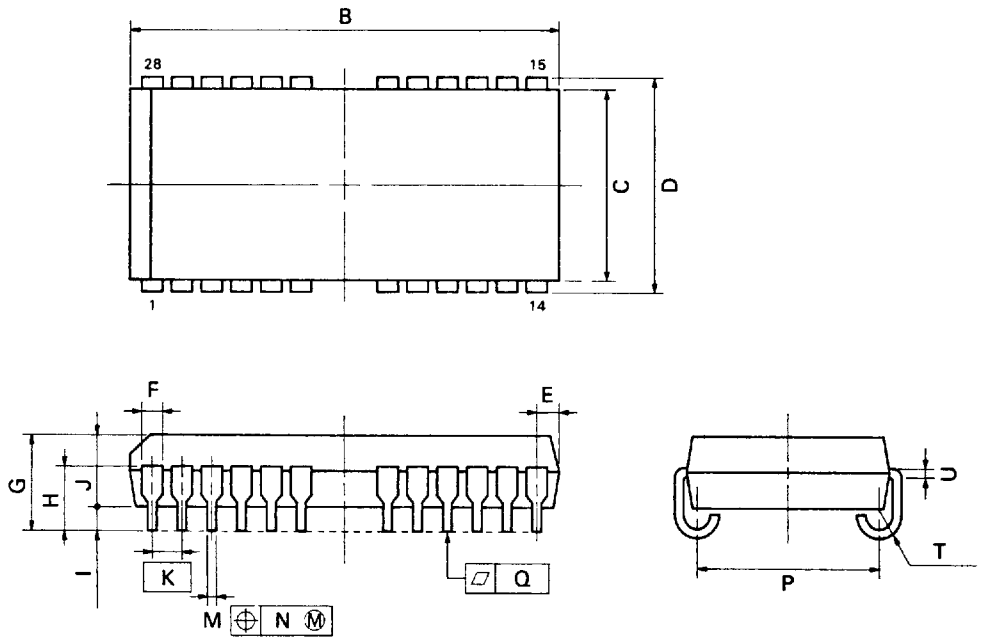
S26LA-300A

ITEM	MILLIMETERS	INCHES
B	$17.1^{+0.25}_{-0.05}$	$0.673^{+0.010}_{-0.002}$
C	7.62	0.300
D	8.47±0.2	$0.333^{+0.009}_{-0.008}$
E	1.03±0.15	$0.041^{+0.006}_{-0.007}$
F	0.74	0.029
G	3.5±0.2	0.138±0.008
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	6.73±0.20	0.265±0.008
Q	0.10	0.004
T	R 0.85	R 0.033
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

28 PIN PLASTIC SOJ (400mil)

24 Leads

NEC Cord:P28LE-400A



P28LE-400A

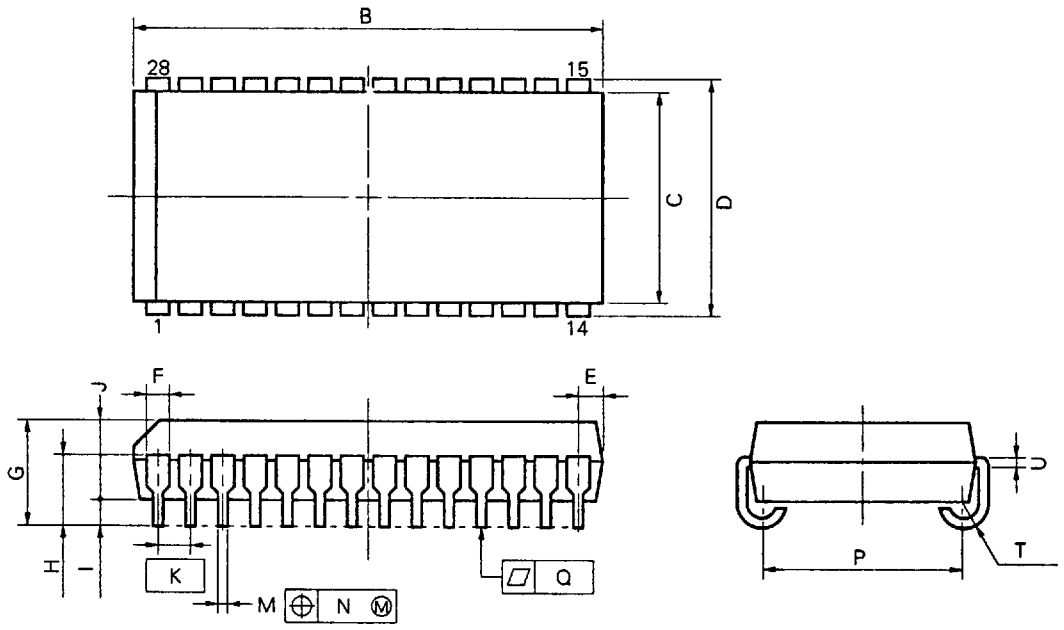
NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	$18.67^{+0.2}_{-0.35}$	$0.735^{+0.008}_{-0.013}$
C	10.16	0.400
D	$11.18^{\pm 0.2}$	$0.440^{+0.008}_{-0.007}$
E	$1.08^{\pm 0.15}$	$0.043^{+0.006}_{-0.007}$
F	0.7	0.028
G	$3.5^{\pm 0.2}$	$0.138^{+0.008}_{-0.007}$
H	$2.4^{\pm 0.2}$	$0.094^{+0.009}_{-0.008}$
I	0.8 MIN	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	$0.40^{\pm 0.10}$	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	$9.40^{\pm 0.20}$	$0.370^{+0.008}_{-0.007}$
Q	0.15	0.006
T	R0.85	R0.033
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

28 PIN PLASTIC SOJ (400mil)
28 Leads

NEC Cord:P28LE-400A1



NOTE

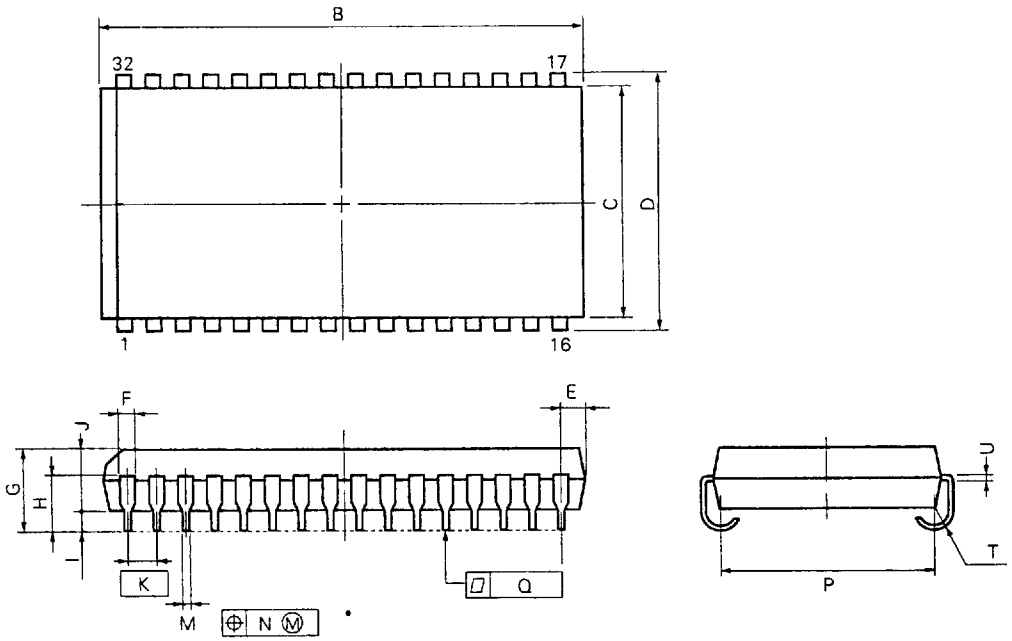
Each lead centerline is located within 0.12 mm (0 005 inch) of its true position (T.P.) at maximum material condition.

P28LE-400A1

ITEM	MILLIMETERS	INCHES
B	$18.67^{+0\ 2}_{-0\ 35}$	$0.735^{+0\ 008}_{-0\ 013}$
C	10.16	0.400
D	11.18±0.2	$0.440^{+0\ 008}_{-0\ 007}$
E	1.08±0.15	$0.043^{+0\ 006}_{-0\ 007}$
F	0.74	0.029
G	3.5±0.2	$0.138^{+0\ 008}_{-0\ 007}$
H	2.545±0.2	0.100±0.008
I	0.8 MIN	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P)	0 050 (T.P.)
M	0 40±0.10	$0.016^{+0\ 004}_{-0\ 005}$
N	0.12	0.005
P	9 40±0.20	$0.370^{+0\ 008}_{-0\ 007}$
Q	0.10	0.004
T	R 0 85	R 0.033
U	$0\ 20^{+0\ 10}_{-0\ 05}$	$0\ 008^{+0\ 004}_{-0\ 002}$

32 PIN PLASTIC SOJ (400mil)

NEC Cord:P32LE-400A



NOTE

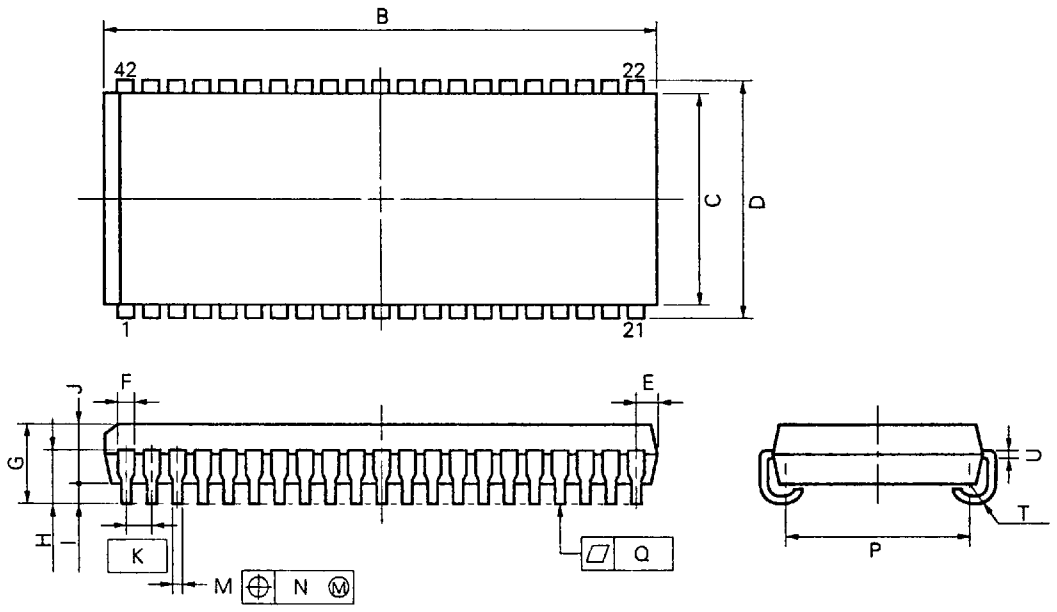
Each lead centerline is located within 0 12 mm (0 005 inch) of its true position (T P) at maximum material condition

P32LE-400A

ITEM	MILLIMETERS	INCHES
B	21.06±0 2	0 829±0 008
C	10 16	0 400
D	11 18±0 2	0.440±0 008
E	1 005±0.1	$0\ 040^{+0\ 004}_{-0\ 005}$
F	0.74	0 029
G	3.5±0.2	0 138±0 008
H	2 545±0 2	0 100±0.008
I	0 8 MIN	0 031 MIN
J	2 6	0.102
K	1 27 (T.P.)	0 050 (T P.)
M	0 40±0 10	$0\ 016^{+0\ 004}_{-0\ 005}$
N	0.12	0 005
P	9 4±0 20	0 370±0 008
Q	0.1	0.004
T	R 0 85	R 0.033
U	$0.20^{+0\ 10}_{-0\ 05}$	$0\ 008^{+0\ 004}_{-0\ 002}$

42 PIN PLASTIC SOJ (400mil)

NEC Cord:P42LE-400A



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

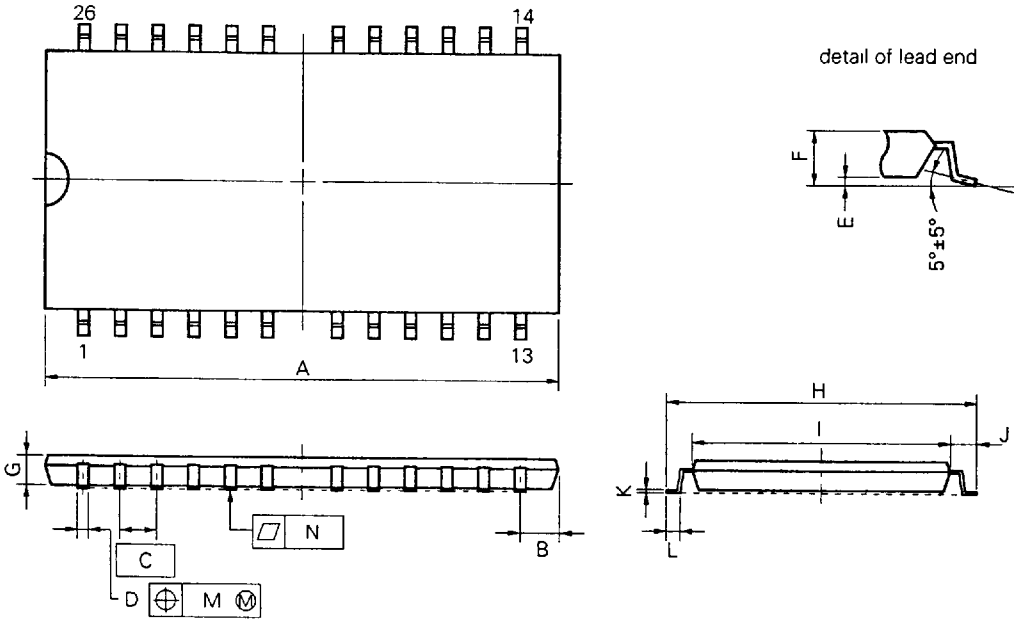
P42LE-400A

ITEM	MILLIMETERS	INCHES
B	$27.56^{+0.2}_{-0.35}$	$1.085^{+0.008}_{-0.014}$
C	10.16	0.400
D	11.18±0.2	0.440±0.008
E	1.08±0.15	$0.043^{+0.006}_{-0.007}$
F	0.74	0.029
G	3.5±0.2	0.138±0.008
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	9.4±0.20	0.370±0.008
Q	0.10	0.004
T	R 0.85	R 0 033
U	$0\ 20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

26 PIN PLASTIC TSOP (300mil) *
24 Leads

* : under development

NEC Cord:S26G3-50-7JD



NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

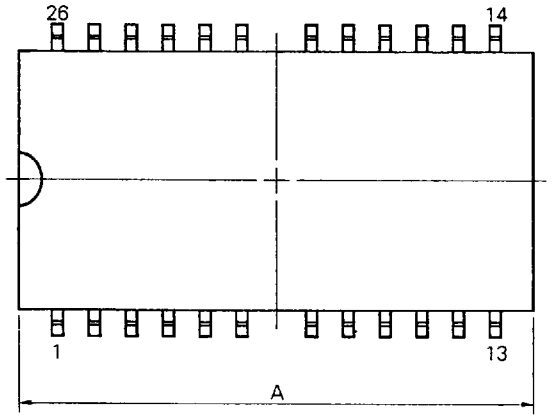
S26G3-50-7JD

ITEM	MILLIMETERS	INCHES
A	17.40 MAX.	0.685 MAX.
B	1.06 MAX.	0.042 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40 ± 0.10	$0.016^{+0.004}_{-0.005}$
E	0.05 ± 0.05	0.002 ± 0.002
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	9.22 ± 0.2	0.363 ± 0.008
I	7.62 ± 0.1	0.300 ± 0.004
J	0.8 ± 0.2	$0.031^{+0.009}_{-0.008}$
K	$0.125^{+0.10}_{-0.05}$	$0.005^{+0.004}_{-0.002}$
L	0.5 ± 0.1	$0.020^{+0.004}_{-0.005}$
M	0.21	0.009
N	0.10	0.004

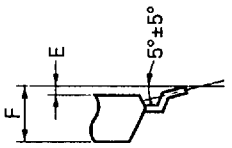
26 PIN PLASTIC TSOP (300mil) *
24 Leads Reverse bent

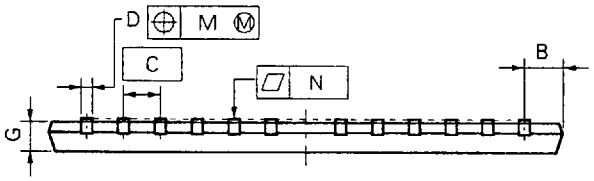
* : under development

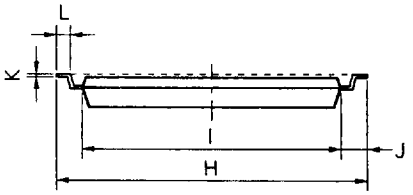
NEC Cord:S26G3-50-7KD



detail of lead end







NOTE

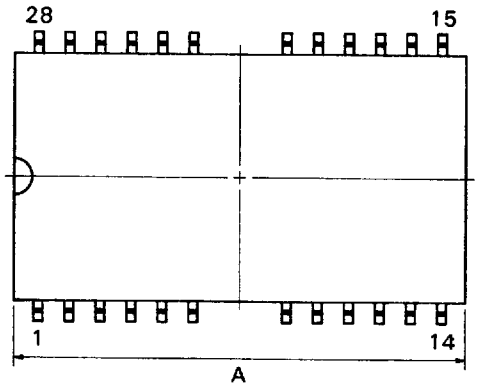
Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition

S26G3-50-7KD

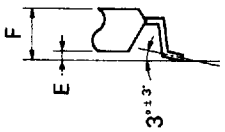
ITEM	MILLIMETERS	INCHES
A	17.40 MAX.	0.685 MAX.
B	1.06 MAX.	0.042 MAX.
C	1.27 (T P)	0.050 (T.P.)
D	0 40±0.10	$0.016^{+0.004}_{-0.005}$
E	0.05±0.05	0.002±0.002
F	1.1 MAX.	0 044 MAX.
G	0 97	0.038
H	9.22±0.2	0.363±0.008
I	7.62±0.1	0.300±0.004
J	0.8±0 2	$0.031^{+0.009}_{-0.008}$
K	$0.125^{+0.10}_{-0.05}$	$0.005^{+0.004}_{-0.002}$
L	0 5±0.1	$0.020^{+0.004}_{-0.005}$
M	0.21	0.009
N	0 10	0 004

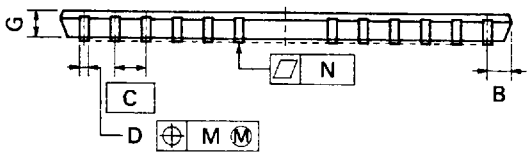
28 PIN PLASTIC TSOP (400mil)
24 Leads

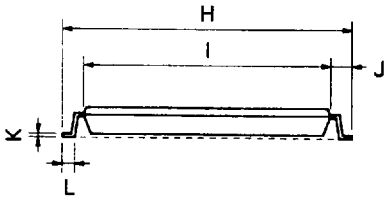
NEC Cord:S28G5-50-7JD1



detail of lead end







S28G5-50-7JD1

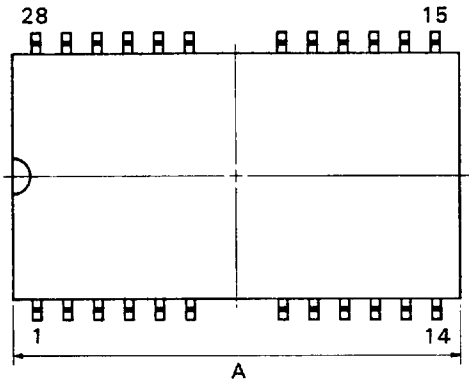
ITEM	MILLIMETERS	INCHES
A	18.81 MAX.	0 741 MAX.
B	1.15 MAX	0.046 MAX.
C	1 27 (T.P.)	0 050 (T.P)
D	$0\ 40^{\pm 0\ 10}$	$0.016^{+0\ 004}_{-0\ 005}$
E	$0.05^{\pm 0\ 05}$	$0.002^{\pm 0\ 002}$
F	1.1 MAX.	0 044 MAX.
G	0.97	0 038
H	$11\ 76^{\pm 0\ 2}$	$0.463^{\pm 0\ 008}$
I	$10\ 16^{\pm 0\ 1}$	$0.400^{\pm 0\ 004}$
J	$0.8^{\pm 0\ 2}$	$0.031^{+0\ 009}_{-0\ 008}$
K	$0\ 125^{-0\ 10}_{-0\ 05}$	$0.005^{+0\ 004}_{-0\ 002}$
L	$0\ 5^{\pm 0\ 1}$	$0\ 020^{+0\ 004}_{-0\ 005}$
M	0 21	0 009
N	0.10	0.004

NOTE

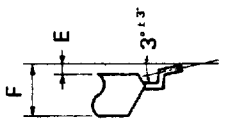
Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

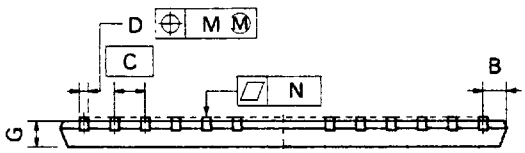
28 PIN PLASTIC TSOP (400mil)
24 Leads Reverse bent

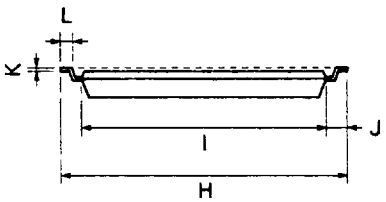
NEC Cord:S28G5-50-7KD1



detail of lead end







S28G5-50-7KD1

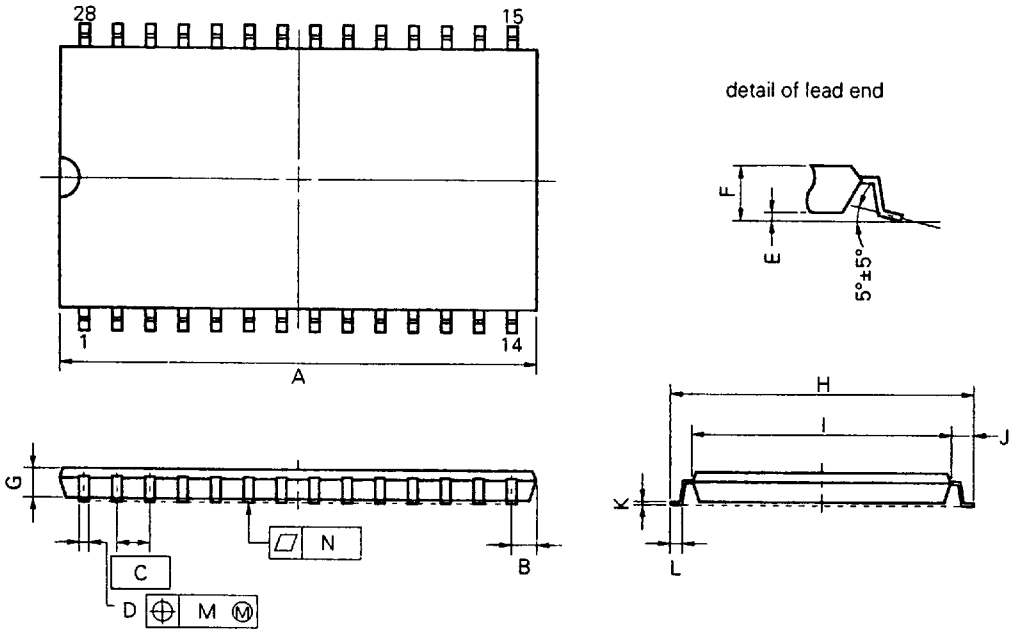
NOTE
Each lead centerline is located within 0 21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	18.81 MAX.	0.741 MAX.
B	1.15 MAX.	0.046 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{\pm 0\ 10}$	$0.016^{-0\ 004}_{-0\ 005}$
E	$0\ 05^{\pm 0\ 05}$	$0.002^{\pm 0\ 002}$
F	1 1 MAX.	0 044 MAX.
G	0 97	0.038
H	$11\ 76^{\pm 0\ 2}$	$0.463^{\pm 0\ 008}$
I	$10.16^{\pm 0\ 1}$	$0.400^{\pm 0\ 004}$
J	$0.8^{\pm 0\ 2}$	$0.031^{-0\ 009}_{-0\ 008}$
K	$0.125^{+0\ 10}_{-0\ 05}$	$0.005^{-0\ 004}_{-0\ 002}$
L	$0\ 5^{\pm 0\ 1}$	$0.020^{-0\ 004}_{-0\ 005}$
M	0.21	0.009
N	0.10	0.004

28 PIN PLASTIC TSOP (400mil)

28 Leads

NEC Cord:S28G5-50-7JD2



NOTE

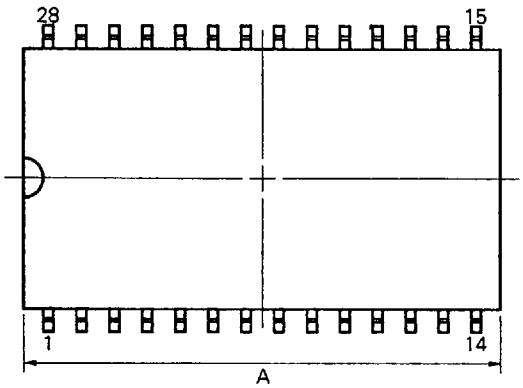
Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

S28G5-50-7JD2

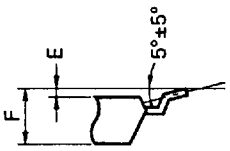
ITEM	MILLIMETERS	INCHES
A	18.81 MAX.	0.741 MAX.
B	1.15 MAX.	0.046 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40±0.10	$0.016^{+0.004}_{-0.005}$
E	0 05±0.05	0.002±0.002
F	1.1 MAX.	0 044 MAX.
G	0.97	0.038
H	11.76±0.2	0 463±0.008
I	10 16±0.1	0 400±0 004
J	0.8±0 2	$0.031^{+0.009}_{-0.008}$
K	$0.125^{+0.10}_{-0.05}$	$0\ 005^{+0.004}_{-0.002}$
L	0.5±0 15	$0.020^{+0.006}_{-0.007}$
M	0.21	0.009
N	0.10	0.004

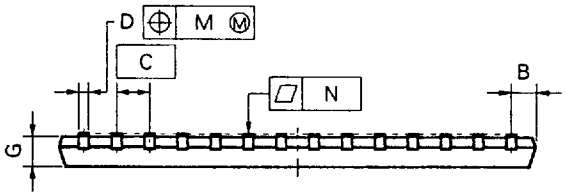
28 PIN PLASTIC TSOP (400mil)
28 Leads Reverse bent

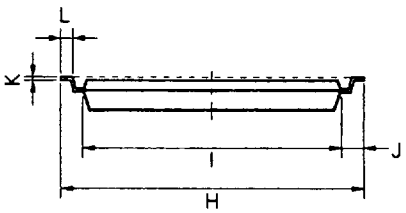
NEC Cord:S28G5-50-7KD2



detail of lead end







S28G5-50-7KD2

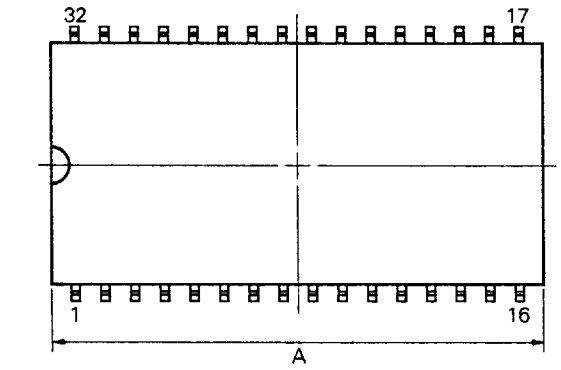
ITEM	MILLIMETERS	INCHES
A	18.81 MAX.	0.741 MAX.
B	1.15 MAX.	0.046 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0 40±0.10	$0.016^{+0\ 004}_{-0\ 005}$
E	0 05±0.05	0.002±0 002
F	1 1 MAX.	0.044 MAX.
G	0.97	0.038
H	11 76±0 2	0.463±0.008
I	10.16±0.1	0.400±0 004
J	0 8±0 2	$0\ 031^{+0\ 009}_{-0\ 008}$
K	$0.125^{+0\ 10}_{-0\ 05}$	$0.005^{+0\ 004}_{-0\ 002}$
L	0 5±0 15	$0\ 020^{+0\ 006}_{-0\ 007}$
M	0.21	0 009
N	0 10	0.004

NOTE

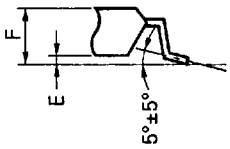
Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

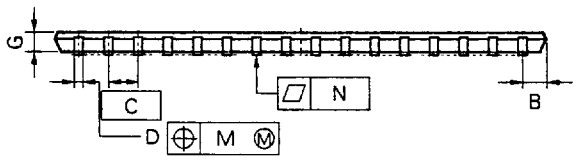
32 PIN PLASTIC TSOP (400mil)

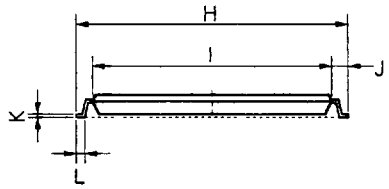
NEC Cord:S32G5-50-7JD1



detail of lead end







NOTE

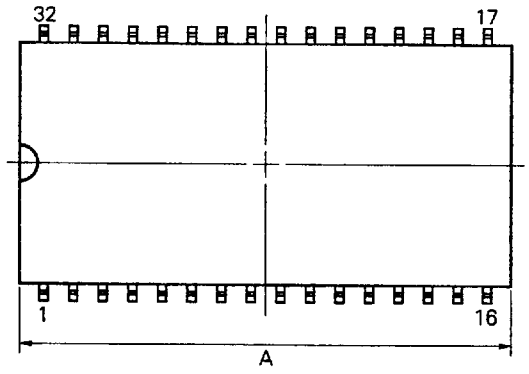
Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

S32G5-50-7JD1

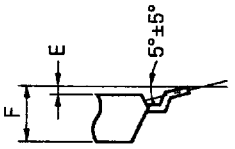
ITEM	MILLIMETERS	INCHES
A	21.17 MAX.	0.834 MAX.
B	1.06 MAX.	0.042 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40 ± 0.10	$0.016^{+0.004}_{-0.005}$
E	0.05 ± 0.05	0.002 ± 0.002
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	11.76 ± 0.2	0.463 ± 0.008
I	10.16 ± 0.1	0.400 ± 0.004
J	0.8 ± 0.2	$0.031^{+0.009}_{-0.008}$
K	$0.125^{+0.10}_{-0.05}$	$0.005^{+0.004}_{-0.002}$
L	0.5 ± 0.15	$0.020^{+0.006}_{-0.007}$
M	0.21	0.009
N	0.10	0.004

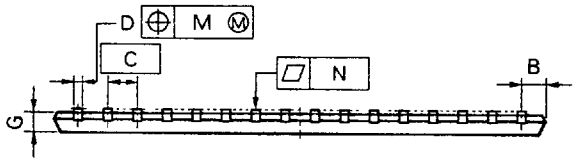
32 PIN PLASTIC TSOP (400mil)
Reverse bent

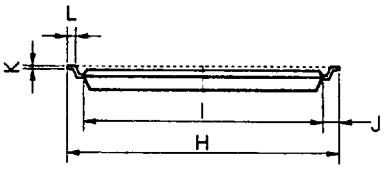
NEC Cord:S32G5-50-7KD1



detail of lead end







NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

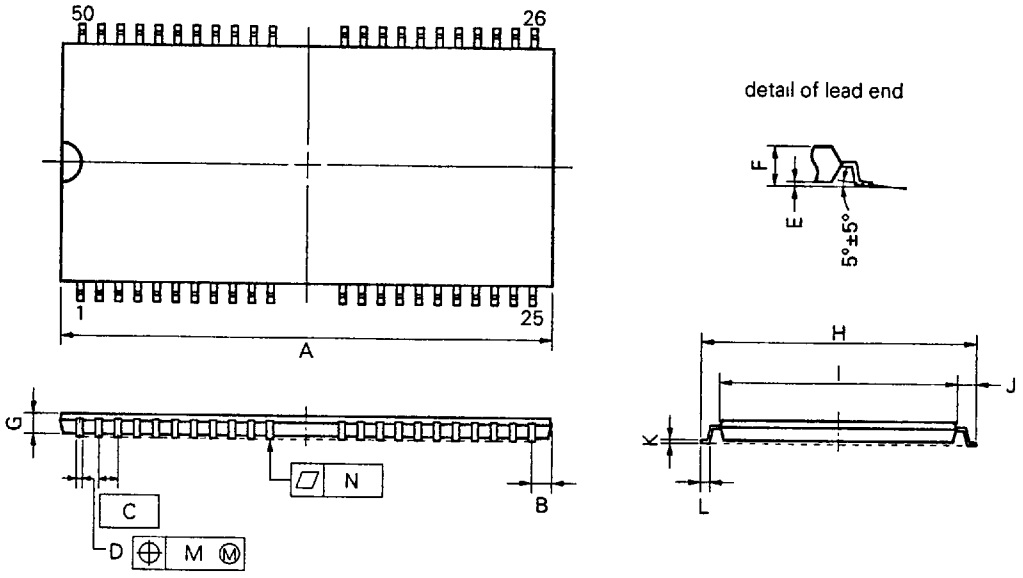
S32G5-50-7KD1

ITEM	MILLIMETERS	INCHES
A	21.17 MAX.	0.834 MAX.
B	1.06 MAX.	0.042 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40 ± 0.10	$0.016^{+0.004}_{-0.005}$
E	0.05 ± 0.05	0.002 ± 0.002
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	11.76 ± 0.2	0.463 ± 0.008
I	10.16 ± 0.1	0.400 ± 0.004
J	0.8 ± 0.2	$0.031^{+0.009}_{-0.008}$
K	$0.125^{+0.10}_{-0.05}$	$0.005^{+0.004}_{-0.002}$
L	0.5 ± 0.15	$0.020^{+0.006}_{-0.007}$
M	0.21	0.009
N	0.10	0.004

50 PIN PLASTIC TSOP (400mil)

44 Leads

NEC Cord:S50G5-80-7JF



NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

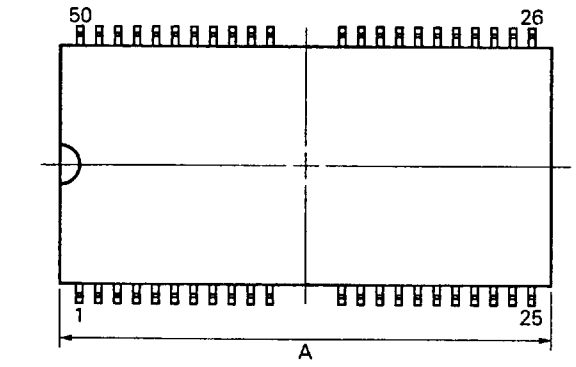
S50G5-80-7JF

ITEM	MILLIMETERS	INCHES
A	21.45 MAX.	0.845 MAX.
B	1.13 MAX.	0.045 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	0.30±0.10	$0.012^{+0.004}_{-0.005}$
E	0.05±0 05	0.002±0.002
F	1.1 MAX.	0.044 MAX.
G	0 97	0.038
H	11.76±0 2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	$0.125^{+0.10}_{-0.05}$	$0.005^{+0.004}_{-0.002}$
L	0.5±0.15	$0.020^{+0.006}_{-0.007}$
M	0.13	0.005
N	0.10	0.004

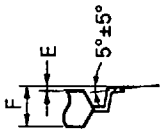
50 PIN PLASTIC TSOP (400mil)

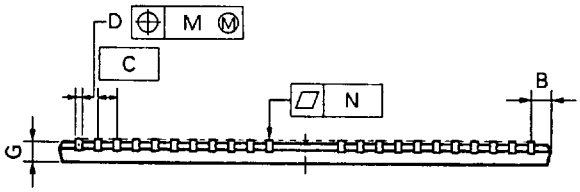
44 Leads Reverse bent

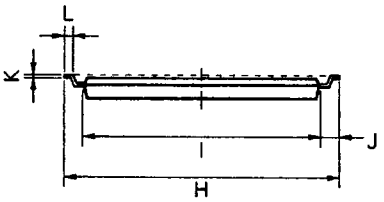
NEC Cord:S50G5-80-7KF



detail of lead end







NOTE

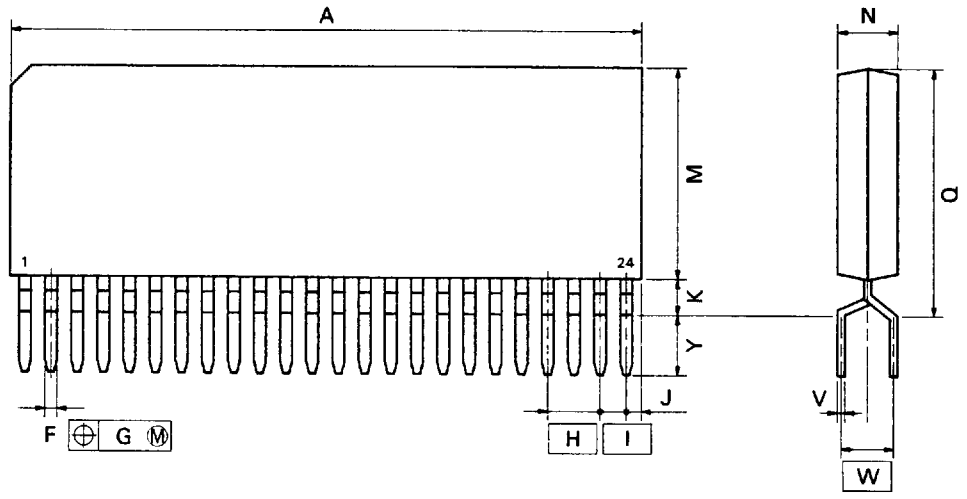
Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

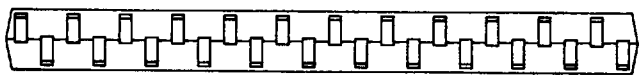
S50G5-80-7KF

ITEM	MILLIMETERS	INCHES
A	21.45 MAX.	0.845 MAX.
B	1.13 MAX.	0.045 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	0.30 ± 0.10	$0.012^{+0.004}_{-0.005}$
E	0.05 ± 0.05	0.002 ± 0.002
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	11.76 ± 0.2	0.463 ± 0.008
I	10.16 ± 0.1	0.400 ± 0.004
J	0.8 ± 0.2	$0.031^{+0.009}_{-0.008}$
K	$0.125^{+0.10}_{-0.05}$	$0.005^{+0.004}_{-0.002}$
L	0.5 ± 0.15	$0.020^{+0.006}_{-0.007}$
M	0.13	0.005
N	0.10	0.004

24 PIN PLASTIC ZIP (475mil)

NEC Cord:P24V-100-475A





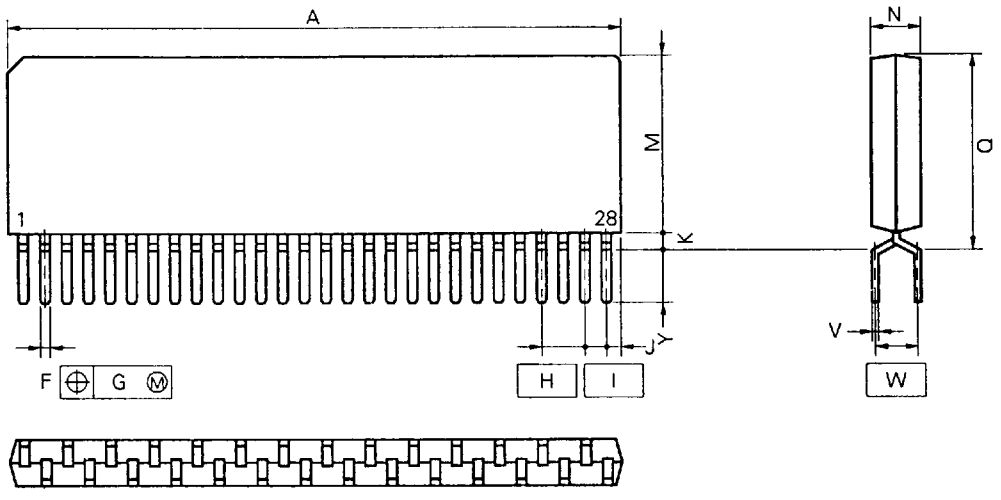
NOTE
Each lead centerline is located within 0.25 mm (0.010 inch) of its true position (T.P.) at maximum material condition.

P24V-100-475A

ITEM	MILLIMETERS	INCHES
A	31.75 MAX.	1.250 MAX.
F	$0.50^{\pm 0.1}$	$0.020^{+0.004}_{-0.005}$
G	ϕ0 25	ϕ0.010
H	2.54	0.100
I	1.27	0.050
J	1.27 MAX.	0.050 MAX.
K	1 0 MIN	0.039 MIN.
M	10 8 MAX	0 426 MAX
N	$2\ 8^{\pm 0.2}$	$0.110^{+0.009}_{-0.008}$
Q	12.07 MAX.	0.476 MAX
V	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
W	2.54	0.100
Y	$3.3^{+0.5}$	$0.130^{\pm 0.02}$

28 PIN PLASTIC ZIP (475mil)

NEC Cord:P28VF-100-475A



NOTE

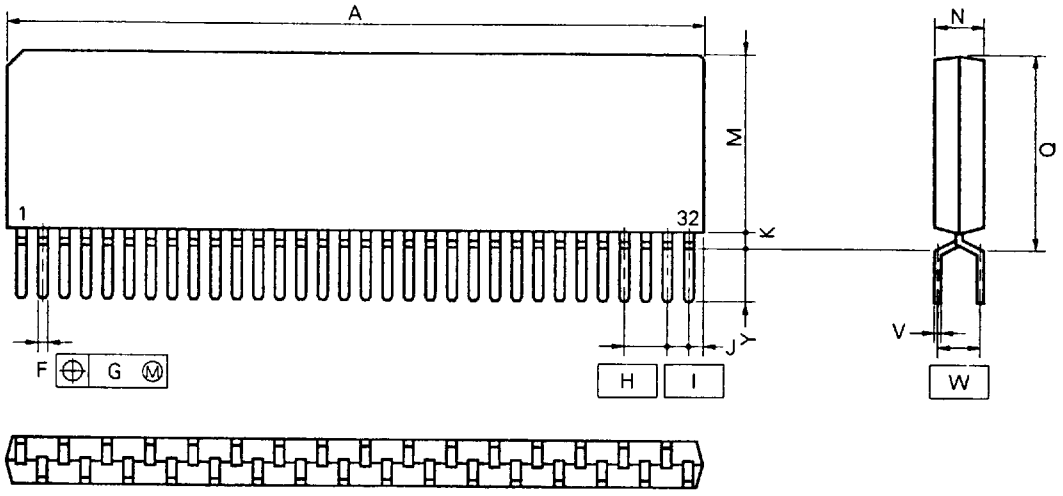
Each lead centerline is located within 0 25 mm (0.010 inch) of its true position (T.P) at maximum material condition.

P28VF-100-475A

ITEM	MILLIMETERS	INCHES
A	36.83 MAX.	1 450 MAX.
F	0 5±0 10	$0.020^{+0\ 004}_{-0\ 005}$
G	0.25	0.010
H	2 54 (T.P.)	0.100 (T P)
I	1 27 (T P.)	0.050 (T P.)
J	1 27 MAX.	0 050 MAX
K	0 9 MIN	0.035 MIN.
M	10 8 MAX.	0 426 MAX
N	2 8±0 2	$0.110^{+0\ 009}_{-0\ 008}$
Q	12 07 MAX	0 475 MAX.
V	$0\ 25^{+0\ 10}_{-0\ 05}$	$0.010^{+0\ 004}_{-0\ 003}$
W	2 54 (T.P.)	0.100 (T.P)
Y	3 25±0.2	0.128±0 008

32 PIN PLASTIC ZIP (475mil)

NEC Cord:P32VF-100-475A



NOTE

Each lead centerline is located within 0.25 mm (0.010 inch) of its true position (T.P.) at maximum material condition.

P32VF-100-475A

ITEM	MILLIMETERS	INCHES
A	41.91 MAX.	1.650 MAX
F	0.5±0.10	$0.020^{+0.004}_{-0.005}$
G	0.25	0.010
H	2.54 (T.P.)	0.100 (T.P.)
I	1 27 (T.P)	0.050 (T.P.)
J	1.27 MAX.	0.050 MAX.
K	0 9 MIN.	0.035 MIN.
M	10.8 MAX.	0.426 MAX.
N	2 8±0.2	$0.110^{+0.009}_{-0.008}$
Q	12.07 MAX.	0.475 MAX.
V	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
W	2.54 (T.P.)	0 100 (T P.)
Y	3.25±0.2	0.128±0.008