

Description

The μPD431018 is a 65,536-word by 18-bit static RAM fabricated with advanced silicon-gate technology, unique CMOS peripheral circuits, and N-channel memory cells. It is suitable for cache memory and buffer memory applications where high speed, high density, and wide I/O SRAMs are required.

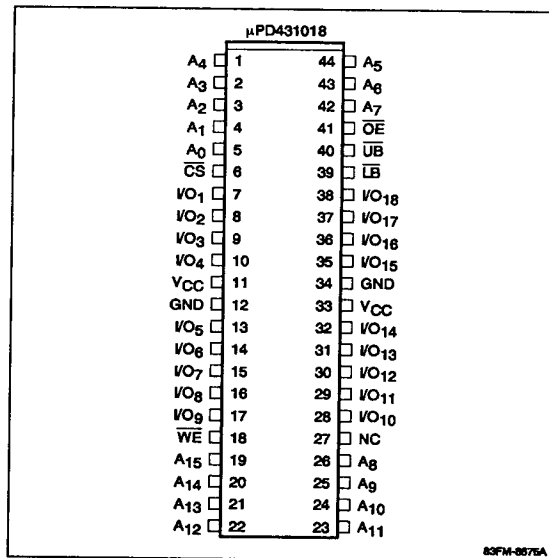
The μPD431018 operates with low power from a single +5-volt supply. No clock or refreshing is required. The plastic package is a standard 44-pin SOJ or TSOP.

Features

- 65,536-word x 18-bit organization
- Single +5-volt power supply
- Fully static operation—no clock or refreshing
- TTL-compatible inputs and outputs
- Common I/O capability
- Output buffer control: $\overline{OE}$
- Data byte control: $\overline{LB}$, $\overline{UB}$
- Low power dissipation
 - 260 mA max (active)
 - 10 mA max (standby)
- Standard 44-pin, 400-mil SOJ or TSOP plastic package

Pin Configurations

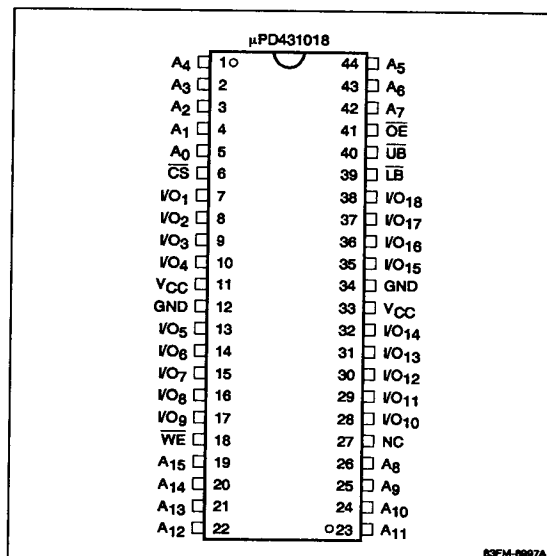
44-Pin Plastic SOJ



Ordering Information

Part Number	Access Time (max)	Package
μPD431018LE-15	15 ns	44-pin plastic SOJ
LE-17	17 ns	
LE-20	20 ns	
μPD431018G5-15	15 ns	44-pin plastic TSOP
G5-17	17 ns	
G5-20	20 ns	

44-Pin Plastic TSOP



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Pin Identification

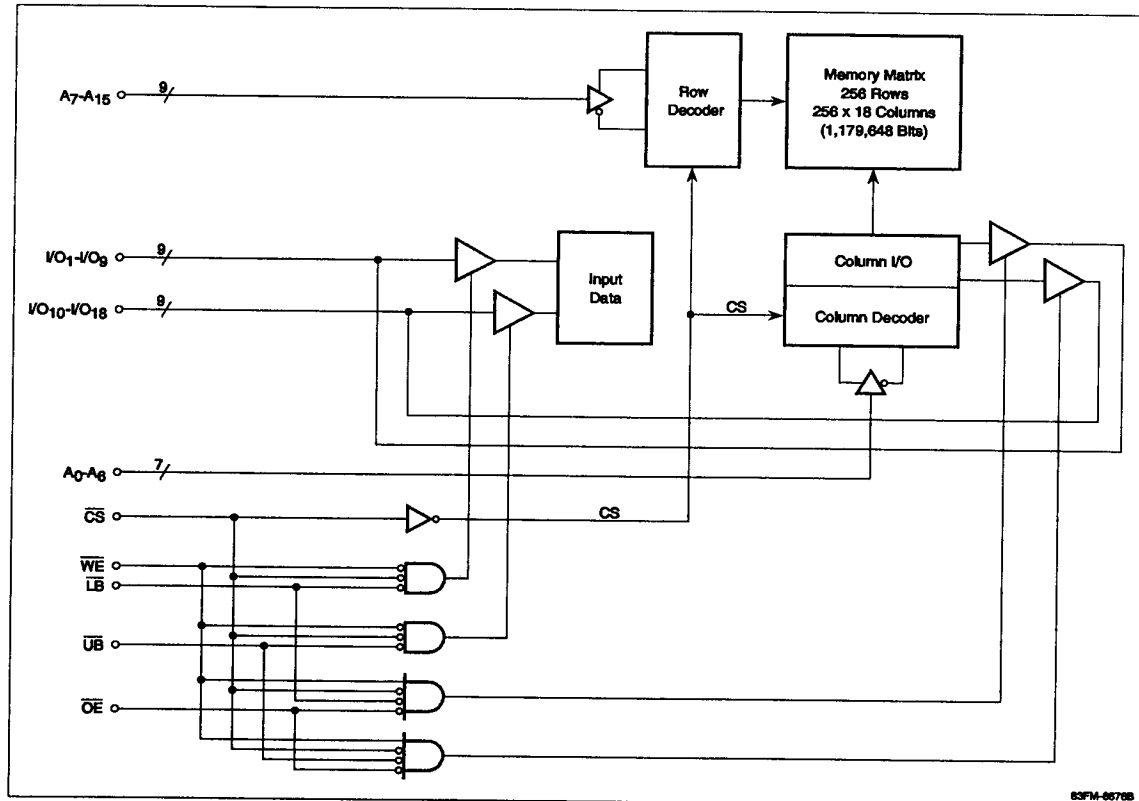
Symbol	Function
A ₀ - A ₁₅	Address inputs
I/O ₁ - I/O ₁₈	Data inputs and outputs
$\overline{CS}$	Chip select
$\overline{LB}$	Lower byte select (I/O ₁ - I/O ₉)
$\overline{OE}$	Output enable
$\overline{UB}$	Upper byte select (I/O ₁₀ - I/O ₁₈)
$\overline{WE}$	Write enable
GND	Ground
V _{CC}	+5-volt power supply
NC	No connection

Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	Mode	I/O ₁ - I/O ₉	I/O ₁₀ - I/O ₁₈	Power
H	X	X	X	X	Not selected	Hi-Z	Hi-Z	Standby
L	L	H	L	L	Read	D _{OUT}	D _{OUT}	Active
			L	H	Read	D _{OUT}	Hi-Z	
			H	L	Read	Hi-Z	D _{OUT}	
L	X	L	L	L	Write	D _{IN}	D _{IN}	
			L	H	Write	D _{IN}	Hi-Z	
			H	L	Write	Hi-Z	D _{IN}	
L	H	H	X	X	—	Hi-Z	Hi-Z	
L	X	X	H	H	—	Hi-Z	Hi-Z	

X = Don't care.

Block Diagram



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Absolute Maximum Ratings

Supply voltage, V_{CC}	- 0.5 to +7.0 V
Input and output voltages, V_{IO} (Note 1)	- 0.5 to V_{CC} + 0.5 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	- 55 to +125°C
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Note:

(1) V_{IN} (min) = -3.0 V for 10-ns pulse.

Capacitance

$T_A = 25^\circ\text{C}$; V_{IN} and $V_{DOUT} = 0\text{ V}$; $f = 1\text{ MHz}$

Parameter	Symbol	Min	Max	Unit
Input capacitance	C_{IN}		6	pF
Output capacitance	C_{DOUT}		8	pF

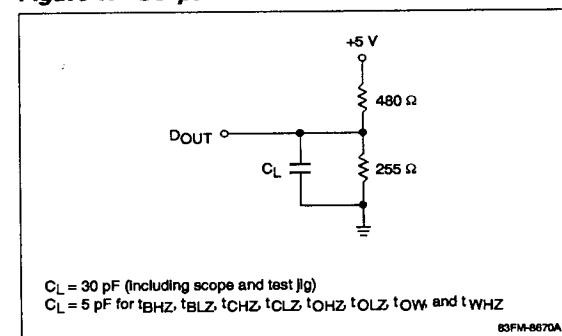
Capacitance is sampled and not 100% tested.

DC Characteristics

$T_A = 0\text{ to }+70^\circ\text{C}$; $V_{CC} = +5.0\text{ V} \pm 10\%$

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	-2		2	μA	$V_{IN} = 0\text{ V to }V_{CC}$
Output leakage current	I_{LO}	-2		2	μA	$V_{OUT} = 0\text{ V to }V_{CC}$; $\overline{CS}$, $\overline{OE}$, $\overline{LB}$, or $UB = V_{IH}$ or $WE = V_{IL}$
Standby supply current	I_{SB}			30	mA	$\overline{CS} = V_{IH}$
	I_{SB1}			10	mA	$\overline{CS} \geq V_{CC} - 0.2\text{ V}$; $V_{IN} \leq 0.2\text{ V}$ or $\geq V_{CC} - 0.2\text{ V}$
Output voltage, low	V_{OL}			0.4	V	$I_{OL} = 8.0\text{ mA}$
Output voltage, high	V_{OH}	2.4			V	$I_{OH} = -4.0\text{ mA}$

Figure 1. Output Loads



AC Characteristics

$T_A = 0 \text{ to } +70^\circ\text{C}$; $V_{CC} = +5.0 \text{ V} \pm 10\%$

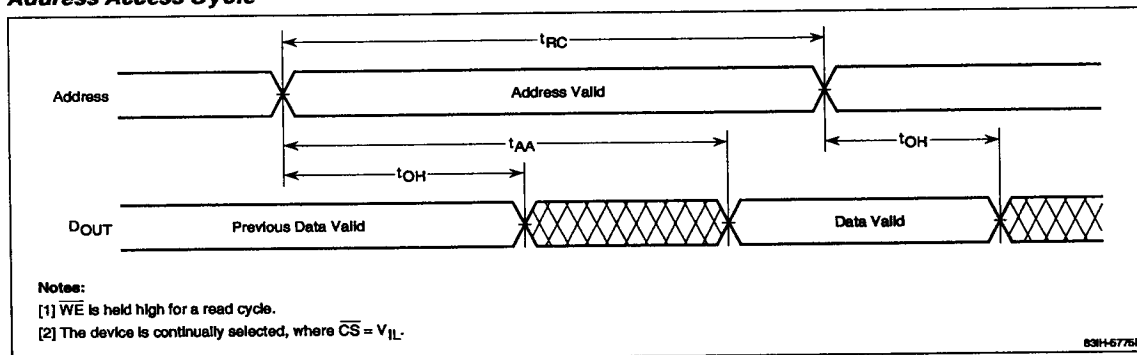
Parameter	Symbol	μPD431018-15		μPD431018-17		μPD431018-20		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
Read Operation									
Operating supply current	I _{CC}		260		220		200	mA	$\overline{CS} = V_{IL}; I_{DOUT} = 0 \text{ mA}$ (Note 5)
Address access time	t _{AA}		15		17		20	ns	
Chip select access time	t _{ACS}		15		17		20	ns	
Data byte select access time	t _{ADB}		8		9		10	ns	
Data byte select to output in high-Z	t _{BHZ}		7		7		7	ns	
Data byte select to output in low-Z	t _{BLZ}	1		1		1		ns	
Chip deselection to output in high-Z	t _{CHZ}	0	7	0	7	0	7	ns	(Note 4)
Chip selection to output in low-Z	t _{CLZ}	5		5		5		ns	(Note 3)
Output enable access time	t _{OE}		8		8		10	ns	
Output hold from address change	t _{OH}	5		5		5		ns	
Output enable to output in high-Z	t _{OHZ}		7		7		7	ns	
Output enable to output in low-Z	t _{OLZ}	1		1		1		ns	
Read cycle time	t _{RC}	15		17		20		ns	(Note 2)
Write Operation									
Address setup time	t _{AS}	0		0		0		ns	
Address valid to end of write	t _{AW}	9		11		12		ns	
Data byte select to end of write	t _{BW}	9		11		12		ns	
Chip select to end of write	t _{CW}	10		11		12		ns	
Data hold time	t _{DH}	0		0		0		ns	
Data valid to end of write	t _{DW}	8		9		10		ns	
Output active from end of write	t _{OW}	3		3		3		ns	(Note 3)
Write enable to output in high-Z	t _{WHZ}	0	7	0	7	0	7	ns	(Note 4)
Write cycle time	t _{WC}	15		17		20		ns	(Note 2)
Write pulse width	t _{WP}	9		10		10		ns	
Write recovery time	t _{WR}	0		0		0		ns	

Notes:

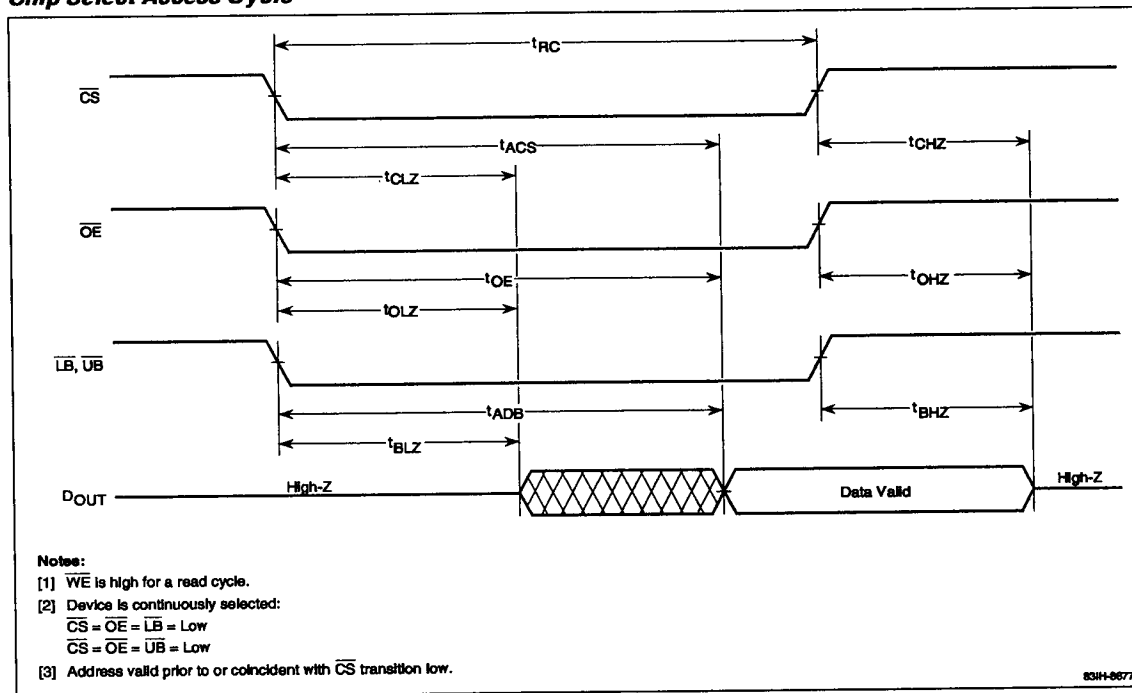
- (1) Input pulse levels = GND to 3.0 V; input pulse rise and fall times = 3 ns; timing reference levels = 1.5 V; see figure 1 for output loads.
- (2) All read cycle timings are referenced from the last valid address to the first transitioning address.
- (3) Transition is measured at $\pm 200 \text{ mV}$ from steady-state voltage with the load shown in figure 1.
- (4) Transition is measured at $V_{OL} + 200 \text{ mV}$ and $V_{OH} - 200 \text{ mV}$ with the load shown in figure 1.
- (5) $I_{CC} = 140 \text{ ma max}$ at $t_{AA} = 50 \text{ ns}$.

Timing Waveforms

Address Access Cycle

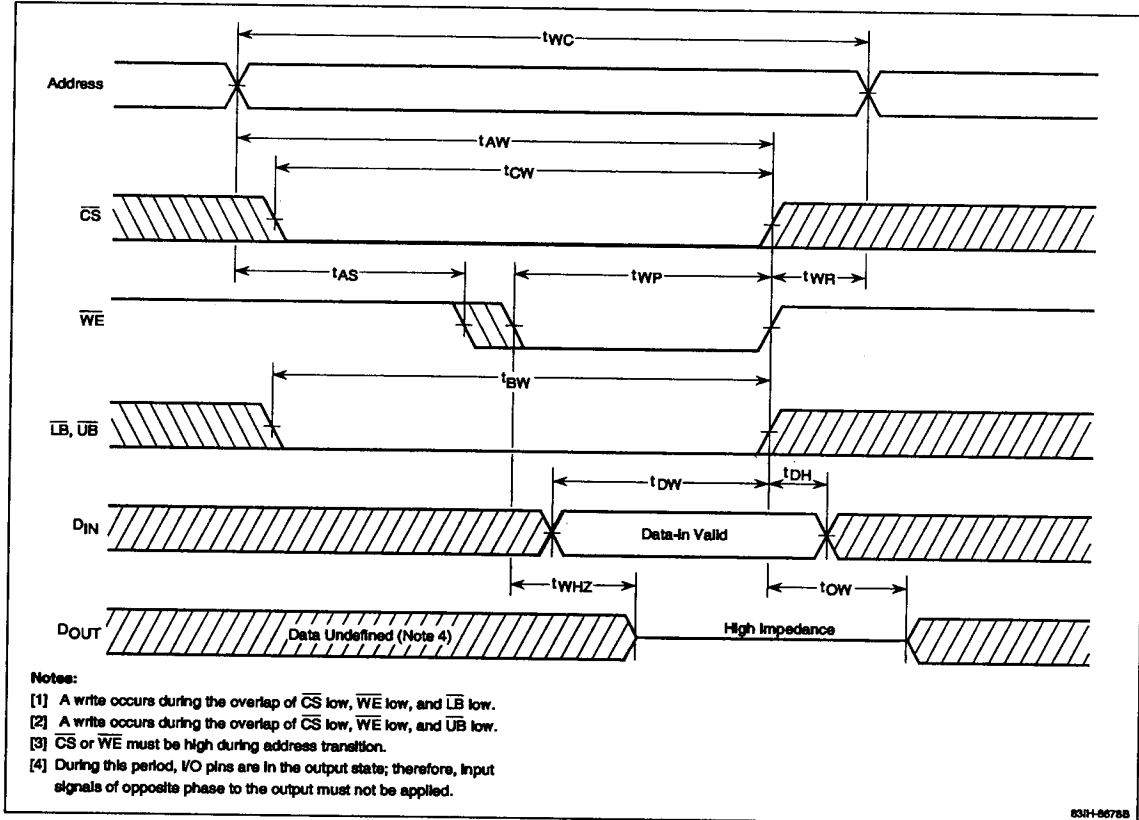


Chip Select Access Cycle

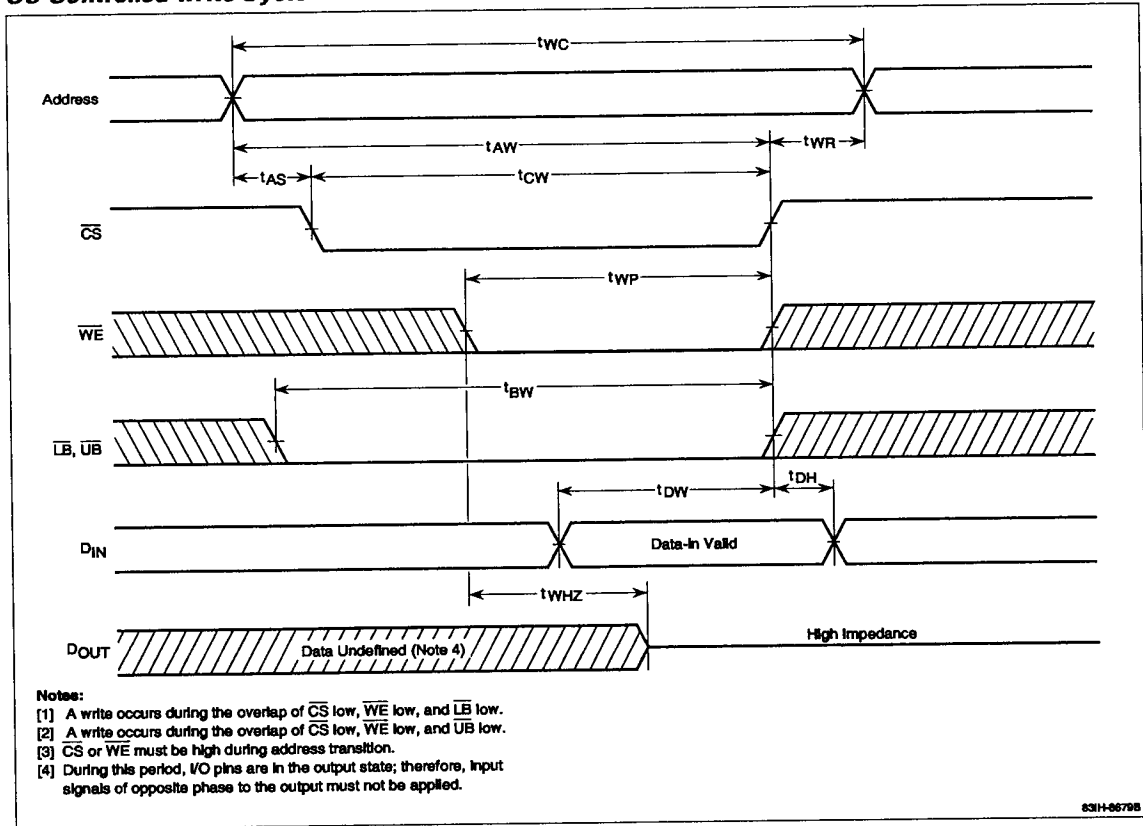


Timing Waveforms (cont)

WE-Controlled Write Cycle



Timing Waveforms (cont)

 $\overline{CS}$ -Controlled Write Cycle

Timing Waveforms (cont)

LB/UB-Controlled Write Cycle

