

**1M-BIT CMOS SYNCHRONOUS FAST SRAM
32K-WORD BY 32-BIT****Description**

The μ PD431232L is 32,768-word by 32-bit synchronous static RAM fabricated with advanced CMOS technology using N-channel memory cells.

The use of this technology and unique peripheral circuits makes these products high-speed devices. This is suitable for applications which require high-speed, low-voltage, high-density memory and wide bit configuration, such as cache and buffer memory.

Products are packaged in 100-pin plastic TQFPs with a 1.4 mm package thickness (LQFP in EIAJ).

Features

- Single 3.3 V power supply
- Synchronous operation
- Burst Read/Write: Interleave burst and Linear burst sequence
- Fully registered inputs and outputs for Pipelined operation
- All registers triggered off positive clock edge
- LVTTTL compatible: All inputs and outputs
- Fast clock access time: 8 ns/66 MHz, 10 ns/60 MHz, 12 ns/50 MHz
- Asynchronous output enable: $\overline{G}$
- Burst mode selectable: MODE
- Separate byte write enable: $\overline{BW1}$ - $\overline{BW4}$, $\overline{BWE}$ and global write enable: $\overline{GW}$
- Three chip enables for easy depth expansion
- Common I/O using three state outputs
- 5 V - tolerant I/O

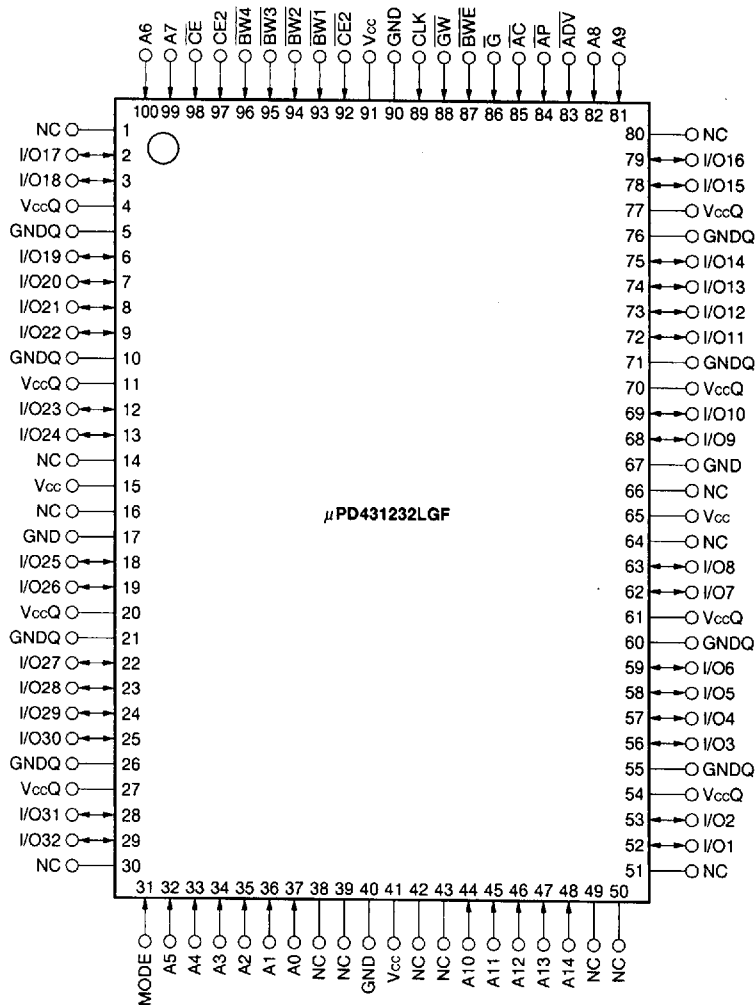
The information in this document is subject to change without notice.

Ordering Information

Part number	Access time ns (MAX.)	Clock frequency MHz	Burst sequence	Operation	Package
μPD431232LGF-A8	8	66	Interleave and linear	Pipelined operation	100-pin plastic TQFP (14 × 20 mm)
μPD431232LGF-A10	10	60			
μPD431232LGF-A12	12	50			

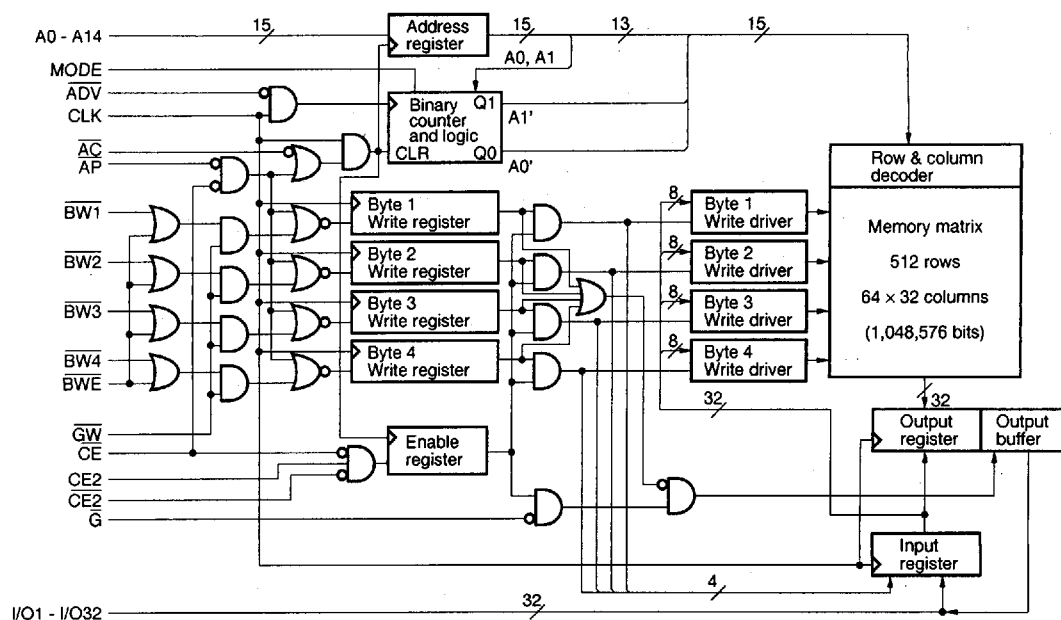
Pin Configuration (Marking Side)

100-pin plastic TQFP (14 × 20 mm)



A0 - A14	: Address inputs	CLK	: System clock input
I/O1 - I/O32	: Data inputs/outputs	MODE	: Mode select
ADV	: Burst address advance	Vcc	: Power supply (3.3 V)
AC	: Controller address status	GND	: Ground
AP	: Processor address status	VccQ	: Power for outputs (3.3 V)
CE, CE2, CE2	: Chip enable	GNDQ	: Ground for outputs
BW1 - BW4, BWE	: Byte write enable	NC	: No connection
GW	: Global write		
G	: Output enable		

Block Diagram



Burst Sequence Table

1. Interleave burst sequence [MODE = Open or V_{CC}]

External Address	A14 - A2, A1, A0
1st Burst Address	A14 - A2, A1, $\overline{A0}$
2nd Burst Address	A14 - A2, $\overline{A1}$, A0
3rd Burst Address	A14 - A2, $\overline{A1}$, $\overline{A0}$

Remark The burst sequence wraps around to its initial state upon completion.

2. Linear burst sequence [MODE = GND]

External Address	A14 - A2, 0, 0	A14 - A2, 0, 1	A14 - A2, 1, 0	A14 - A2, 1, 1
1st Burst Address	A14 - A2, 0, 1	A14 - A2, 1, 0	A14 - A2, 1, 1	A14 - A2, 0, 0
2nd Burst Address	A14 - A2, 1, 0	A14 - A2, 1, 1	A14 - A2, 0, 0	A14 - A2, 0, 1
3rd Burst Address	A14 - A2, 1, 1	A14 - A2, 0, 0	A14 - A2, 0, 1	A14 - A2, 1, 0

Remark The burst sequence wraps around to its initial state upon completion.

Asynchronous Truth Table

Operation	$\overline{G}$	I/O
Read Cycle	L	D _{OUT}
	H	Hi-Z
Write Cycle	x	Hi-Z - D _{IN}
Deselected	x	Hi-Z

Remark x means "Don't care".

Synchronous Truth Table

Operation	$\overline{CE}$	$\overline{CE2}$	$CE2$	$\overline{AP}$	$\overline{AC}$	$\overline{ADV}$	$\overline{WRITE}$	CLK	Address
Deselected	H	x	x	x	L	x	x	L-H	N/A
Deselected	L	x	L	L	x	x	x	L-H	N/A
Deselected	L	H	x	L	x	x	x	L-H	N/A
Deselected	L	x	L	H	L	x	x	L-H	N/A
Deselected	L	H	x	H	L	x	x	L-H	N/A
Read cycle/Begin burst	L	L	H	L	x	x	x	L-H	External
Read cycle/Begin burst	L	L	H	H	L	x	H	L-H	External
Read cycle/Continue burst	x	x	x	H	H	L	H	L-H	Next
Read cycle/Continue burst	H	x	x	x	H	L	H	L-H	Next
Read cycle/Suspend burst	x	x	x	H	H	H	H	L-H	Current
Read cycle/Suspend burst	H	x	x	x	H	H	H	L-H	Current
Write cycle/Begin burst	L	L	H	H	L	x	L	L-H	External
Write cycle/Continue burst	x	x	x	H	H	L	L	L-H	Next
Write cycle/Continue burst	H	x	x	x	H	L	L	L-H	Next
Write cycle/Suspend burst	x	x	x	H	H	H	L	L-H	Current
Write cycle/Suspend burst	H	x	x	x	H	H	L	L-H	Current

Remark x means "Don't care".

$\overline{WRITE} = L$ means any one or more byte write enables ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, or $\overline{BW4}$) and $\overline{BWE}$ are low or $\overline{GW}$ is low.

$\overline{WRITE} = H$ means all byte write enables are high.

Partial Truth Table for Write Enables

Operation	$\overline{GW}$	$\overline{BWE}$	$\overline{BW1}$	$\overline{BW2}$	$\overline{BW3}$	$\overline{BW4}$
Read cycle	H	H	x	x	x	x
	H	L	H	H	H	H
Write cycle/Byte1 only	H	L	L	H	H	H
Write cycle/All bytes	H	L	L	L	L	L
	L	x	x	x	x	x

Note x means "Don't care".

Pass-through Truth Table

Previous Cycle		Present Cycle				Next Cycle
Operation	$\overline{BWs}$	Operation	$\overline{CE}$	$\overline{BWs}$	$\overline{G}$	Operation
Write cycle, all bytes Address = A(n-1), Data = D(n-1)	All L	Initiate read cycle register A (n), Q = D(n-1)	L	All H	L	Read D(n)
Write cycle, all bytes Address = A(n-1), Data = D(n-1)	All L	No new cycle Q = D(n-1)	H	All H	L	No carryover from previous cycle
Write cycle, all bytes Address = A(n-1), Data = D(n-1)	All L	No new cycle Q = Hi-Z	H	All H	H	No carryover from previous cycle
Write cycle, one byte Address = A(n-1), Data = D(n-1)	One L	No new cycle Q = D(n-1) for one byte	H	All H	L	No carryover from previous cycle

Electrical Characteristics

- The device is tested under the minimum transverse air flow of 2.5 meters per second for the DC and AC specifications shown in the tables.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V _{CC}	-0.5 ^{Note} to +4.6	V
Input voltage	V _{IN}	-0.5 ^{Note} to +6.0	V
Input/Output voltage	V _{IO}	-0.5 ^{Note} to +6.0	V
Operating ambient temperature	T _A	0 to +70	°C
Storage temperature	T _{stg}	-55 to +125	°C

Note -2.0 V (MIN.) (Pulse width: 2 ns)

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V _{CC} , V _{CCQ}	3.1	3.3	3.6	V
High level input voltage	V _{IH}	2.0		5.5	V
Low level input voltage	V _{IL}	-0.5 ^{Note}		+0.8	V
Operating ambient temperature	T _A	0		+70	°C

Note -2.5 V (MIN.) (Pulse width: 3 ns)

Capacitance (T_A = +25 °C, f = 1 MHz)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C _{IN}	V _{IN} = 0 V			4	pF
Input/Output capacitance	C _{IO}	V _{IO} = 0 V			7	pF

Remarks 1. V_{IN}: Input voltage

2. These parameters are periodically sampled and not 100 % tested.

DC Characteristics (Recommended operating conditions unless otherwise noted)

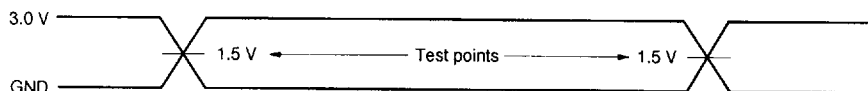
Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Input leakage current	I_{LI}	$V_{IN} = 0 \text{ V to } V_{CC}$	-2		+2	μA
Output leakage current	I_{LO}	$V_{IO} = 0 \text{ V to } V_{CC}$, Output is disabled	-2		+2	μA
Operating supply current	I_{CC}	Device selected, $V_{IN} \leq V_{IL}$ or $V_{IN} \geq V_{IH}$, $I_{IO} = 0 \text{ mA}$, Cycle = 66 MHz			250	mA
	I_{CC1}	Suspend read cycle, $\overline{AC}$, $\overline{AP}$, $\overline{ADV}$, $\overline{GW}$, $\overline{BWs} \geq V_{IH}$, $V_{IN} \leq V_{IL}$ or $V_{IN} \geq V_{IH}$, $I_{IO} = 0 \text{ mA}$, Cycle = 66 MHz			45	
Standby supply current	I_{SB}	Device deselected, $V_{IN} \leq V_{IL}$ or $V_{IN} \geq V_{IH}$, Cycle = 0 MHz, All inputs are static			20	mA
	I_{SB1}	Device deselected, $V_{IN} \leq 0.2 \text{ V}$ or $V_{IN} \geq V_{CC} - 0.2 \text{ V}$, Cycle = 0 MHz, All inputs are static			2	
	I_{SB2}	Device deselected, $V_{IN} \leq V_{IL}$ or $V_{IN} \geq V_{IH}$, Cycle = 66 MHz			50	
High level output voltage	V_{OH}	$I_{OH} = -4 \text{ mA}$	2.4			V
Low level output voltage	V_{OL}	$I_{OL} = 8 \text{ mA}$			0.4	V

Remark V_{IN} : Input voltage

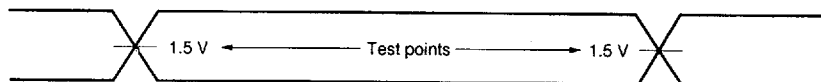
AC Characteristics (Recommended operating conditions unless otherwise noted)

AC Test Conditions

Input waveform (Rise/fall time ≤ 1.5 ns)



Output waveform



Output load

Fig. 1

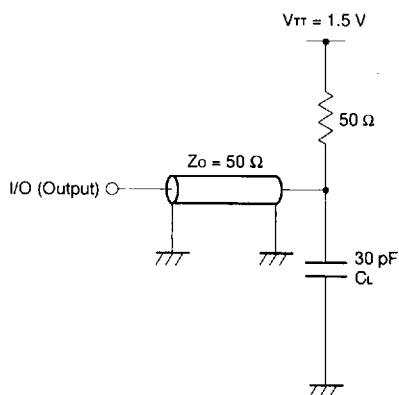
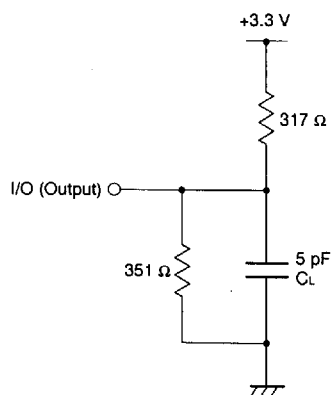


Fig. 2

(For TDC1, TDC2, TOLZ, TOHZ, TCZ)



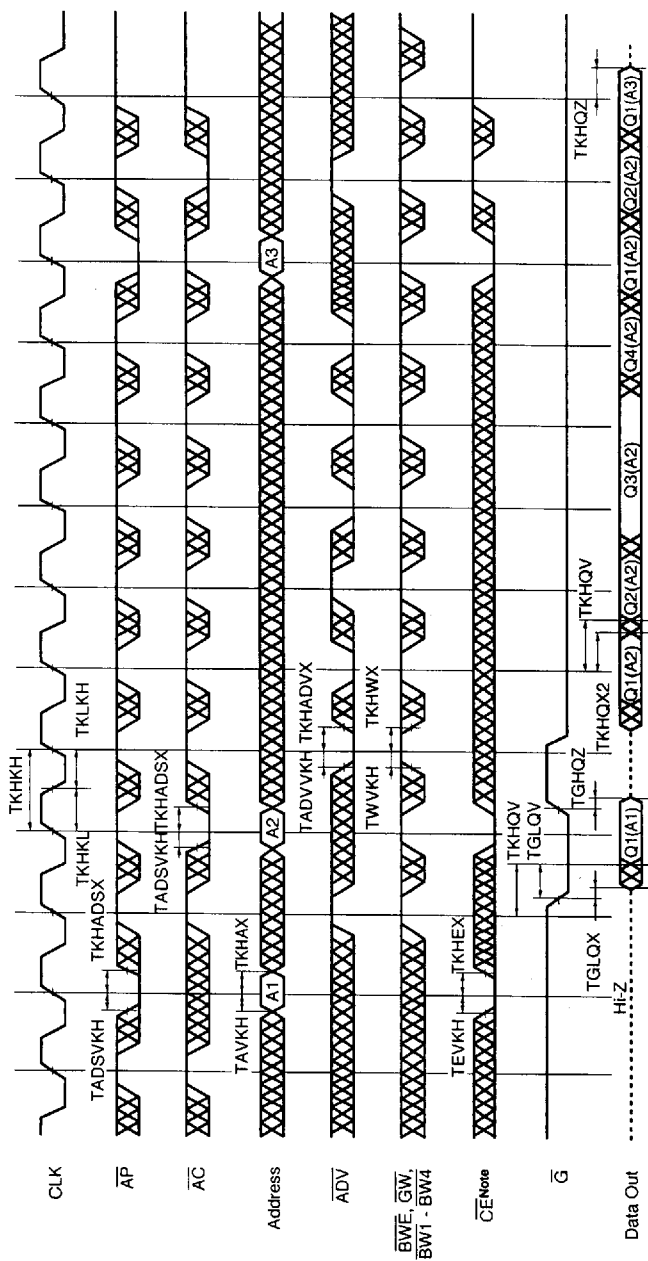
Remark CL includes capacitances of the probe and jig, and stray capacitances.

Read and Write Cycle

Parameter		Symbol		-A8 (66 MHz)		-A10 (60 MHz)		-A12 (50 MHz)		Unit	Note
		Standard	Alternate	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Cycle time		TKHKH	TCYC	15	—	16.7	—	20	—	ns	
Clock access time		TKHQV0	TCD0	—	8	—	10	—	12	ns	1
Clock access time		TKHQV	TCD	—	9	—	11	—	13	ns	
Output Enable to output valid		TGLQV	TOE	—	6	—	6	—	6	ns	
Clock high to output active		TKHQX1	TDC1	2	—	2	—	2	—	ns	
Clock high to output change		TKHQX2	TDC2	3	—	3	—	3	—	ns	
Output Enable to output active		TGLQX	TOLZ	2	—	2	—	2	—	ns	
Output disable to output Hi-Z		TGHQZ	TOHZ	—	5	—	5	—	6	ns	
Clock high to output Hi-Z		TKHQZ	TCZ	—	5	—	5	—	6	ns	
Clock high pulse width		TKHKL	TCH	5.5	—	6.5	—	6.5	—	ns	
Clock low pulse width		TKLKH	TCL	5.5	—	6.5	—	6.5	—	ns	
Setup times	Address	TAVKH	TAS	2.5	—	3	—	3	—	ns	
	Address status	TADSVKH	TSS								
	Data In	TDVKH	TDS								
	Write Enable	TWVKH	TWS								
	Address advance	TADVVKH	—								
	Chip Enable	TEVKH	—								
Hold times	Address	TKHAX	TAH	0.5	—	0.5	—	0.5	—	ns	
	Address status	TKHADSX	TSH								
	Data In	TKHDX	TDH								
	Write Enable	TKHWX	TWH								
	Address advance	TKHADVX	—								
	Chip Enable	TKHEX	—								

Note 1. No output load. Values are simulated.

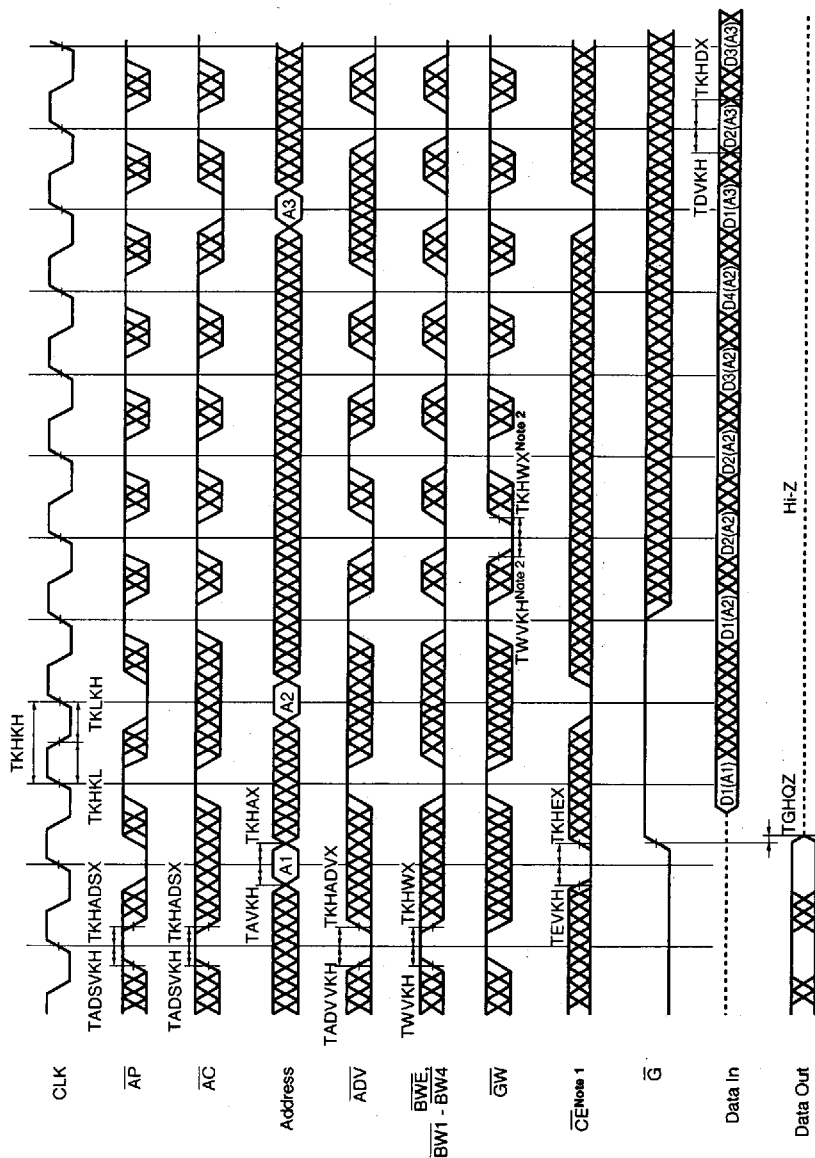
Read Cycle



Note $\overline{\text{CE2}}$ and CE2 have the same timing as $\overline{\text{CE}}$. In this timing, when $\overline{\text{CE}}$ is low, $\overline{\text{CE2}}$ is low and CE2 is high. When $\overline{\text{CE}}$ is high, $\overline{\text{CE2}}$ is high and CE2 is low.

Remark $Q_n(A2)$ refers to output from address A2. $Q1 - Q4$ refers to outputs according to burst sequence.

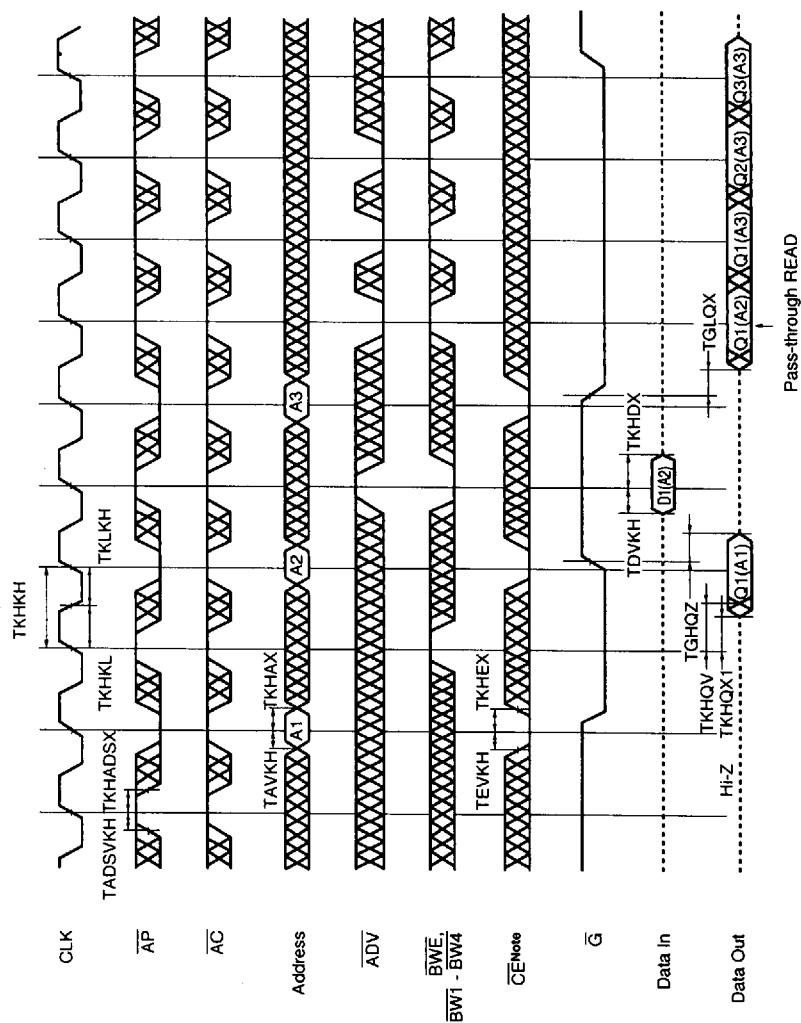
Write Cycle



Notes 1. $\overline{CE2}$ and $\overline{CE2}$ have the same timing as $\overline{CE}$. In this timing, when $\overline{CE}$ is low, $\overline{CE2}$ is low and $\overline{CE2}$ is high. When $\overline{CE}$ is high, $\overline{CE2}$ is high and $\overline{CE2}$ is low.

2. All bytes **WRITE** can be initiated by $\overline{GW}$ low or $\overline{GW}$ high and $\overline{BWE}$, $\overline{BW1-BW4}$ low.

Read/Write Cycle



Pass-through READ

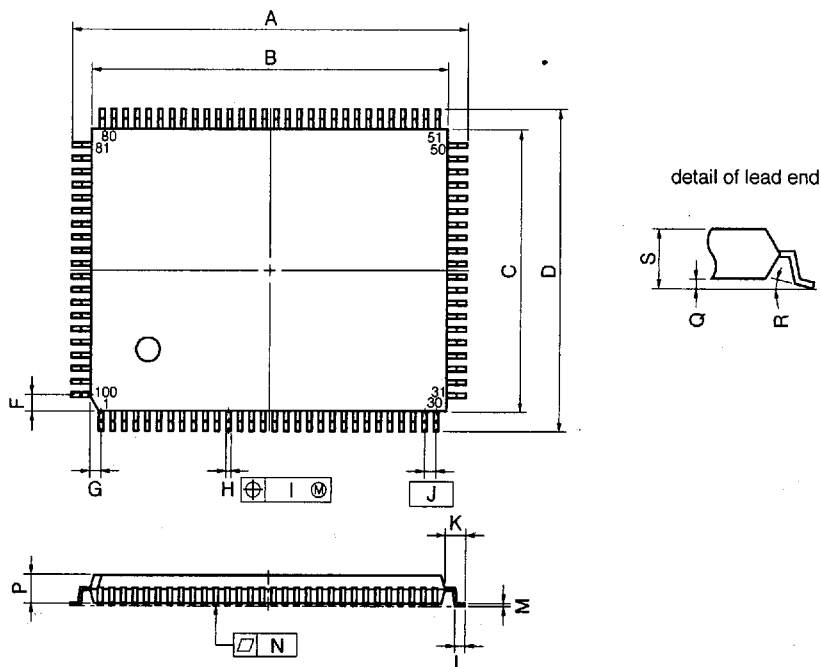
Note $\overline{CE2}$ and $\overline{CE}$ have the same timing as $\overline{CE}$. In this timing, when $\overline{CE}$ is low, $\overline{CE2}$ is low and $\overline{CE2}$ is high. When $\overline{CE}$ is high, $\overline{CE2}$ is high and $\overline{CE2}$ is low.

Remarks 1. $\overline{GW}$ is high.

2. The data out remains in Hi-Z following a WRITE cycle unless an $\overline{AP}$, $\overline{AC}$ or $\overline{ADV}$ cycle is performed.

Package Drawing

100 PIN PLASTIC LQFP (14X20)



NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	22.0±0.2	0.866±0.008
B	20.0±0.2	0.787 ^{+0.009} _{-0.008}
C	14.0±0.2	0.551 ^{+0.009} _{-0.008}
D	16.0±0.2	0.630±0.008
F	0.825	0.032
G	0.575	0.023
H	0.32 ^{+0.08} _{-0.07}	0.013±0.003
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.0±0.2	0.039 ^{+0.009} _{-0.008}
L	0.5±0.2	0.020 ^{+0.008} _{-0.009}
M	0.17 ^{+0.06} _{-0.05}	0.007±0.002
N	0.10	0.004
P	1.4	0.055
Q	0.125±0.075	0.005±0.003
R	3 ⁺⁷ ₋₃	3 ⁺⁷ ₋₃
S	1.7 MAX.	0.067 MAX.

S100GF-65-8ET

Remark TQFPs with a 1.4 mm package thickness are called LQFP in EIAJ.

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of μ PD431232L.

Type of Surface Mount Device

μ PD431232LGF: 100-pin plastic TQFP (14 × 20 mm)