μPD43251B
262,144 x 1-Bit
Static CMOS RAM

Description

The μPD43251B is a 262,144-word by 1-bit static RAM fabricated with advanced silicon-gate technology. A unique design that uses CMOS peripheral circuits and N-channel memory cells with polysilicon resistors makes the μPD43251B a high-speed device that requires no clock or refreshing.

The μPD43251B is available in 24-pin plastic DIP or 24-pin plastic SOJ packaging.

Features

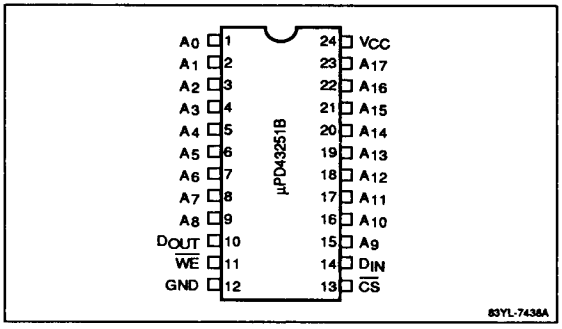
- 262,144-word x 1-bit organization
- Single +5-volt power supply
- Fully static operation—no clock or refreshing
- TTL-compatible inputs and outputs
- Separated data input and output
- Three-state outputs
- Power dissipation
  - —120 mA max (active)
  - —2 mA max (standby)
- Standard 300-mil, 24-pin plastic DIP or 24-pin plastic SOJ packaging

Ordering Information

Part Number	Access Time (max)	Package
μPD43251BCR-15	15 ns	24-pin plastic DIP
CR-20	20 ns	
CR-25	25 ns	
μPD43251BLA-15	15 ns	24-pin plastic SOJ
LA-20	20 ns	
LA-25	25 ns	

Pin Configuration

24-Pin Plastic DIP or SOJ



Pin Identification

Symbol	Function
A_0 - A_{17}	Address inputs
D_{IN}	Data input
D_{OUT}	Data output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply

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Absolute Maximum Ratings

Power supply voltage, V_{CC}	−0.5 to +7.0 V
Input voltage, V_{IN} (Note 1)	−0.5 to +V_{CC} + 0.3
Output voltage, V_{OUT}	−0.5 to +V_{CC} + 0.3
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Notes:

(1) V_{IN} = −3.0 V min for 10 ns maximum pulse.

Truth Table

Function	$\overline{CS}$	$\overline{WE}$	D_{OUT}	I_{CC}
Not selected	H	X	High-Z	Standby
Read	L	H	Output data	Active
Write	L	L	High-Z	Active

Capacitance

T_A = +25°C; f = 1 MHz (Note 1); V_{IN} and V_{OUT} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I			6	pF
Output capacitance	C_O			8	pF

Notes:

(1) This parameter is sampled and not 100% tested.

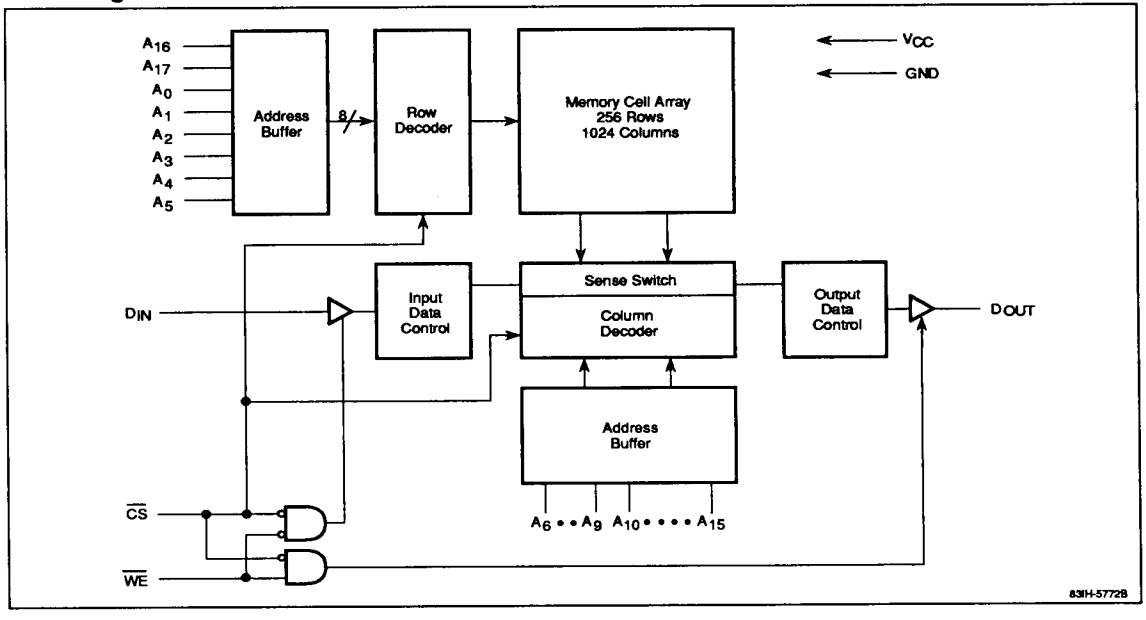
Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, low (Note 1)	V_{IL}	−0.5		0.8	V
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V
Ambient temperature	T_A	0		70	°C

Notes:

(1) V_{IL} = −3.0 V min for 10 ns maximum pulse.

Block Diagram



DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	−2		2	μA	V_{IN} = 0 V to V_{CC}
Output leakage current	I_{LO}	−2		2	μA	V_{OUT} = 0 V to V_{CC}; $\overline{CS}$ = V_{IH}
Standby supply current	I_{SB}			30	mA	$\overline{CS}$ = V_{IH}; V_{IN} = V_{IH} or V_{IL}
	I_{SB1}			2	mA	$\overline{CS}$ ≥ V_{CC} − 0.2 V; V_{IN} ≤ 0.2 V or ≥ V_{CC} − 0.2 V
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 8.0 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −4.0 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		μPD43251B-15		μPD43251B-20		μPD43251B-25			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions (Note 1)
Read Operation									
Operating supply current	I_{CC}		120		100		100	mA	$\overline{CS}$ = V_{IL} (min cycle); I_{OUT} = 0 mA
Read cycle time	t_{RC}	15		20		25		ns	(Note 2)
Read access time	t_{AA}		15		20		25	ns	
Chip select access time	t_{ACS}		15		20		25	ns	
Output hold from address change	t_{OH}	3		3		3		ns	
Chip select to output in low-Z	t_{CLZ}	3		3		3		ns	(Note 3)
Chip deselect to output in high-Z	t_{CHZ}	0	6	0	8	0	10	ns	(Note 4)
Write Operation									
Write cycle time	t_{WC}	15		20		25		ns	(Note 2)
Chip select to end of write	t_{CW}	13		15		20		ns	
Address valid to end of write	t_{AW}	13		15		20		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write pulse width	t_{WP}	12		14		18		ns	
Write recovery time	t_{WR}	0		0		0		ns	
Data valid to end of write	t_{DW}	10		12		14		ns	
Data hold time	t_{DH}	0		0		0		ns	
Write enable to output in high-Z	t_{WHZ}	0	6	0	8	0	10	ns	(Note 4)
Output active from end of write	t_{OW}	0		0		0		ns	(Note 3)

Notes:

(1) Input pulse levels = GND to 3.0 V; input pulse rise and fall time = 5 ns; timing reference levels = 1.5 V; see figures 1 and 2 for the output load.

(2) All read and write cycle timings are referenced from the last valid address to the first transitioning address.

(3) The transition is measured ±200 mV from steady-state voltage with the loading shown in figure 2.

(4) The transition is measured at V_{OL} + 200 mV and V_{OH} − 200 mV with the loading shown in figure 2.

Figure 1. Output Load

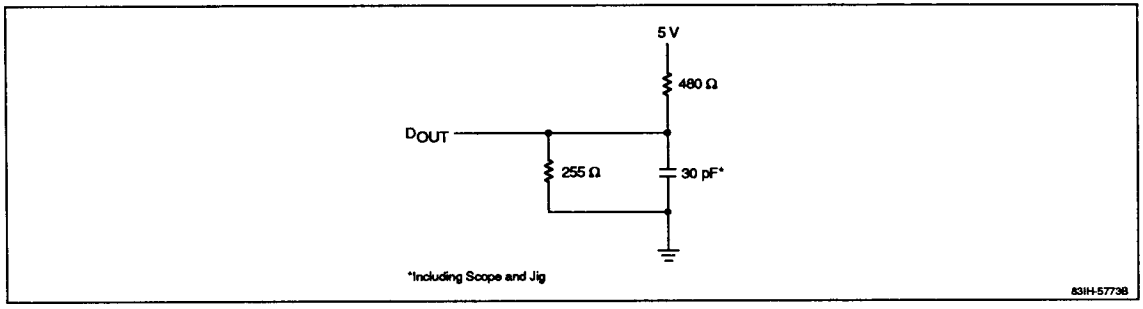
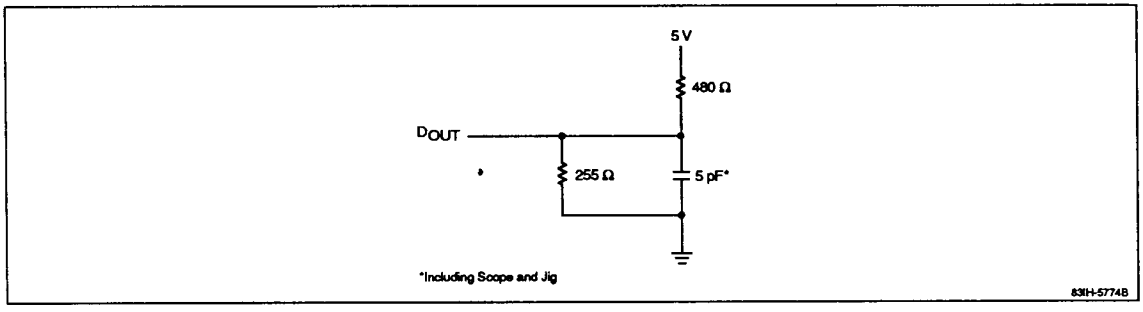
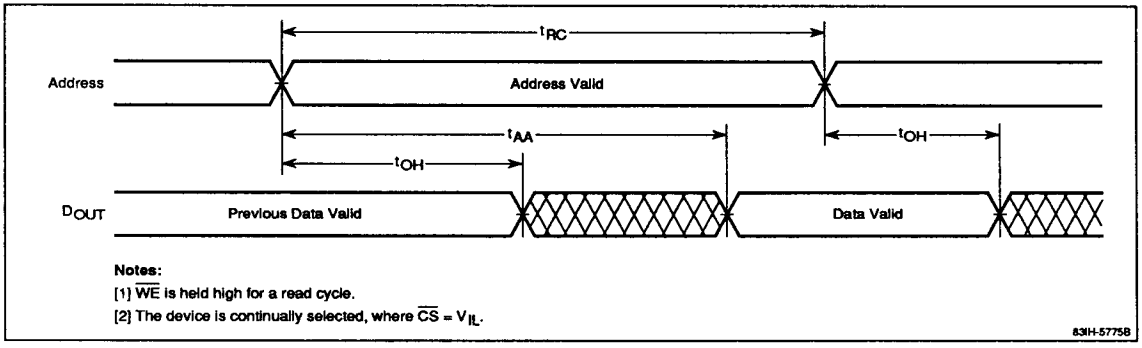


Figure 2. Output Load for t_{CHZ}, t_{CLZ}, t_{OW}, and t_{WHZ}



Timing Waveforms

Address Access Cycle



Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] The device is continually selected, where $\overline{CS} = V_{IL}$.

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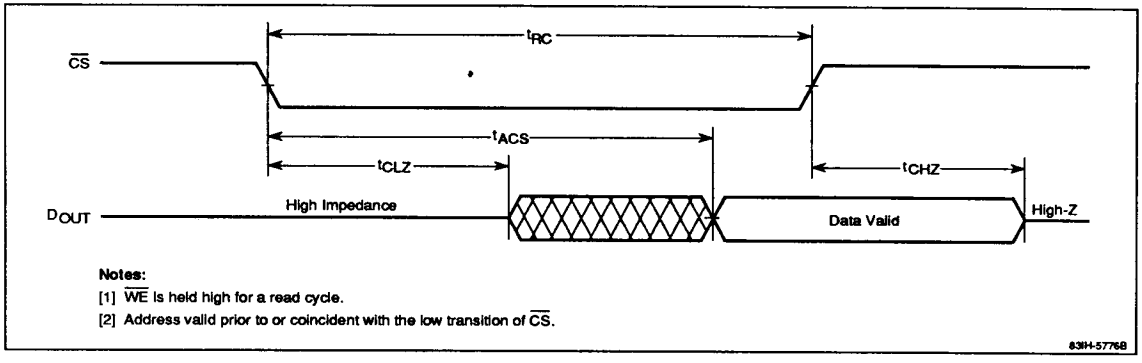
Chip Select Access Cycle



Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] Address valid prior to or coincident with the low transition of $\overline{CS}$.

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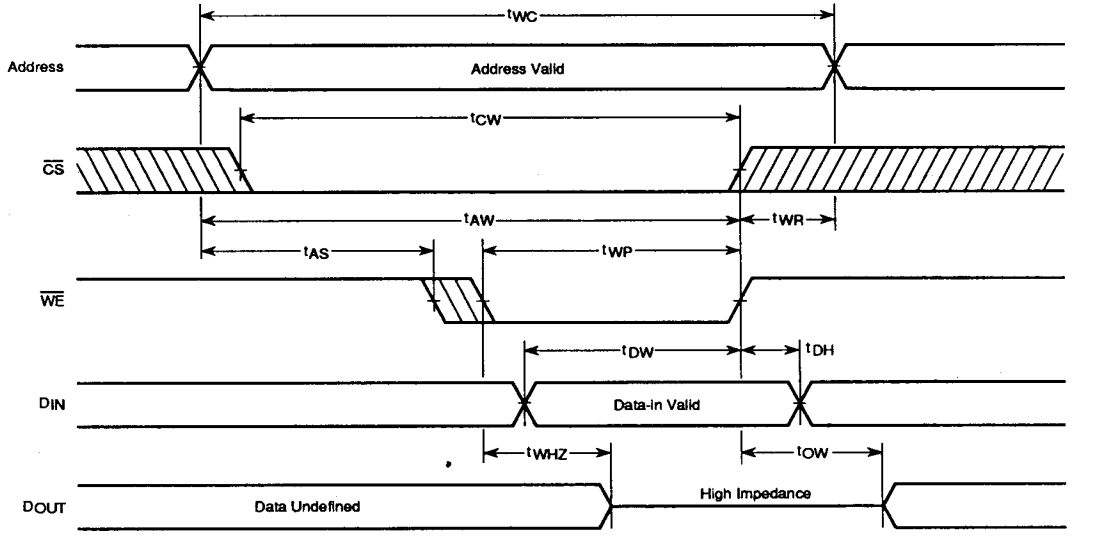
Timing Waveforms (cont)

$\overline{WE}$-Controlled Write Cycle



Notes:

[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

[2] A write cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

[3] t_{WR} is measured between $\overline{CS}$ or $\overline{WE}$, whichever rising edge occurs first, and the end of t_{WC}.

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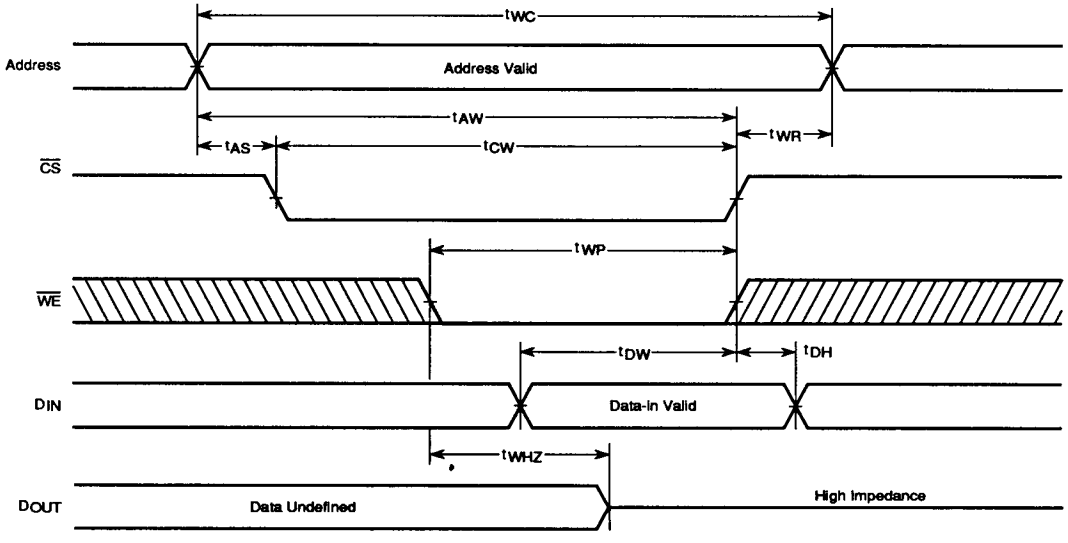
Timing Waveforms (cont)

$\overline{CS}$-Controlled Write Cycle



Notes:

[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

[2] A write cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

[3] t_{WR} is measured between $\overline{CS}$ or $\overline{WE}$, whichever rising edge occurs first, and the end of t_{WC}.

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