

256K-BIT CMOS STATIC RAM
32K-WORD BY 8-BIT
Description

The μ PD43256B is a high speed, low power, and 262,144 bits (32,768 words by 8 bits) CMOS static RAM. Battery backup is available (L, LL, A, and B versions). And A and B versions are wide voltage operations. The μ PD43256B is packed in 28-pin plastic DIP, 28-pin plastic SOP, and 32-pin plastic TSOP(I).

Features

- 32,768 words by 8 bits organization
- Fast access time: 55 ns (MAX.)
- Wide voltage range (A version: $V_{CC} = 3.0$ to 5.5 V, B version: $V_{CC} = 2.7$ to 5.5 V)
- 2 V data retention
- $\overline{OE}$ input for easy application

Part number	Access time ns (MAX.)	Operating supply voltage V	Operating temperature °C	Standby supply current μ A (MAX.)	^{Note 1} Data retention supply current μ A (MAX.)
μ PD43256B	55, 70, 85	4.5 to 5.5	0 to 70	2000	—
μ PD43256B-L	55, 70, 85			100	15
μ PD43256B-LL	55, 70, 85			50	3
μ PD43256B-A	85 ^{Note 2} , 100, 120	3.0 to 5.5			
μ PD43256B-B	85 ^{Note 2} , 100, 120	2.7 to 5.5			

Note 1. $T_A \leq 40^\circ\text{C}$, $V_{CC} = 3\text{ V}$

2. $V_{CC} = 4.5$ to 5.5 V

The information in this document is subject to change without notice.

Ordering Information (1/2)

Part number	Package	Access time ns (MAX.)	Operating supply voltage V	Operating temperature °C	Remark	
μPD43256BCZ-55	28-pin plastic DIP (600 mil)	55	4.5 to 5.5	0 to 70	—	
μPD43256BCZ-70		70				
μPD43256BCZ-85		85				
μPD43256BCZ-55L		55			L Version	
μPD43256BCZ-70L		70				
μPD43256BCZ-85L		85				
μPD43256BCZ-55LL		55			LL Version	
μPD43256BCZ-70LL		70				
μPD43256BCZ-85LL		85				
μPD43256BGU-55L		28-pin plastic SOP (450 mil)			55	3.0 to 5.5
μPD43256BGU-70L	70					
μPD43256BGU-85L	85					
μPD43256BGU-55LL	55		LL Version			
μPD43256BGU-70LL	70					
μPD43256BGU-85LL	85					
μPD43256BGU-A10	100		A Version			
μPD43256BGU-A12	120					
μPD43256BGU-B10	100		2.7 to 5.5	B Version		
μPD43256BGU-B12	120					

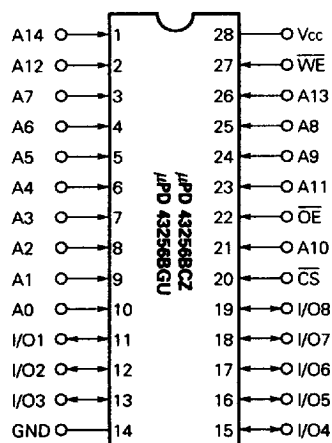
Ordering Information (2/2)

Part number	Package	Access time ns (MAX.)	Operating supply voltage V	Operating temperature °C	Remark
μPD43256BGX-55L-EJA	32-pin plastic TSOP(I)(600 mil) (Normal bent)	55	4.5 to 5.5	0 to 70	L Version
μPD43256BGX-70L-EJA		70			
μPD43256BGX-85L-EJA		85			
μPD43256BGX-55LL-EJA		55			LL Version
μPD43256BGX-70LL-EJA		70			
μPD43256BGX-85LL-EJA		85			
μPD43256BGX-A10-EJA		100	3.0 to 5.5		A Version
μPD43256BGX-A12-EJA		120			
μPD43256BGX-B10-EJA		100	2.7 to 5.5		B Version
μPD43256BGX-B12-EJA		120			
μPD43256BGX-55L-EKA	32-pin plastic TSOP(I)(600 mil) (Reverse bent)	55	4.5 to 5.5	0 to 70	L Version
μPD43256BGX-70L-EKA		70			
μPD43256BGX-85L-EKA		85			
μPD43256BGX-55LL-EKA		55			LL Version
μPD43256BGX-70LL-EKA		70			
μPD43256BGX-85LL-EKA		85			
μPD43256BGX-A10-EKA		100	3.0 to 5.5		A Version
μPD43256BGX-A12-EKA		120			
μPD43256BGX-B10-EKA		100	2.7 to 5.5		B Version
μPD43256BGX-B12-EKA		120			

Pin Configuration (Marking Side)

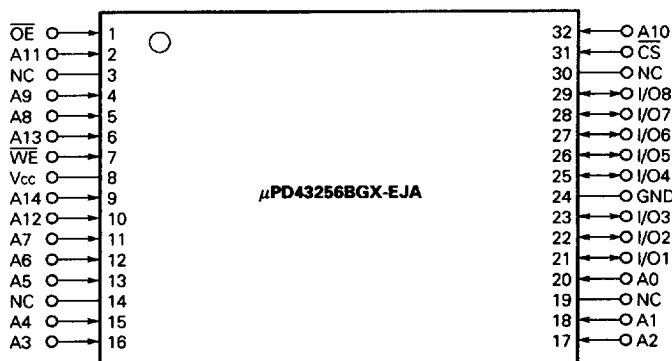
28-pin plastic DIP (600 mil)

28-pin plastic SOP (450 mil)



32-pin plastic TSOP (I) (600 mil)

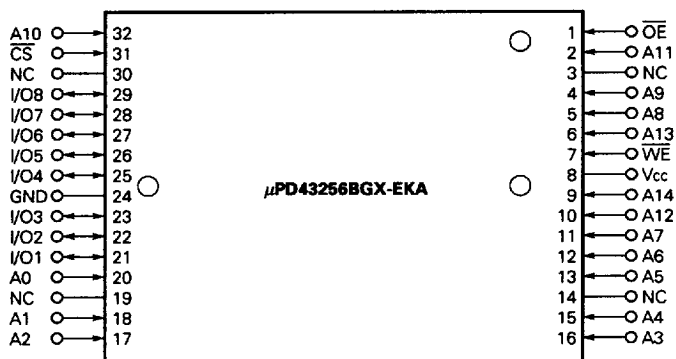
(Normal bent)



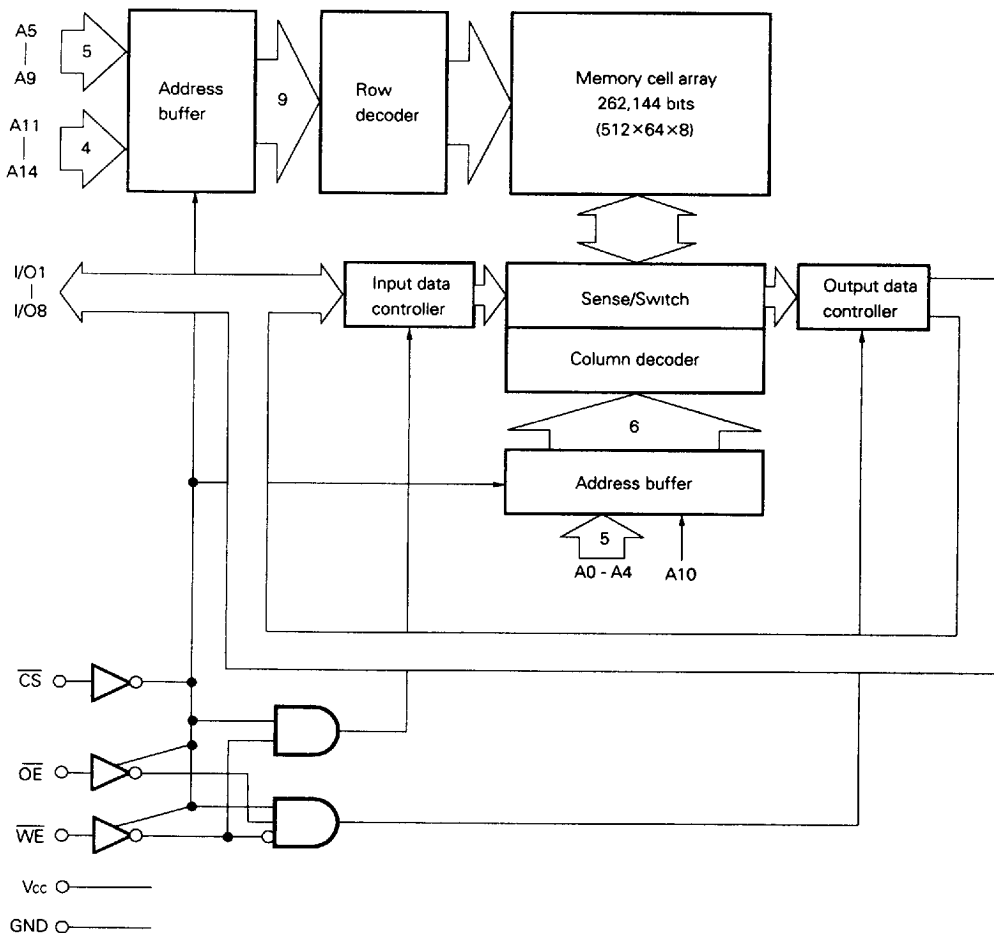
32-pin plastic TSOP (I) (600 mil)

(Reverse bent)

- A0 - A14 : Address inputs
 I/O1 - I/O8 : Data inputs/outputs
 CS : Chip Select
 WE : Write Enable
 OE : Output Enable
 Vcc : Power supply
 GND : Ground
 NC : No connection



Block Diagram



Truth Table

CS	OE	WE	Mode	I/O	Supply current
H	X	X	Not selected	High impedance	I _{SB}
L	H	H	Output disable		I _{CCA}
L	X	L	Write	D _{IN}	
L	L	H	Read	D _{OUT}	

Remark X : Don't care

Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	-0.5 ^{Note} to +7.0	V
Input/Output voltage	V_I	-0.5 ^{Note} to $V_{CC} + 0.5$	V
Operating ambient temperature	T_A	0 to 70	°C
Storage temperature	T_{stg}	-55 to +125	°C

Note -3.0 V (MIN.) (Pulse width 50 ns)

Caution Exposing the device to stress above those listed in absolute maximum ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this characteristics. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	μ PD43256B μ PD43256B-L μ PD43256B-LL		μ PD43256B-A		μ PD43256B-B		Unit
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Supply voltage	V_{CC}	4.5	5.5	3.0	5.5	2.7	5.5	V
High level input voltage	V_{IH}	2.2	$V_{CC} + 0.5$	2.2	$V_{CC} + 0.5$	2.2	$V_{CC} + 0.5$	V
Low level input voltage	V_{IL}	-0.3 ^{Note}	+0.8	-0.3 ^{Note}	+0.5	-0.3 ^{Note}	+0.5	V
Operating ambient temperature	T_A	0	70	0	70	0	70	°C

Note -3.0 V (MIN.) (Pulse width 50 ns)

DC Characteristics (Recommended operating conditions unless otherwise noted) (1/2)

Parameter	Symbol	Test conditions		μPD43256B			μPD43256B-L			μPD43256B-LL			Unit
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input leakage current	I _{LI}	V _{IN} = 0 V to V _{CC}		-1.0		+1.0	-1.0		+1.0	-1.0		+1.0	μA
I/O leakage current	I _{LO}	V _{IO} = 0 V to V _{CC} OE = V _{IH} or CS = V _{IH} or $\overline{WE}$ = V _{IL}		-1.0		+1.0	-1.0		+1.0	-1.0		+1.0	μA
Operating supply current	I _{CCA1}	CS = V _{IL} , Minimum cycle time, I _{IO} = 0 mA	μPD43256B-55			50			50			50	mA
			μPD43256B-70			45			45		45		
			μPD43256B-85										
	I _{CCA2}	$\overline{CS}$ = V _{IL} , I _{IO} = 0 mA				10			10			10	
	I _{CCA3}	CS ≤ 0.2 V, Cycle = 1 MHz, I _{IO} = 0 mA V _{IL} ≤ 0.2 V, V _{IH} ≥ V _{CC} - 0.2 V				10			10			10	
Standby supply current	I _{SB}	$\overline{CS}$ = V _{IH}				5			3			3	mA
	I _{SB1}	$\overline{CS}$ ≥ V _{CC} - 0.2 V			20	2000		2.0	100		1.0	50	μA
High level output voltage	V _{OH1}	I _{OH} = -1.0 mA		2.4			2.4			2.4			V
	V _{OH2}	I _{OH} = -0.1 mA		V _{CC} -0.5			V _{CC} -0.5			V _{CC} -0.5			
Low level output voltage	V _{OL}	I _{OL} = 2.1 mA				0.4			0.4			0.4	V

Remark 1. V_{IN} : Input voltage

2. These DC Characteristics are in common regardless of package types.

DC Characteristics (Recommended operating conditions unless otherwise noted) (2/2)

Parameter	Symbol	Test conditions		μ PD43256B-A			μ PD43256B-B			Unit
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input leakage current	I_{LI}	$V_{IN} = 0 \text{ V to } V_{CC}$		-1.0		+1.0	-1.0		+1.0	μA
I/O leakage current		$V_{IO} = 0 \text{ V to } V_{CC}$ $\overline{CS} = V_{IH}$ or $\overline{WE} = V_{IL}$ or $\overline{OE} = V_{IH}$		-1.0		+1.0	-1.0		+1.0	μA
Operating supply current	I_{CCA1}	$\overline{CS} = V_{IL}$, Minimum cycle time, $I_{IO} = 0 \text{ mA}$	$\mu\text{PD43256B-A10}$			45			—	mA
			$\mu\text{PD43256B-A12}$							
			$\mu\text{PD43256B-B10}$						45	
			$\mu\text{PD43256B-B12}$							
	I_{CCA2}	$\overline{CS} = V_{IL}$, $I_{IO} = 0 \text{ mA}$	$V_{CC} \leq 3.3 \text{ V}$				—			20
Standby supply current	I_{SB}	$\overline{CS} = V_{IH}$	$V_{CC} \leq 3.3 \text{ V}$				10			10
										5
	I_{CCA3}	$\overline{CS} \leq 0.2 \text{ V}$, Cycle = 1 MHz, $I_{IO} = 0 \text{ mA}$, $V_{IL} \leq 0.2 \text{ V}$, $V_{IH} \geq V_{CC} - 0.2 \text{ V}$	$V_{CC} \leq 3.3 \text{ V}$				10			10
										5
Standby supply current	I_{SB}	$\overline{CS} = V_{IH}$	$V_{CC} \leq 3.3 \text{ V}$				3			3
										2
	I_{SB1}	$\overline{CS} \geq V_{CC} - 0.2 \text{ V}$	$V_{CC} \leq 3.3 \text{ V}$			1.0	50		1.0	50
									0.5	25
High level output voltage	V_{OH1}	$I_{OH} = -1.0 \text{ mA}$, $V_{CC} \geq 4.5 \text{ V}$	2.4			2.4			V	
		$I_{OH} = -0.5 \text{ mA}$, $V_{CC} < 4.5 \text{ V}$	2.4			2.4				
	V_{OH2}	$I_{OH} = -0.1 \text{ mA}$	—			—				
		$I_{OH} = -0.02 \text{ mA}$	$V_{CC}-0.1$			$V_{CC}-0.1$				
Low level output voltage	V_{OL}	$I_{OL} = 2.1 \text{ mA}$, $V_{CC} \geq 4.5 \text{ V}$			0.4			0.4	V	
		$I_{OL} = 1.0 \text{ mA}$, $V_{CC} < 4.5 \text{ V}$			0.4			0.4		
	V_{OL1}	$I_{OL} = 0.02 \text{ mA}$			0.1			0.1		

Remark 1. V_{IN} : Input voltage

2. These DC Characteristics are in common regardless of package types.

Capacitance ($T_A = 25^\circ\text{C}$, $f = 1 \text{ MHz}$)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	$V_{IN} = 0 \text{ V}$			5	pF
Input/Output capacitance	C_{IO}	$V_{IO} = 0 \text{ V}$			8	pF

Remark 1. V_{IN} : Input voltage

2. These parameters are periodically sampled and not 100 % tested.

AC Characteristics (Recommended operating conditions unless otherwise noted)

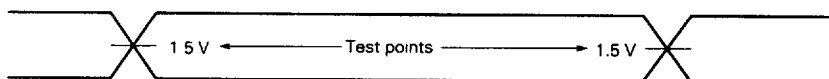
AC Test Conditions

Input waveform (Rise/fall time ≤ 5 ns)

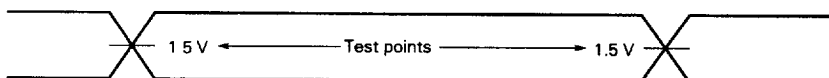
Input pulse levels

0.8 V to 2.2 V : μPD43256B, μPD43256B-L, μPD43256B-LL

0.5 V to 2.2 V : μPD43256B-A, μPD43256B-B



Output waveform



Output load

AC characteristics with notes should be measured with the output load shown in Fig. 1 and Fig. 2.

Fig. 1
(For tAA, tACS, tOE, tOH)

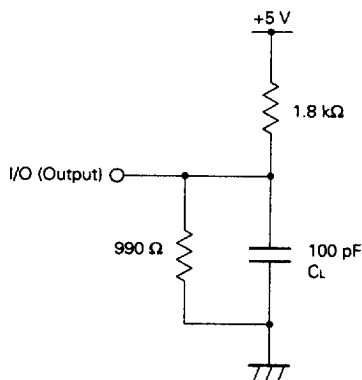
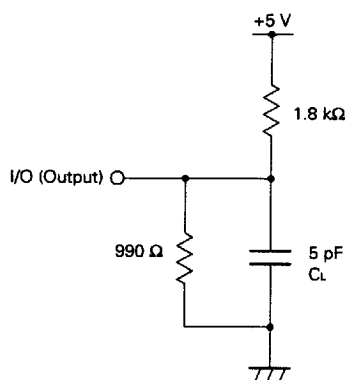


Fig. 2
(For tCHZ, tCLZ, tOHZ, tOLZ, tWHZ, tOW)



Remark CL includes capacitances of the probe and jig, and stray capacitances.

Read Cycle (1/2)

Parameter	Symbol	V _{CC} ≥ 4.5 V						Unit	Condition
		μPD43256B-55		μPD43256B-70		μPD43256B-85 μPD43256B-A10 μPD43256B-A12 μPD43256B-B10 μPD43256B-B12			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t _{RC}	55		70		85		ns	
Address access time	t _{AA}		55		70		85	ns	Note 1
CS access time	t _{ACS}		55		70		85	ns	
OE to output valid	t _{OE}		30		35		40	ns	
Output hold from address change	t _{OH}	10		10		10		ns	
CS to output in low impedance	t _{CLZ}	10		10		10		ns	Note 2
OE to output in low impedance	t _{OLZ}	5		5		5		ns	
CS to output in high impedance	t _{CHZ}		30		30		30	ns	
OE to output in high impedance	t _{OHZ}		30		30		30	ns	

Note 1. See the output load shown in Fig. 1.

2. See the output load shown in Fig. 2.

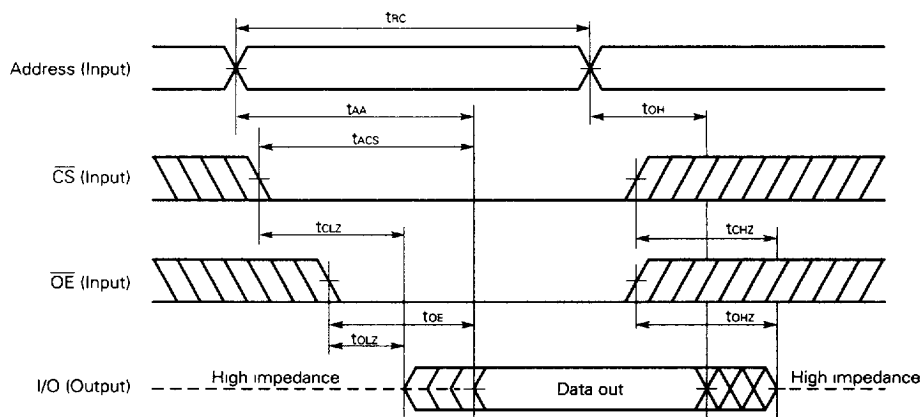
Read Cycle (2/2)

Parameter	Symbol	$V_{CC} \geq 3.0 \text{ V}$				$V_{CC} \geq 2.7 \text{ V}$				Unit	Condition
		$\mu\text{PD43256B-A10}$		$\mu\text{PD43256B-A12}$		$\mu\text{PD43256B-B10}$		$\mu\text{PD43256B-B12}$			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	100		120		100		120		ns	
Address access time	t_{AA}		100		120		100		120	ns	Note 1
$\overline{CS}$ access time	t_{ACS}		100		120		100		120	ns	
$\overline{OE}$ access time	t_{OE}		60		60		60		60	ns	
Output hold from address change	t_{OH}	10		10		10		10		ns	
$\overline{CS}$ to output in low impedance	t_{CLZ}	10		10		10		10		ns	Note 2
$\overline{OE}$ to output in low impedance	t_{OLZ}	5		5		5		5		ns	
$\overline{CS}$ to output in high impedance	t_{CHZ}		35		40		35		40	ns	
$\overline{OE}$ to output in high impedance	t_{OHZ}		35		40		35		40	ns	

Note 1. See the output load shown in Fig. 1.

2. See the output load shown in Fig. 2.

Read Cycle Timing Chart



Remark In read cycle, $\overline{WE}$ should be fixed to high level.

Write Cycle (1/2)

Parameter	Symbol	V _{CC} ≥ 4.5 V						Unit	Condition
		μPD43256B-55		μPD43256B-70		μPD43256B-85 μPD43256B-A10 μPD43256B-A12 μPD43256B-B10 μPD43256B-B12			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	t _{WC}	55		70		85		ns	
CS to end of write	t _{CS}	50		60		70		ns	
Address valid to end of write	t _{AW}	50		60		70		ns	
Write pulse width	t _{WP}	45		55		65		ns	
Data valid to end of write	t _{DV}	30		30		35		ns	
Data hold time	t _{DH}	0		0		0		ns	
Address setup time	t _{AS}	0		0		0		ns	
Write recovery time	t _{WR}	5		5		5		ns	
WE to output in high impedance	t _{WHZ}		30		30		30	ns	Note
Output active from end of write	t _{OW}	10		10		10		ns	

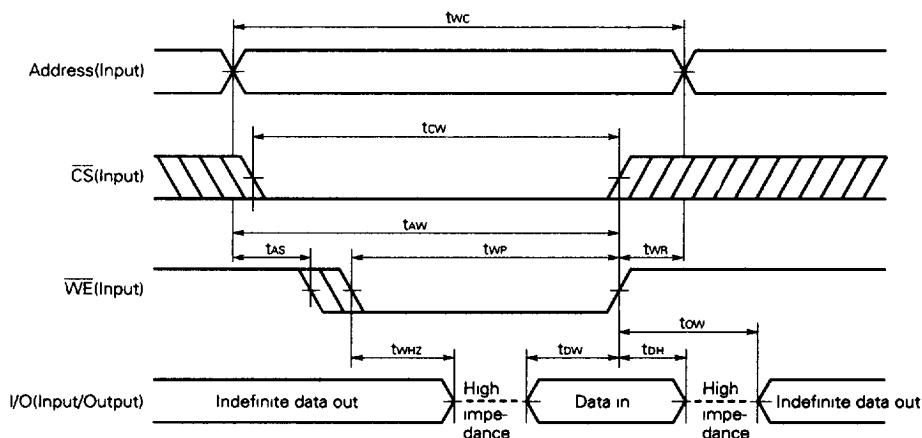
Note See the output load shown in Fig. 2.

Write Cycle (2/2)

Parameter	Symbol	V _{CC} ≥ 3.0 V				V _{CC} ≥ 2.7 V				Unit	Condition
		μPD43256B-A10		μPD43256B-A12		μPD43256B-B10		μPD43256B-B12			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	t _{WC}	100		120		100		120		ns	
$\overline{\text{CS}}$ to end of write	t _{CSW}	90		110		90		110		ns	
Address valid to end of write	t _{AW}	90		110		90		110		ns	
Write pulse width	t _{WP}	80		100		80		100		ns	
Data valid to end of write	t _{DW}	60		70		60		70		ns	
Data hold time	t _{DH}	0		0		0		0		ns	
Address setup time	t _{AS}	0		0		0		0		ns	
Write recovery time	t _{WR}	5		5		5		5		ns	
$\overline{\text{WE}}$ to output in high impedance	t _{WHZ}		35		40		35		40	ns	Note
Output active from end of write	t _{OW}	10		10		10		10		ns	

Note See the output load shown in Fig. 2.

Write Cycle Timing Chart 1 ($\overline{WE}$ Controlled)

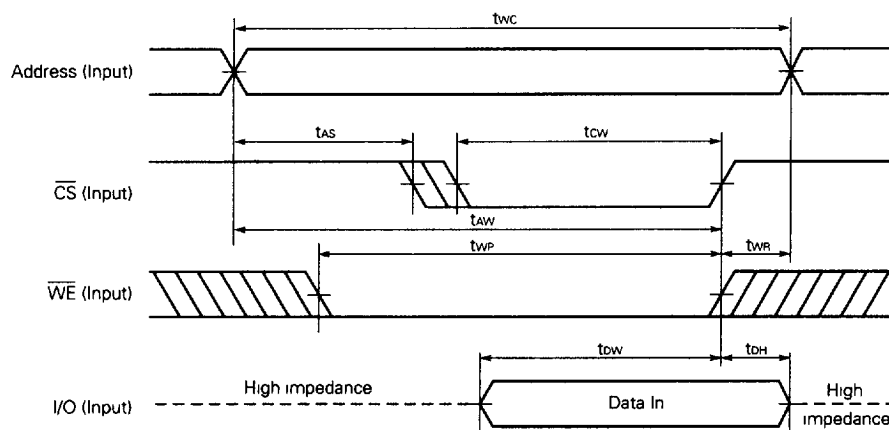


Caution $\overline{CS}$ or $\overline{WE}$ should be fixed to high level during address transition.

Remark 1. Write operation is done during the overlap time of a low level $\overline{CS}$ and a low level $\overline{WE}$.

2. When $\overline{WE}$ is at low level, the I/O pins are always high impedance. When $\overline{WE}$ is at high level, read operation is executed. Therefore $\overline{OE}$ should be at high level to make the I/O pins high impedance.
3. If $\overline{CS}$ changes to low level at the same time or after the change of $\overline{WE}$ to low level, the I/O pins will remain high impedance state.

Write Cycle Timing Chart 2 ($\overline{CS}$ Controlled)



Caution $\overline{CS}$ or $\overline{WE}$ should be fixed to high level during address transition.

Remark Write operation is done during the overlap time of a low level $\overline{CS}$ and a low level $\overline{WE}$.

Low Vcc Data Retention Characteristics

L Version (μ PD43256B-L: $T_A = 0$ to 70°C)

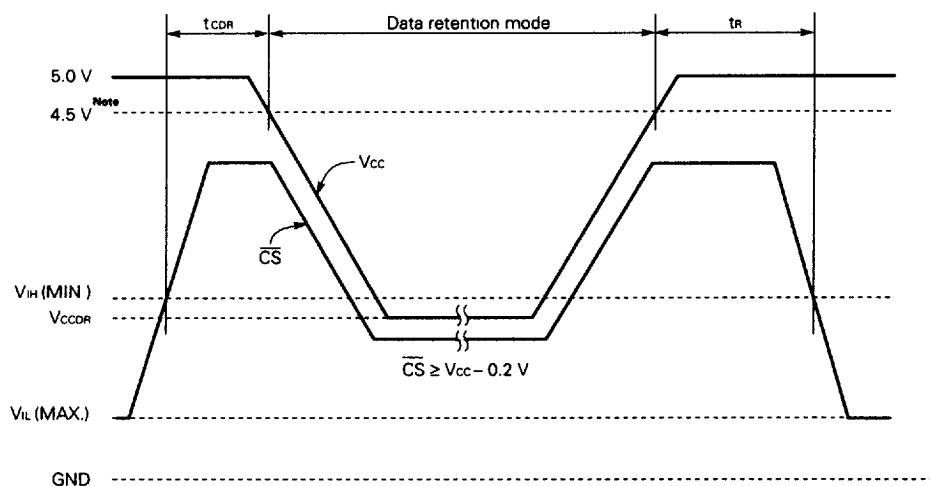
Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{CCDR}	$\overline{CS} \geq V_{CC} - 0.2\text{ V}$	2.0		5.5	V
Data retention supply current	I_{CCDR}	$V_{CC} = 3.0\text{ V}$, $\overline{CS} \geq V_{CC} - 0.2\text{ V}$		1	50 ^{Note}	μA
Chip deselection to data retention mode	t_{CDR}		0			ns
Operation recovery time	t_R		5			ms

Note 15 μA ($T_A \leq 40^\circ\text{C}$)LL Version (μ PD43256B-LL: $T_A = 0$ to 70°C)A Version (μ PD43256B-A: $T_A = 0$ to 70°C)B Version (μ PD43256B-B: $T_A = 0$ to 70°C)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{CCDR}	$\overline{CS} \geq V_{CC} - 0.2\text{ V}$	2.0		5.5	V
Data retention supply current	I_{CCDR}	$V_{CC} = 3.0\text{ V}$, $\overline{CS} \geq V_{CC} - 0.2\text{ V}$		0.5	20 ^{Note}	μA
Chip deselection to data retention mode	t_{CDR}		0			ns
Operation recovery time	t_R		5			ms

Note 3 μA ($T_A \leq 40^\circ\text{C}$), 1 μA ($T_A \leq 25^\circ\text{C}$)

Data Retention Timing Chart

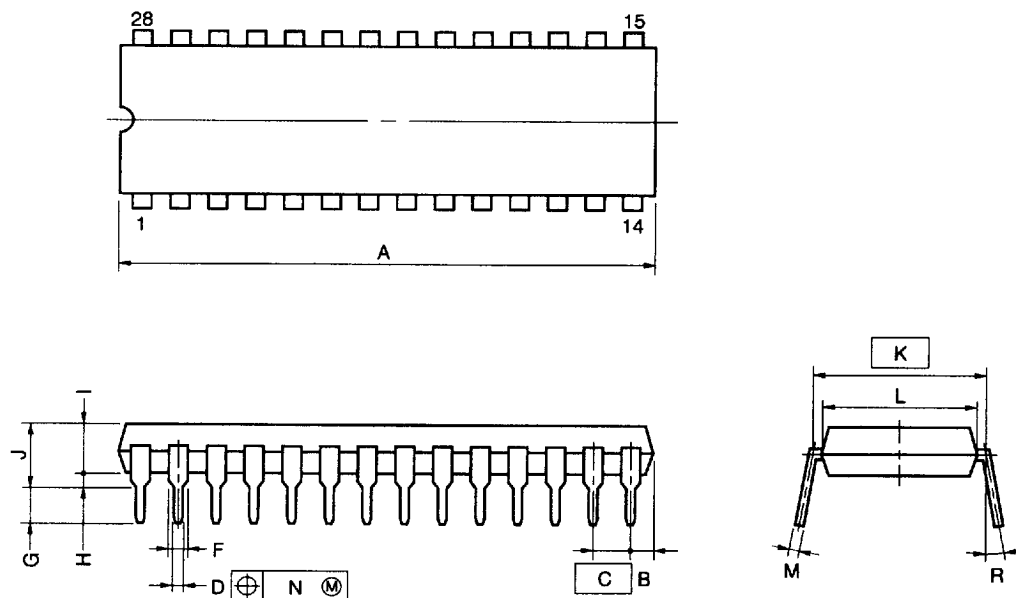


Note A Version: 3.0 V, B Version: 2.7 V

Remark The other pins (address, $\overline{OE}$, $\overline{WE}$, I/Os) can be in high impedance state.

Package Drawings

28 PIN PLASTIC DIP (600 mil)



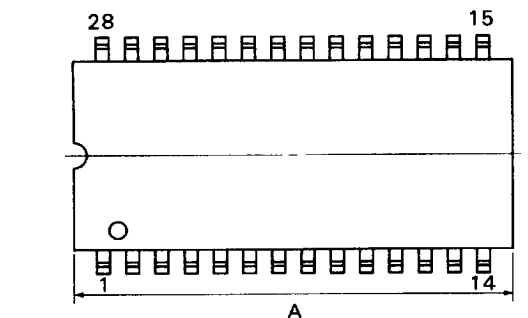
NOTES

- 1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.
- 2) Item "K" to center of leads when formed parallel.

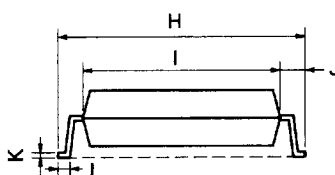
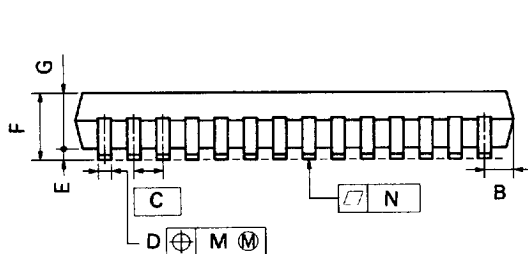
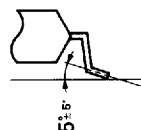
ITEM	MILLIMETERS	INCHES
A	38.10 MAX.	1.500 MAX.
B	2.54 MAX.	0.100 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	0.50±0.10	0.020 ^{+0.004} _{-0.005}
F	1.2 MIN.	0.047 MIN.
G	3.6±0.3	0.142±0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.72 MAX.	0.226 MAX.
K	15.24 (T.P.)	0.600 (T.P.)
L	13.2	0.520
M	0.25 ^{+0.10} _{-0.05}	0.010 ^{+0.004} _{-0.003}
N	0.25	0.01
R	0 ~ 15°	0 ~ 15°

P28C-100-600A1-1

28 PIN PLASTIC SOP(450mil)



detail of lead end



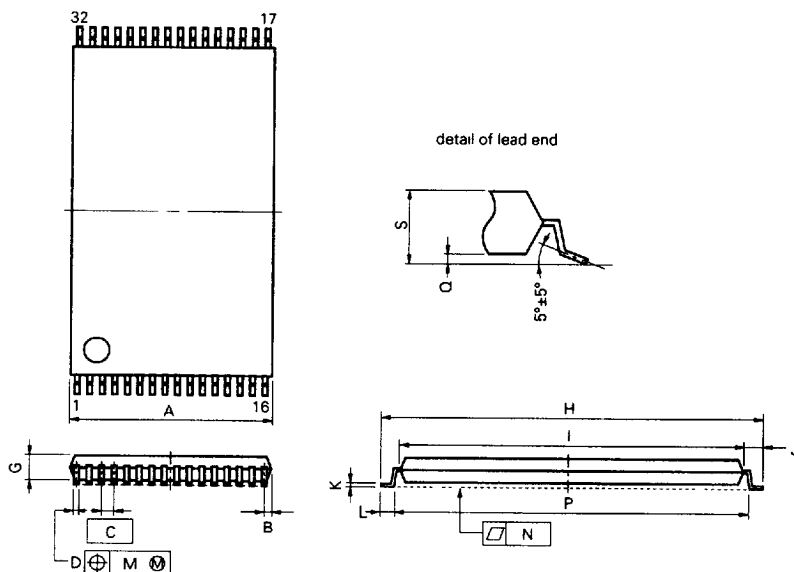
P28GU-50-450A

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	19.05MAX.	0.750MAX.
B	1.27MAX.	0.050MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40 $\pm$ 0.10	0.016 $\pm$ 0.004
E	0.2 $\pm$ 0.1	0.008 $\pm$ 0.004
F	3.0MAX.	0.119MAX.
G	2.55 $\pm$ 0.1	0.100 $\pm$ 0.004
H	11.8 $\pm$ 0.3	0.465 $\pm$ 0.012
I	8.4 $\pm$ 0.1	0.331 $\pm$ 0.004
J	1.7 $\pm$ 0.2	0.067 $\pm$ 0.008
K	0.20 $\pm$ 0.03	0.008 $\pm$ 0.001
L	0.7 $\pm$ 0.2	0.028 $\pm$ 0.008
M	0.12	0.005
N	0.10	0.004

32 PIN PLASTIC TSOP(I) (600 mil)

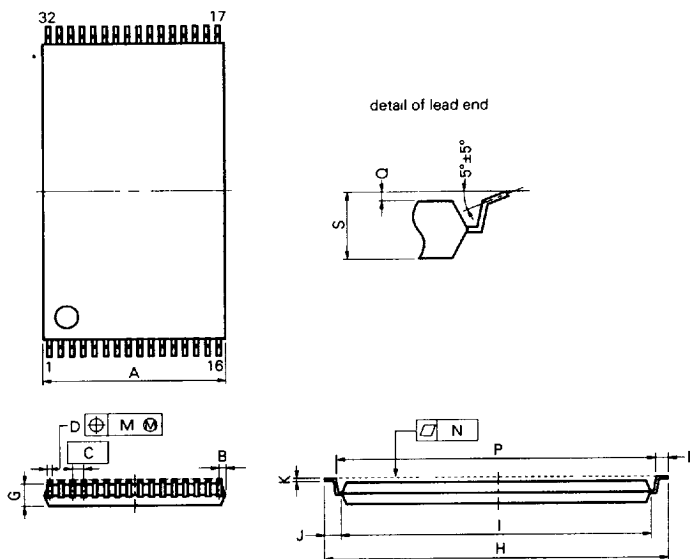
**NOTE**

Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition

S32GX-50-EJA-1

ITEM	MILLIMETERS	INCHES
A	8.2 MAX.	0.323 MAX.
B	0.45 MAX.	0.018 MAX.
C	0.5 (T.P.)	0.020 (T.P.)
D	0.20±0.10	0.008±0.004
G	1.05	0.041
H	15.3±0.2	0.602 ^{+0.009} _{-0.008}
I	13.7	0.539
J	0.8±0.2	0.031 ^{+0.009} _{-0.008}
K	0.125 ^{+0.10} _{-0.05}	0.005 ^{+0.004} _{-0.002}
L	0.5±0.1	0.020 ^{+0.004} _{-0.005}
M	0.08	0.003
N	0.10	0.004
P	14.3±0.2	0.563±0.008
Q	0.05±0.05	0.002±0.002
S	1.27 MAX.	0.050 MAX.

32 PIN PLASTIC TSOP(I) (600 mil)



NOTE

Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

S32GX-50-EKA-1

ITEM	MILLIMETERS	INCHES
A	8.2 MAX	0.323 MAX.
B	0.45 MAX.	0.018 MAX.
C	0.5 (T.P.)	0.020 (T.P.)
D	0.20±0.10	0.008±0.004
G	1.05	0.041
H	15.3±0.2	0.602 ^{+0.009} _{-0.008}
I	13.7	0.539
J	0.8±0.2	0.031 ^{+0.009} _{-0.008}
K	0.125 ^{+0.10} _{-0.05}	0.005 ^{+0.004} _{-0.002}
L	0.5±0.1	0.020 ^{+0.004} _{-0.005}
M	0.08	0.003
N	0.10	0.004
P	14.3±0.2	0.563±0.008
Q	0.05±0.05	0.002±0.002
S	1.27 MAX.	0.050 MAX.

Recommended Soldering Conditions

The following conditions (See tables below and next page) must be met when soldering μ PD43256B. For more details, refer to our document "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

Types of Surface Mount Device

μ PD43256BGU: 28-pin plastic SOP (450 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 230 °C or below, Reflow time: 30 seconds or below (210 °C or higher), Number or reflow processes: 1 Exposure limit ^{Note} : 7 days (10 hours pre-baking is required at 125 °C afterwards)	IR30-107-1
VPS	Peak package's temperature: 215 °C or below, Reflow time: 40 seconds or below (200 °C or higher), Number of reflow processes: 1 Exposure limit ^{Note} : 7 days (10 hours pre-baking is required at 125 °C afterwards)	VP15-107-1
Wave soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or below, Temperature of pre-heat: 120 °C or below (Plastic surface temperature) Number of reflow processes: 1 Exposure limit ^{Note} : 7 days (10 hours pre-baking is required at 125 °C afterwards)	WS60-107-1
Partial heating method	Terminal temperature: 300 °C or below, Time: 3 seconds or below (Per side of leads)	—

Note Exposure limit before soldering after dry-pack package is opened.

Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method."

μ PD43256BGX-EJA: 32-pin plastic TSOP (I) (600 mil) (Normal bent)

μ PD43256BGX-EKA: 32-pin plastic TSOP (I) (600 mil) (Reverse bent)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 235 °C or below, Reflow time: 30 seconds or below (210 °C or higher), Number or reflow processes: 1 Exposure limit ^{Note} : 8 hours (10 hours pre-baking is required at 125 °C afterwards)	IR35-10B-1
VPS	Peak package's temperature: 215 °C or below, Reflow time: 40 seconds or below (200 °C or higher), Number of reflow processes: 1 Exposure limit ^{Note} : 8 hours (10 hours pre-baking is required at 125 °C afterwards)	VP15-10B-1
Partial heating method	Terminal temperature: 300 °C or below, Time: 3 seconds or below (Per side of leads)	—

Note Exposure limit before soldering after dry-pack package is opened.

Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method."

Type of Through Hole Mount Device

μPD43256BCZ: 28-pin plastic DIP (600 mil)

Soldering process	Soldering conditions
Wave soldering (only to leads)	Solder temperature: 260 °C or below, Flow time: 10 seconds or below
Partial heating method	Terminal temperature: 300 °C or below, Time: 3 seconds or below (Per one lead)

Caution Do not jet molten solder on the surface of package.

Information

μPD43256B New Line Up

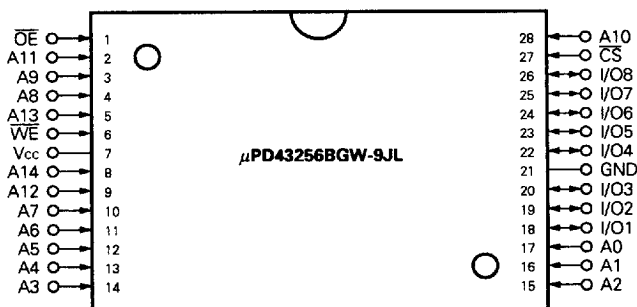
(1) Package : 28-pin plastic TSOP (I) (0.55pitch, 8 × 13.4 mm) (Normal, Reverse bent)

(2) Part Number : μPD43256BGW-70L/85L
 μPD43256BGW-70LL/85LL
 μPD43256BGW-A10/A12
 μPD43256BGW-B12

(3) Release : Ex-factory 1995. October

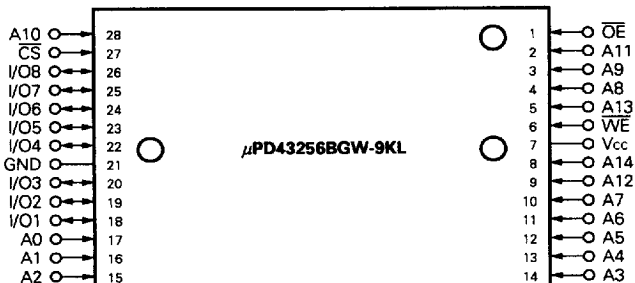
(4) Pin Configuration (Marking Side)

28-pin plastic TSOP (I) (Normal bent)



A0 to A14 : Address Input
 I/O1 to I/O8 : Data Input / Output
 CS : Chip Select Input
 WE : Write Enable Input
 OE : Output Enable Input
 Vcc : Power Supply
 GND : Ground

28-pin plastic TSOP (I) (Reverse bent)



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