

16M-bit Synchronous DRAM**Description**

The μ PD4516421A, 4516821A, 4516161A are high-speed 16,777,216-bit synchronous dynamic random-access memories, organized as $2,097,152 \times 4 \times 2$, $1,048,576 \times 8 \times 2$ and $524,288 \times 16 \times 2$ (word $\times$ bit $\times$ bank), respectively.

The synchronous DRAMs achieve high-speed data transfer using the pipeline architecture.

All inputs and outputs are synchronized with the positive edge of the clock.

The synchronous DRAMs are compatible with Low Voltage TTL (LVTTL).

The synchronous DRAMs are packaged in 44-pin TSOP (II) ($\times 4$, $\times 8$) and 50-pin TSOP (II) ($\times 16$).

Features

- Fully Synchronous Dynamic RAM, with all signals referenced to a positive clock edge
- Pulsed interface
- Possible to assert random column address in every cycle
- Dual internal banks controlled by A11 (Bank Select)
- Programmable burst-length (1, 2, 4, 8, Full Page)
- Programmable wrap sequence (Sequential/Interleave)
- Programmable $\overline{\text{CAS}}$ latency (2, 3)
- Automatic precharge and controlled precharge
- CBR (Auto) refresh and self refresh
- $\times 4$, $\times 8$, $\times 16$ organization
- Single + 3.3 $\pm$ 0.3 V power supply
- LVTTL compatible
- Byte control ($\times 16$) by LDQM and UDQM
- 2,048 refresh cycles/32 ms
- Burst termination by Burst Stop command and Precharge command

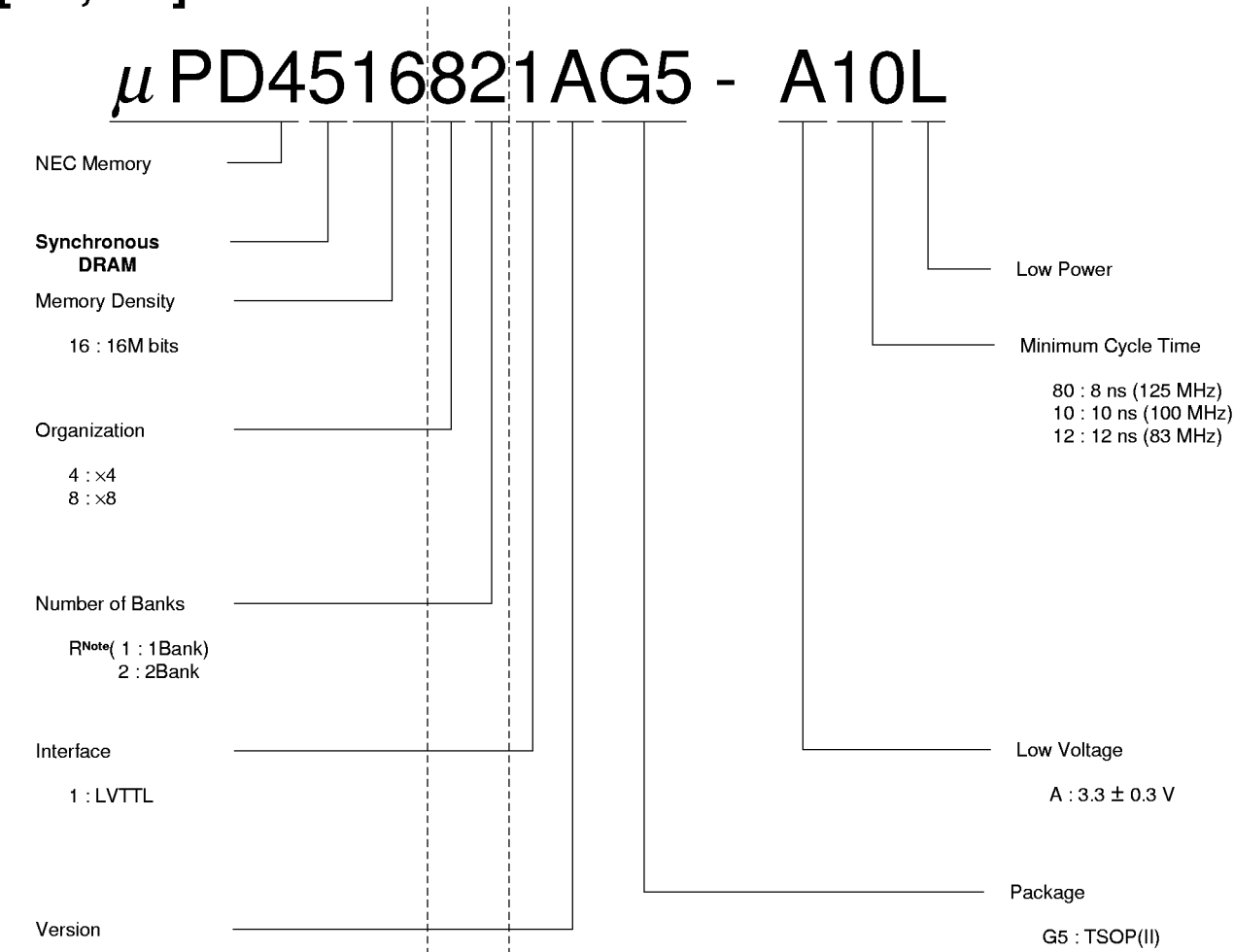
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★ Ordering Information

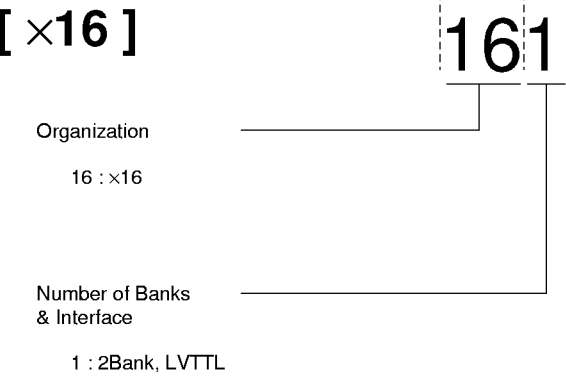
Part number	Organization (word × bit × bank)	Clock frequency MHz (MAX.)	Package
μ PD4516421AG5-A80-7JF	2 M × 4 × 2	125	44-pin Plastic TSOP(II) (400 mil)
μ PD4516421AG5-A10-7JF		100	
μ PD4516421AG5-A12-7JF		83	
μ PD4516821AG5-A80-7JF	1 M × 8 × 2	125	44-pin Plastic TSOP(II) (400 mil)
μ PD4516821AG5-A10-7JF		100	
μ PD4516821AG5-A12-7JF		83	
μ PD4516161AG5-A80-9NF	512 K × 16 × 2	125	50-pin Plastic TSOP(II) (400 mil)
μ PD4516161AG5-A10-9NF		100	
μ PD4516161AG5-A12-9NF		83	
μ PD4516421AG5-A80L-7JF	2 M × 4 × 2	125	44-pin Plastic TSOP(II) (400 mil)
μ PD4516421AG5-A10L-7JF		100	
μ PD4516421AG5-A12L-7JF		83	
μ PD4516821AG5-A80L-7JF	1 M × 8 × 2	125	44-pin Plastic TSOP(II) (400 mil)
μ PD4516821AG5-A10L-7JF		100	
μ PD4516821AG5-A12L-7JF		83	
μ PD4516161AG5-A80L-9NF	512 K × 16 × 2	125	50-pin Plastic TSOP(II) (400 mil)
μ PD4516161AG5-A10L-9NF		100	
μ PD4516161AG5-A12L-9NF		83	

Part Number

[×4, ×8]



[×16]

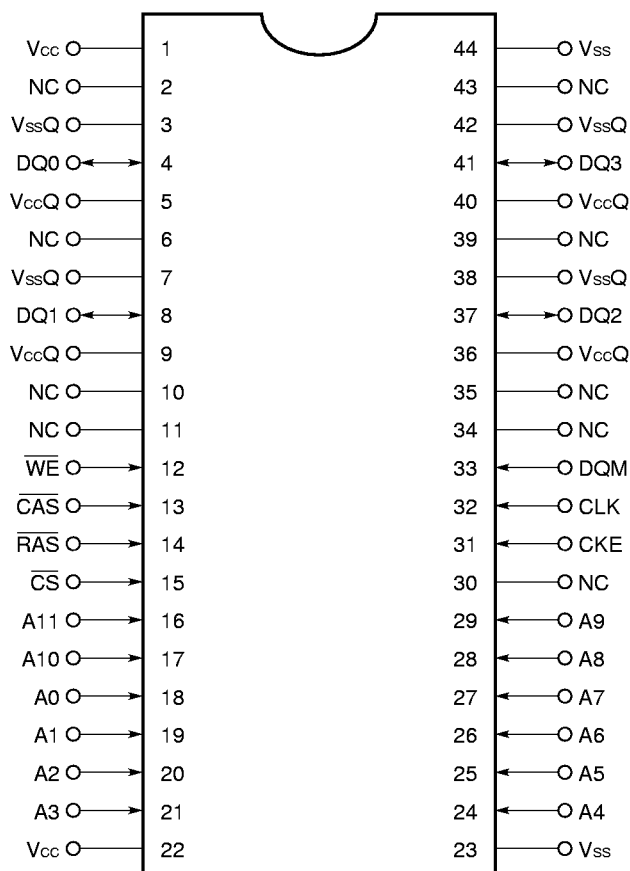


Note R: Reserved

Pin Configurations

[μ PD4516421A]

44-pin Plastic TSOP(II) (400 mil)

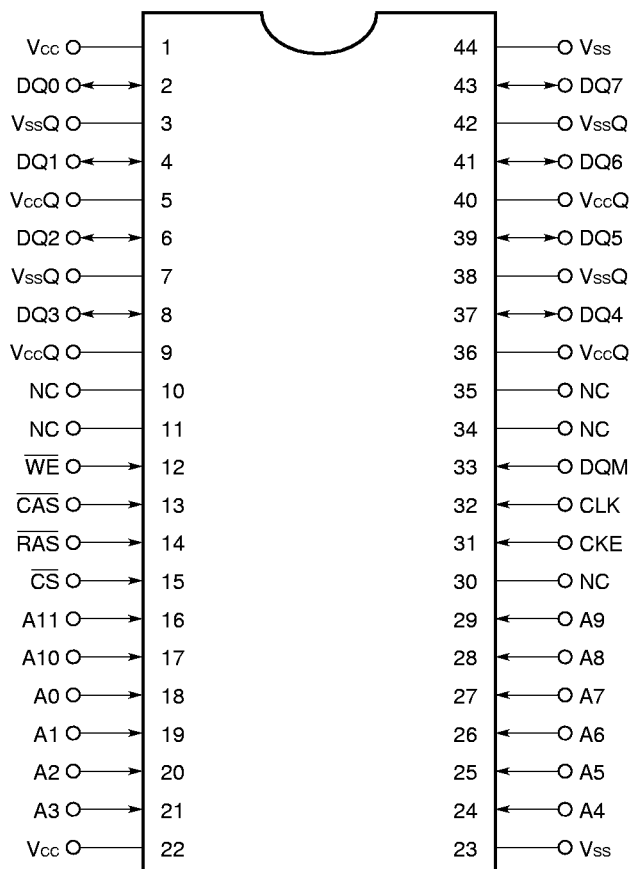
 μ PD4516421AG5-7JF

Note : Address inputs
 DQ0 to DQ3 : Data inputs/outputs
 CLK : System clock input
 CKE : Clock enable
 $\overline{CS}$: Chip select
 $\overline{RAS}$: Row address strobe
 $\overline{CAS}$: Column address strobe
 $\overline{WE}$: Write enable
 DQM : DQ mask enable
 Vcc : Supply voltage
 Vss : Ground
 VccQ : Supply voltage for DQ
 VssQ : Ground for DQ
 NC : No connection

Note A0 to A10: Row address inputs
 A0 to A9 : Column address inputs
 A11 : Bank select

[μ PD4516821A]

44-pin Plastic TSOP(II) (400 mil)

 μ PD4516821AG5-7JFA0 to A11 **Note**: Address inputs

DQ0 to DQ7 : Data inputs/outputs

CLK : System clock input

CKE : Clock enable

 $\overline{CS}$: Chip select $\overline{RAS}$: Row address strobe $\overline{CAS}$: Column address strobe $\overline{WE}$: Write enable

DQM : DQ mask enable

Vcc : Supply voltage

Vss : Ground

VccQ : Supply voltage for DQ

VssQ : Ground for DQ

NC : No connection

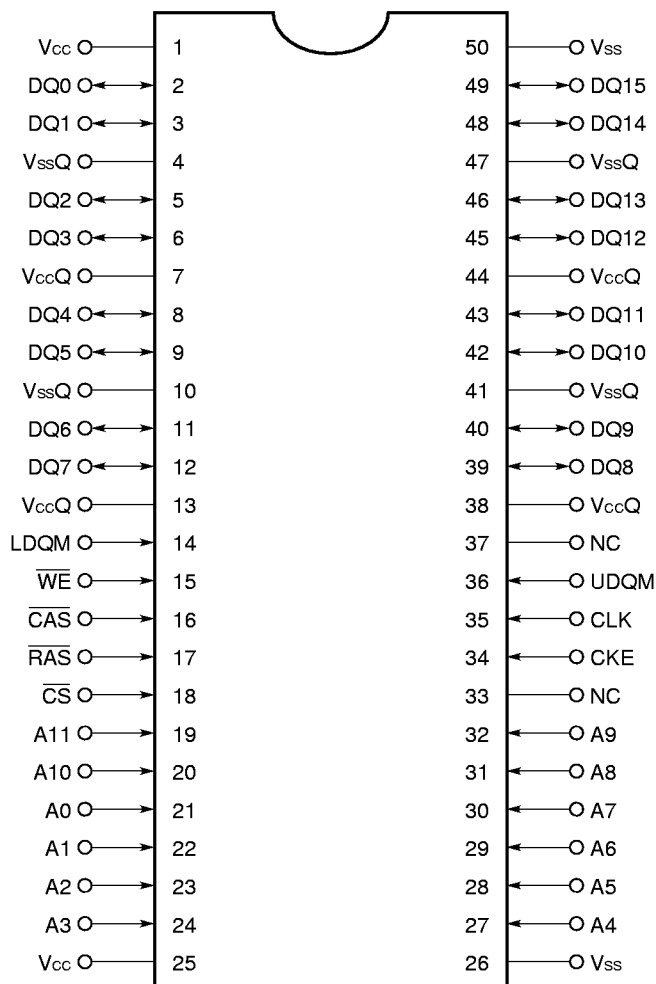
Note A0 to A10: Row address inputs

A0 to A8 : Column address inputs

A11 : Bank select

[μ PD4516161A]

50-pin Plastic TSOP(II) (400 mil)

 μ PD4516161AG5-9NFA0 to A11 **Note**: Address inputs

DQ0 to DQ15 : Data inputs/outputs

CLK : System clock input

CKE : Clock enable

 $\overline{CS}$: Chip select $\overline{RAS}$: Row address strobe $\overline{CAS}$: Column address strobe $\overline{WE}$: Write enable

UDQM : Upper DQ mask enable

LDQM : Lower DQ mask enable

Vcc : Supply voltage

Vss : Ground

VccQ : Supply voltage for DQ

VssQ : Ground for DQ

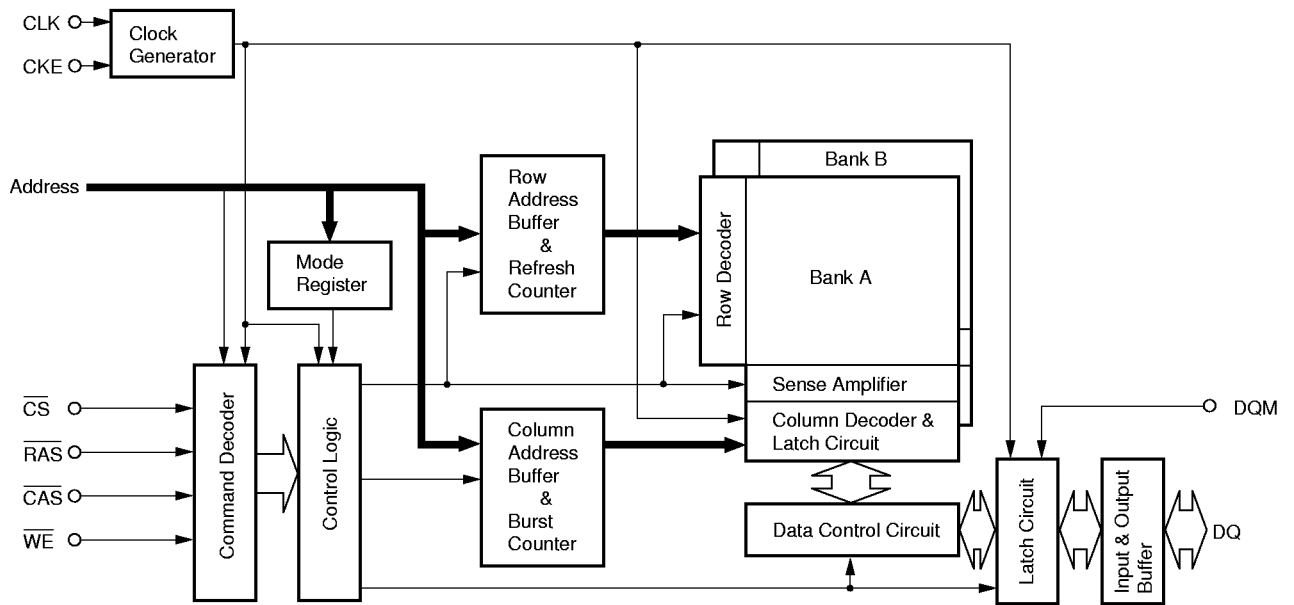
NC : No connection

Note A0 to A10: Row address inputs

A0 to A7 : Column address inputs

A11 : Bank select

Block Diagram



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1. Input/Output Pin Function

Pin name	Input/Output	Function
CLK	Input	CLK is the master clock input. Other inputs signals are referenced to the CLK rising edge.
CKE	Input	CKE determine validity of the next CLK (clock). If CKE is high, the next CLK rising edge is valid; otherwise it is invalid. If the CLK rising edge is invalid, the internal clock is not issued and the μ PD4516xxxA suspends operation. When the μ PD4516xxxA is not in burst mode and CKE is negated, the device enters power down mode. During power down mode, CKE must remain low.
$\overline{\text{CS}}$	Input	$\overline{\text{CS}}$ low starts the command input cycle. When $\overline{\text{CS}}$ is high, commands are ignored but operations continue.
$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$	Input	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ have the same symbols on conventional DRAM but different functions. For details, refer to the command table.
A0 - A11	Input	Row Address is determined by A0 - A10 at the CLK (clock) rising edge in the activate command cycle. It does not depend on the bit organization. Column Address is determined by A0 - A9 at the CLK rising edge in the read or write command cycle. It depends on the bit organization: A0 - A9 for $\times 4$ device, A0 - A8 for $\times 8$ device and A0 - A7 for $\times 16$ device. A11 is the bank select signal (BS). In command cycle, A11 low selects bank A and A11 high selects bank B. A10 defines the precharge mode. When A10 is high in the precharge command cycle, both banks are precharged; when A10 is low, only the bank selected by A11 is precharged. When A10 high in read or write command cycle, the precharge start automatically after the burst access.
DQM UDQM LDQM	Input	DQM controls I/O buffers. In $\times 16$ products, UDQM and LDQM control upper byte and lower byte I/O buffers, respectively. In read mode, DQM controls the output buffers like a conventional $\overline{\text{OE}}$ pin. DQM high and DQM low turn the output buffers off and on, respectively. The DQM latency for the read is two clocks. In write mode, DQM controls the word mask. Input data is written to the memory cell if DQM is low but not if DQM is high. The DQM latency for the write is zero.
DQ0 - DQ15	Input/Output	DQ pins have the same function as I/O pins on a conventional DRAM.
V _{CC} V _{SS} V _{CCQ} V _{SSQ}	(Power supply)	V _{CC} and V _{SS} are power supply pins for internal circuits. V _{CCQ} and V _{SSQ} are power supply pins for the output buffers.

2. Commands

Mode register set command

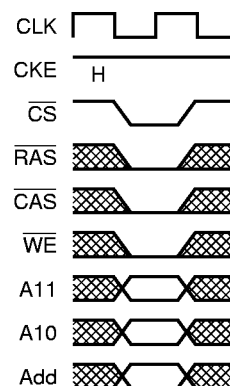
$$(\overline{\text{CS}}, \overline{\text{RAS}}, \overline{\text{CAS}}, \overline{\text{WE}} = \text{Low})$$

The μ PD4516xxxA has a mode register that defines how the device operates. In this command, A0 through A11 are the data input pins. After power on, the mode register set command must be executed to initialize the device.

The mode register can be set only when both banks are in idle state.

During 2CLK (t_{RSC}) following this command, the μ PD4516xxxA cannot accept any other commands.

Fig. 1 Mode register set command



Activate command

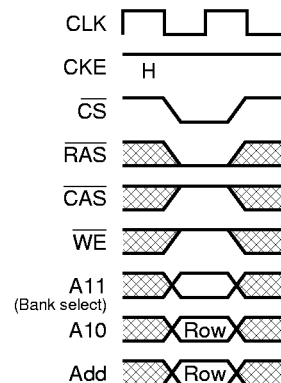
$$(\overline{\text{CS}}, \overline{\text{RAS}} = \text{Low}, \overline{\text{CAS}}, \overline{\text{WE}} = \text{High})$$

The μ PD4516xxxA has two banks, each with 2,048 rows.

This command activates the bank selected by A11 (BS) and a row address selected by A0 through A10.

This command corresponds to a conventional DRAM's $\overline{\text{RAS}}$ falling.

Fig. 2 Row address strobe and bank active command



Precharge command

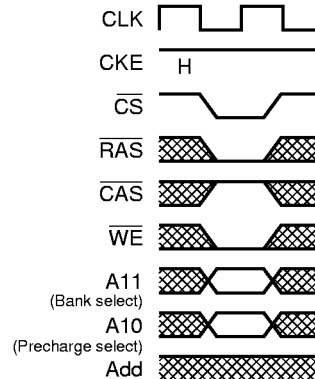
$$(\overline{\text{CS}}, \overline{\text{RAS}}, \overline{\text{WE}} = \text{Low}, \overline{\text{CAS}} = \text{High})$$

This command begins precharge operation of the bank selected by A11 (BS). When A10 is High, both banks are precharged, regardless of A11. When A10 is Low, only the bank selected by A11 is precharged. A11 low selects bank A and A11 high selects bank B.

After this command, the μ PD4516xxxA can't accept the activate command to the precharging bank during t_{RP} (precharge to activate command period).

This command corresponds to a conventional DRAM's $\overline{\text{RAS}}$ rising.

Fig. 3 Precharge command

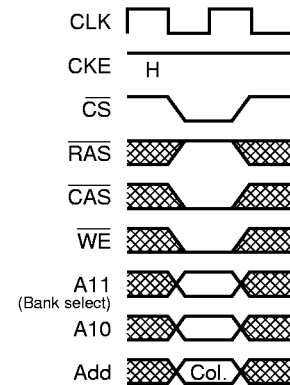


Write command

$$(\overline{\text{CS}}, \overline{\text{CAS}}, \overline{\text{WE}} = \text{Low}, \overline{\text{RAS}} = \text{High})$$

If the mode register is in the burst write mode, this command sets the burst start address given by the column address to begin the burst write operation. The first write data in burst can be input with this command with subsequent data on following clocks.

Fig. 4 Column address and write command

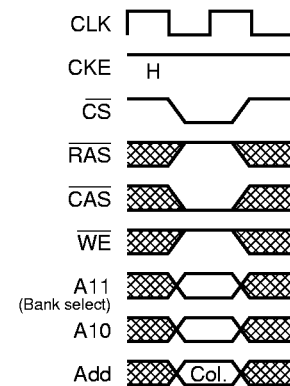


Read command

$$(\overline{\text{CS}}, \overline{\text{CAS}} = \text{Low}, \overline{\text{RAS}}, \overline{\text{WE}} = \text{High})$$

Read data is available after $\overline{\text{CAS}}$ latency requirements have been met. This command sets the burst start address given by the column address.

Fig. 5 Column address and read command



CBR (auto) refresh command

$$(\overline{\text{CS}}, \overline{\text{RAS}}, \overline{\text{CAS}} = \text{Low}, \overline{\text{WE}}, \text{CKE} = \text{High})$$

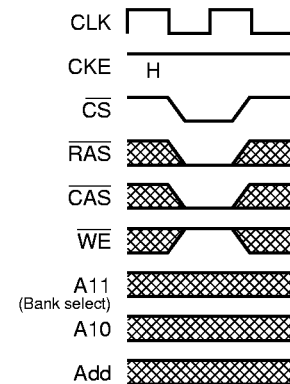
This command is a request to begin the CBR refresh operation. The refresh address is generated internally.

Before executing CBR refresh, both banks must be precharged.

After this cycle, both banks will be in the idle (precharged) state and ready for a row activate command.

During t_{RC} period (from refresh command to refresh or activate command), the μPD4516xxxA cannot accept any other command.

Fig. 6 Auto refresh command



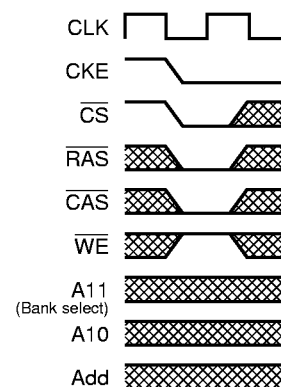
Self refresh entry command

$$(\overline{\text{CS}}, \overline{\text{RAS}}, \overline{\text{CAS}}, \text{CKE} = \text{Low}, \overline{\text{WE}} = \text{High})$$

After the command execution, self refresh operation continues while CKE remains low. When CKE goes to high, the μ PD4516xxxA exits the self refresh mode.

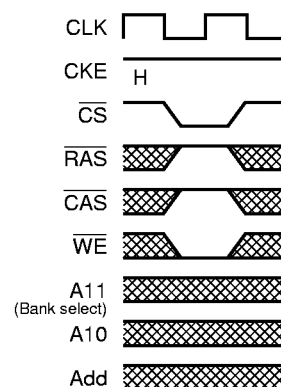
During self refresh mode, refresh interval and refresh operation are performed internally, so there is no need for external control.

Before executing self refresh, both banks must be precharged.

Fig. 7 Self refresh entry command**Burst stop command**

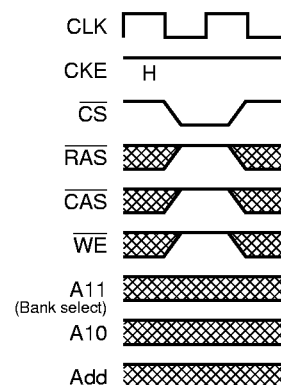
$$(\overline{\text{CS}}, \overline{\text{WE}} = \text{Low}, \overline{\text{RAS}}, \overline{\text{CAS}} = \text{High})$$

This command terminates the current burst operation.

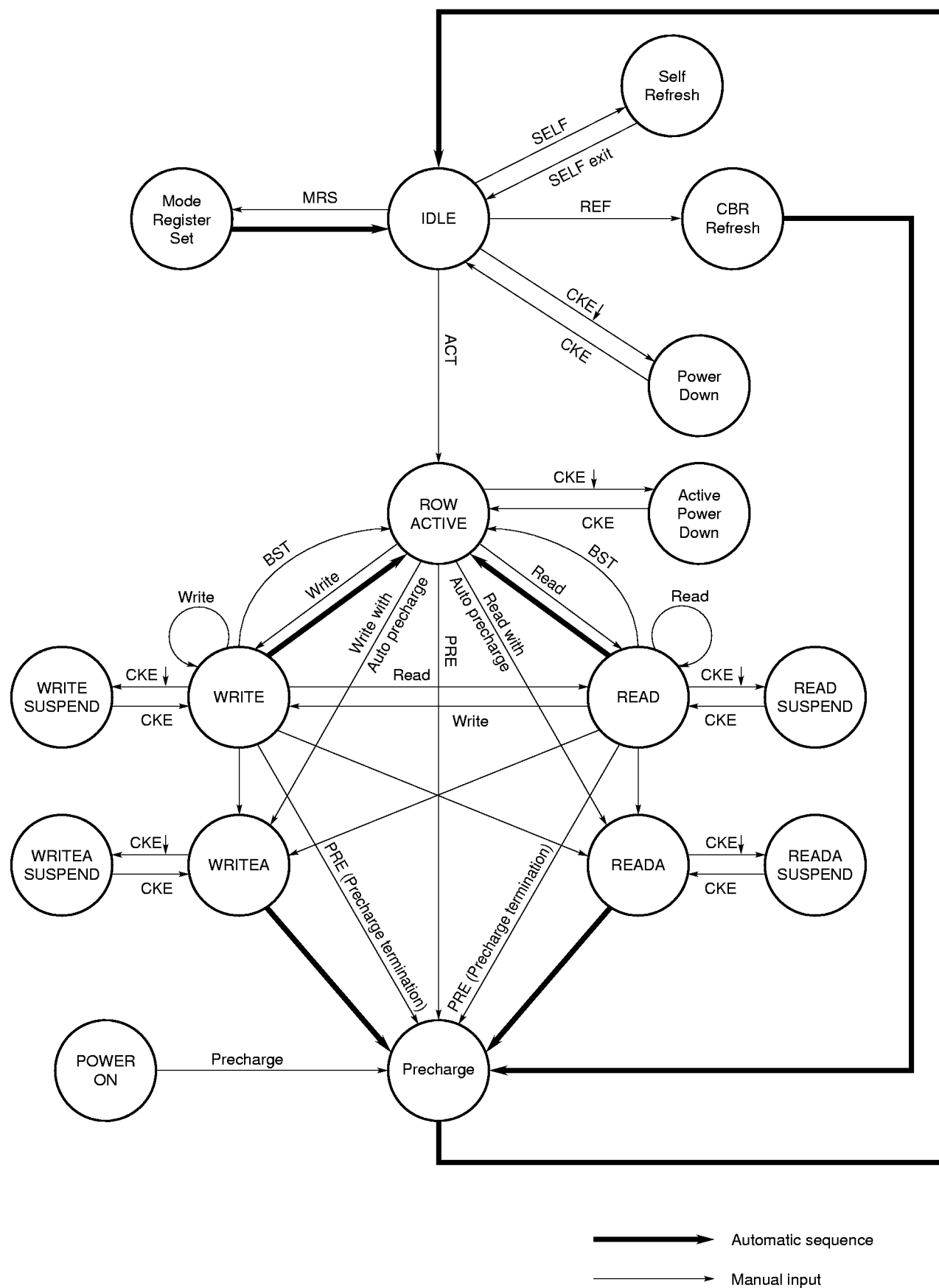
Fig. 8 Burst stop command in Full Page mode**No operation**

$$(\overline{\text{CS}} = \text{Low}, \overline{\text{RAS}}, \overline{\text{CAS}}, \overline{\text{WE}} = \text{High})$$

This command is not a execution command. No operations begin or terminate by this command.

Fig. 9 No operation

3. Simplified State Diagram



4. Truth Table

4.1 Command Truth Table

Function	Symbol	CKE		$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	A11	A10	A9-A0
		n-1	n							
Device deselect	DESL	H	x	H	x	x	x	x	x	x
No operation	NOP	H	x	L	H	H	H	x	x	x
Burst stop	BST	H	x	L	H	H	L	x	x	x
Read	READ	H	x	L	H	L	H	V	L	V
Read with auto precharge	READA	H	x	L	H	L	H	V	H	V
Write	WRIT	H	x	L	H	L	L	V	L	V
Write with auto precharge	WRITA	H	x	L	H	L	L	V	H	V
Bank activate	ACT	H	x	L	L	H	H	V	V	V
Precharge select bank	PRE	H	x	L	L	H	L	V	L	x
Precharge all banks	PALL	H	x	L	L	H	L	x	H	x
Mode register set	MRS	H	x	L	L	L	L	L	L	V

4.2 DQM Truth Table

Function	Symbol	CKE		DQM	
		n-1	n	U	L
Data write/output enable	ENB	H	x	L	
Data mask/output disable	MASK	H	x	H	
Upper byte write enable/output enable	ENBU	H	x	L	x
Lower byte write enable/output enable	ENBL	H	x	x	L
Upper byte write inhibit/output disable	MASKU	H	x	H	x
Lower byte write inhibit/output disable	MASKL	H	x	x	H

4.3 CKE Truth Table

Current state	Function	Symbol	CKE		$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	Add-ress
			n-1	n					
Activating	Clock suspend mode entry		H	L	x	x	x	x	x
Any	Clock suspend		L	L	x	x	x	x	x
Clock suspend	Clock suspend mode exit		L	H	x	x	x	x	x
Idle	CBR refresh command	REF	H	H	L	L	L	H	x
Idle	Self refresh entry	SELF	H	L	L	L	L	H	x
Self refresh	Self refresh exit		L	H	L	H	H	H	x
			L	H	H	x	x	x	x
Idle	Power down entry		H	L	x	x	x	x	x
Power down	Power down exit		L	H	x	x	x	x	x

H: High level, L: Low level

x: High or Low level (Don't care), V: Valid Data input

4.4 Operative Command Table^{Notes1, 2}

(1/3)

Current state	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	Address	Command	Action	Notes
Idle	H	×	×	×	×	DESL	Nop or Power down	3
	L	H	H	×	×	NOP or BST	Nop or Power down	3
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	4
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	4
	L	L	H	H	BA, RA	ACT	Row activating	
	L	L	H	L	BA, A10	PRE/PALL	Nop	
	L	L	L	H	×	REF/SELF	Refresh or Self refresh	5
	L	L	L	L	Op-Code	MRS	Mode register accessing	
Row active	H	×	×	×	×	DESL	Nop	
	L	H	H	×	×	NOP or BST	Nop	
	L	H	L	H	BA, CA, A10	READ/READA	Begin read:Determine AP	6
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Begin write:Determine AP	6
	L	L	H	H	BA, RA	ACT	ILLEGAL	4
	L	L	H	L	BA, A10	PRE/PALL	Precharge	7
	L	L	L	H	×	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Read	H	×	×	×	×	DESL	Continue burst to end → Row active	
	L	H	H	H	×	NOP	Continue burst to end → Row active	
	L	H	H	L	×	BST	Burst stop → Row active	
	L	H	L	H	BA, CA, A10	READ/READA	Term burst, new read:Determine AP	8
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Term burst, start write:Determine AP	8, 9
	L	L	H	H	BA, RA	ACT	ILLEGAL	4
	L	L	H	L	BA, A10	PRE/PALL	Term burst, precharging	
	L	L	L	H	×	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Write	H	×	×	×	×	DESL	Continue burst to end → Write recovering	
	L	H	H	H	×	NOP	Continue burst to end → Write recovering	
	L	H	H	L	×	BST	Burst stop → Row active	
	L	H	L	H	BA, CA, A10	READ/READA	Term burst, start read:Determine AP	8, 9
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Term burst, new write:Determine AP	8
	L	L	H	H	BA, RA	ACT	ILLEGAL	4
	L	L	H	L	BA, A10	PRE/PALL	Term burst, precharging	10
	L	L	L	H	×	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	

(2/3)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action	Notes
Read with auto precharge	H	x	x	x	x	DESL	Continue burst to end → Precharging	
	L	H	H	H	x	NOP	Continue burst to end → Precharging	
	L	H	H	L	x	BST	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	
	L	L	H	H	BA, RA	ACT	ILLEGAL	4
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	4
	L	L	L	H	x	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Write with auto precharge	H	x	x	x	x	DESL	Continue burst to end → Write recovering with auto precharge	
	L	H	H	H	x	NOP	Continue burst to end → Write recovering with auto precharge	
	L	H	H	L	x	BST	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	
	L	L	H	H	BA, RA	ACT	ILLEGAL	4
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	4
	L	L	L	H	x	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Precharging	H	x	x	x	x	DESL	Nop → Enter idle after t_{RP}	
	L	H	H	H	x	NOP	Nop → Enter idle after t_{RP}	
	L	H	H	L	x	BST	Nop → Enter idle after t_{RP}	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	4
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	4
	L	L	H	H	BA, RA	ACT	ILLEGAL	4
	L	L	H	L	BA, A10	PRE/PALL	Nop → Enter idle after t_{RP}	
	L	L	L	H	x	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Row activating	H	x	x	x	x	DESL	Nop → Enter row active after t_{RCO}	
	L	H	H	H	x	NOP	Nop → Enter row active after t_{RCO}	
	L	H	H	L	x	BST	Nop → Enter row active after t_{RCO}	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	4
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	4
	L	L	H	H	BA, RA	ACT	ILLEGAL	4, 11
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	4
	L	L	L	H	x	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	

(3/3)

Current state	CS	RAS	CAS	WE	Address	Command	Action	Notes
Write recovering	H	×	×	×	×	DESL	Nop → Enter row active after t _{DPL}	
	L	H	H	H	×	NOP	Nop → Enter row active after t _{DPL}	
	L	H	H	L	×	BST	Nop → Enter row active after t _{DPL}	
	L	H	L	H	BA, CA, A10	READ/READA	Start read, Determine AP	9
	L	H	L	L	BA, CA, A10	WRIT/WRITA	New write, Determine AP	
	L	L	H	H	BA, RA	ACT	ILLEGAL	4
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	4
	L	L	L	H	×	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Write recovering with auto precharge	H	×	×	×	×	DESL	Nop → Enter precharge after t _{DPL}	
	L	H	H	H	×	NOP	Nop → Enter precharge after t _{DPL}	
	L	H	H	L	×	BST	Nop → Enter precharge after t _{DPL}	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	4, 9
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	4
	L	L	H	H	BA, RA	ACT	ILLEGAL	4
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	4
	L	L	L	H	×	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Refreshing	H	×	×	×	×	DESL	Nop → Enter idle after t _{RC}	
	L	H	H	×	×	NOP/BST	Nop → Enter idle after t _{RC}	
	L	H	L	×	×	READ/WRIT	ILLEGAL	
	L	L	H	×	×	ACT/PRE/PALL	ILLEGAL	
	L	L	L	×	×	REF/SELF/MRS	ILLEGAL	
Mode register accessing	H	×	×	×	×	DESL	Nop → Enter idle after t _{RSC}	
	L	H	H	H	×	NOP	Nop → Enter idle after t _{RSC}	
	L	H	H	L	×	BST	ILLEGAL	
	L	H	L	×	×	READ/WRITE	ILLEGAL	
	L	L	×	×	×	ACT/PRE/PALL/REF/SELF/MRS	ILLEGAL	

- Notes**
1. H: High level, L: Low level, ×: High or Low level (Don't care), V: Valid data input
 2. All entries assume that CKE was active (High level) during the preceding clock cycle.
 3. If both banks are idle, and CKE is inactive (Low level), μPD4516×××A will enter Power down mode. All input buffers except CKE will be disabled.
 4. Illegal to bank in specified states; Function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.
 5. If both banks are idle, and CKE is inactive (Low level), μPD4516×××A will enter Self refresh mode. All input buffers except CKE will be disabled.
 6. Illegal if t_{RCD} is not satisfied.
 7. Illegal if t_{RAS} is not satisfied.
 8. Must satisfy burst interrupt condition.
 9. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
 10. Must mask preceding data which don't satisfy t_{DPL}.
 11. Illegal if t_{RRD} is not satisfied.

4.5 Command Truth Table for CKE^{Note 1}

Current state	CKE _{n-1}	CKE _n	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	Address	Action	Notes
Self refresh (S.R.)	H	x	x	x	x	x	x	INVALID, CLK(n-1) would exit S.R.	
	L	H	H	x	x	x	x	S.R. Recovery	
	L	H	L	H	H	x	x	S.R. Recovery	
	L	H	L	H	L	x	x	ILLEGAL	
	L	H	L	L	x	x	x	ILLEGAL	
	L	L	x	x	x	x	x	Maintain S.R.	
Self refresh recovery	H	H	H	x	x	x	x	Idle after t _{RC}	
	H	H	L	H	H	x	x	Idle after t _{RC}	
	H	H	L	H	L	x	x	ILLEGAL	
	H	H	L	L	x	x	x	ILLEGAL	
	H	L	H	x	x	x	x	ILLEGAL	
	H	L	L	H	H	x	x	ILLEGAL	
	H	L	L	H	L	x	x	ILLEGAL	
	H	L	L	L	x	x	x	ILLEGAL	
Power down (P.D.)	H	x	x	x	x	x		INVALID, CLK(n-1) would exit P.D.	
	L	H	x	x	x	x	x	EXIT P.D. → Idle	
	L	L	x	x	x	x	x	Maintain power down mode	
Both banks idle	H	H	H	x	x	x		Refer to operations in Operative Command Table	
	H	H	L	H	x	x		Refer to operations in Operative Command Table	
	H	H	L	L	H	x		Refer to operations in Operative Command Table	
	H	H	L	L	L	H	x	Refresh	
	H	H	L	L	L	L	Op-Code	Refer to operations in Operative Command Table	
	H	L	H	x	x	x		Refer to operations in Operative Command Table	
	H	L	L	H	x	x		Refer to operations in Operative Command Table	
	H	L	L	L	H	x		Refer to operations in Operative Command Table	
	H	L	L	L	L	H	x	Self refresh	2
	H	L	L	L	L	L	Op-Code	Refer to operations in Operative Command Table	
	L	x	x	x	x	x	x	Power down	2
Row active	H	x	x	x	x	x		Refer to operations in Operative Command Table	
	L	x	x	x	x	x		Power down	3
Any state other than listed above	H	H	x	x	x	x	x	Refer to operations in Operative Command Table	
	H	L	x	x	x	x	x	Begin clock suspend next cycle	3
	L	H	x	x	x	x	x	Exit clock suspend next cycle	
	L	L	x	x	x	x	x	Maintain clock suspend	

Notes 1. H: High level, L: Low level, X: High or low level (Don't care)

2. Self refresh can be entered only from the both banks idle state. Power down can be entered from the both banks idle state or row active state.
3. Must be legal command as defined in Operative Command Table.

4.6 Command Truth Table for Two Banks Operation Notes 1, 2

$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	BA	A10	A9 - A0	Action	"FROM" State Note 3	"TO" State Note 4
H	x	x	x	x	x	x	NOP	Any	Any
L	H	H	H	x	x	x	NOP	Any	Any
L	H	H	L	x	x	x	BST	(R/W/A)0(I/A)1	A0(I/A)1
								I0(I/A)1	I0(I/A)1
								(R/W/A)1(I/A)0	A1(I/A)0
								I1(I/A)0	I1(I/A)0
L	H	L	H	H	H	CA	Read	(R/W/A)1(I/A)0	RP1(I/A)0
				H	H	CA		A1(R/W)0	RP1A0
				H	L	CA		(R/W/A)1(I/A)0	R1(I/A)0
				H	L	CA		A1(R/W)0	R1A0
				L	H	CA		(R/W/A)0(I/A)1	RP0(I/A)1
				L	H	CA		A0(R/W)1	RP0A1
				L	L	CA		(R/W/A)0(I/A)1	R0(I/A)1
				L	L	CA		A0(R/W)1	R0A1
L	H	L	L	H	H	CA	Write	(R/W/A)1(I/A)0	WP1(I/A)0
				H	H	CA		A1(R/W)0	WP1A0
				H	L	CA		(R/W/A)1(I/A)0	W1(I/A)0
				H	L	CA		A1(R/W)0	W1A0
				L	H	CA		(R/W/A)0(I/A)1	WP0(I/A)1
				L	H	CA		A0(R/W)1	WP0A1
				L	L	CA		(R/W/A)0(I/A)1	W0(I/A)1
				L	L	CA		A0(R/W)1	W0A1
L	L	H	H	H	RA		Activate Row	I1Any0	A1Any0
				L	RA			I0Any1	A0Any1
L	L	H	L	x	H	x	Precharge	(R/W/A/I)0(I/A)1	I0I1
				x	H	x		(R/W/A/I)1(I/A)0	I1I0
				H	L	x		(R/W/A/I)1(I/A)0	I1(I/A)0
				H	L	x		(I/A)1(R/W/A/I)0	I1(R/W/A/I)0
				L	L	x		(R/W/A/I)0(I/A)1	I0(I/A)1
				L	L	x		(I/A)0(R/W/A/I)1	I0(R/W/A/I)1
L	L	L	H	x	x	x	Refresh	I0I1	I0I1
L	L	L	L	Op-Code			Mode Register Access	I0I1	I0I1

Notes 1. Logic level abbreviations

H: High level, L: Low level, x: High or low level (Don't care)

Pin name abbreviation

BA: Bank address (A11)

2. State abbreviations

I = Idle

A = Row active

R = Read with No precharge (No precharge is posted)

W = Write with No precharge (No precharge is posted)

RP = Read with auto precharge (Precharge is posted)

WP = Write with auto precharge (Precharge is posted)

Any = Any State

X0Y1 = Y1X0 = Bank A is in state "X", Bank B is in state "Y"

(X/Y)0Z1 = Z1(X/Y)0 = Bank A is in state "X" or "Y", Bank B is in state "Z"

3. If the μ PD4516 $\times\times\times$ A is in a state other than above listed in the "From State" column, the command is illegal.

4. The states listed under "To" might not be entered on the next clock cycle.

Timing restrictions apply.

5. Initialization

The synchronous DRAM is initialized in the power-on sequence according to the following.

- (1) To stabilize internal circuits, when power is applied, a 100- μ s or longer pause must precede any signal toggling.
- (2) After the pause, both banks must be precharged using the Precharge command (The Precharge all banks command is convenient).
- (3) Once the precharge is completed and the minimum t_{RP} is satisfied, the mode register can be programmed. After the mode register set cycle, t_{RSC} (2CLK minimum) pause must be satisfied as well.
- (4) Two or more CBR (Auto) refresh must be performed.

Remarks 1. The sequence of Mode register programming and Refresh above may be transposed.

2. CKE and DQM may be held high until the Precharge command is issued to ensure data bus Hi-Z.

6. Programming the Mode Register

The mode register is programmed by the Mode register set command using address bits A11 through A0 as data inputs. The register retains data until it is reprogrammed or the device loses power.

The mode register has four fields;

Options : A11 through A7

$\overline{\text{CAS}}$ latency: A6 through A4

Wrap type : A3

Burst length : A2 through A0

Following mode register programming, no command can be issued before at least 2CLK have elapsed.

$\overline{\text{CAS}}$ Latency

$\overline{\text{CAS}}$ latency is the most critical of the parameters being set. It tells the device how many clocks must elapse before the data will be available.

The value is determined by the frequency of the clock and the speed grade of the device. The table on page 43 shows the relationship of $\overline{\text{CAS}}$ latency to the clock period and the speed grade of the device.

Burst Length

Burst Length is the number of words that will be output or input in a read or write cycle. After a read burst is completed, the output bus will become Hi-Z.

The burst length is programmable as 1, 2, 4, 8 or full page.

Wrap Type (Burst Sequence)

The wrap type specifies the order in which the burst data will be addressed. This order is programmable as either "Sequential" or "Interleave". The method chosen will depend on the type of CPU in the system.

Some microprocessor cache system are optimized for sequential addressing and others for interleaved addressing. The table on the page 24 shows the addressing sequence for each burst length using them. Both sequences support bursts of 1, 2, 4 and 8. Additionally, sequential sequence supports the full page length.

7. Mode Register

11	10	9	8	7	6	5	4	3	2	1	0	
0	0	0	0	1								JEDEC Standard Test Set (refresh counter test)

11	10	9	8	7	6	5	4	3	2	1	0	
×	×	1	0	0	LTMODE		WT		BL			Burst Read and Single Write (for Write Through Cache)

11	10	9	8	7	6	5	4	3	2	1	0	
			1	0								Use in future

11	10	9	8	7	6	5	4	3	2	1	0	
×	×	×	1	1	V	V	V	V	V	V	V	Vender Specific

11	10	9	8	7	6	5	4	3	2	1	0	
0	0	0	0	0	LTMODE		WT		BL			Mode Register Set

V = Valid
× = Don't care

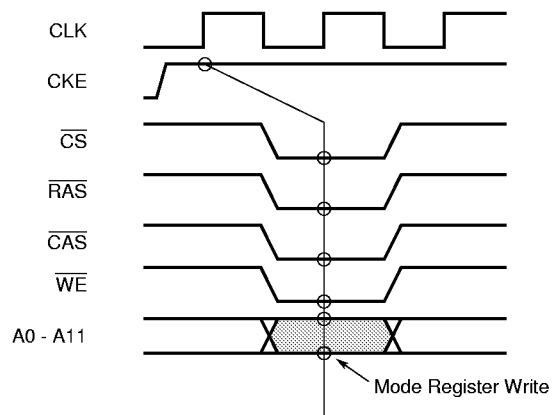
Burst length	Bits2-0	WT = 0	WT = 1
	000	1	1
	001	2	2
	010	4	4
	011	8	8
	100	R	R
	101	R	R
	110	R	R
	111	Full page	R

Wrap type	0	Sequential
	1	Interleave

Latency mode	Bits6-4	CAS latency
	000	R
	001	R
	010	2
	011	3
	100	R
	101	R
	110	R
	111	R

Remark R: Reserved

Mode Register Write Timing



7.1 Burst Length and Sequence

[Burst of Two]

Starting Address (column address A0, binary)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (decimal)
0	0, 1	0, 1
1	1, 0	1, 0

[Burst of Four]

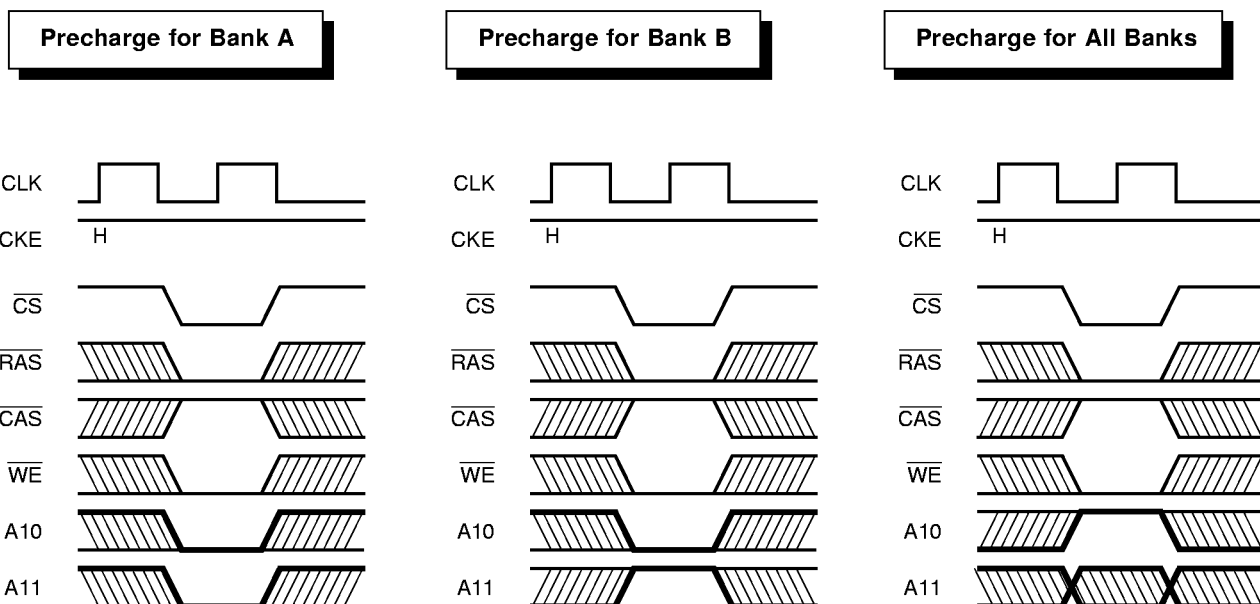
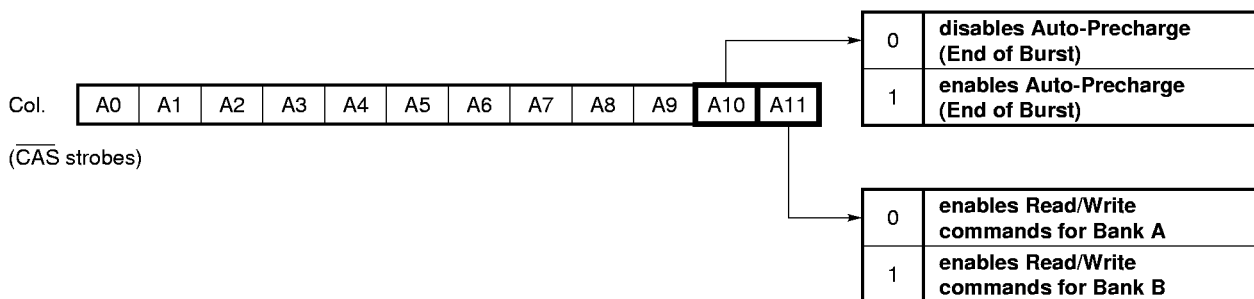
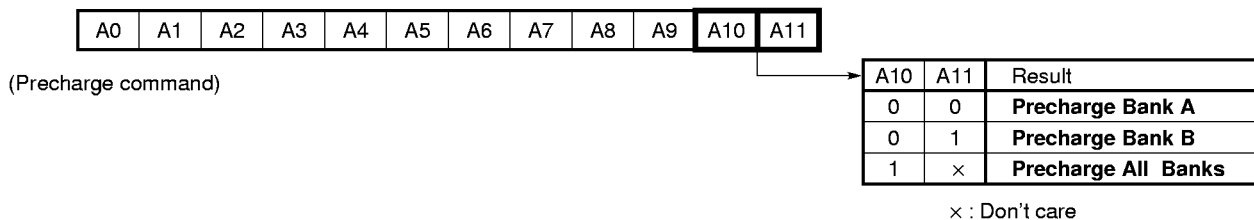
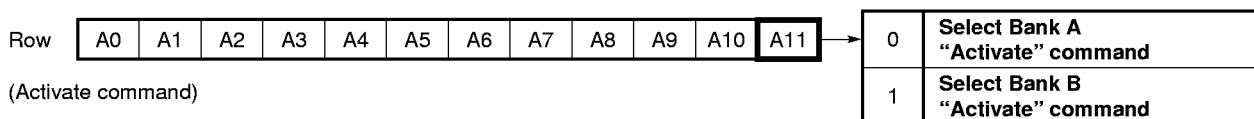
Starting Address (column address A1 - A0, binary)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (decimal)
00	0, 1, 2, 3	0, 1, 2, 3
01	1, 2, 3, 0	1, 0, 3, 2
10	2, 3, 0, 1	2, 3, 0, 1
11	3, 0, 1, 2	3, 2, 1, 0

[Burst of Eight]

Starting Address (column address A2 - A0, binary)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (decimal)
000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
001	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
010	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
011	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
101	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
110	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
111	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0

Full page burst is an extension of the above tables of Sequential Addressing, with the length being 512 (for 2 M $\times$ 8 device), 1,024 (for 4 M $\times$ 4 device) and 256 (for 1 M $\times$ 16 device).

8. Address Bits of Bank-Select and Precharge



9. Precharge

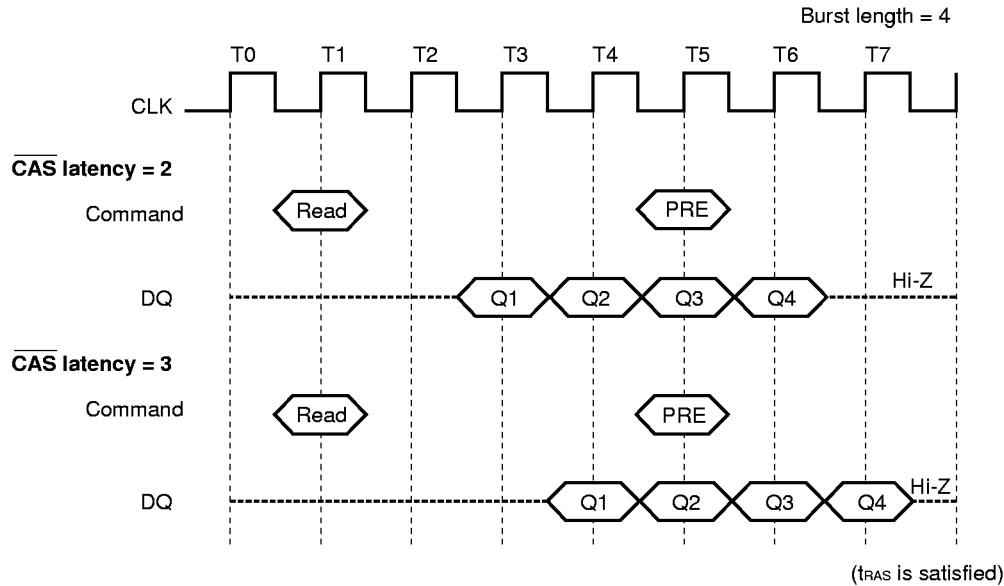
The precharge command can be issued anytime after $t_{RAS(MIN.)}$ is satisfied.

Soon after the precharge command is issued, precharge operation performed and the synchronous DRAM enters the idle state after t_{RP} is satisfied. The parameter t_{RP} is the time required to perform the precharge.

The earliest timing in a read cycle that a precharge command can be issued without losing any data in the burst is as follows.

$\overline{CAS}$ latency = 2: One clock earlier than the last read data.

$\overline{CAS}$ latency = 3: Two clocks earlier than the last read data.



In order to write all data to the memory cell correctly, the asynchronous parameter " t_{DPL} " must be satisfied. The $t_{DPL(MIN.)}$ specification defines the earliest time that a precharge command can be issued. Minimum number of clocks are calculated by dividing $t_{DPL(MIN.)}$ with clock cycle time.

In summary, the precharge command can be issued relative to reference clock that indicates the last data word is valid. In the following table, minus means clocks before the reference; plus means time after the reference.

$\overline{CAS}$ latency	Read	Write
2	-1	+ $t_{DPL(MIN.)}$
3	-2	+ $t_{DPL(MIN.)}$

10. Auto Precharge

During a read or write command cycle, A10 controls whether auto precharge is selected. A10 high in the Read or Write command (Read with Auto precharge command or Write with Auto precharge command), auto precharge is selected and precharge begins automatically.

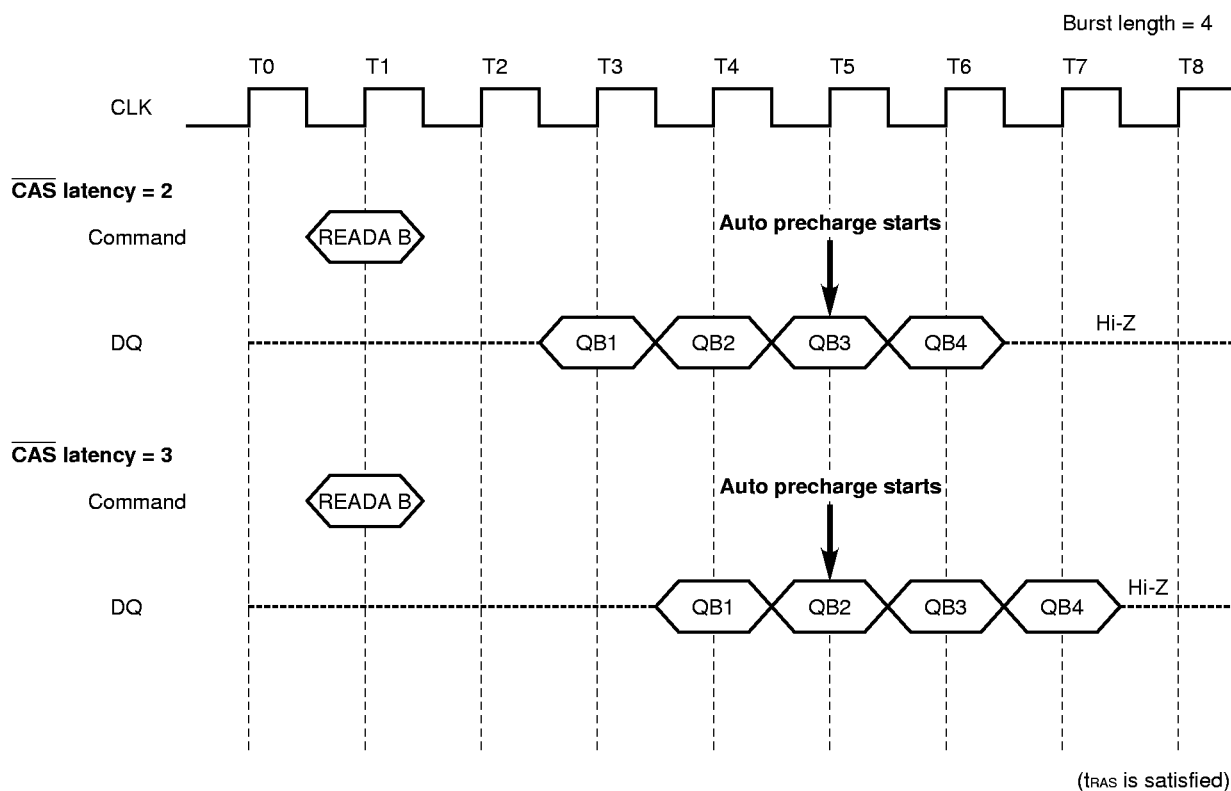
In write cycle, the t_{DAL} must be satisfied to issue the next activate command to the bank being precharged. It is not necessary to know when the precharge starts.

When using auto precharge in read cycle, knowing when the precharge starts is important because the t_{RAS} must be satisfied. In addition, the next activate command to the bank being precharged cannot be executed until the precharge cycle ends. Once auto precharge has started, an activate command to the bank can be issued after t_{RP} has been satisfied.

The timing that begins the auto precharge cycle depends on both the $\overline{CAS}$ latency programmed into the mode register and whether read or write cycle.

10.1 Read with Auto Precharge

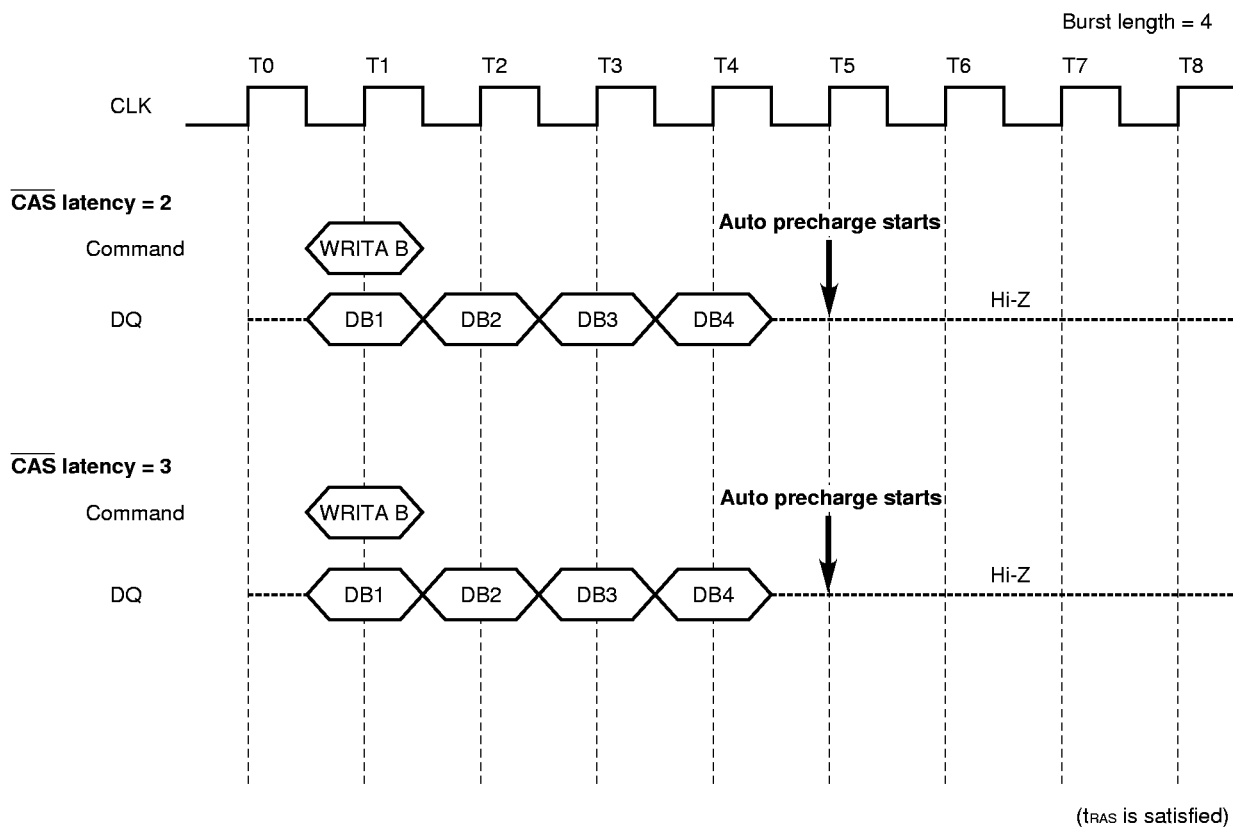
During a read cycle, the auto precharge begins one clock earlier ($\overline{CAS}$ latency of 2) or two clocks earlier ($\overline{CAS}$ latency of 3) the last data word output.



Remark READA means Read with Auto precharge

10.2 Write with Auto Precharge

During a write cycle, the auto precharge begins one clock after the last data word input to the device ($\overline{\text{CAS}}$ latency of 2 or 3).



Remark WRITA means Write with Auto precharge

In summary, the auto precharge cycle begins relative to a reference clock that indicates the last data word is valid. In the table below, minus means clocks before the reference; plus means clocks after the reference.

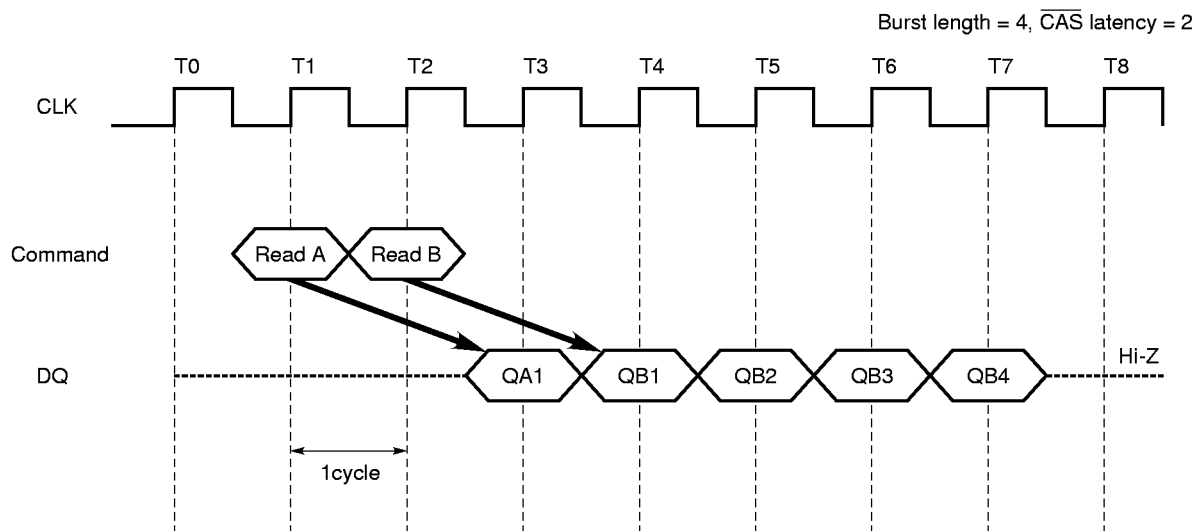
$\overline{\text{CAS}}$ latency	Read	Write
2	-1	+1
3	-2	+1

11. Read/Write Command Interval

11.1 Read to Read Command Interval

During a read cycle, when new Read command is issued, it will be effective after $\overline{\text{CAS}}$ latency, even if the previous read operation does not completed. READ will be interrupted by another READ.

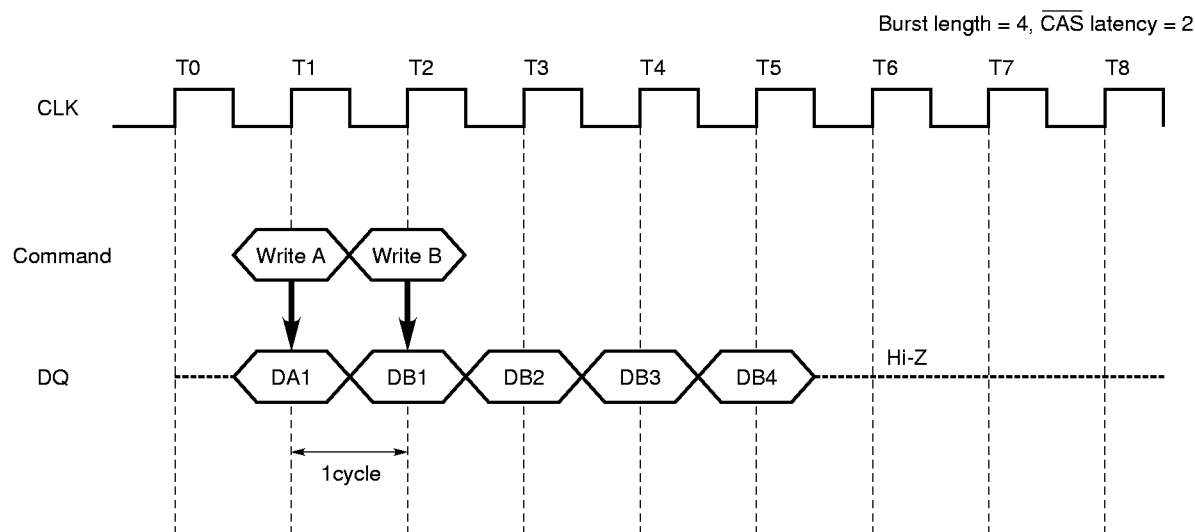
The interval between the commands is 1 cycle minimum. Each read command can be issued in every clock without any restriction.



11.2 Write to Write Command Interval

During a write cycle, when new Write command is issued, the previous burst will terminate and the new burst will begin with a new Write command. WRITE will be interrupted by another WRITE.

The interval between the commands is minimum 1. Each Write command can be issued in every clock without any restriction.

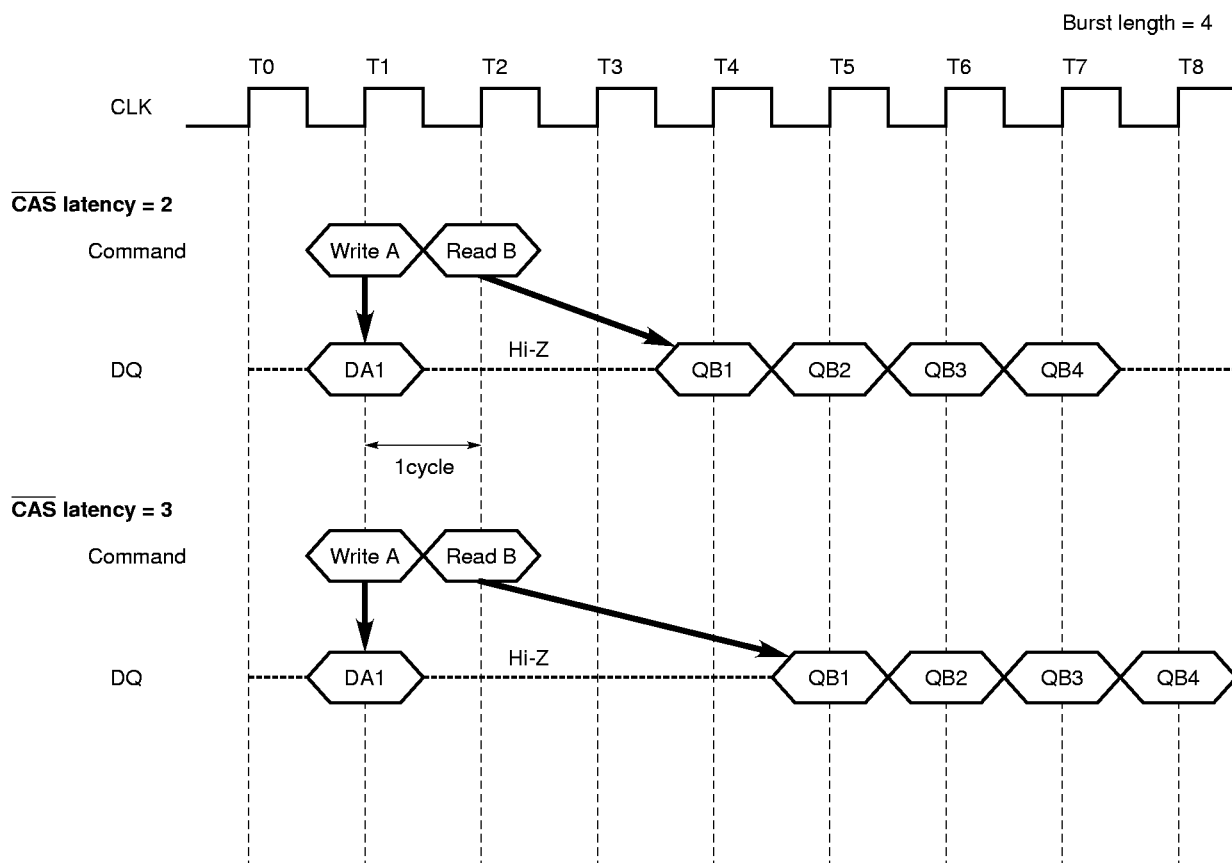


11.3 Write to Read Command Interval

Write command and Read command interval is also 1 cycle.

Only the write data before Read command will be written.

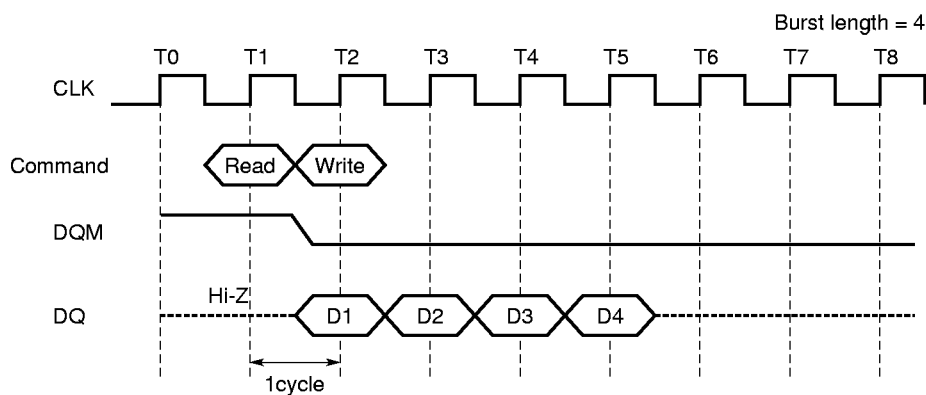
The data bus must be Hi-Z at least one cycle prior to the first D_{OUT}.



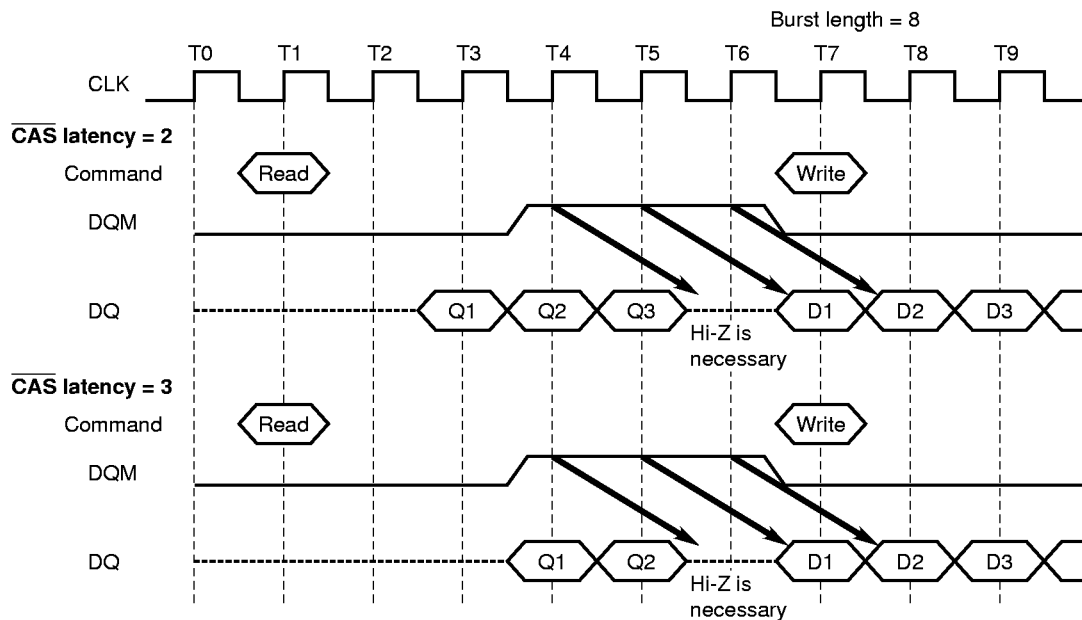
11.4 Read to Write Command Interval

During a read cycle, READ can be interrupted by WRITE.

The Read and Write command interval is 1 cycle minimum. There is a restriction to avoid data conflict. The data bus must be Hi-Z using DQM before WRITE.



READ can be interrupted by WRITE. DQM must be High at least 3 clocks prior to the Write command.

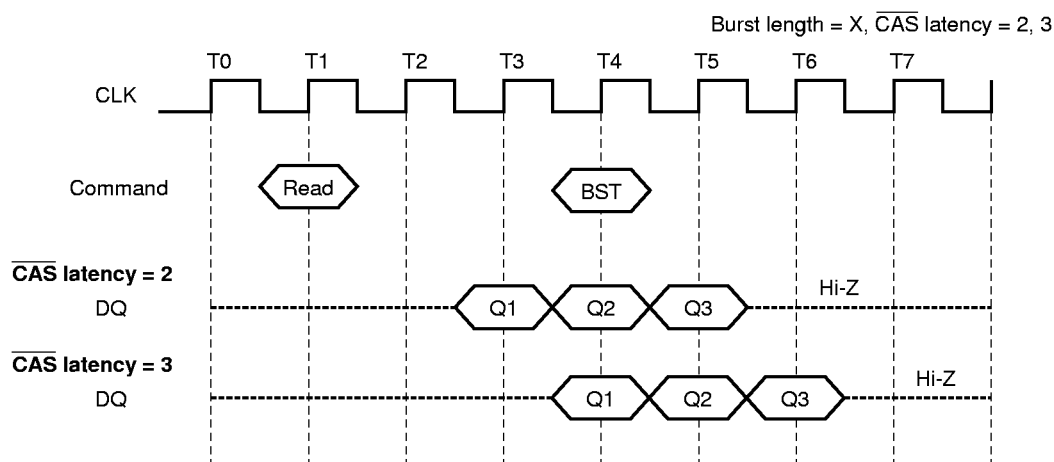


12. Burst Termination

There are two methods to terminate a burst operation other than using a Read or a Write command. One is the burst stop command and the other is the precharge command.

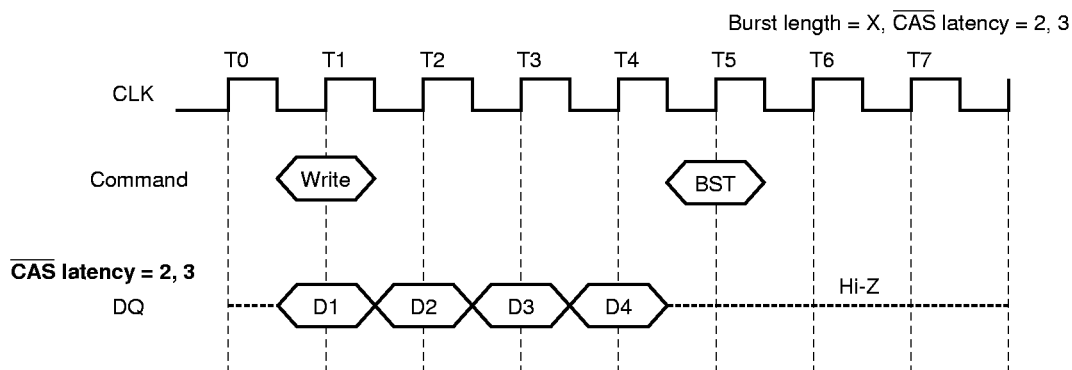
12.1 Burst Stop Command

During a read cycle, when the burst stop command is issued, the burst read data are terminated and the data bus goes to Hi-Z after the $\overline{\text{CAS}}$ latency from the burst stop command.



Remark BST: Burst stop command

During a write cycle, when the burst stop command is issued, the burst write data are terminated and data bus goes to Hi-Z at the same clock with the burst stop command.



Remark BST: Burst stop command

12.2 Precharge Termination

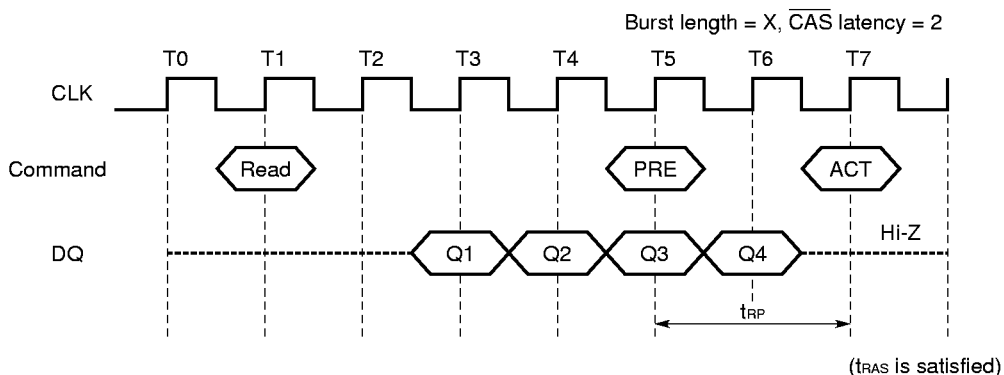
12.2.1 Precharge Termination in READ Cycle

During a read cycle, the burst read operation is terminated by a precharge command.

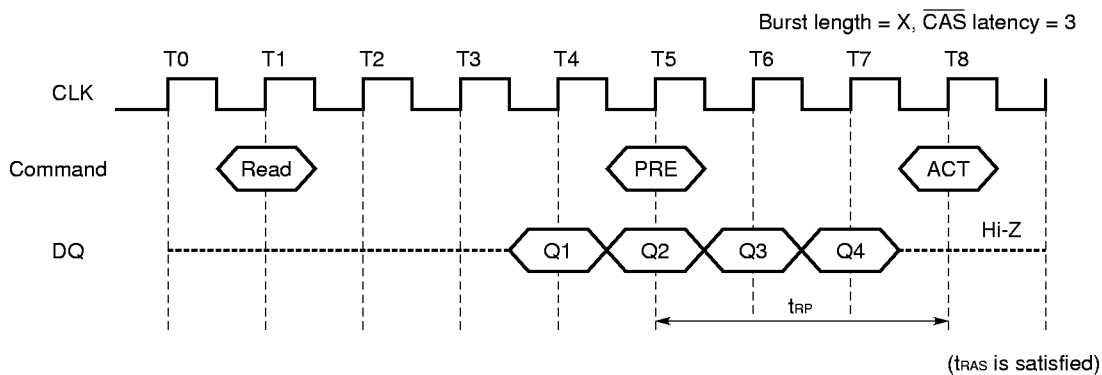
When the precharge command is issued, the burst read operation is terminated and precharge starts.

The same bank can be activated again after t_{RP} from the precharge command.

When $\overline{CAS}$ latency is 2, the read data will remain valid until one clock after the precharge command.



When $\overline{CAS}$ latency is 3, the read data will remain valid until two clocks after the precharge command.



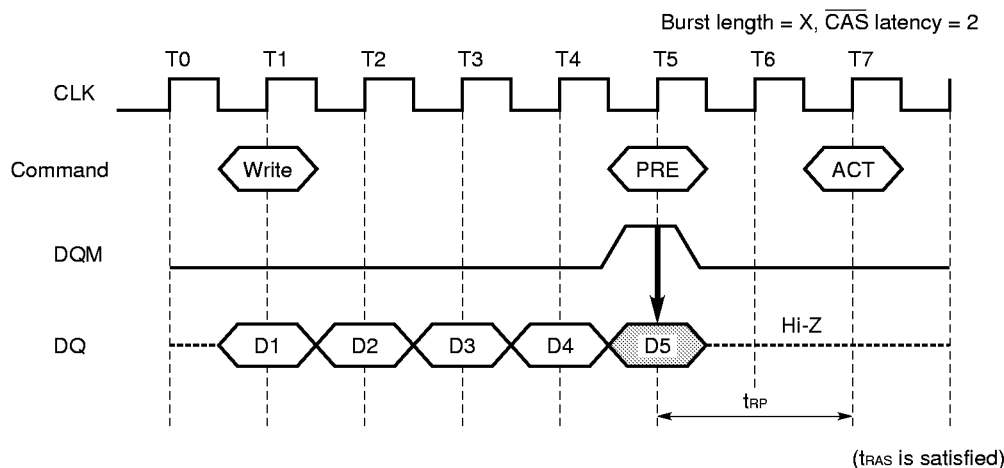
12.2.2 Precharge Termination in WRITE Cycle

During a write cycle, the burst write operation is terminated by a precharge command.

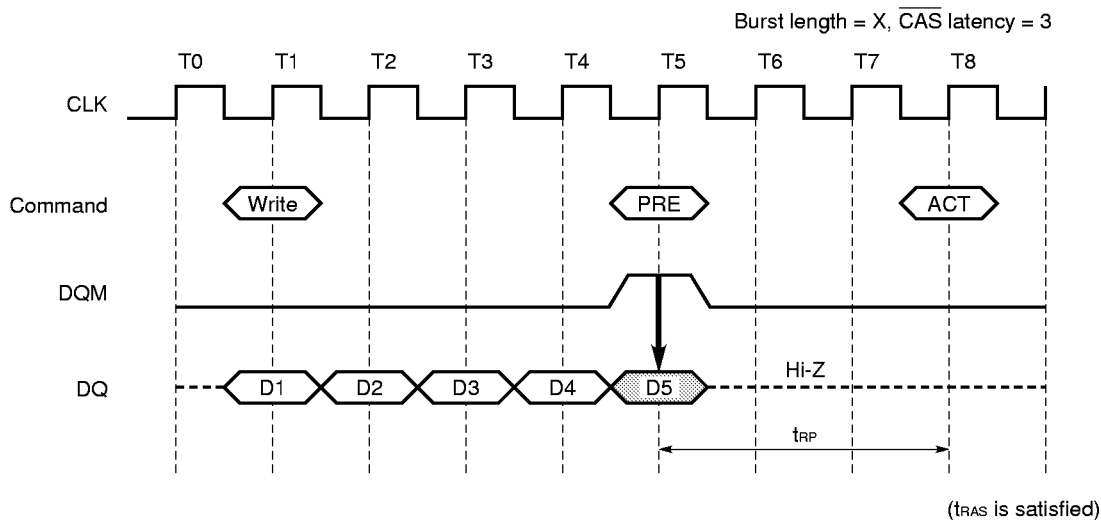
When the precharge command is issued, the burst write operation is terminated and precharge starts.

The same bank can be activated again after t_{RP} from the precharge command.

When $\overline{CAS}$ latency is 2, the write data written prior to the precharge command will be correctly stored. However, invalid data may be written at the same clock as the precharge command. To prevent this from happening, DQM must be high at the same clock as the precharge command. This will mask the invalid data.



When $\overline{CAS}$ latency is 3, the write data written prior to the precharge command will be correctly stored. However, invalid data may be written at the same clock as the precharge command. To prevent this from happening, DQM must be high at the same clock as the precharge command. This will mask the invalid data.



13. Electrical Specifications

- All voltage are referenced to V_{SS} (GND).
- After power up, wait more than 100 μ s and then, execute **Power on sequence and Auto Refresh** before proper device operation is achieved.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on power supply pin relative to GND	V _{CC} , V _{CCQ}		−1.0 to +4.6	V
Voltage on input pin relative to GND	V _T		−1.0 to +4.6	V
Short circuit output current	I _O		50	mA
Power dissipation	P _D		1	W
Operating ambient temperature	T _A		0 to +70	°C
Storage temperature	T _{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V _{CC}		3.0	3.3	3.6	V
High level input voltage	V _{IH}		2.0		4.6	V
Low level input voltage	V _{IL}		−0.3		+0.8	V
Operating ambient temperature	T _A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C _{I1}	A0 to A11	2		4	pF
	C _{I2}	CLK, CKE, $\overline{\text{CS}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, DQM, UDQM, LDQM	2		4	pF
Data input/output capacitance	C _{I/O}	DQ0 to DQ15	2		6	pF

DC Characteristics 1 (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition	CAS latency	Grade	Maximum			Unit	Notes
					×4	×8	×16		
Operating current	I _{CC1}	Burst length=1 t _{RC} ≥ t _{RC} (MIN.) I _O = 0 mA One bank active	CL = 2	–80	95	100	105	mA	1
				–10	85	90	95		
				–12	85	90	95		
			CL = 3	–80	100	105	110		
				–10	90	95	100		
				–12	90	95	100		
Precharge standby current in Power down mode	I _{CC2P}	CKE ≤ V _{IL} (MAX.) t _{CK} = 15 ns			3	3	3	mA	
	I _{CC2PS}	CKE ≤ V _{IL} (MAX.) t _{CK} = ∞			2	2	2		
Precharge standby current in Non power down mode	I _{CC2N}	CKE ≥ V _{IH} (MIN.) t _{CK} = 15 ns CS ≥ V _{IH} (MIN.) Input signals are changed one time during 30 ns.			25	25	25	mA	
	I _{CC2NS}	CKE ≥ V _{IH} (MIN.) t _{CK} = ∞ Input signals are stable.			6	6	6		
Active standby current in Power down mode	I _{CC3P}	CKE ≤ V _{IL} (MAX.) t _{CK} = 15 ns			3	3	3	mA	
	I _{CC3PS}	CKE ≤ V _{IL} (MAX.) t _{CK} = ∞			2	2	2		
Active standby current in Non power down mode	I _{CC3N}	CKE ≥ V _{IH} (MIN.) t _{CK} = 15 ns CS ≥ V _{IH} (MIN.) Input signals are changed one time during 30 ns.			28	28	30	mA	
	I _{CC3NS}	CKE ≥ V _{IH} (MIN.) t _{CK} = ∞ Input signals are stable.			10	10	12		
Operating current (Burst mode)	I _{CC4}	t _{CK} ≥ t _{CK} (MIN.) I _O = 0 mA All banks active	CL = 2	–80	110	125	130	mA	2
				–10	90	100	105		
				–12	70	80	85		
			CL = 3	–80	150	160	170		
				–10	120	130	140		
				–12	100	110	120		
Refresh current	I _{CC5}	t _{RC} = 100 ns t _{CK} = MIN.	CL = 2	–80	90	90	90	mA	3
				–10	90	90	90		
				–12	90	90	90		
			CL = 3	–80	90	90	90		
				–10	90	90	90		
				–12	90	90	90		
Self refresh Current	I _{CC6}	CKE ≤ 0.2V		–**	2	2	2	mA	
				–**L	250	250	250		

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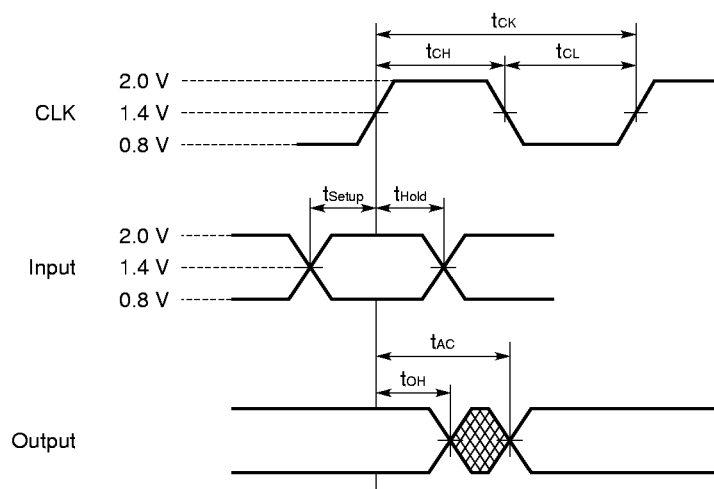
- Notes**
1. I_{CC1} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC1} is measured on condition that addresses are changed only one time during $t_{CK(MIN.)}$.
 2. I_{CC4} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC4} is measured on condition that addresses are changed only one time during $t_{CK(MIN.)}$.
 3. I_{CC5} is measured on condition that addresses are changed only one time during $t_{CK(MIN.)}$.

DC Characteristics 2 (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input leakage current	$I_{I(L)}$	$V_I = 0$ to 3.6 V, all other pins not under test = 0 V	-5.0		+5.0	μ A
Output leakage current	$I_{O(L)}$	D_{OUT} is disabled, $V_O = 0$ to 3.6 V	-5.0		+5.0	μ A
High level output voltage	V_{OH}	$I_O = -2$ mA	2.4			V
Low level output voltage	V_{OL}	$I_O = +2$ mA			0.4	V

AC Characteristics (Recommended Operating Conditions unless otherwise noted)**Test Conditions**

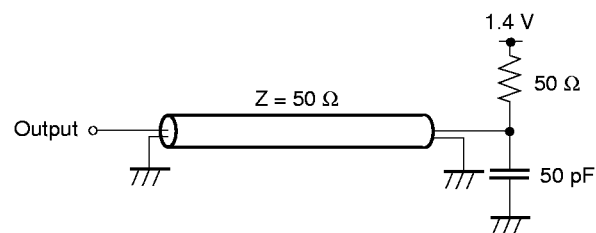
- AC measurements assume $t_r = 1$ ns.
- Reference level for measuring timing of input signals is 1.4 V. Transition times are measured between V_{IH} and V_{IL} .
- If t_r is longer than 1 ns, reference level for measuring timing of input signals is $V_{IH(MIN.)}$ and $V_{IL(MAX.)}$.
- An access time is measured at 1.4 V.



Synchronous Characteristics

Parameter		Symbol	-80		-10		-12		Unit	Note
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Clock cycle time	$\overline{\text{CAS}}$ latency = 3	t_{CK3}	8	(125 MHz)	10	(100 MHz)	12	(83 MHz)	ns	
	$\overline{\text{CAS}}$ latency = 2	t_{CK2}	12	(83 MHz)	13	(77 MHz)	15	(67 MHz)	ns	
Access time from CLK	$\overline{\text{CAS}}$ latency = 3	t_{AC3}		6		7		8	ns	1
	$\overline{\text{CAS}}$ latency = 2	t_{AC2}		7		8		9	ns	1
CLK high level width		t_{CH}	3		3.5		4		ns	
CLK low level width		t_{CL}	3		3.5		4		ns	
Data-out hold time		t_{OH}	3		3		3		ns	1
Data-out low-impedance time		t_{LZ}	0		0		0		ns	
Data-out high-impedance time	$\overline{\text{CAS}}$ latency = 3	t_{HZ3}	3	6	3	7	3	8	ns	
	$\overline{\text{CAS}}$ latency = 2	t_{HZ2}	3	7	3	8	3	9	ns	
Data-in setup time		t_{DS}	2.0		2.5		3.0		ns	
Data-in hold time		t_{DH}	1.0		1.0		1.5		ns	
Address setup time		t_{AS}	2.0		2.5		3.0		ns	
Address hold time		t_{AH}	1.0		1.0		1.5		ns	
CKE setup time		t_{CKS}	2.0		2.5		3.0		ns	
CKE hold time		t_{CKH}	1.0		1.0		1.5		ns	
CKE setup time (Power down exit)		t_{CKSP}	2.0		2.5		3.0		ns	
Command ($\overline{\text{CS}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, DQM) setup time		t_{CMS}	2.0		2.5		3.0		ns	
Command ($\overline{\text{CS}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, DQM) hold time		t_{CMH}	1.0		1.0		1.5		ns	

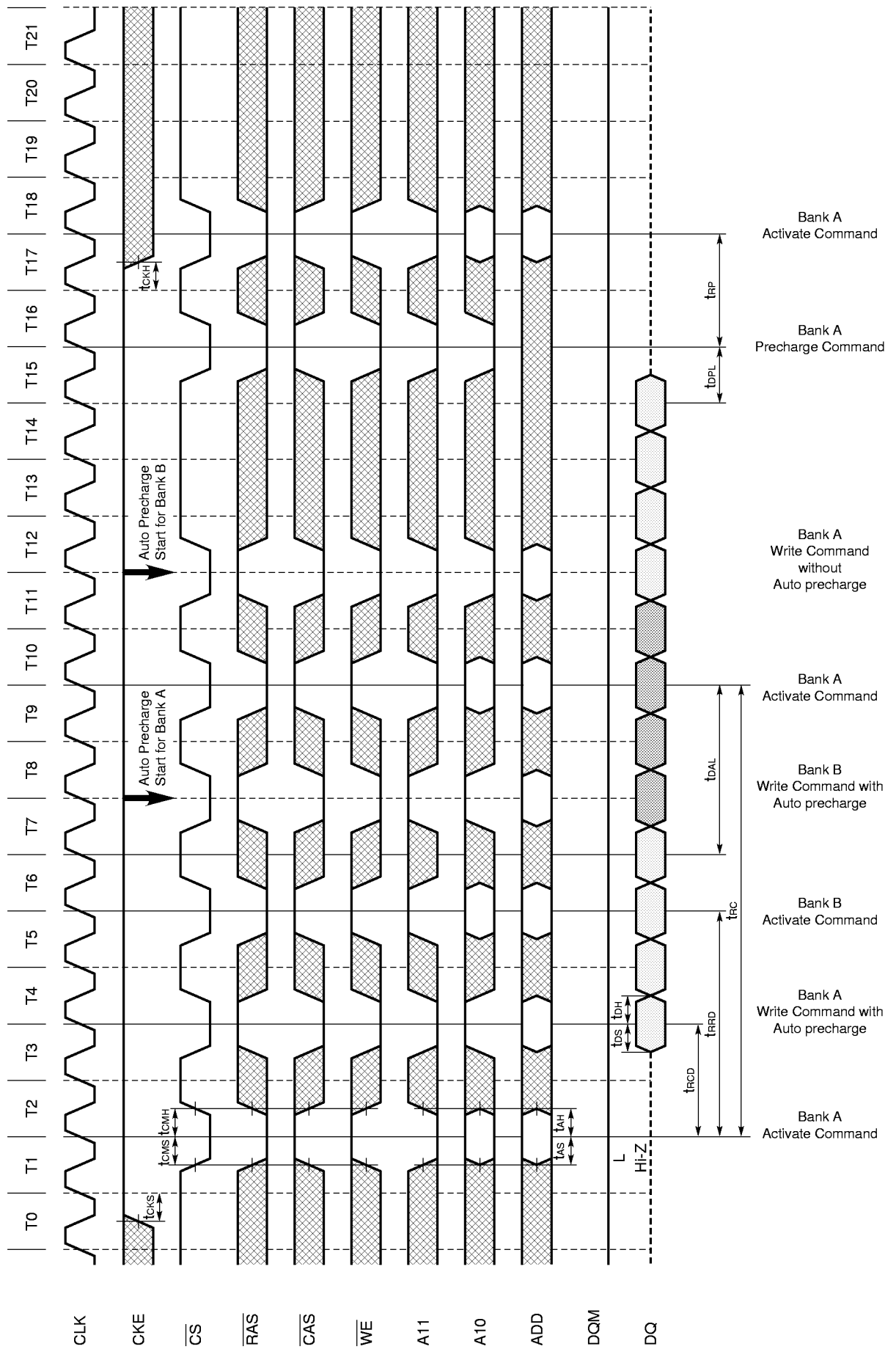
Notes 1. Output load



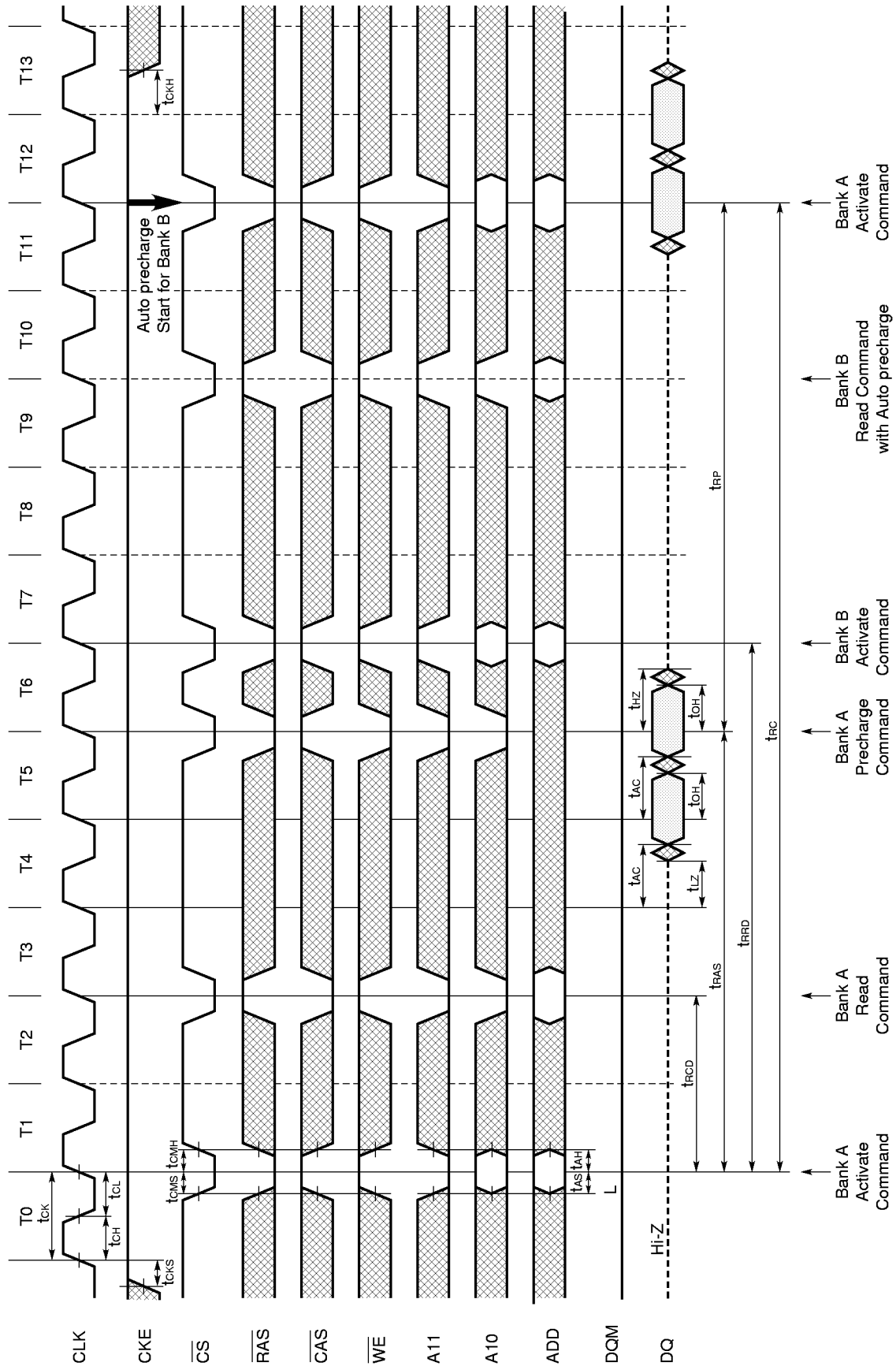
Asynchronous Characteristics

Parameter	Symbol	-80		-10		-12		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
REF to REF/ACT Command period	t_{RC}	80		90		90		ns	
ACT to PRE Command period	t_{RAS}	48	120,000	60	120,000	60	120,000	ns	
PRE to ACT Command period	t_{RP}	24		26		30		ns	
Delay time ACT to READ/WRITE Command	t_{RCD}	24		26		30		ns	
ACT(0) to ACT(1) Command period	t_{RRD}	16		20		24		ns	
Data-in to PRE Command period	t_{DPL}	8		10		12		ns	
Data-in to ACT (REF) Command (Auto precharge) period	$\overline{CAS}$ latency = 3 t_{DAL3}	1CLK + 24		1CLK + 26		1CLK + 30		ns	
	$\overline{CAS}$ latency = 2 t_{DAL2}	1CLK + 24		1CLK + 26		1CLK + 30		ns	
Mode register set cycle time	t_{RSC}	2		2		2		CLK	
Transition time	t_T	0.5	30	1	30	1	30	ns	
Refresh time	—**	t_{REF}	32		32		32	ms	
	—**L		64		64		64	ms	

13.1 AC Parameters for Write Timing (Burst length = 4, CAS latency = 2)



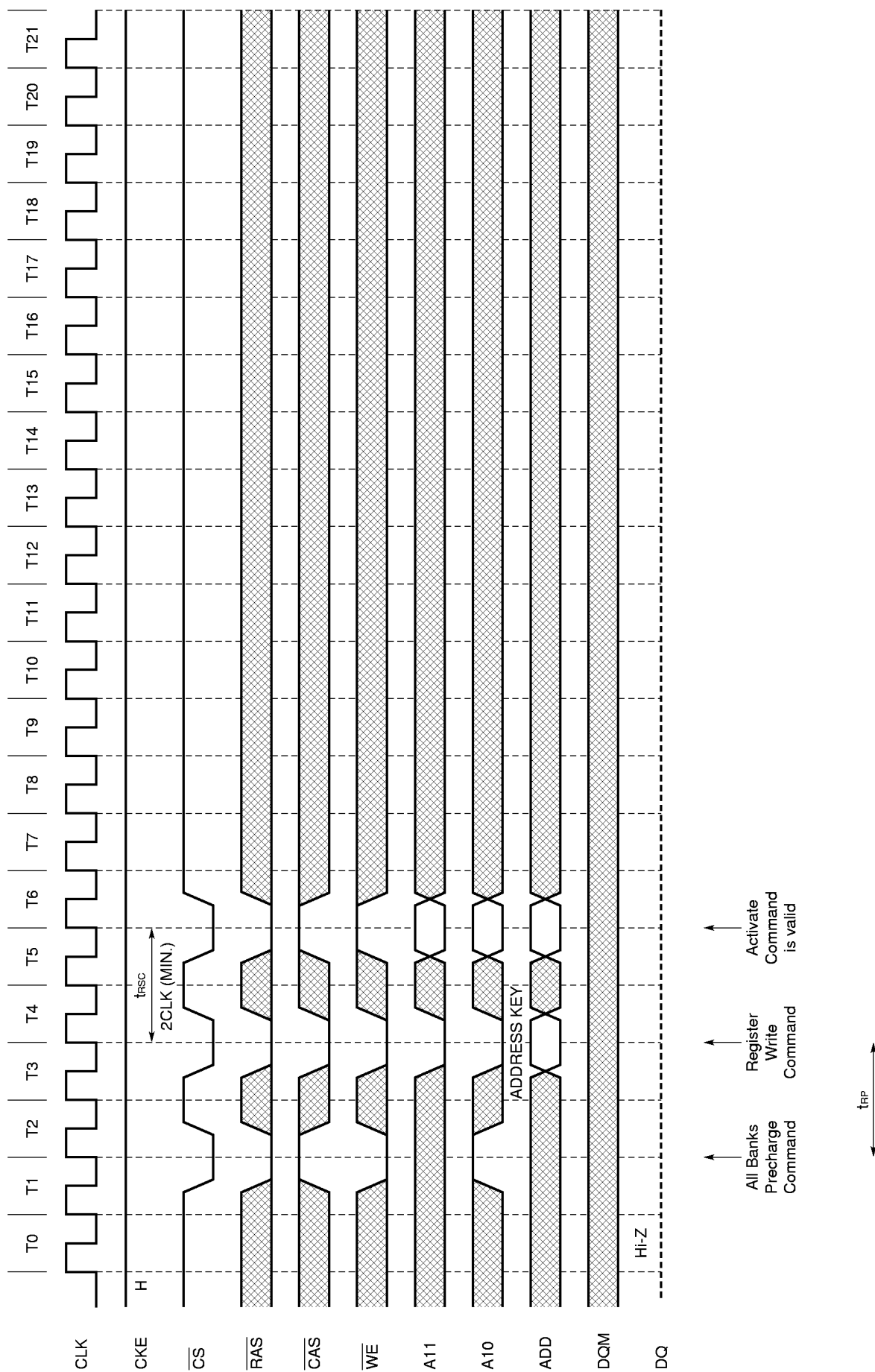
42



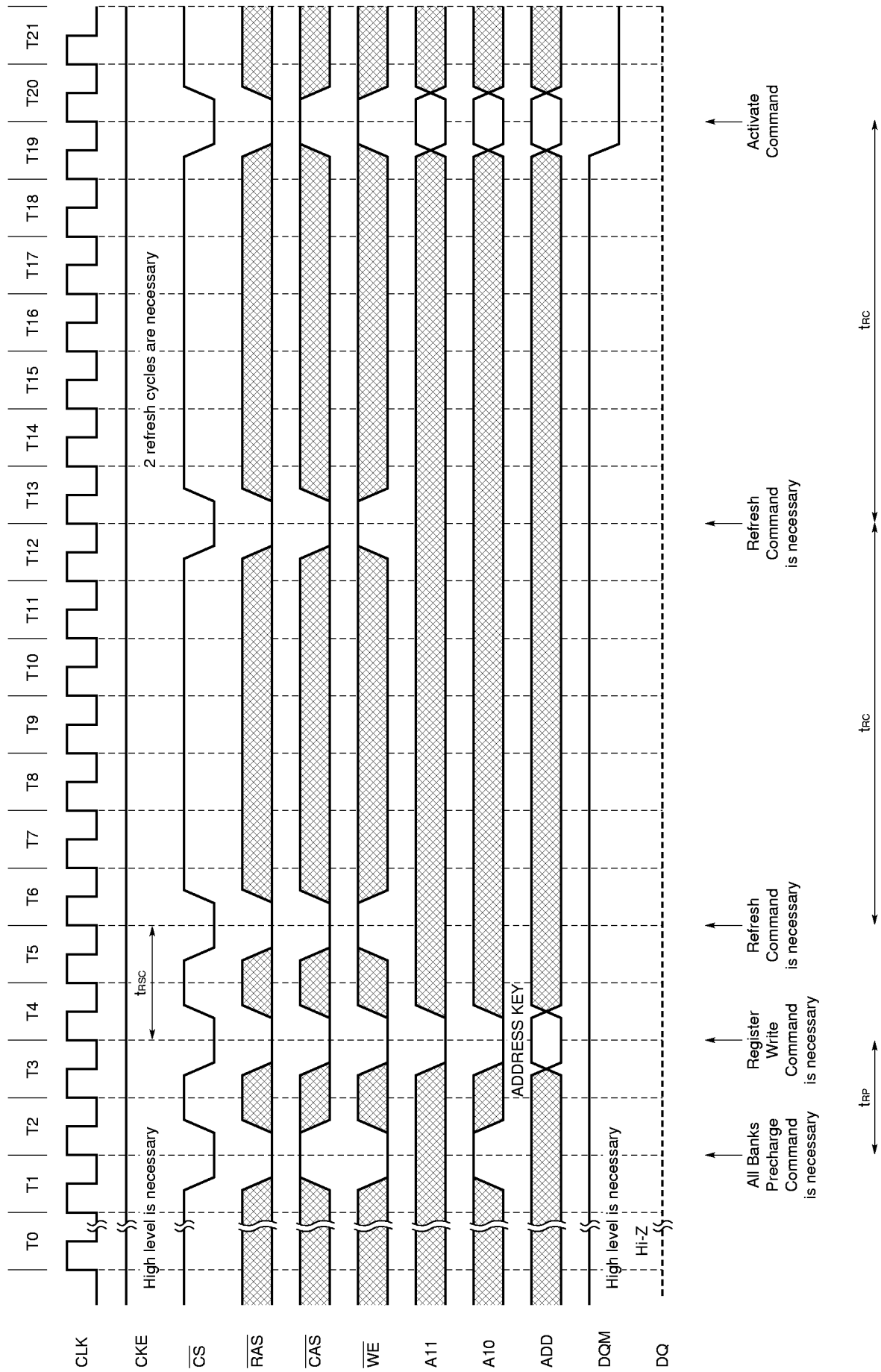
13.3 Relationship between Frequency and Latency

Speed version	-80		-10		-12	
Clock cycle time [ns]	8	12	10	13	12	15
Frequency [MHz]	125	83	100	77	83	67
CAS latency	3	2	3	2	3	2
[t _{RC} D]	3	2	3	2	3	2
RAS latency (CAS latency + [t _{RC} D])	6	4	6	4	6	4
[t _{RC}]	10	7	9	7	8	6
[t _{RA} S]	6	4	6	5	5	4
[t _{RR} D]	2	2	2	2	2	2
[t _{RP}]	3	2	3	2	3	2
[t _D PL]	1	1	1	1	1	1
[t _D AL]	4	3	4	3	4	3
[t _{RS} C]	2	2	2	2	2	2

13.4 Mode Register Write (Burst length = 4, CAS latency = 2)

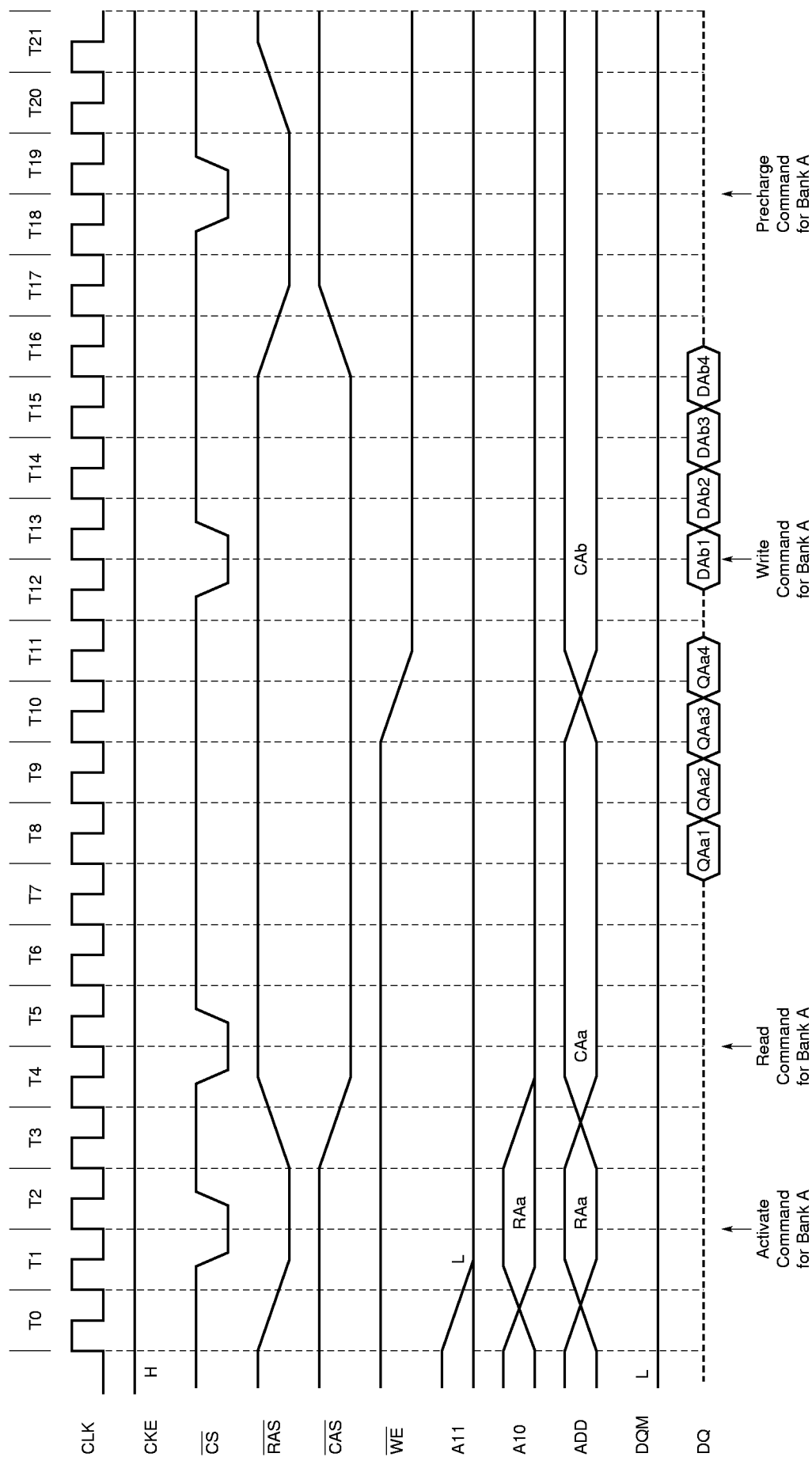


13.5 Power on Sequence and Auto Refresh

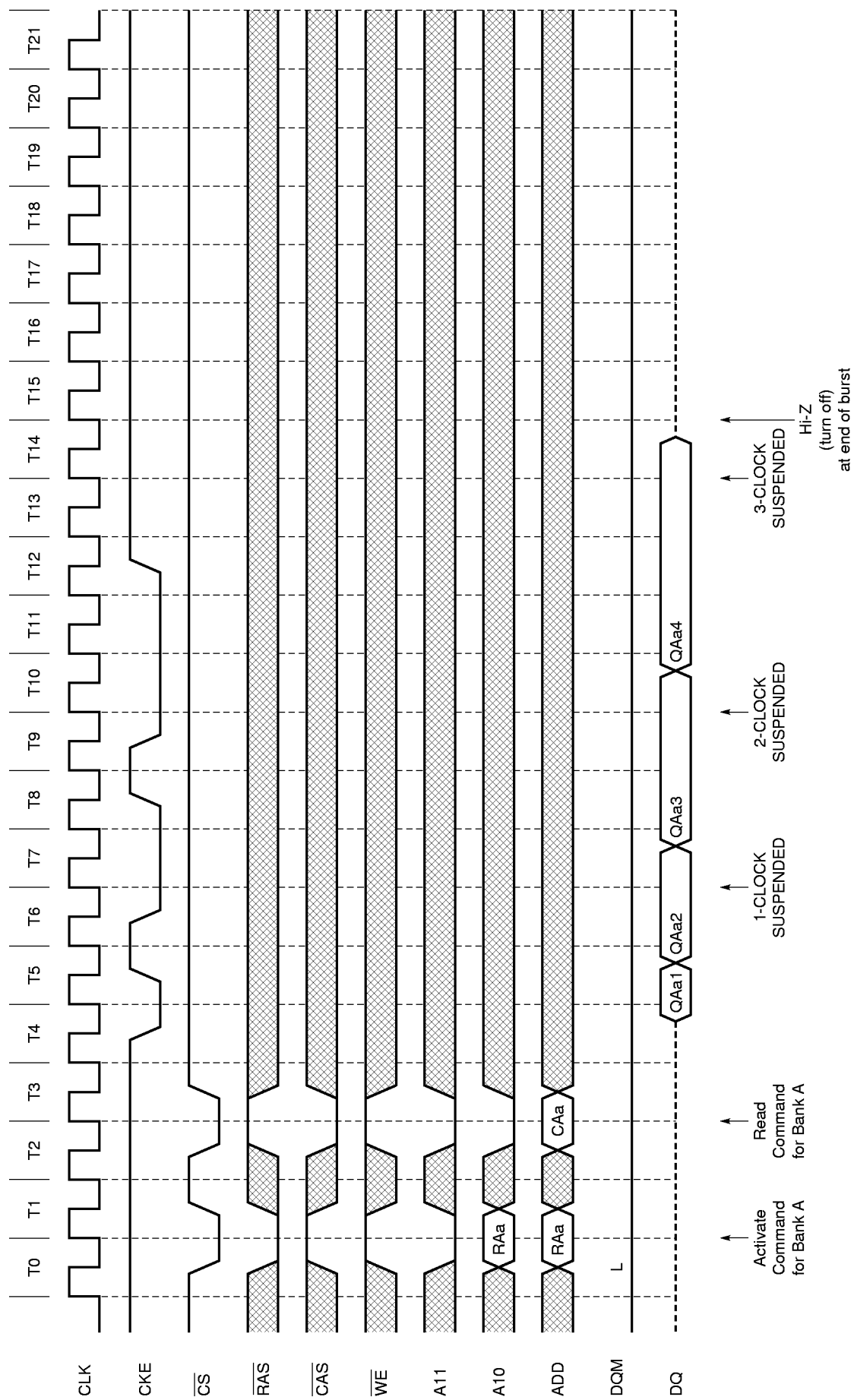


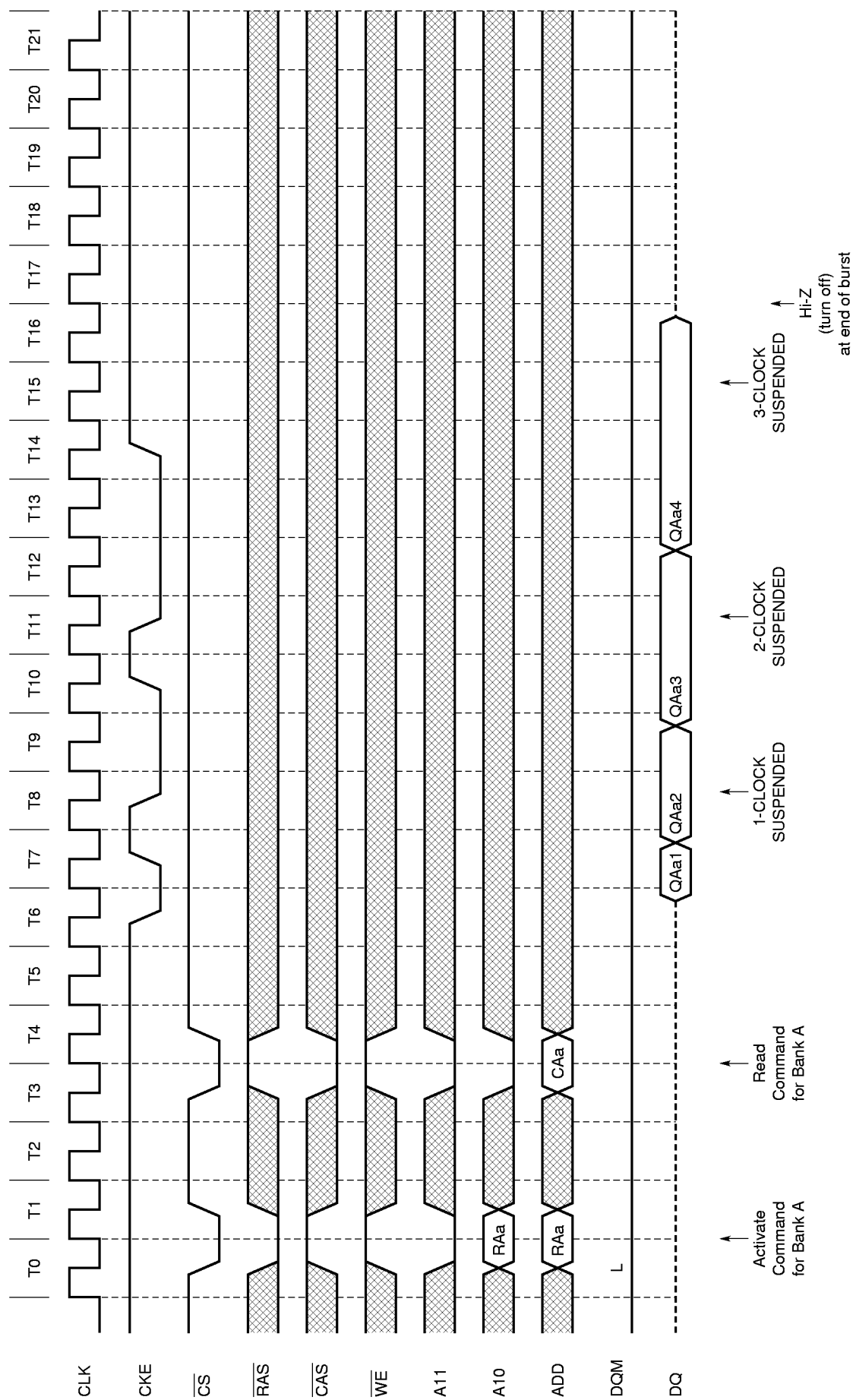
13.6 $\overline{\text{CS}}$ Function (at 100 MHz, Burst length = 4, $\overline{\text{CAS}}$ latency = 3)

Only $\overline{\text{CS}}$ signal needs to be issued at minimum rate

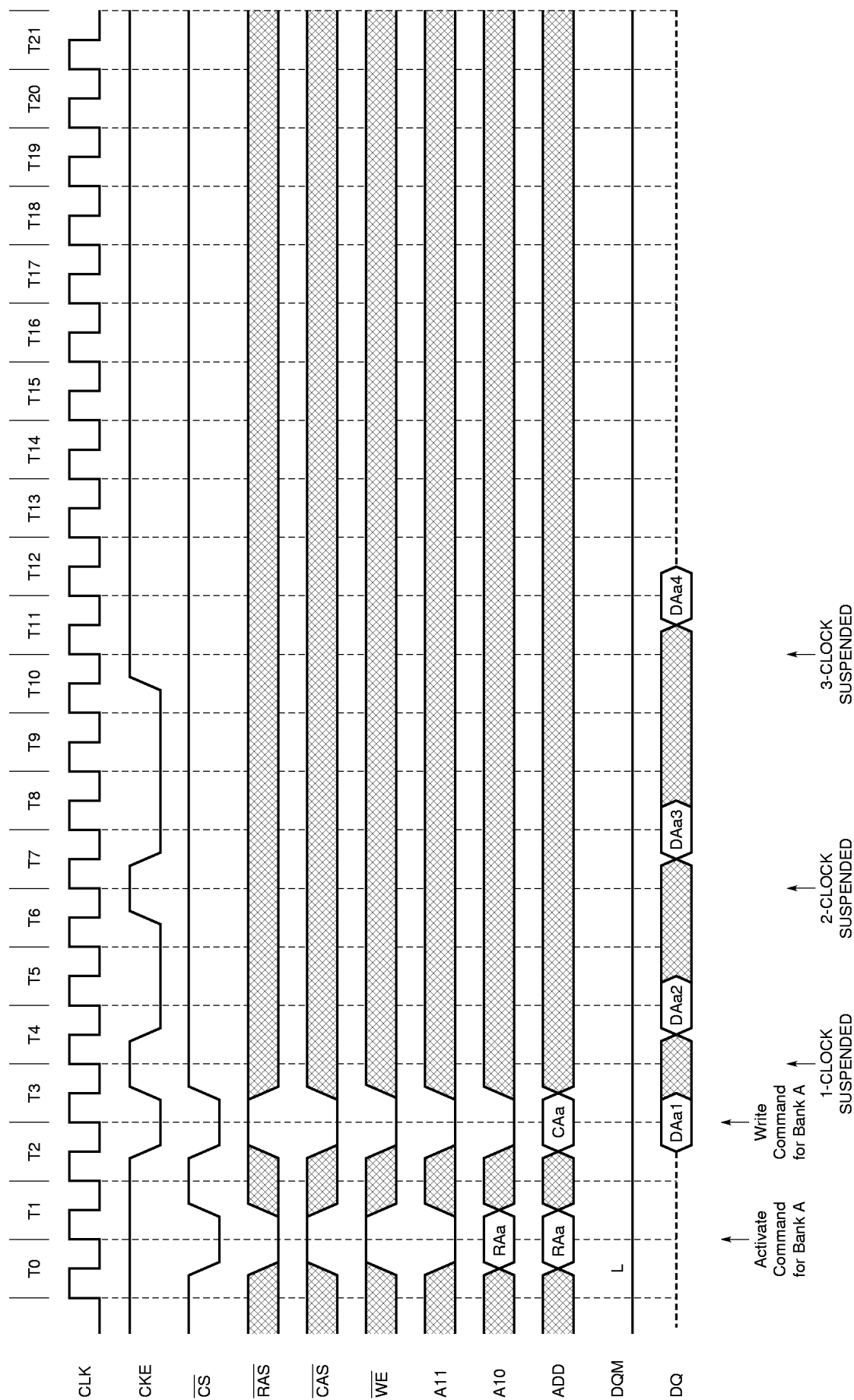


13.7 Clock Suspension during Burst Read (using CKE Function) (1/2) (Burst length = 4, CAS latency = 2)

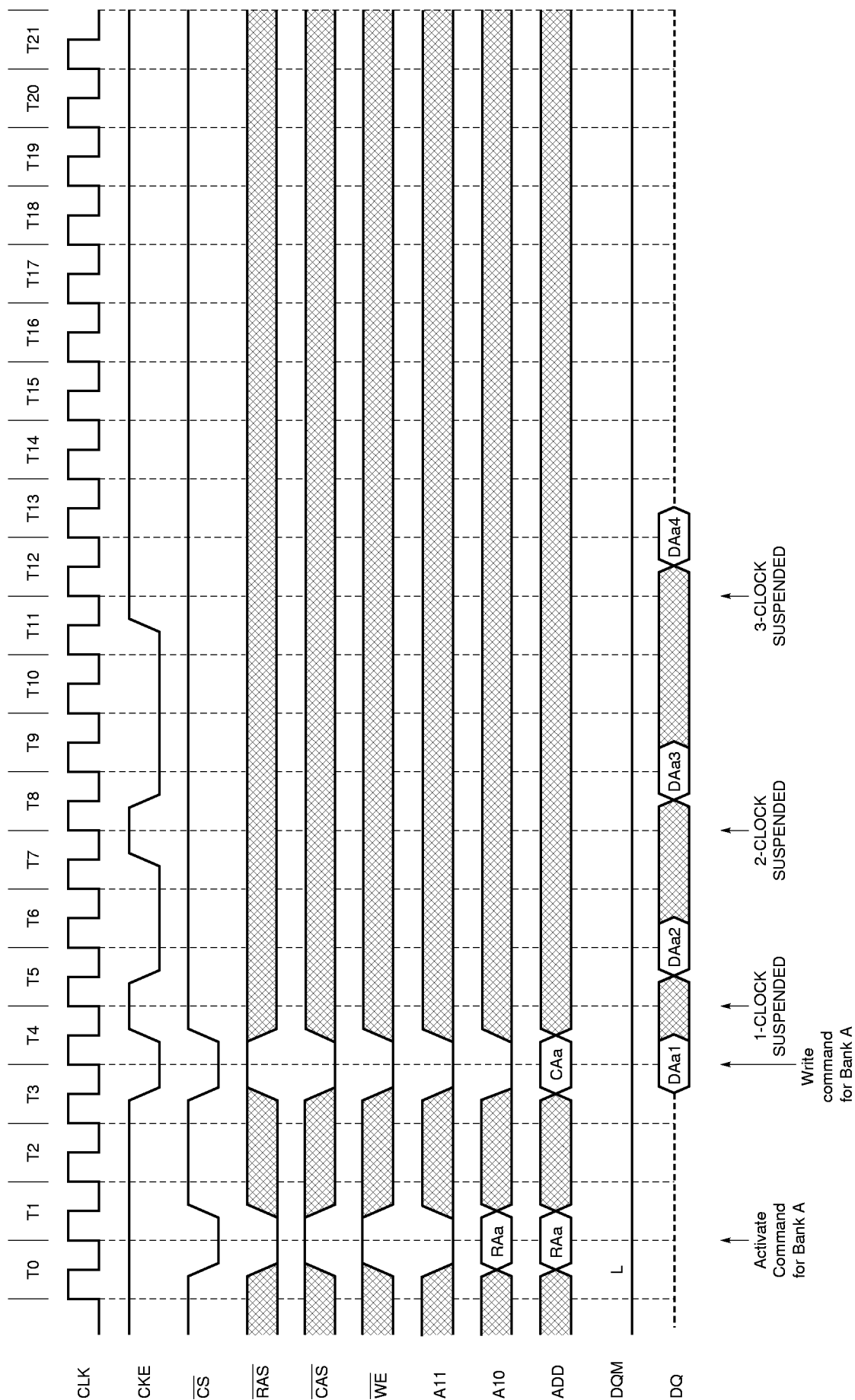




13.8 Clock Suspension during Burst Write (using CKE Function) (1/2) (Burst length = 4, CAS latency = 2)



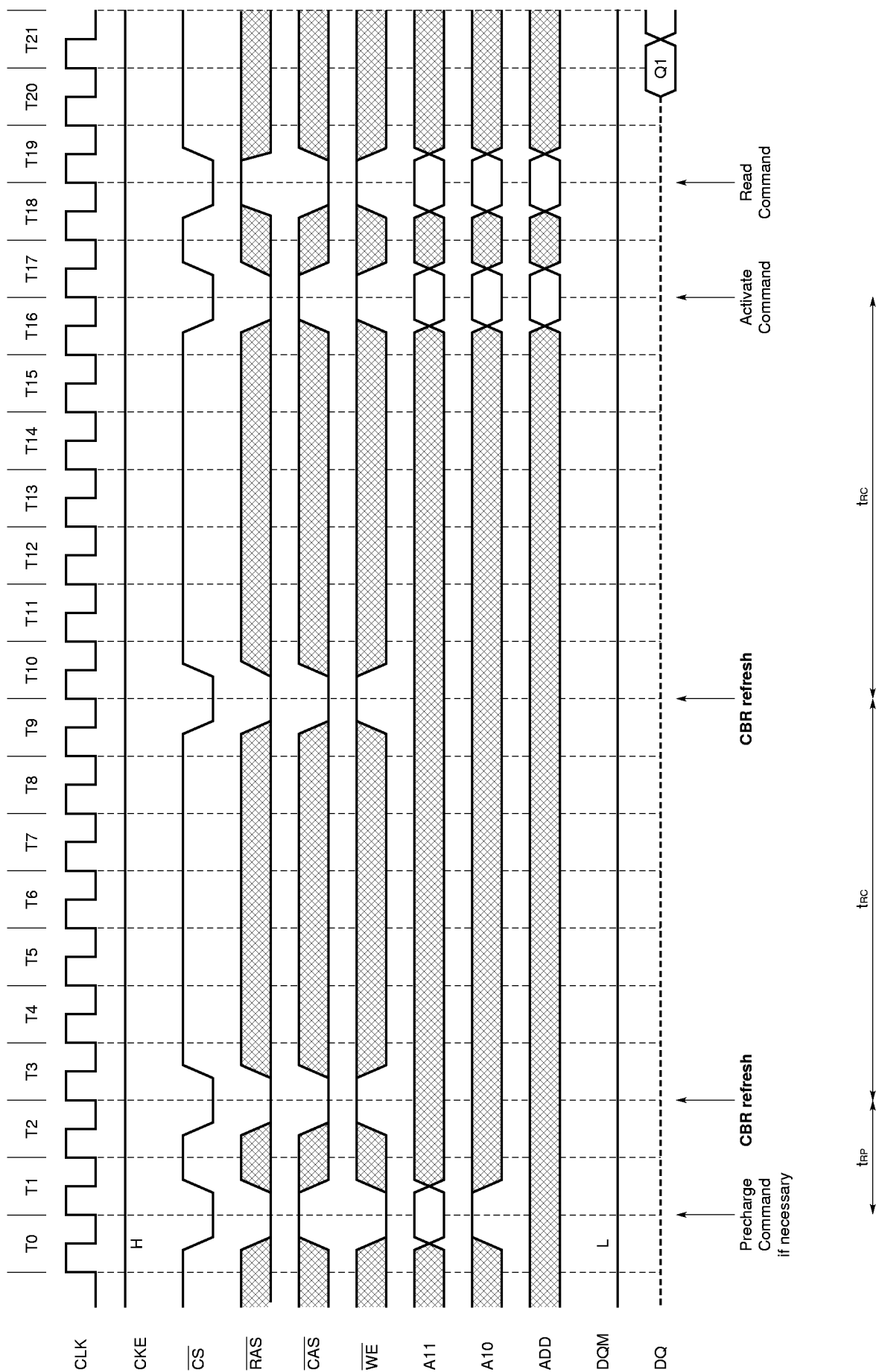
Clock Suspension during Burst Write (using CKE Function) (2/2) (Burst length = 4, CAS latency = 3)



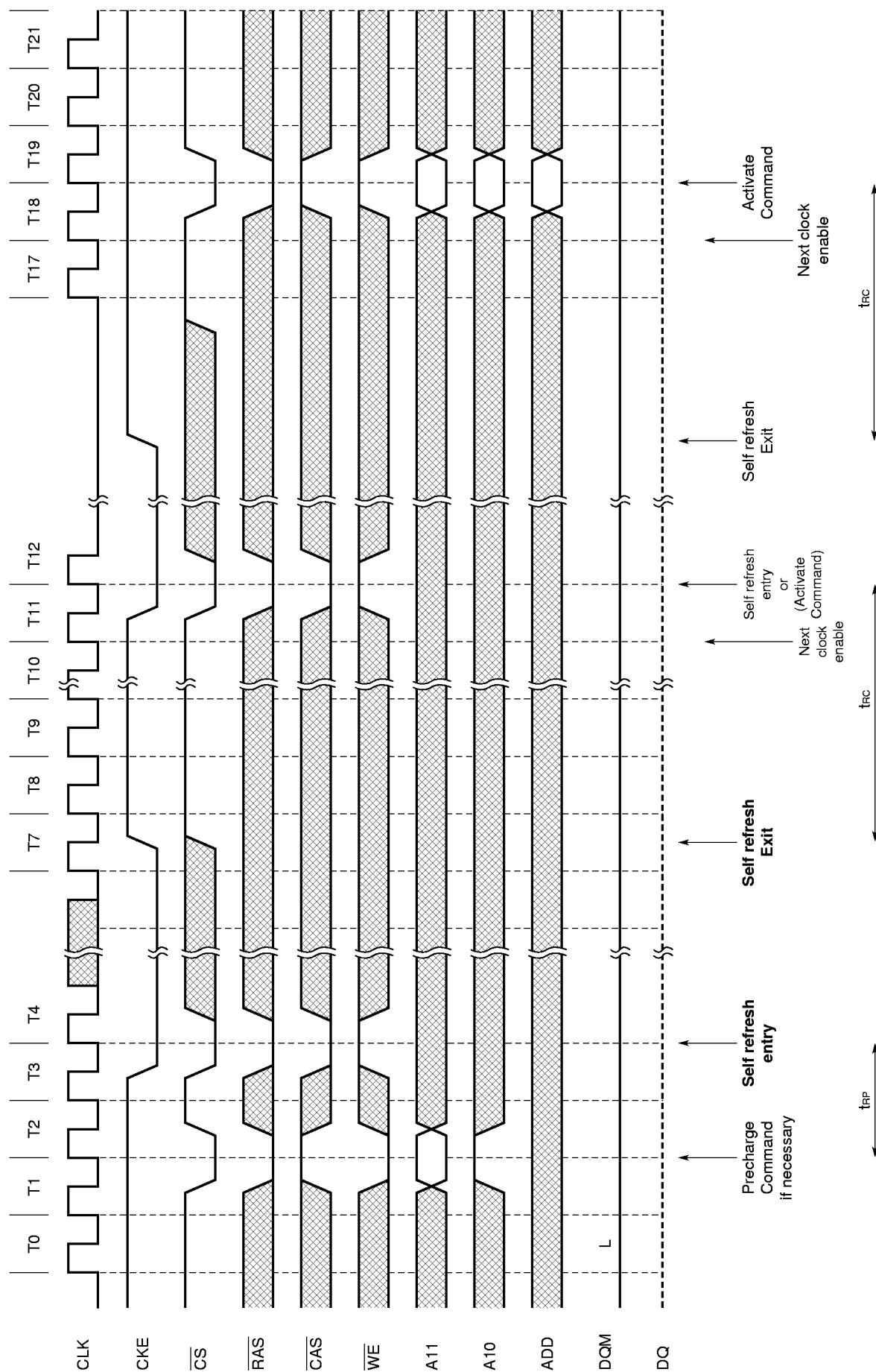
Timing diagram showing the sequence of signals (CLK, CKE, CS, RAS, CAS, WE, A11, A10, ADD, DQM, DQ) over time (T0 to T21). The diagram illustrates the timing relationships between the clock (CLK), chip enable (CS), row address strobe (RAS), column address strobe (CAS), write enable (WE), address (A11, A10), data (ADD), data mask (DQM), and data (DQ) signals. Key timing parameters are indicated: t_{CKSRP} for CKE setup/hold relative to CLK, t_{CKSRP} for CS setup/hold relative to CLK, and t_{CKSRP} for RAS, CAS, and WE setup/hold relative to CLK. The data bus DQ shows a sequence of data bytes: RAa, RAa, CAA, and QAA1, QAA2, QAA3, QAA4.

The diagram illustrates the timing for Precharge Standby mode. It shows two parallel sequences of events. The first sequence, labeled 'ACTIVE STANDBY', includes 'Activate Command for Bank A', 'Power Down Mode Entry', 'Power Down Mode Exit', and 'Read Command for Bank A'. The second sequence, labeled 'PRECHARGE STANDBY', includes 'Precharge Command', 'Power Down Mode Entry', 'Clock Mask Start', 'Clock Mask End', and 'Power Down Mode Exit'. Arrows indicate the timing of each command or event.

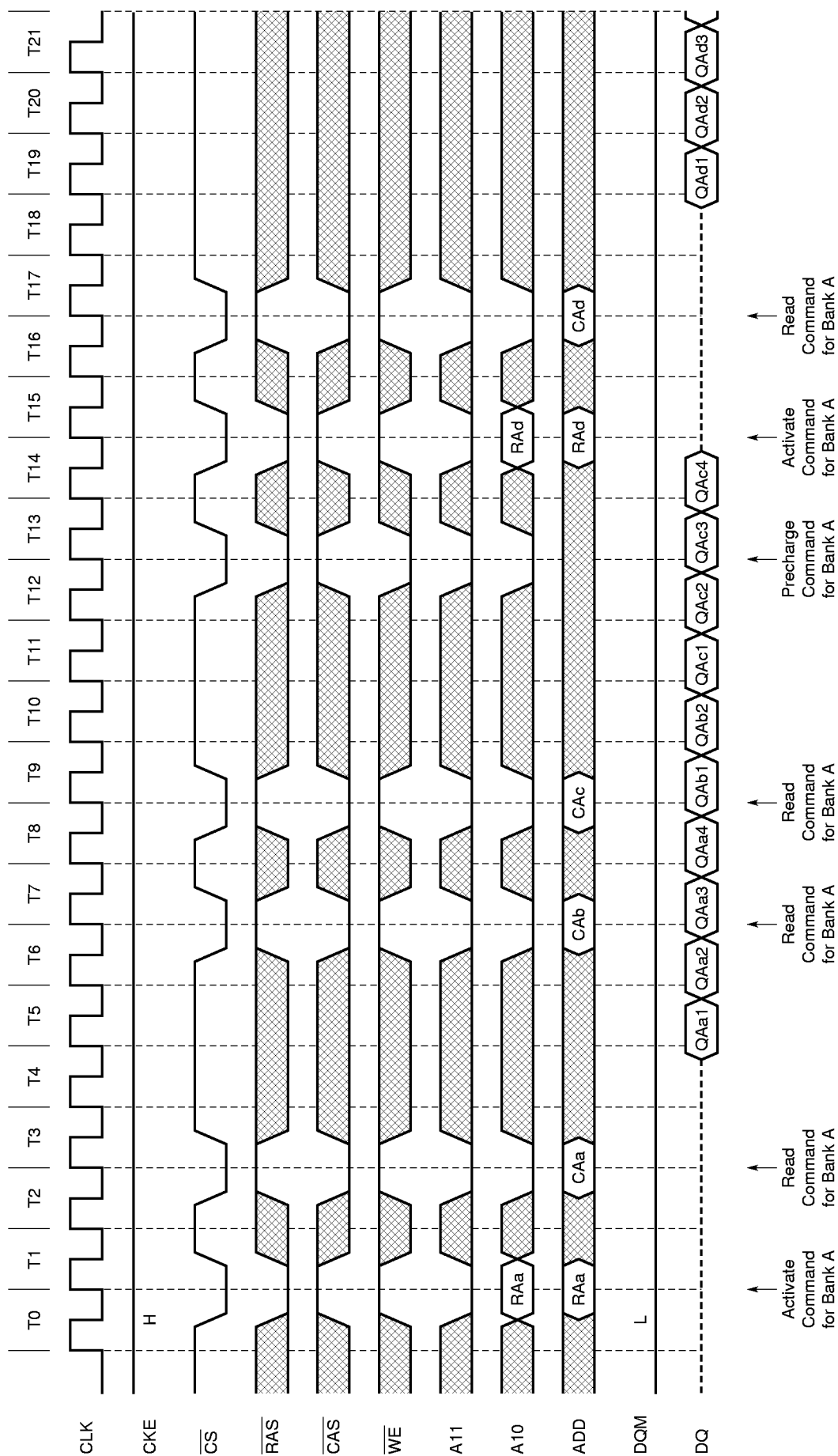
13.10 CBR Refresh



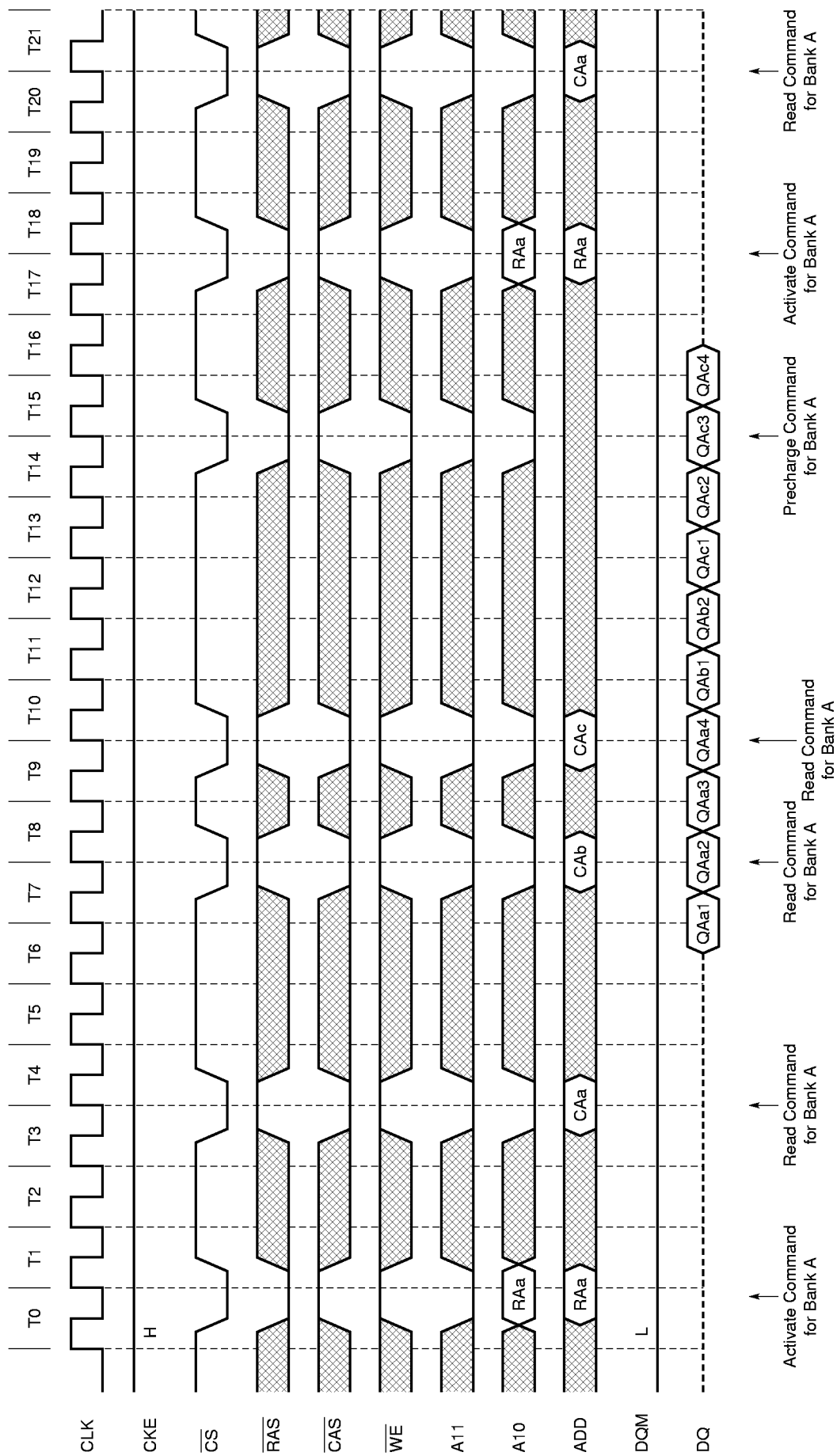
13.11 Self Refresh (entry and exit)



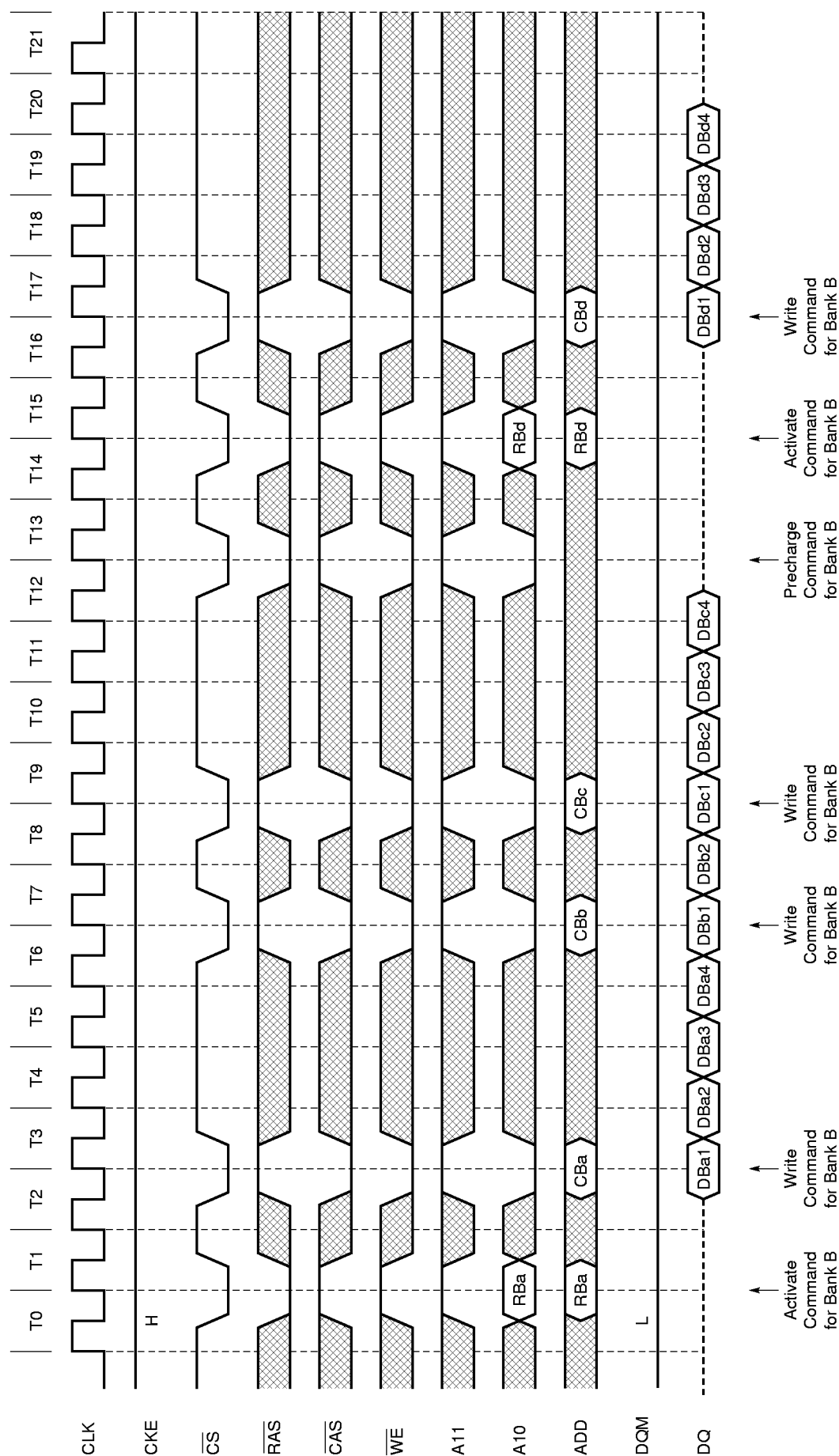
13.12 Random Column Read (Page with same bank) (1/2) (Burst length = 4, CAS latency = 2)



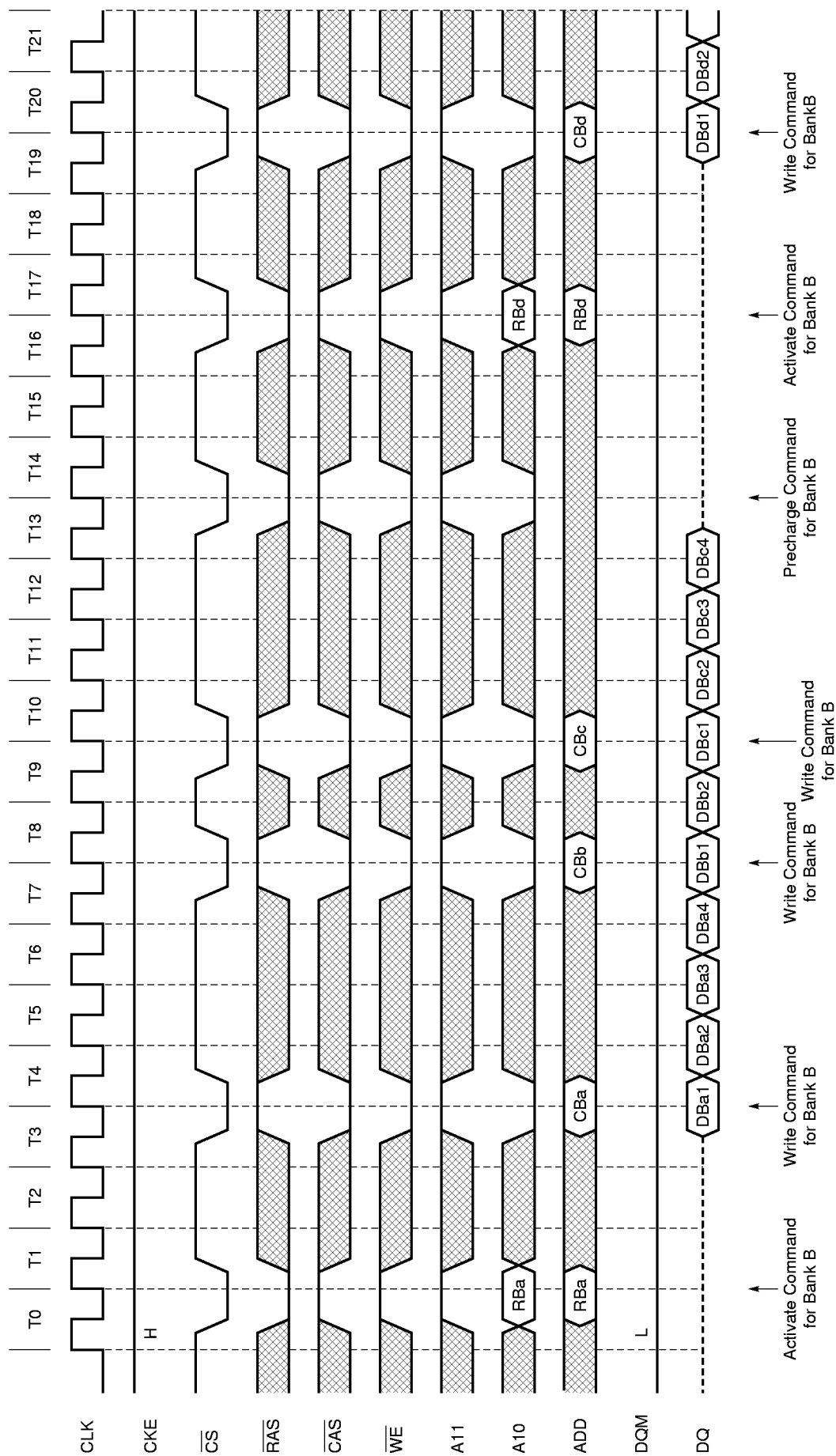
Random Column Read (Page with same bank) (2/2) (Burst length = 4, CAS latency = 3)



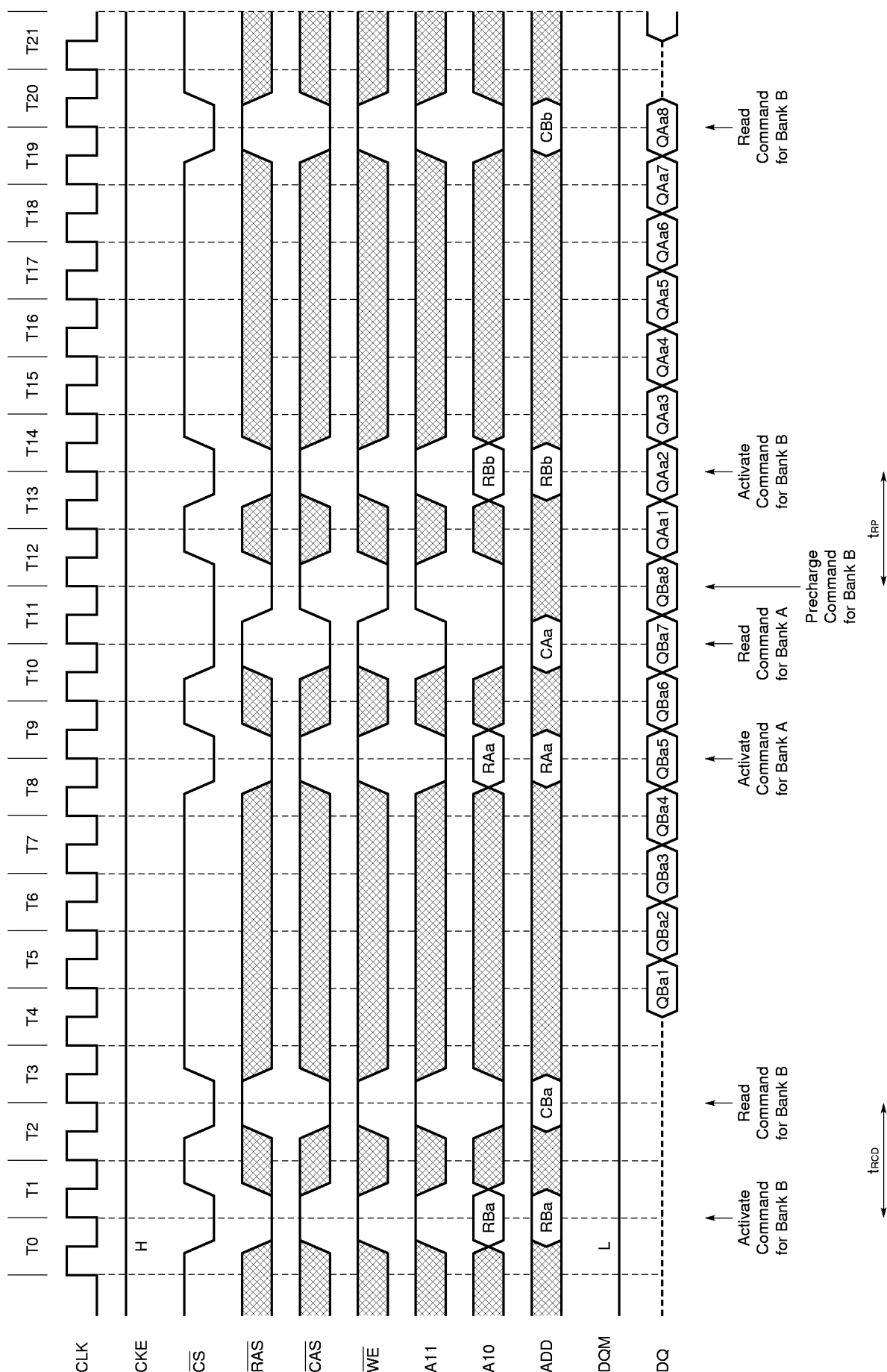
13.13 Random Column Write (Page with same bank) (1/2) (Burst length = 4, CAS latency = 2)



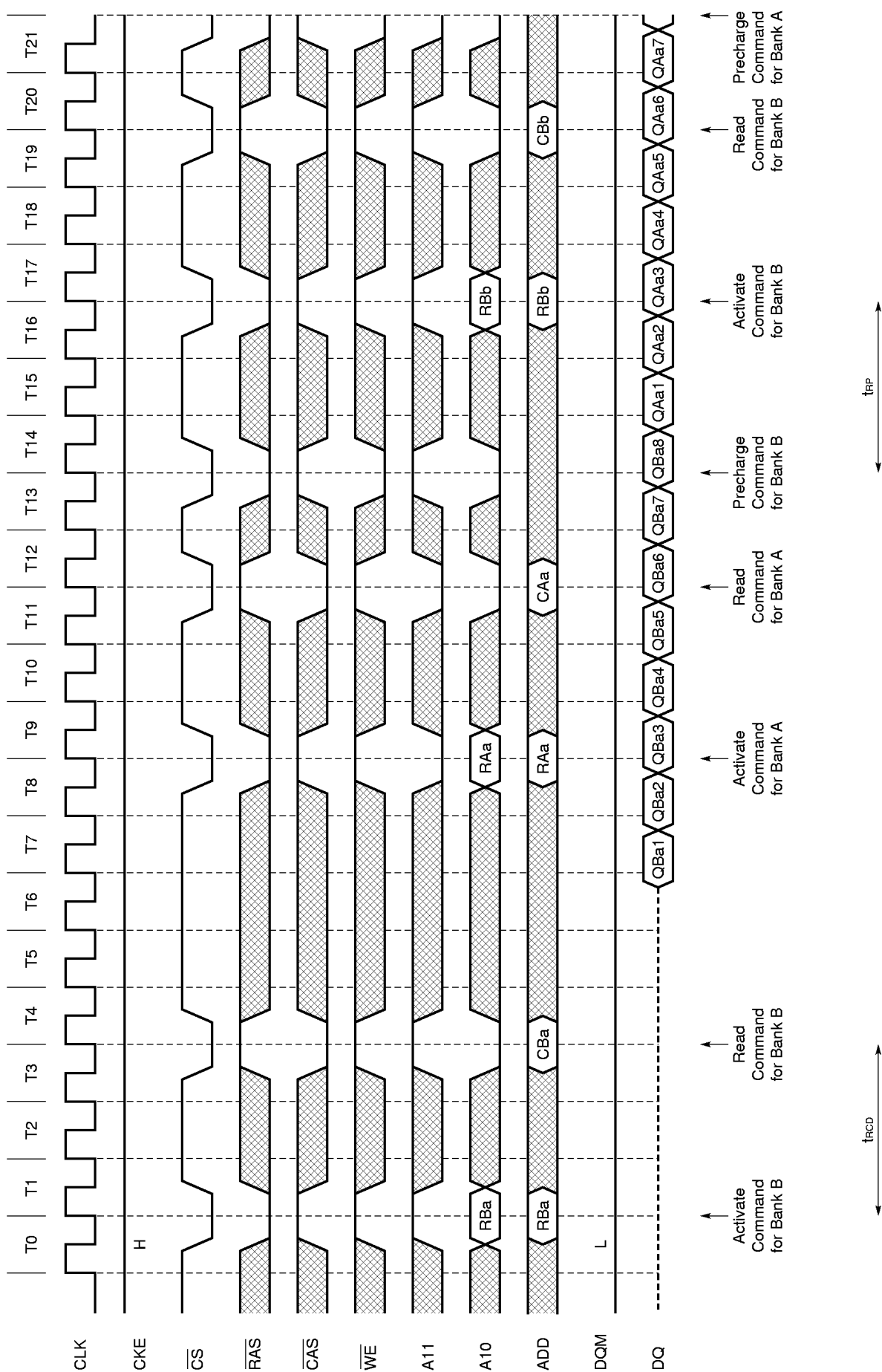
Random Column Write (Page with same bank) (2/2) (Burst length = 4, CAS latency = 3)



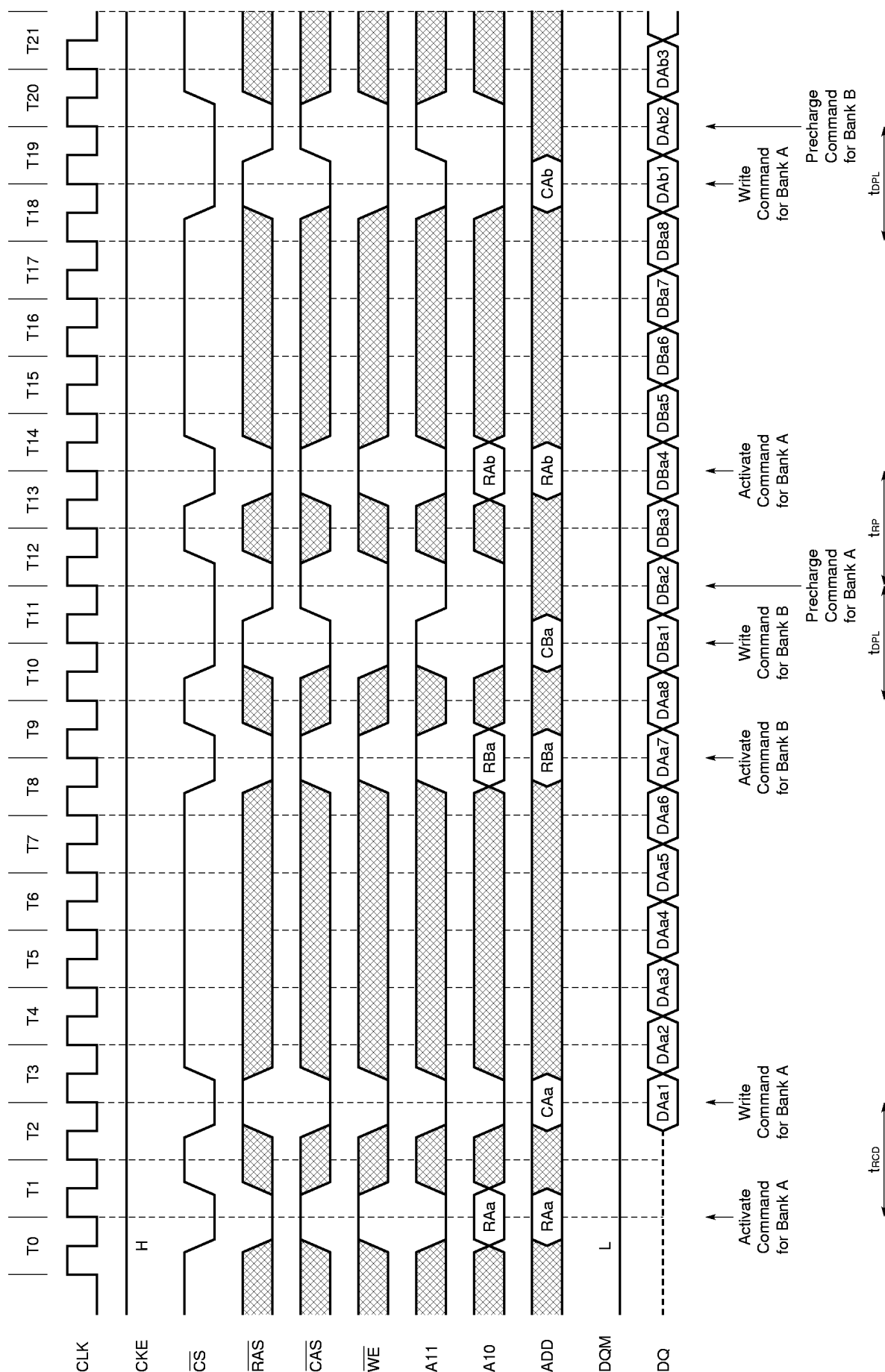
13.14 Random Row READ (Pingpong banks) (1/2) (Burst length = 8, CAS latency = 2)

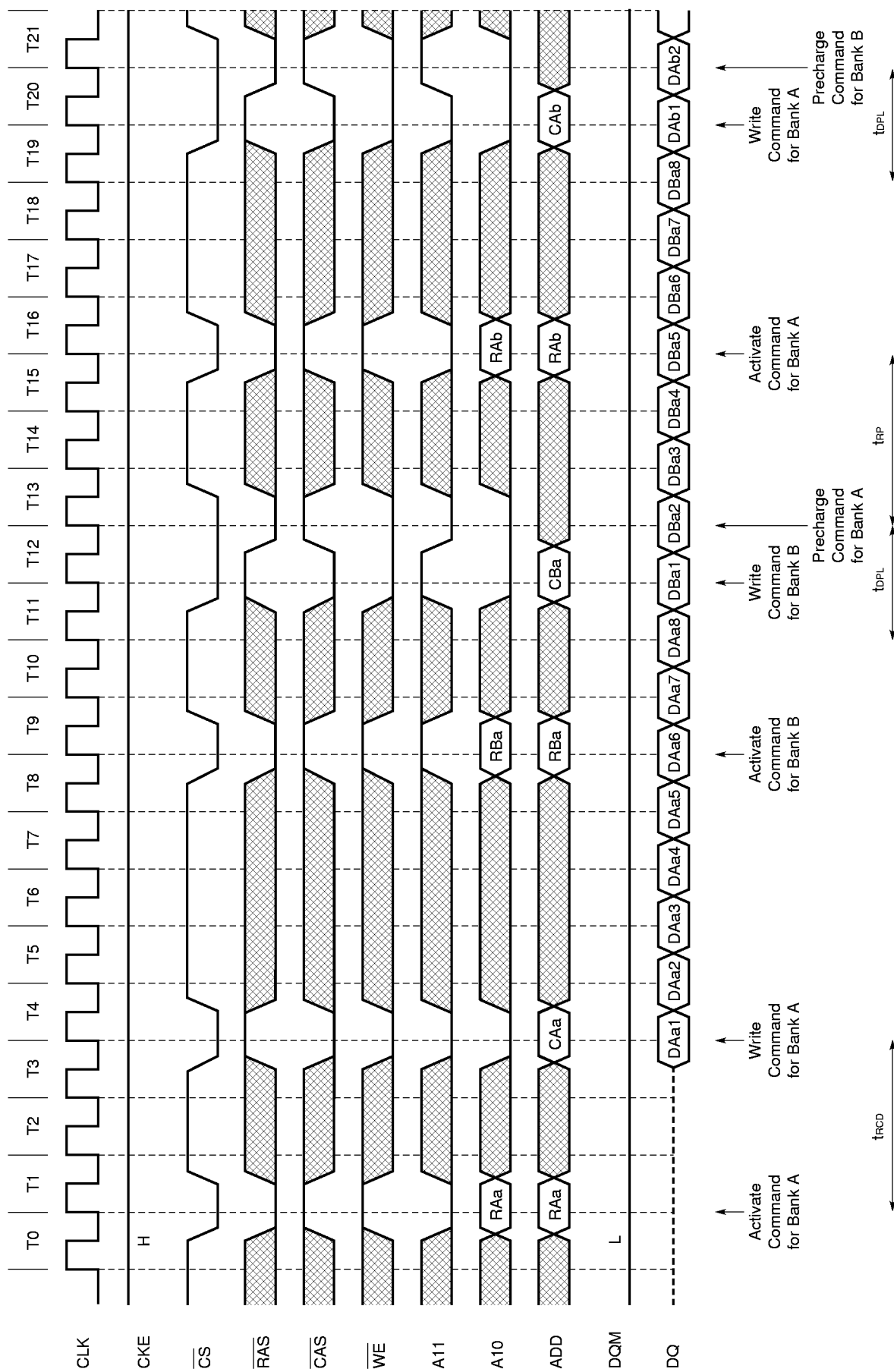


Random Row READ (Pingpong banks) (2/2) (Burst length = 8, CAS latency = 3)

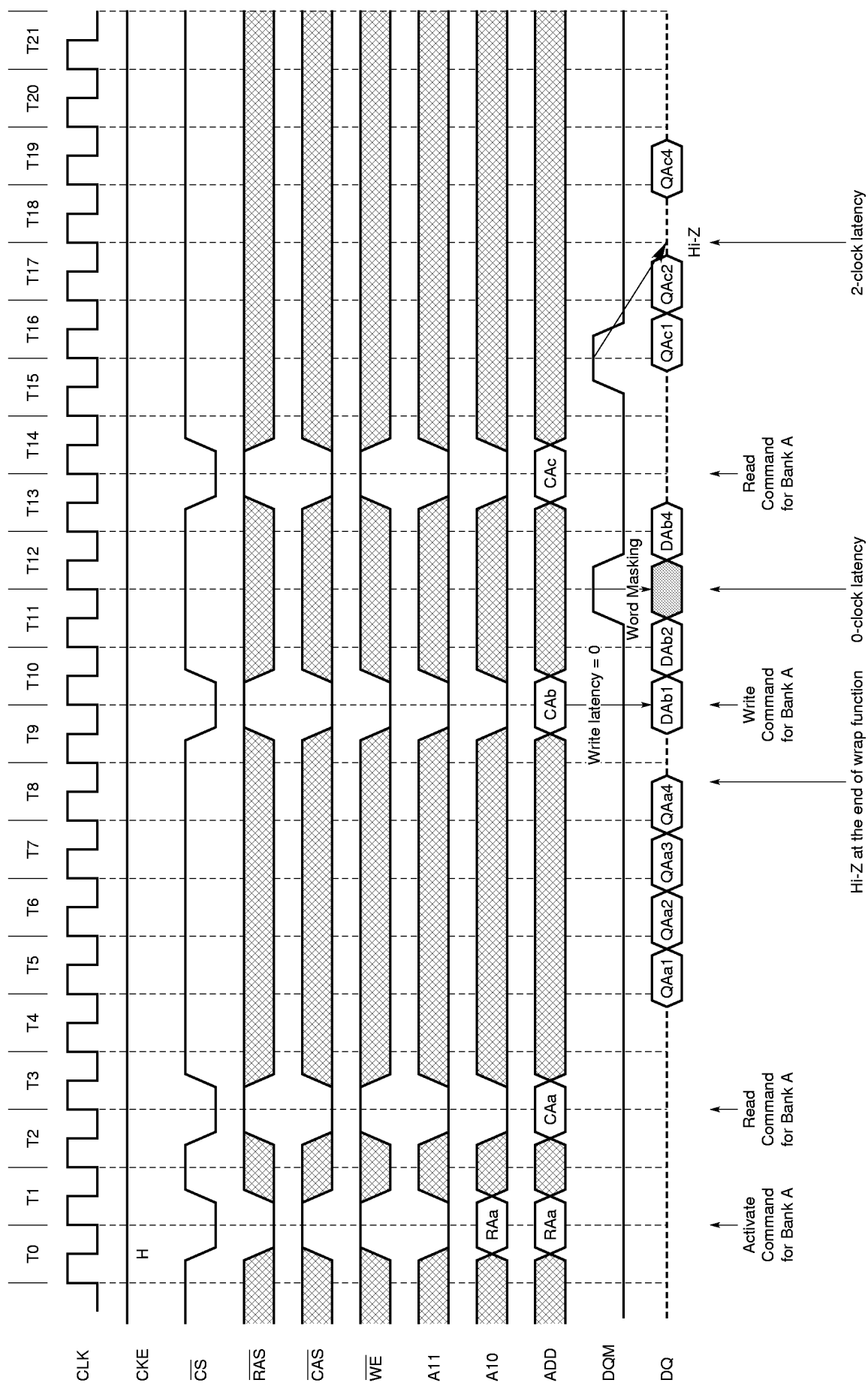


13.15 Random Row Write (Pingpong banks) (1/2) (Burst length = 8, CAS latency = 2)

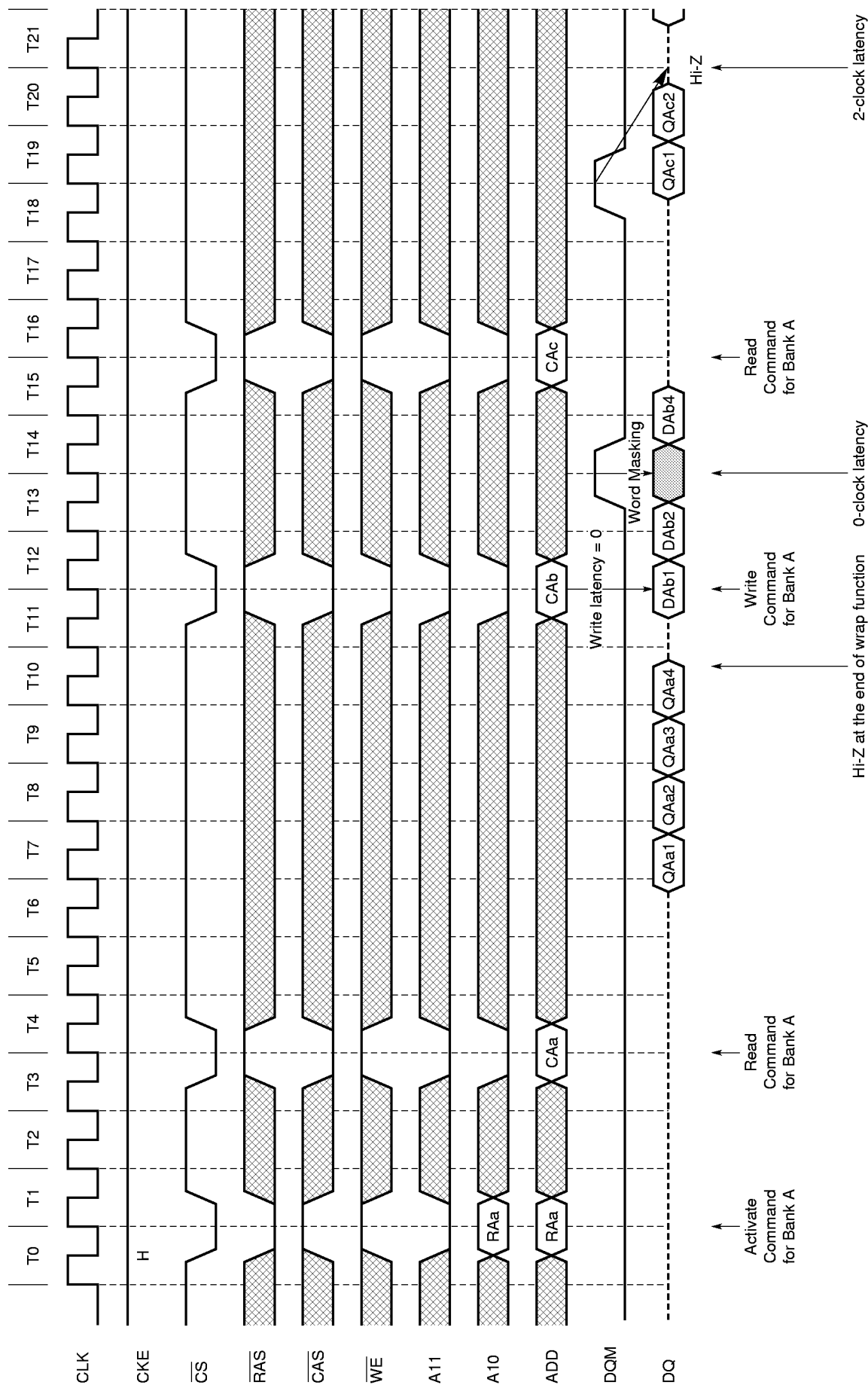


Random Row Write (Pingpong banks) (2/2) (Burst length = 8, $\overline{\text{CAS}}$ latency = 3)

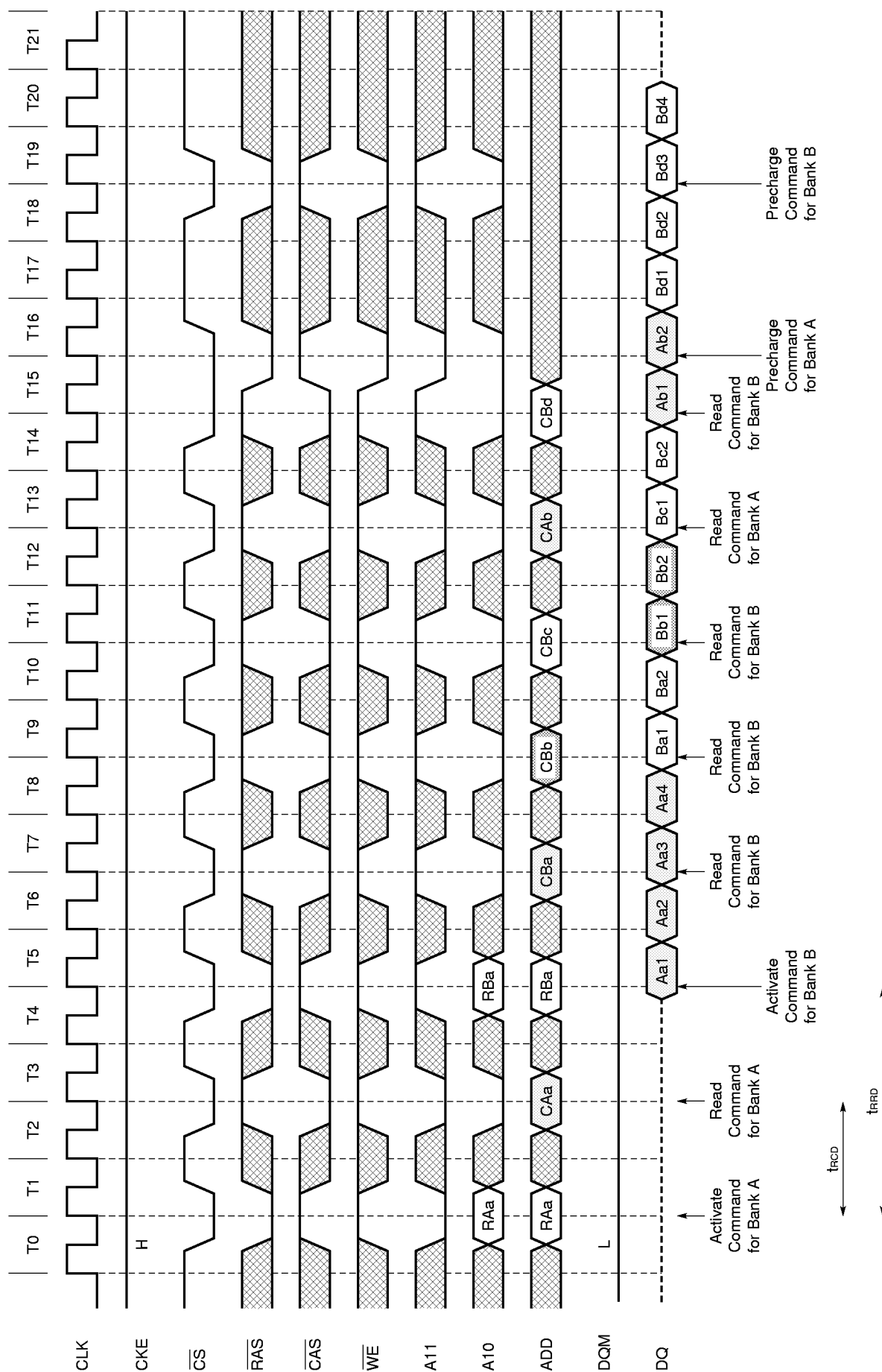
13.16 READ and WRITE (1/2) (Burst length = 4, CAS latency = 2)



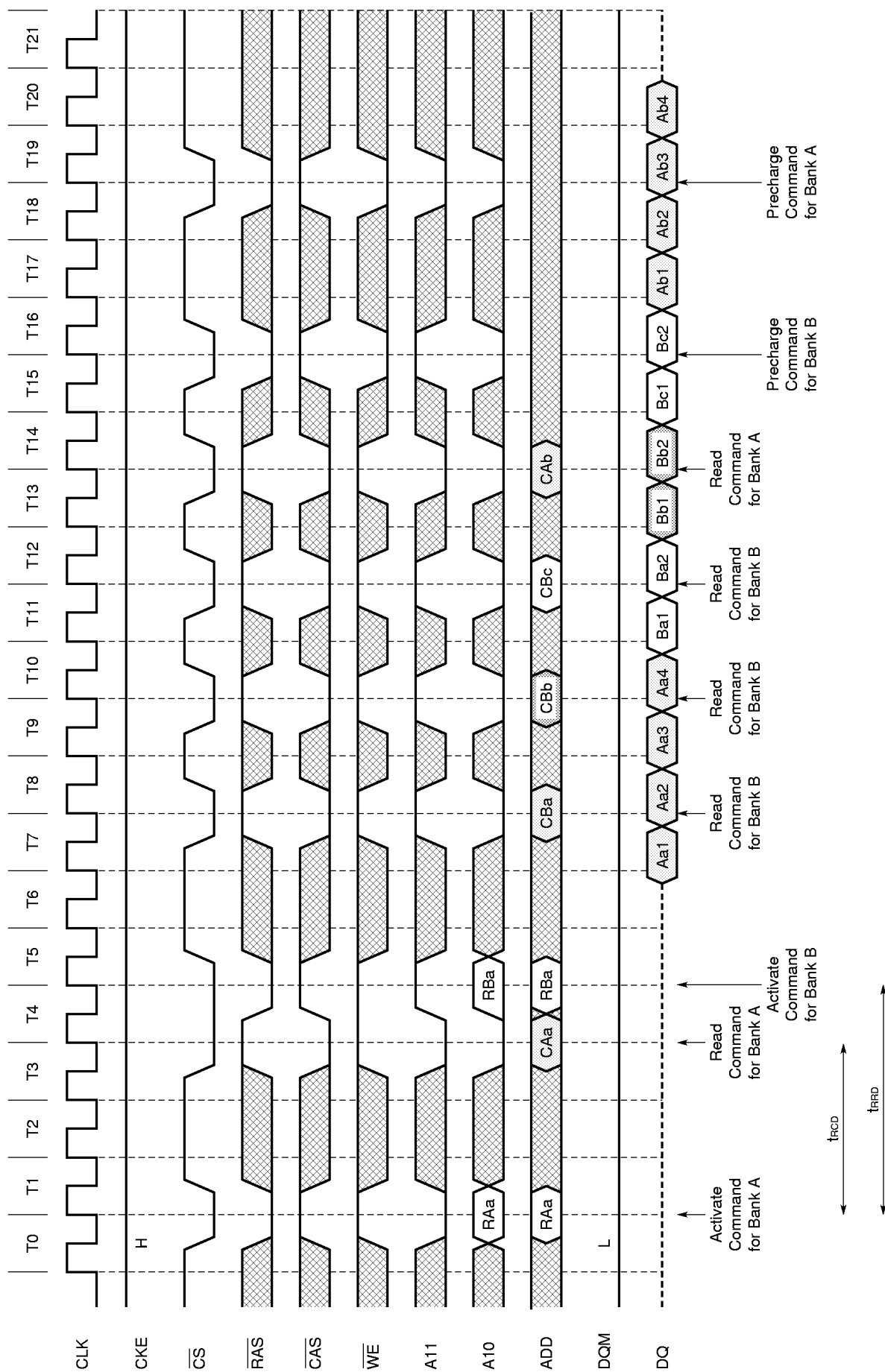
READ and WRITE (2/2) (Burst length = 4, CAS latency = 3)



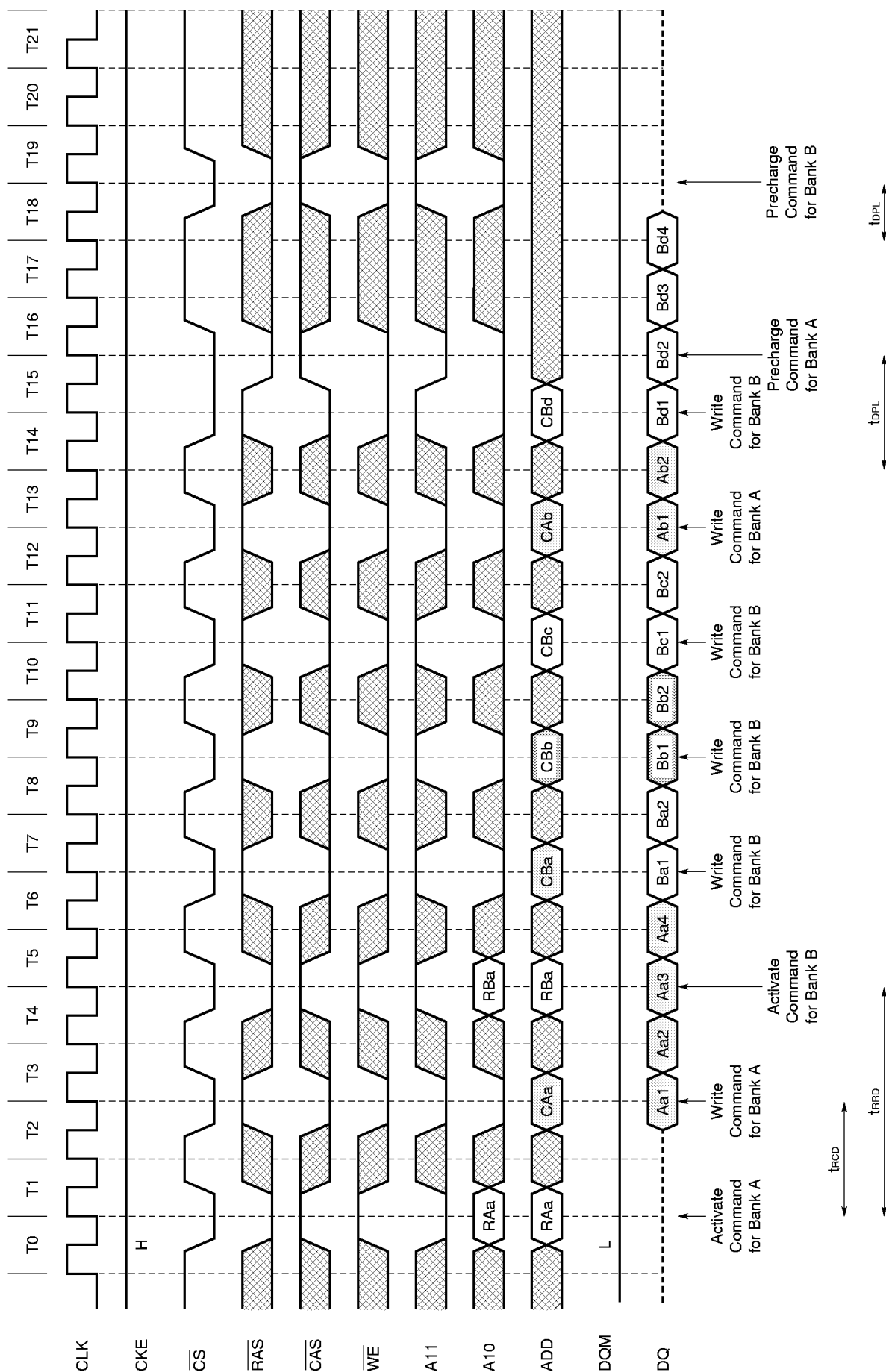
13.17 Interleaved Column READ Cycle (1/2) (Burst length = 4, CAS latency = 2)



Interleaved Column READ Cycle (2/2) (Burst length = 4, CAS latency = 3)



13.18 Interleaved Column WRITE Cycle (1/2) (Burst length = 4, CAS latency = 2)



The diagram illustrates the timing of a 2-bank DDR2 SDRAM. The horizontal axis represents time, divided into clock cycles T0 through T21. The vertical axis lists the signals: CLK, CKE, CS, RAS, CAS, WE, A11, A10, ADD, DQM, and DQ.

Signal Waveforms:

- CLK:** A periodic square wave clock signal.
- CKE:** A signal that is high (H) from T0 to T1 and then low (L) for the remainder of the sequence.
- CS:** A signal that is high (H) from T0 to T1 and then low (L) for the remainder of the sequence.
- RAS:** A signal that is high (H) from T0 to T1 and then low (L) for the remainder of the sequence.
- CAS:** A signal that is high (H) from T0 to T1 and then low (L) for the remainder of the sequence.
- WE:** A signal that is high (H) from T0 to T1 and then low (L) for the remainder of the sequence.
- A11:** A signal that is high (H) from T0 to T1 and then low (L) for the remainder of the sequence.
- A10:** A signal that is high (H) from T0 to T1 and then low (L) for the remainder of the sequence.
- ADD:** A signal that is high (H) from T0 to T1 and then low (L) for the remainder of the sequence.
- DQM:** A signal that is high (H) from T0 to T1 and then low (L) for the remainder of the sequence.
- DQ:** A signal that is high (H) from T0 to T1 and then low (L) for the remainder of the sequence.

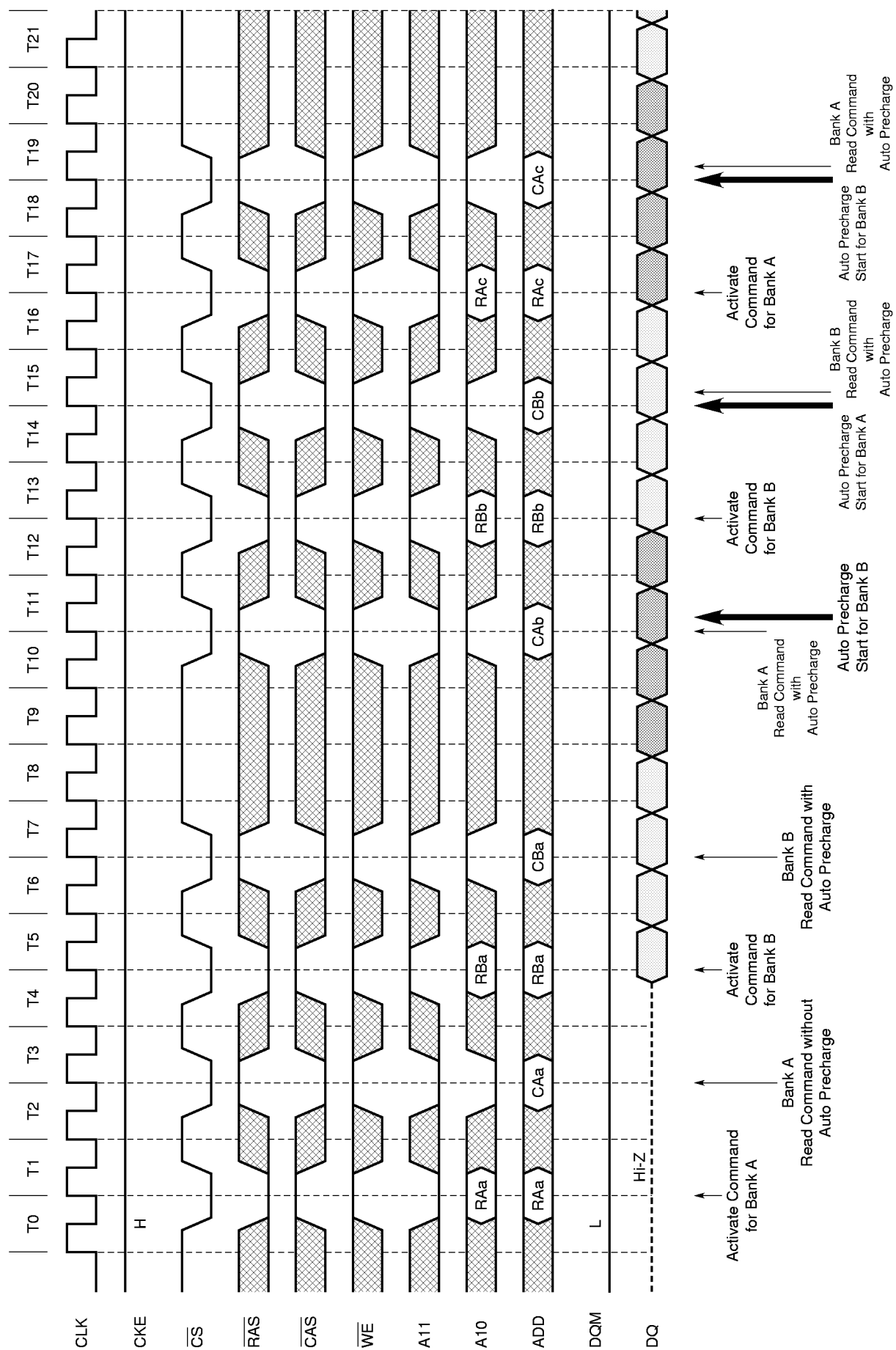
Command Sequence:

- Bank A:**
 - Activate Command for Bank A (Aa1) at T0.
 - Write Command for Bank A (Aa2) at T1.
 - Write Command for Bank A (Aa3) at T2.
 - Write Command for Bank A (Aa4) at T3.
 - Write Command for Bank A (Ba1) at T4.
 - Write Command for Bank A (Ba2) at T5.
 - Write Command for Bank A (Bb1) at T6.
 - Write Command for Bank A (Bb2) at T7.
 - Write Command for Bank A (Bc1) at T8.
 - Write Command for Bank A (Bc2) at T9.
 - Write Command for Bank A (Ab1) at T10.
 - Write Command for Bank A (Ab2) at T11.
 - Write Command for Bank A (Bd1) at T12.
 - Write Command for Bank A (Bd2) at T13.
 - Precharge Command for Bank A (Bd4) at T14.
- Bank B:**
 - Activate Command for Bank B (Ba1) at T0.
 - Write Command for Bank B (Ba2) at T1.
 - Write Command for Bank B (Bb1) at T2.
 - Write Command for Bank B (Bb2) at T3.
 - Write Command for Bank B (Bc1) at T4.
 - Write Command for Bank B (Bc2) at T5.
 - Write Command for Bank B (Cb1) at T6.
 - Write Command for Bank B (Cb2) at T7.
 - Write Command for Bank B (Cb3) at T8.
 - Write Command for Bank B (Cb4) at T9.
 - Precharge Command for Bank B (Cb4) at T10.

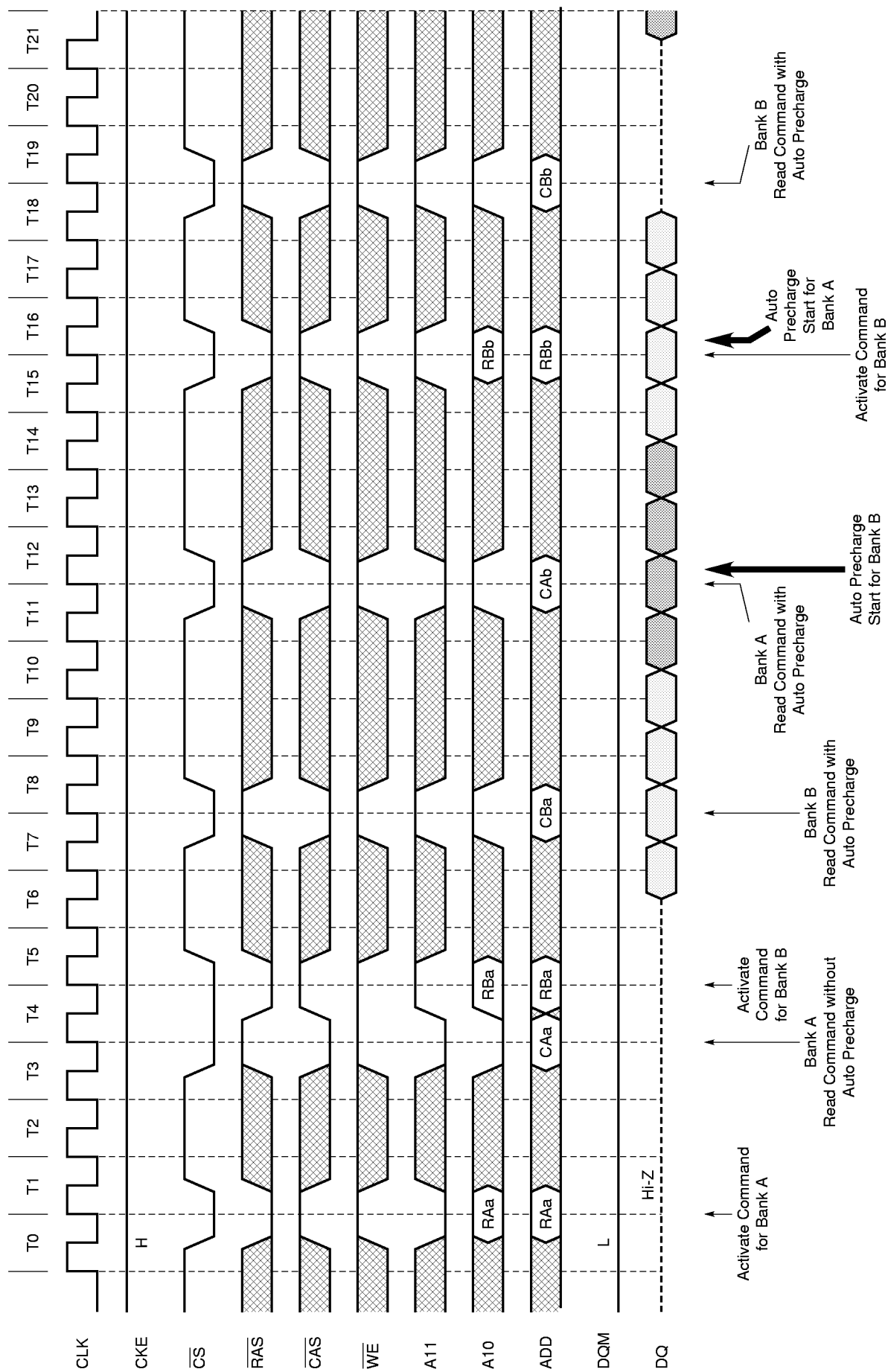
Timing Parameters:

- t_{RCD}:** Read to Command Delay, the time from the end of the activate command to the start of the first write command.
- t_{RPD}:** Row Precharge Delay, the time from the end of the precharge command to the start of the next activate command.

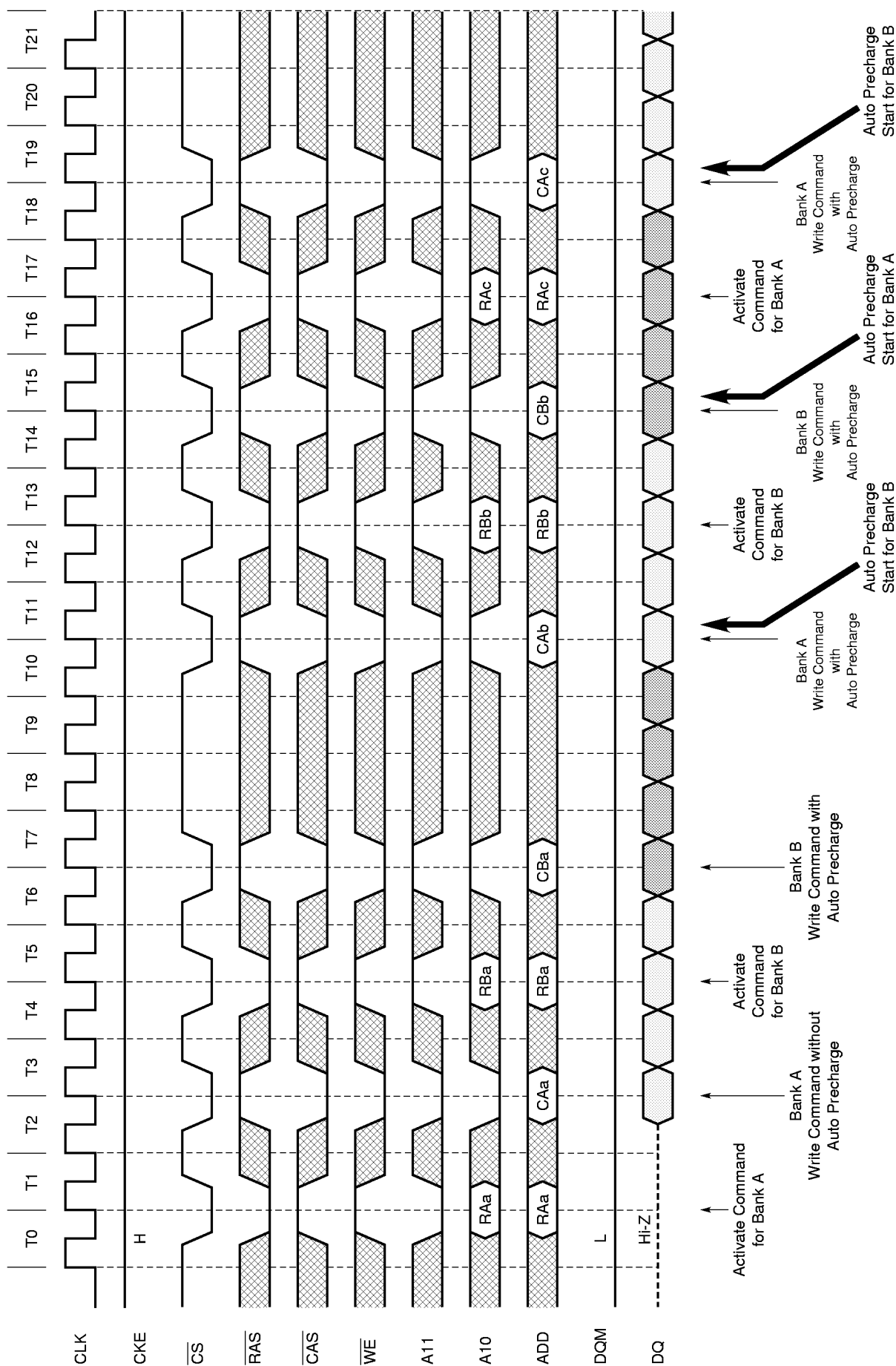
13.19 Auto Precharge after Read Burst (1/2) (Burst length = 4, CAS latency = 2)



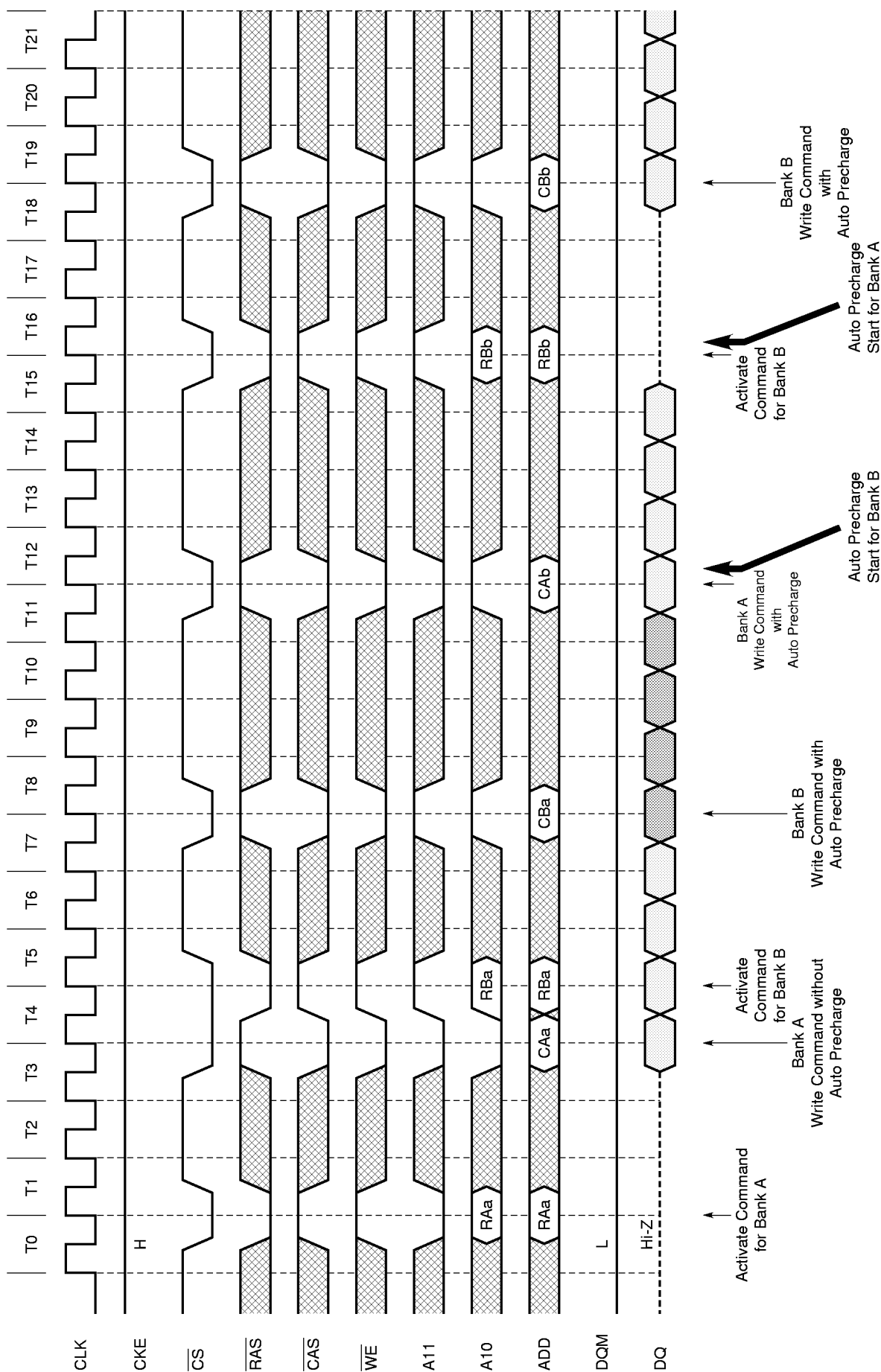
Auto Precharge after Read Burst (2/2) (Burst length = 4, CAS latency = 3)



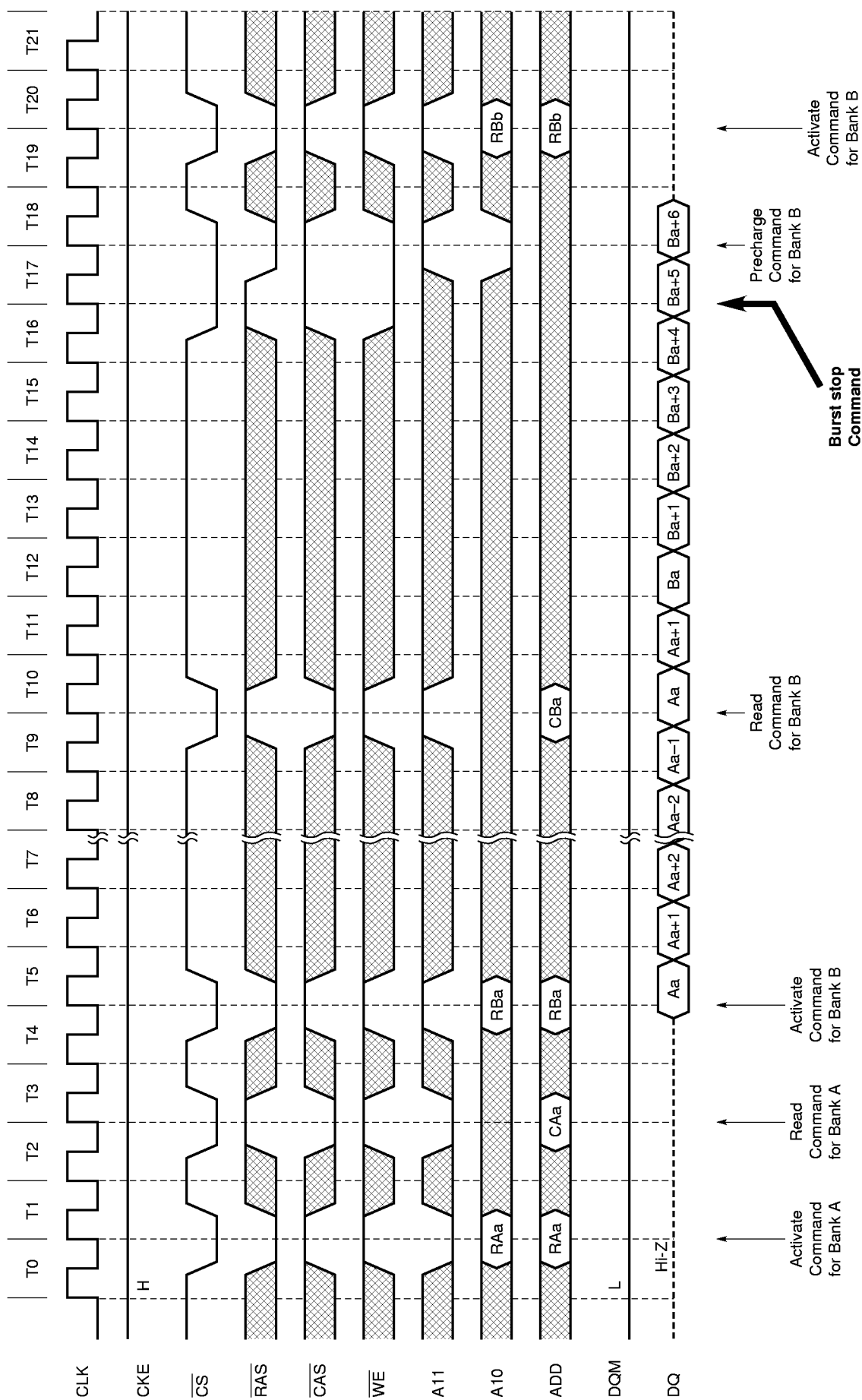
13.20 Auto Precharge after Write Burst (1/2) (Burst length = 4, CAS latency = 2)



Auto Precharge after Write Burst (2/2) (Burst length = 4, CAS latency = 3)



13.21 Full Page READ Cycle (1/2) (CAS latency = 2)



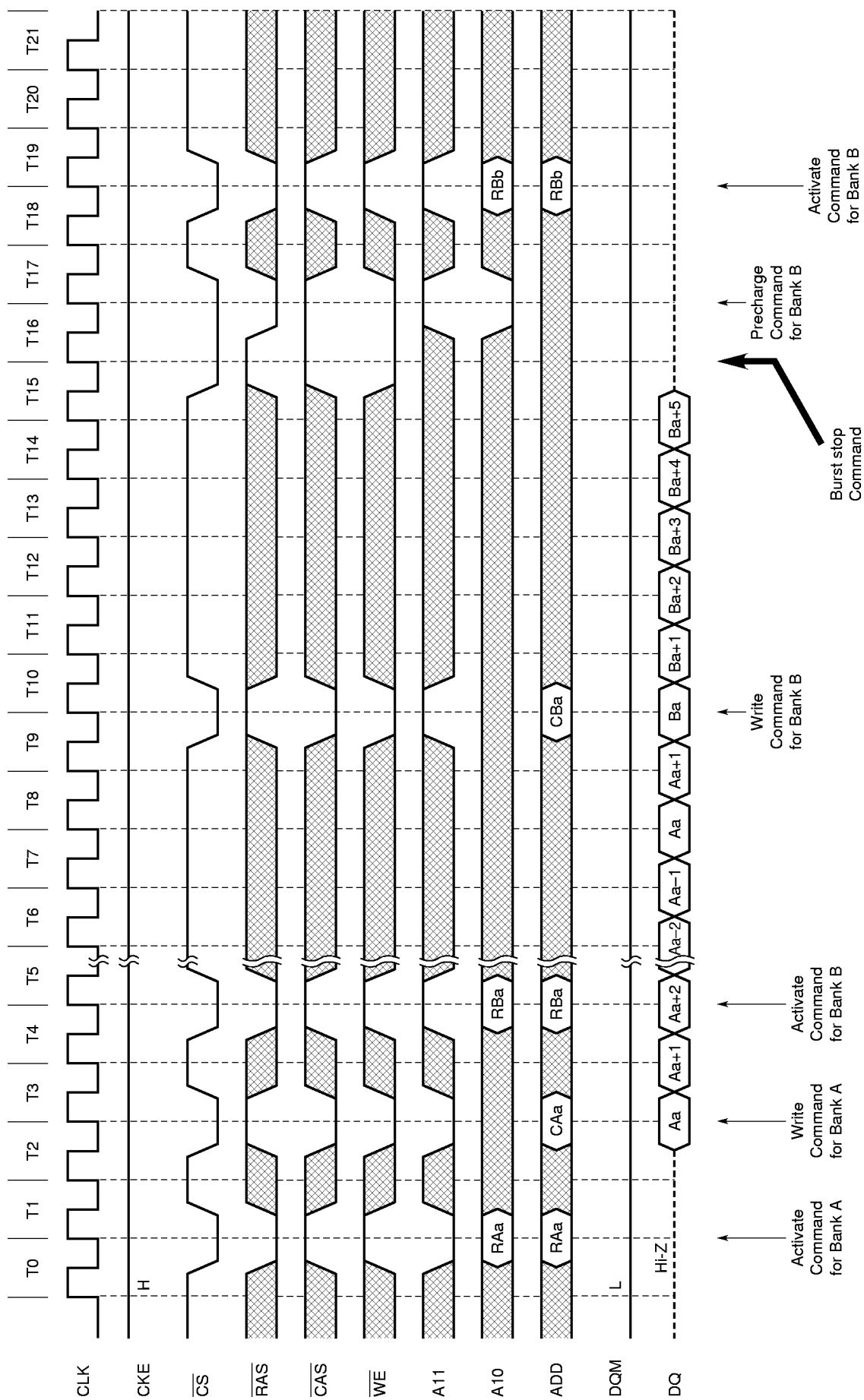
The diagram illustrates the timing of a burst stop command sequence. The horizontal axis represents time slots from T0 to T21. The vertical axis lists the signals: CLK, CKE, CS, RAS, CAS, WE, A11, A10, ADD, DQM, and DQ.

- CLK:** A periodic clock signal.
- CKE:** Clock Enable, shown as a high signal (H).
- CS:** Chip Select, shown as a high signal (H).
- RAS:** Row Address Strobe, shown as a series of pulses.
- CAS:** Column Address Strobe, shown as a series of pulses.
- WE:** Write Enable, shown as a series of pulses.
- A11:** Address bus signal, shown as a series of pulses.
- A10:** Address bus signal, shown as a series of pulses.
- ADD:** Address bus signal, shown as a series of pulses.
- DQM:** Data Mask, shown as a low signal (L).
- DQ:** Data bus signal, showing data for Bank A (Aa) and Bank B (Ba) with commands RAa, CAa, RBa, CBa, RBb, and RBb.

Annotations on the right side of the diagram indicate the following events:

- Activate Command for Bank A:** Occurs at T0.
- Read Command for Bank A:** Occurs at T3.
- Activate Command for Bank B:** Occurs at T5.
- Precharge Command for Bank B:** Occurs at T17.
- Burst stop Command:** Occurs at T15.
- Read Command for Bank B:** Occurs at T10.
- Activate Command for Bank B:** Occurs at T20.

13.22 Full Page WRITE Cycle (1/2) (CAS latency = 2)



The diagram illustrates the timing of memory controller signals over 22 clock cycles (T0 to T21). The signals are:

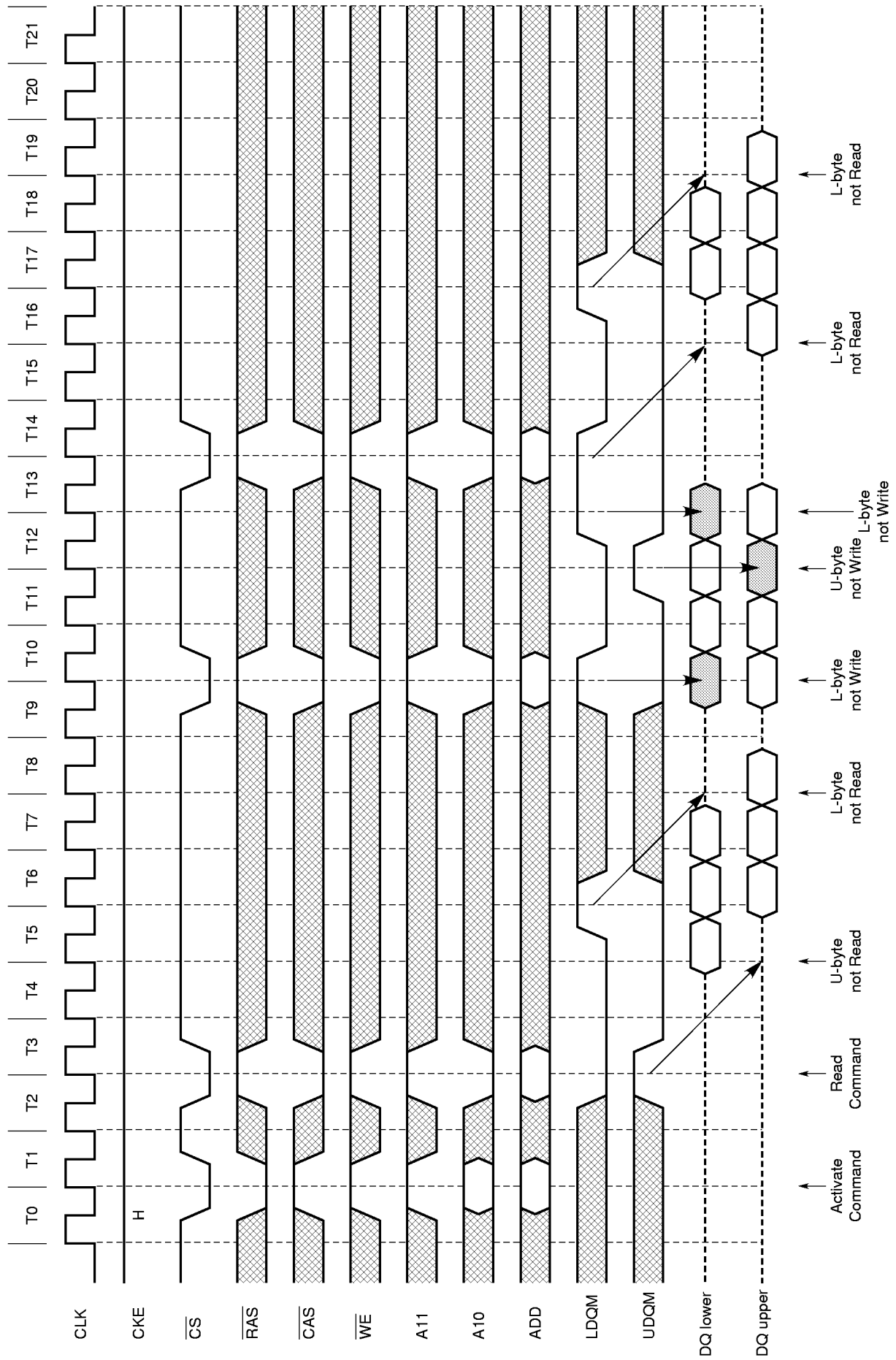
- CLK**: Clock signal, shown as a square wave.
- CKE**: Clock Enable, shown as a high signal.
- CS**: Chip Select, shown as a high signal.
- RAS**: Row Address Strobe, shown as a pulse.
- CAS**: Column Address Strobe, shown as a pulse.
- WE**: Write Enable, shown as a pulse.
- A11**: Address bus signal, shown as a sequence of pulses.
- A10**: Address bus signal, shown as a sequence of pulses.
- ADD**: Address bus signal, shown as a sequence of pulses.
- DQM**: Data Mask, shown as a low signal.
- DQ**: Data bus signal, shown as a sequence of pulses.

The diagram is divided into two main sections by a dashed line at T10. The first section (T0 to T10) shows the sequence of commands for Bank A, and the second section (T11 to T21) shows the sequence of commands for Bank B. The commands are:

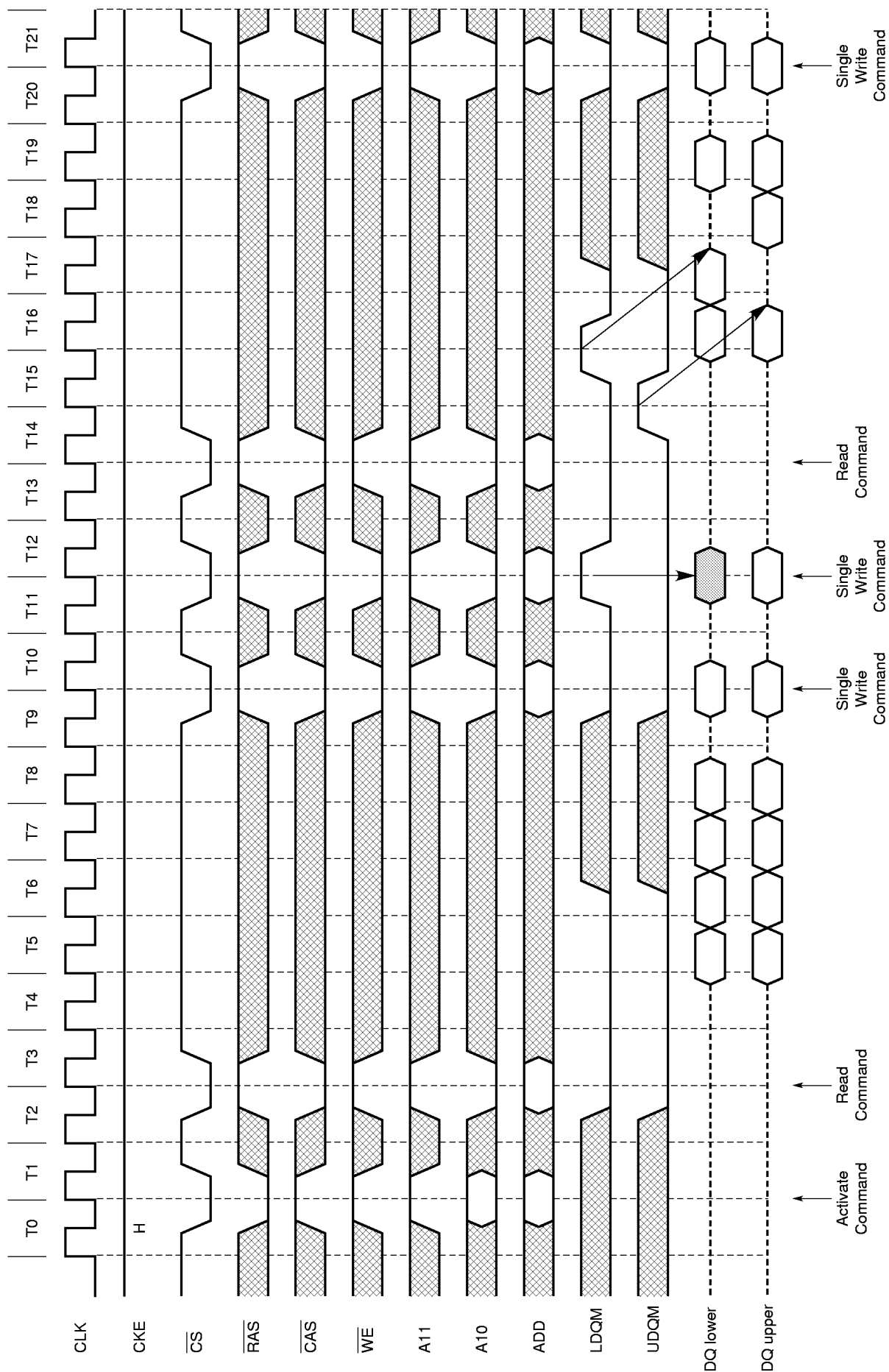
- Bank A Commands:** Activate Command for Bank A (T0), Write Command for Bank A (T1), Activate Command for Bank A (T2), Write Command for Bank A (T3), Activate Command for Bank A (T4), Write Command for Bank A (T5), Activate Command for Bank A (T6), Write Command for Bank A (T7), Activate Command for Bank A (T8), Write Command for Bank A (T9), Activate Command for Bank A (T10).
- Bank B Commands:** Activate Command for Bank B (T11), Write Command for Bank B (T12), Activate Command for Bank B (T13), Write Command for Bank B (T14), Activate Command for Bank B (T15), Precharge Command for Bank B (T16), Activate Command for Bank B (T17), Write Command for Bank B (T18), Activate Command for Bank B (T19), Write Command for Bank B (T20), Activate Command for Bank B (T21).

The data bus (DQ) shows the resulting data bursts for each command. The bursts are labeled with addresses: Aa, Aa+1, Aa+2, Aa+3, Aa+4, Ba, Ba+1, Ba+2, Ba+3, Ba+4. The diagram also shows the timing of the data mask (DQM) and the data bus (DQ) signals.

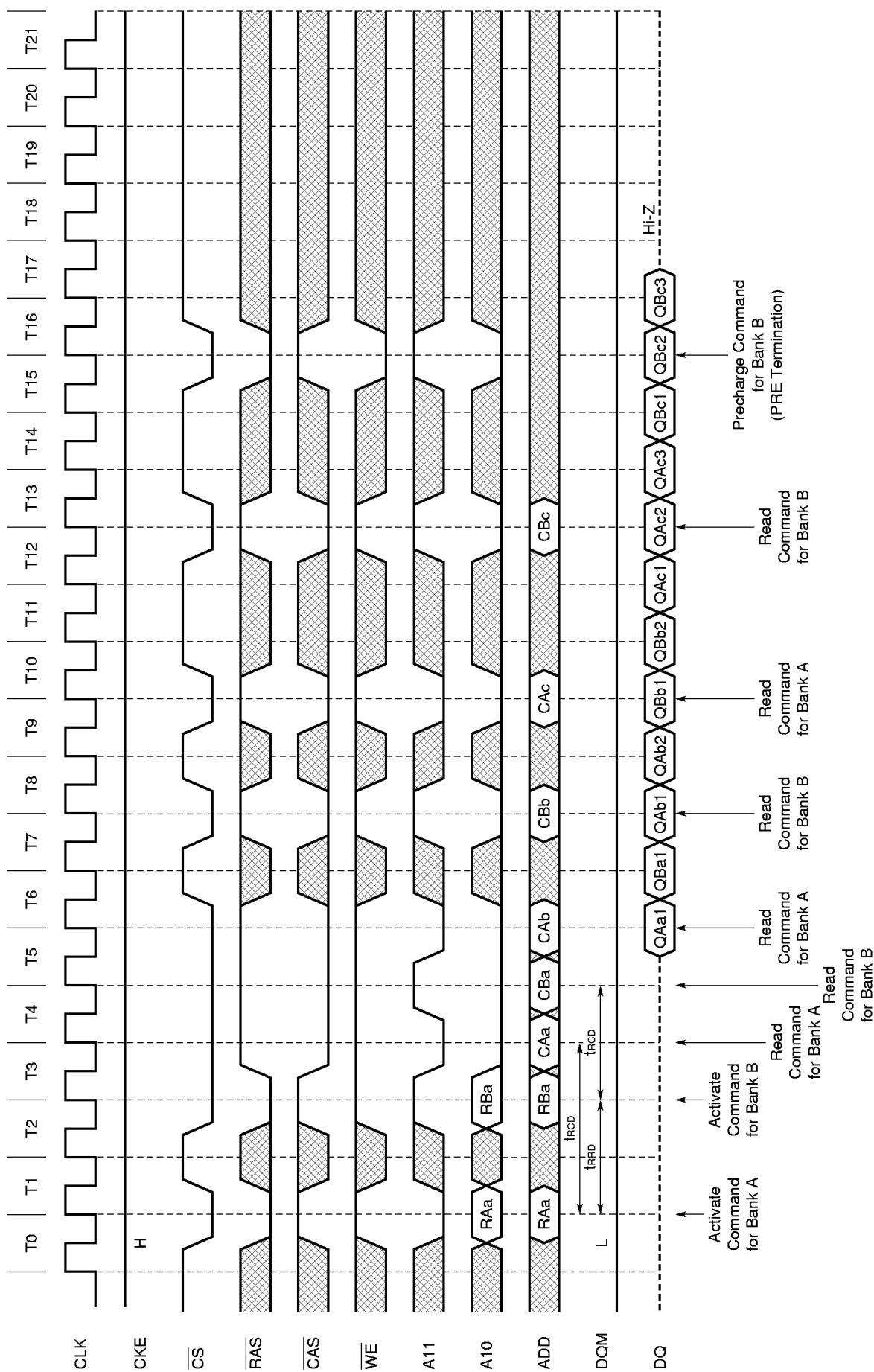
13.23 Byte Write Operation (Burst length = 4, CAS latency = 2)



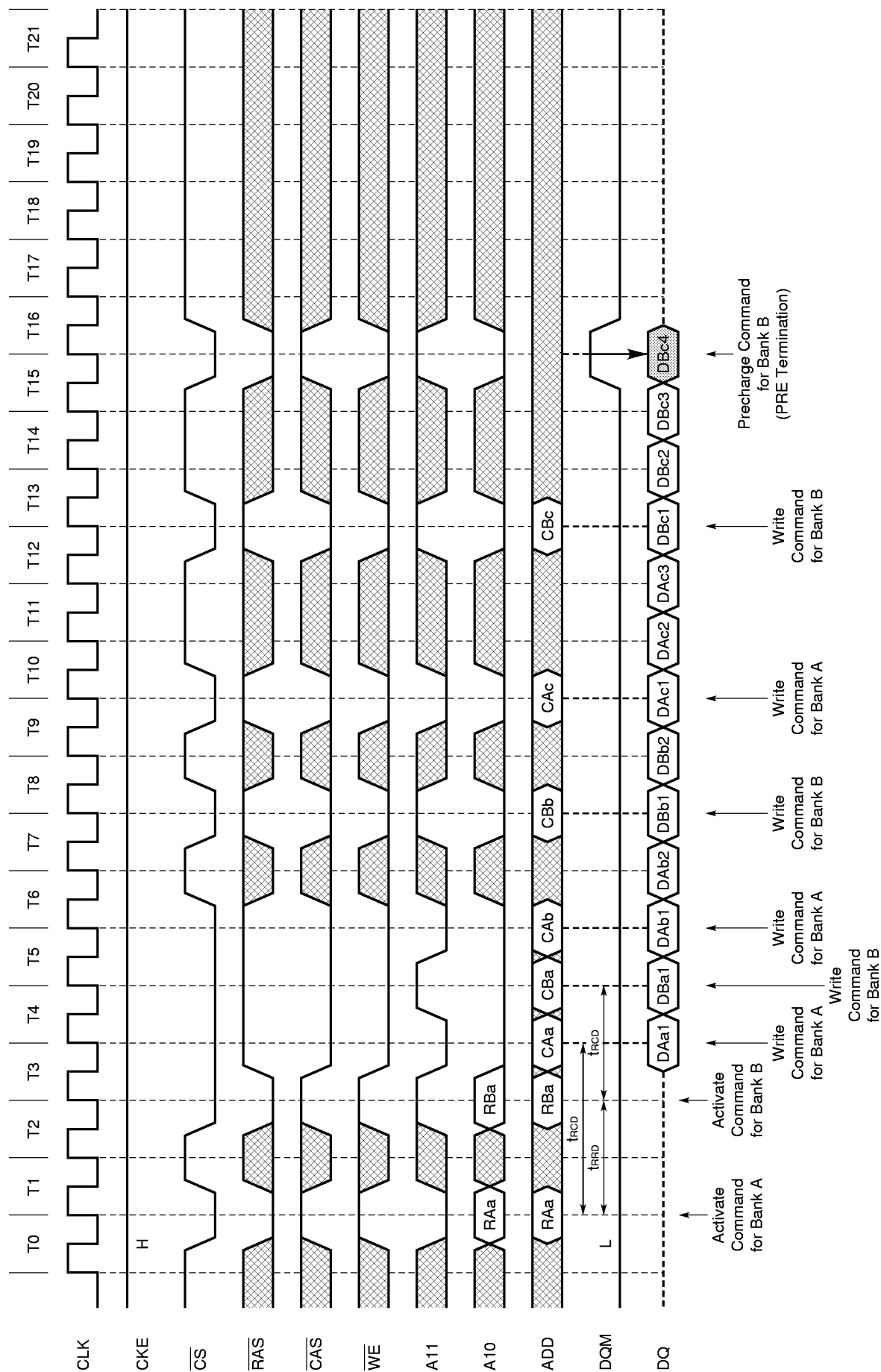
13.24 Burst Read and Single Write (Option) (Burst length = 4, CAS latency = 2)



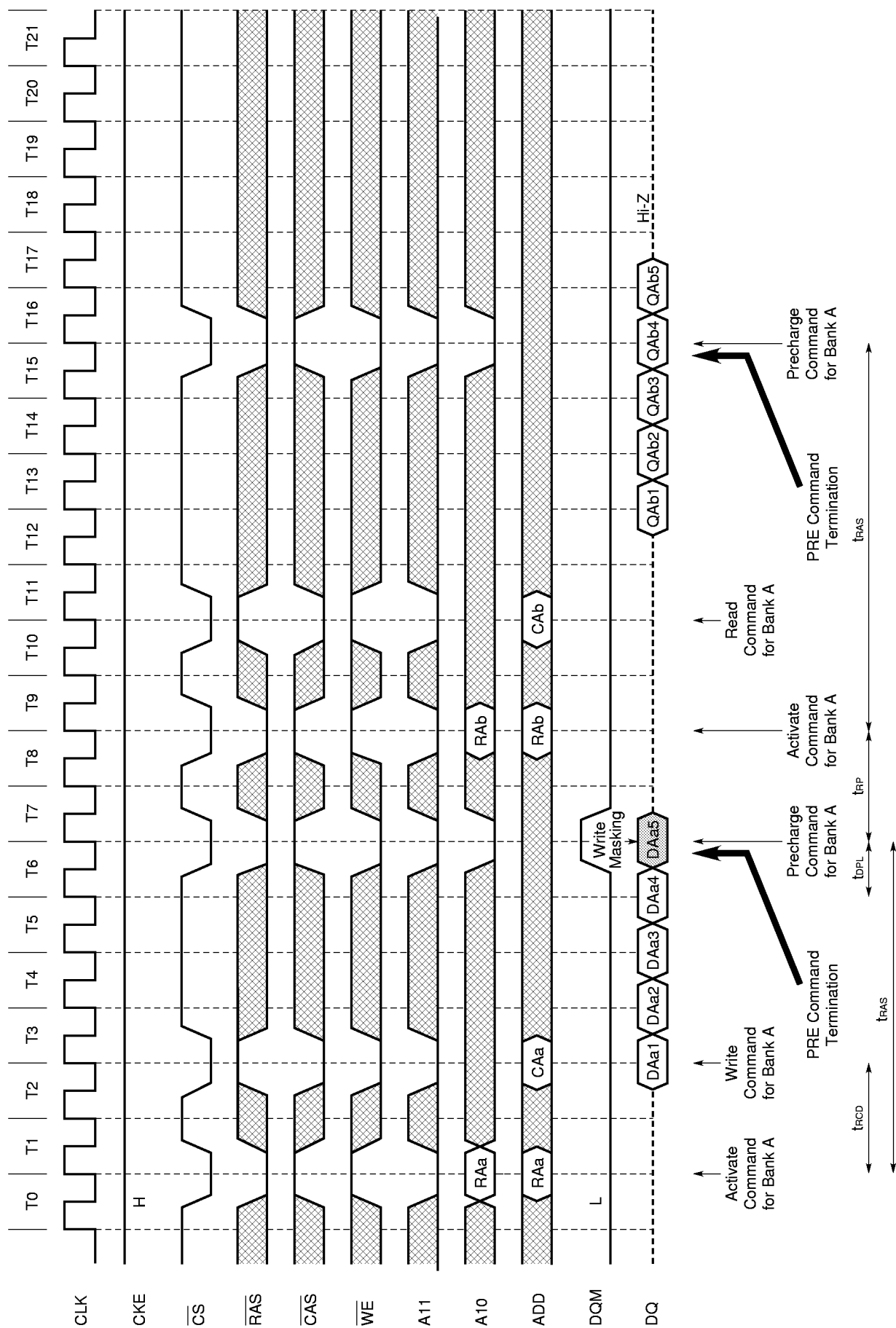
13.2.5 Full Page Random Column Read (Burst length = Full Page, CAS latency = 2)



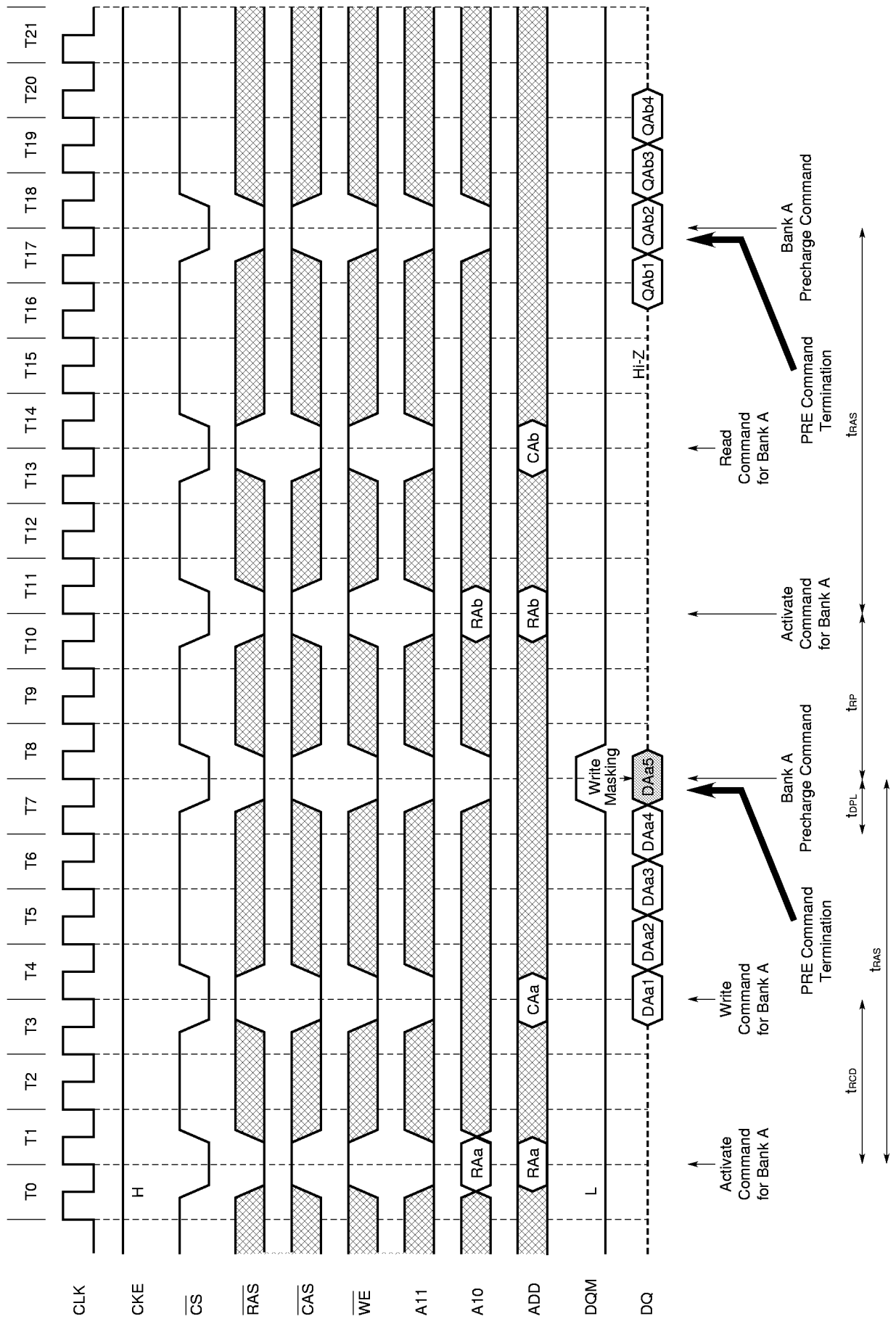
13.26 Full Page Random Column Write (Burst length = Full Page, CAS latency = 2)



13.27 PRE(Precharge)Termination of Burst (1/2) (Burst length = 8, CAS latency = 2)

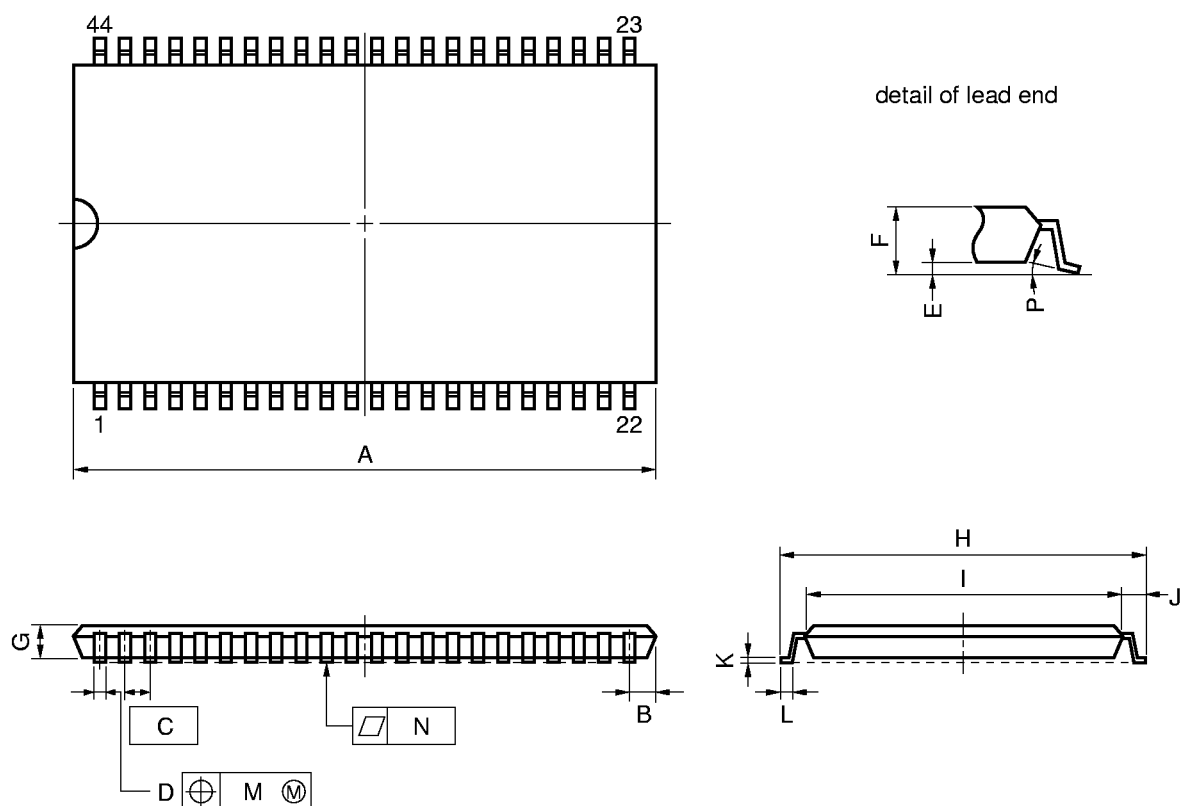


PRE(Precharge)Termination of Burst (2/2) (Burst length = 8, CAS latency = 3)



14. Package Drawings

44PIN PLASTIC TSOP(II) (400 mil)



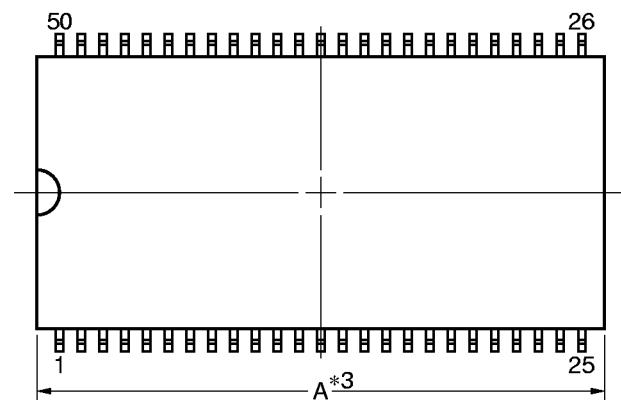
NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

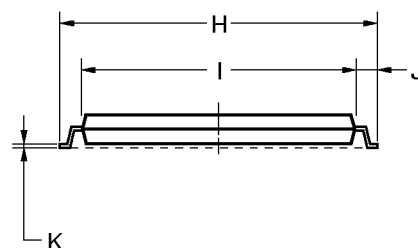
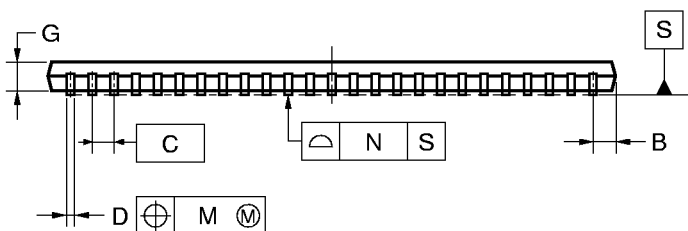
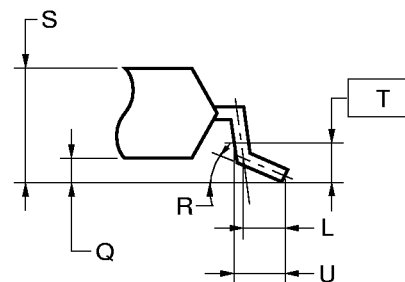
ITEM	MILLIMETERS	INCHES
A	18.63 MAX.	0.734 MAX.
B	0.93 MAX.	0.037 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	$0.32^{+0.08}_{-0.07}$	0.013 ± 0.003
E	0.1 ± 0.05	0.004 ± 0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	11.76 ± 0.2	0.463 ± 0.008
I	10.16 ± 0.1	0.400 ± 0.004
J	0.8 ± 0.2	$0.031^{+0.009}_{-0.008}$
K	$0.145^{+0.025}_{-0.015}$	0.006 ± 0.001
L	0.5 ± 0.1	$0.020^{+0.004}_{-0.005}$
M	0.13	0.005
N	0.10	0.004
P	$3^{\circ} + 7^{\circ}_{-3^{\circ}}$	$3^{\circ} + 7^{\circ}_{-3^{\circ}}$

S44G5-80-7JF3

50PIN PLASTIC TSOP(II) (400 mil)



detail of lead end



NOTE

1. Controlling dimension — millimeter.
2. Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.
- *3. Dimension "A" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm(0.006inch) per side.

ITEM	MILLIMETERS	INCHES
A	20.86±0.04	0.821±0.002
B	1.0 MAX.	0.040 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	0.32 ^{+0.08} _{-0.07}	0.013±0.003
G	1.0±0.05	0.039 ^{+0.003} _{-0.002}
H	11.76±0.2	0.463±0.008
I	10.11±0.04	0.398±0.002
J	0.825±0.2	0.032 ^{+0.009} _{-0.008}
K	0.145 ^{+0.025} _{-0.015}	0.006±0.001
L	0.5	0.020
M	0.13	0.005
N	0.10	0.004
Q	0.1±0.05	0.004±0.002
R	3 ^{+5°} _{-3°}	3 ^{+5°} _{-3°}
S	1.2MAX.	0.048MAX.
T	0.25(T.P.)	0.010(T.P.)
U	0.60±0.15	0.024 ^{+0.006} _{-0.007}

S50G5-80-9NF

15. Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μ PD4516421A, 4516821A, 4516161A.

Types of Surface Mount Device

μ PD4516421AG5-7JF, 4516821AG5-7JF: 44-pin plastic TSOP (II) (400 mil)

μ PD4516161AG5-9NF: 50-pin plastic TSOP (II) (400 mil)