NEC

MOS INTEGRATED CIRCUIT

μPD46258, 46259L

256K-BIT BiCMOS FAST STATIC RAM
32K-WORD BY 8-BIT/32K-WORD BY 9-BIT

Description

The μPD46258 is 262,144 bits (32,768 words by 8 bits) and the μPD46259L is 294,912 bits (32,768 words by 9 bits) BiCMOS static RAMs.

Operating supply voltage is 5 V ±10 % for the μPD46258 or 3.3 V ±0.3 V for the μPD46259L.

The μPD46258 and 46259L are packed in 32-pin plastic SOJ.

Features

- 32,768 words by 8 or 9 bits organization
- Output Enable input for easy application
- Fast access time

Ordering Information

Part number	Package	Word organization	Access time ns (MAX.)	Supply voltage (TYP.)	Supply current mA (MAX.)	
					Operating	Standby
μPD46258LA-6	32-Pin plastic SOJ (300 mil)	32K × 8 bits	6	5 V ± 10 %	190	50
μPD46258LA-7			7			
μPD46258LA-8			8			
μPD46259LLA-A12		32K × 9 bits	12	3.3 V ± 0.3 V	130	20

Quality grade

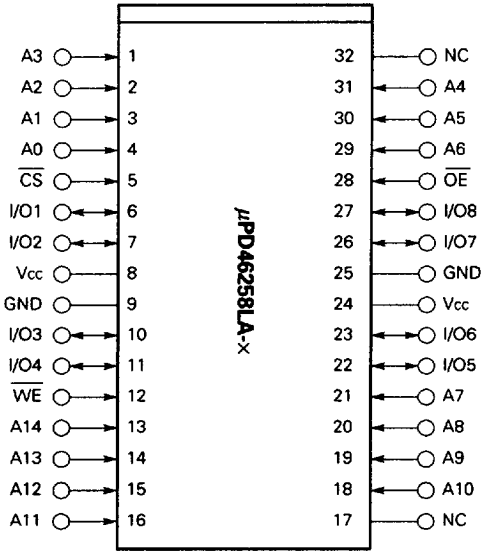
Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

Pin Configuration (Marking Side)

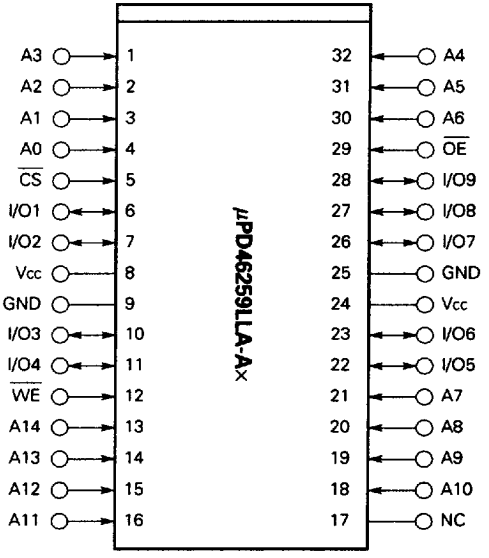
- **μPD46258**

32-pin Plastic SOJ (300 mil)



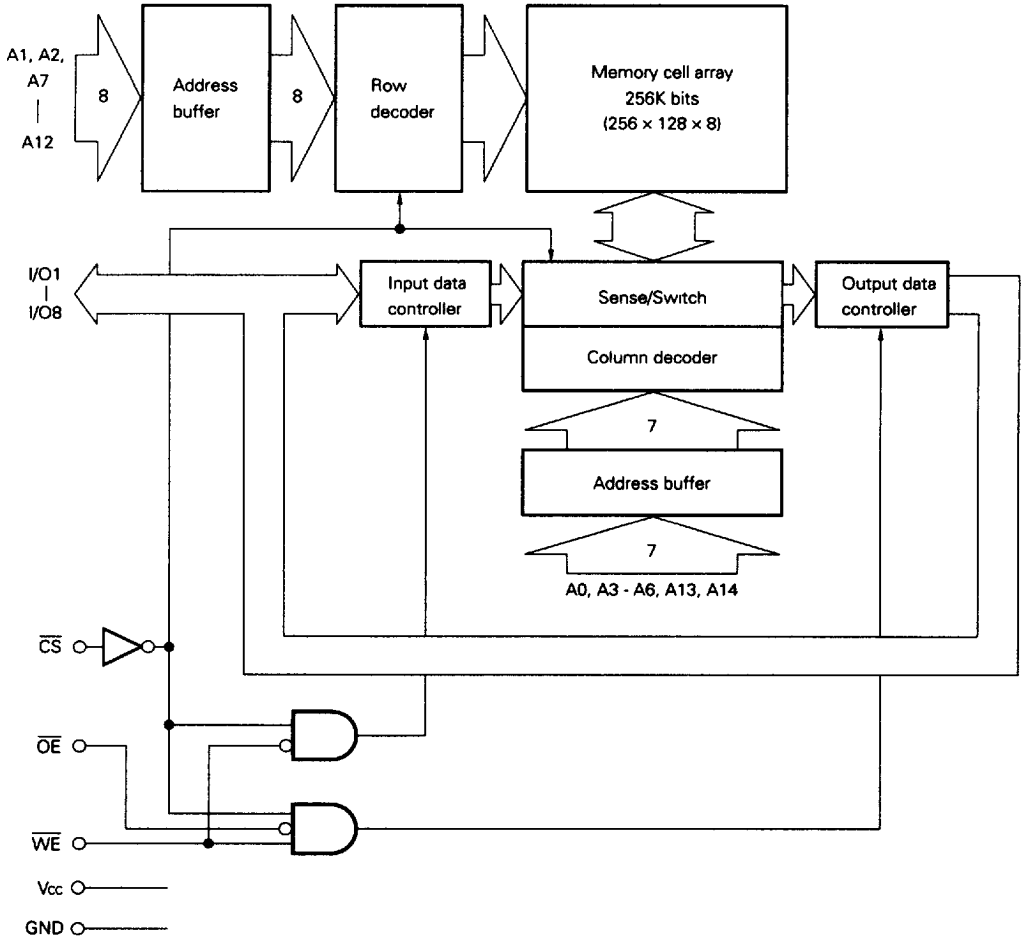
- **μPD46259L**

32-pin Plastic SOJ (300 mil)

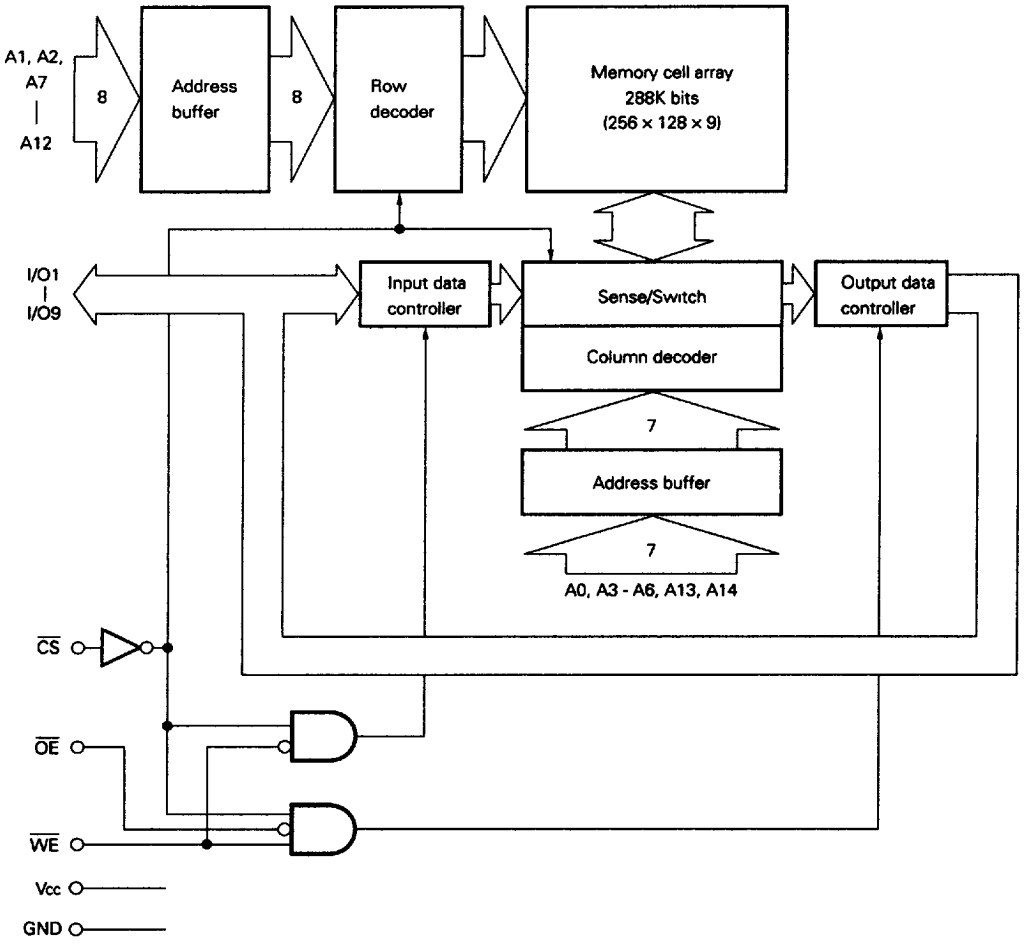


A0 - A14	:	Address inputs
I/O1 - I/O9	:	Data inputs/outputs
$\overline{CS}$	:	Chip Select
$\overline{WE}$	:	Write Enable
$\overline{OE}$	:	Output Enable
Vcc	:	Power Supply
GND	:	Ground
NC	:	No Connection

Block Diagram (μPD46258)



Block Diagram (μPD46259L)



Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Supply current
H	×	×	Not selected	High impedance	I_{SB}
L	L	H	Read	D_{OUT}	I_{CC}
L	×	L	Write	D_{IN}	
L	H	H	Output disable	High impedance	

Remark ×: Don't care

Electrical Characteristics

The device is tested under the minimum transverse air flow of 2.5 meters per second for the DC and AC specifications shown in the following tables.

Absolute Maximum Ratings

Parameter	Symbol	μPD46258	μPD46259L	Unit
Supply voltage	V_{CC}	−0.5 Note 1 to +7.0	−0.5 Note 2 to +4.5	V
Input voltage	V_{IN}	−0.5 Note 1 to V_{CC} + 0.5	−0.5 Note 2 to V_{CC} + 0.5	V
Input/Output voltage	$V_{I/O}$	−0.5 Note 1 to +4.5	−0.5 Note 2 to V_{CC}	V
Operating temperature	T_{opt}	0 to 70		°C
Storage temperature	T_{stg}	−55 to +125		°C

Note 1. −1.0 V (MIN.): (Pulse width 3 ns)
2. −2.5 V (MIN.): (Pulse width 3 ns)

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	μPD46258			μPD46259L			Unit
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply voltage	V_{CC}	4.5	5.0	5.5	3.0	3.3	3.6	V
High level input voltage	V_{IH}	2.2		3.5	2.0		V_{CC} + 0.5	V
Low level input voltage	V_{IL}	−0.5 Note 1		+0.8	−0.5 Note 2		+0.8	°C
Ambient temperature	T_a	0		+70	0		+70	°C

Note 1. −1.0 V (MIN.): (Pulse width 3 ns)
2. −2.5 V (MIN.): (Pulse width 3 ns)

DC Characteristics (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test conditions		μPD46258			μPD46259L			Unit
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input leakage current	I_{LI}	V_{IN} = 0 V to V_{CC}		−10		+10	−10		+10	μA
I/O leakage current	I_{LO}	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}	$V_{I/O}$ = 0 V to 3.5 V	−10		+10	−		−	μA
			$V_{I/O}$ = 0 V to V_{CC}	−		−	−10		+10	
Operating supply current	I_{CC}	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA	Cycle frequency ≤ 100 MHz			190			130	mA
			Cycle frequency = 0 MHz			130			110	
Standby supply current	I_{SB}	$\overline{CS}$ = V_{IH}, V_{IN} = V_{IH} or V_{IL}				70			40	mA
	I_{SB1}	$\overline{CS}$ ≥ V_{CC} − 0.2 V, V_{IN} ≤ 0.2 V or V_{IN} ≥ V_{CC} − 0.2 V				50			20	
High level output voltage	V_{OH}	I_{OH} = −4.0 mA		2.4			−			V
		I_{OH} = −2.0 mA		−			2.4			
Low level output voltage	V_{OL}	I_{OL} = 8.0 mA				0.4			−	V
		I_{OL} = 4.0 mA				−			0.4	

Remark V_{IN}: Input voltage

Capacitance (T_a = 25 °C, f = 1 MHz)

Parameter	Symbol	Test conditions	μPD46258			μPD46259L			Unit
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input capacitance	C_{IN}	V_{IN} = 0 V			7			8	pF
Input/Output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			5			6	pF

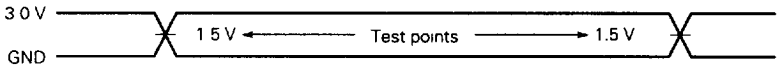
Remark 1. V_{IN}: Input voltage

2. These parameters are sampled and not 100 % tested.

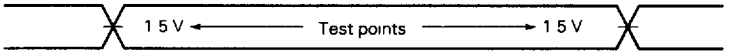
AC Characteristics (Recommended operating conditions unless otherwise noted)

AC Test Conditions

Input waveform (Rise/Fall Time ≤ 2 ns)



Output waveform



Output load

AC characteristics directed with the **notes** should be measured with the following output load shown in **Fig. 1** to **Fig. 4**.

t_{AA}, t_{ACS}, t_{DE}, t_{OH} (for μPD46258) are measured with the output load shown in **Fig. 1**.
t_{AA}, t_{ACS}, t_{OE}, t_{OH} (for μPD46259L) are measured with the output load shown in **Fig. 2**.
t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, t_{OW} (for μPD46258) are measured with the output load shown in **Fig. 3**.
t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, t_{OW} (for μPD46259L) are measured with the output load shown in **Fig. 4**.

Fig. 1 Output load (for μPD46258)
(t_{AA}, t_{ACS}, t_{OE}, t_{OH})

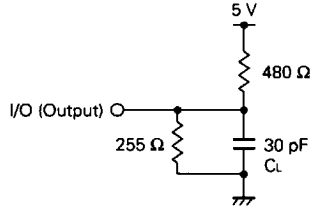


Fig. 2 Output load (for μPD46259L)
(t_{AA}, t_{ACS}, t_{OE}, t_{OH})

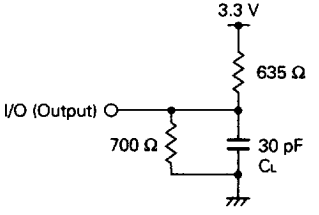


Fig. 3 Output load (for μPD46258)
(t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, t_{OW})

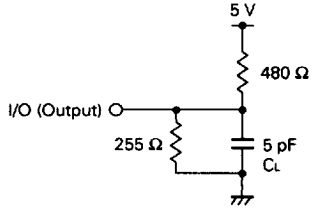
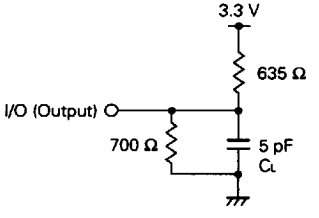


Fig. 4 Output load (for μPD46259L)
(t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, t_{OW})



Remark C_L (for **Fig. 1** to **Fig. 4**) includes capacitances of the probe and jig, stray capacitances.

Read Cycle (μPD46258: Vcc = 5 V ±10 %)

Parameter	Symbol	μPD46258-6		μPD46258-7		μPD46258-8		Unit	Condition
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	6		7		8		ns	
Address access time	t_{AA}		6		7		8	ns	Note 1.
$\overline{CS}$ access time	t_{ACS}		6		7		8	ns	
$\overline{OE}$ access time	t_{OE}		4		5		5	ns	
Output hold from address change	t_{OH}	3		3		3		ns	
$\overline{CS}$ to output in low impedance	t_{CLZ}	2		2		2		ns	Note 2.
$\overline{OE}$ to output in low impedance	t_{OLZ}	1		1		1		ns	
$\overline{CS}$ to output in high impedance	t_{CHZ}		3		4		4	ns	
$\overline{OE}$ to output in high impedance	t_{OHZ}		3		4		4	ns	

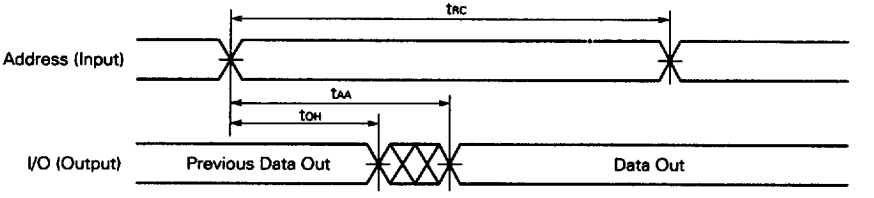
Note 1. See the output load shown in **Fig. 1.**
2. See the output load shown in **Fig. 3.**

Read Cycle (μPD46259L: Vcc = 3.3 V ±0.3 V)

Parameter	Symbol	μPD46259L-A12		Unit	Condition
		MIN.	MAX.		
Read cycle time	t_{RC}	12		ns	
Address access time	t_{AA}		12	ns	Note 1.
$\overline{CS}$ access time	t_{ACS}		12	ns	
$\overline{OE}$ access time	t_{OE}		6	ns	
Output hold from address change	t_{OH}	2		ns	
$\overline{CS}$ to output in low impedance	t_{CLZ}	2		ns	Note 2.
$\overline{OE}$ to output in low impedance	t_{OLZ}	1		ns	
$\overline{CS}$ to output in high impedance	t_{CHZ}		5	ns	
$\overline{OE}$ to output in high impedance	t_{OHZ}		5	ns	

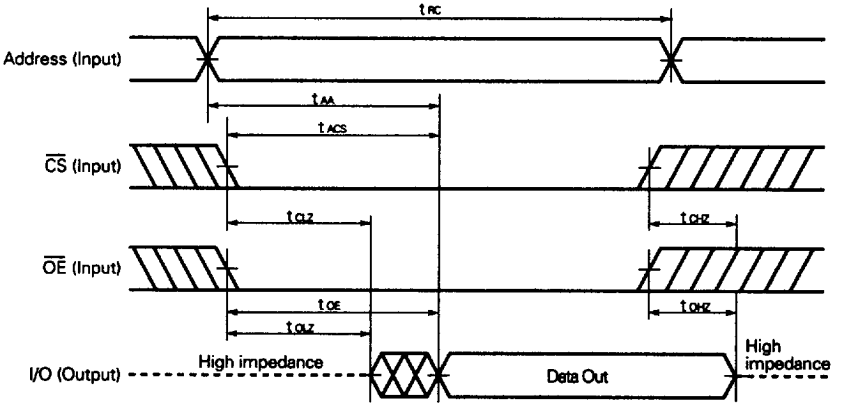
Note 1. See the output load shown in **Fig. 2.**
2. See the output load shown in **Fig. 4.**

Read Cycle Timing Chart 1 (Address Access)



Remark 1. In read cycle, $\overline{WE}$ should be fixed to high level.
2. $\overline{CS}$ = $\overline{OE}$ = V_{IL}

Read Cycle Timing Chart 2 ($\overline{CS}$ Access)



Caution Address valid prior to or coincident with $\overline{CS}$ low level input.

Remark In read cycle, $\overline{WE}$ should be fixed to high level.

Write Cycle (μPD46258: Vcc = 5 V ±10 %)

Parameter	Symbol	μPD46258-6		μPD46258-7		μPD46258-8		Unit	Condition
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	6		7		8		ns	
$\overline{CS}$ to end of write	t_{CW}	4		5		6		ns	
Address valid to end of write	t_{AW}	4		5		6		ns	
Write pulse width	t_{WP}	4		5		6		ns	
Data valid to end of write	t_{DW}	3		4		5		ns	
Data hold time	t_{DH}	0		0		0		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write recovery time	t_{WR}	0		0		0		ns	
$\overline{WE}$ to output in high impedance	t_{WHZ}		3		4		4	ns	Note
Output active from end of write	t_{OW}	1		1		1		ns	

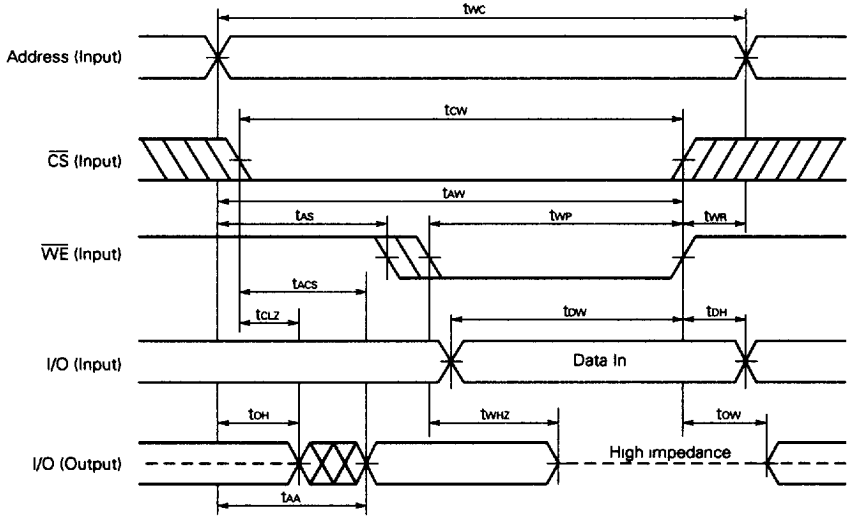
Note See the output load shown in **Fig. 3.**

Write Cycle (μPD46259L: Vcc = 3.3 V ±0.3 V)

Parameter	Symbol	μPD46259L-A12		Unit	Condition
		MIN.	MAX.		
Write cycle time	t_{WC}	10		ns	
$\overline{CS}$ to end of write	t_{CW}	7		ns	
Address valid to end of write	t_{AW}	7		ns	
Write pulse width	t_{WP}	7		ns	
Data valid to end of write	t_{DW}	6		ns	
Data hold time	t_{DH}	0		ns	
Address setup time	t_{AS}	0		ns	
Write recovery time	t_{WR}	0		ns	
$\overline{WE}$ to output in high impedance	t_{WHZ}		5	ns	Note
Output active from end of write	t_{OW}	1		ns	

Note See the output load shown in **Fig. 4.**

Write Cycle Timing Chart 1 ($\overline{WE}$ Controlled)



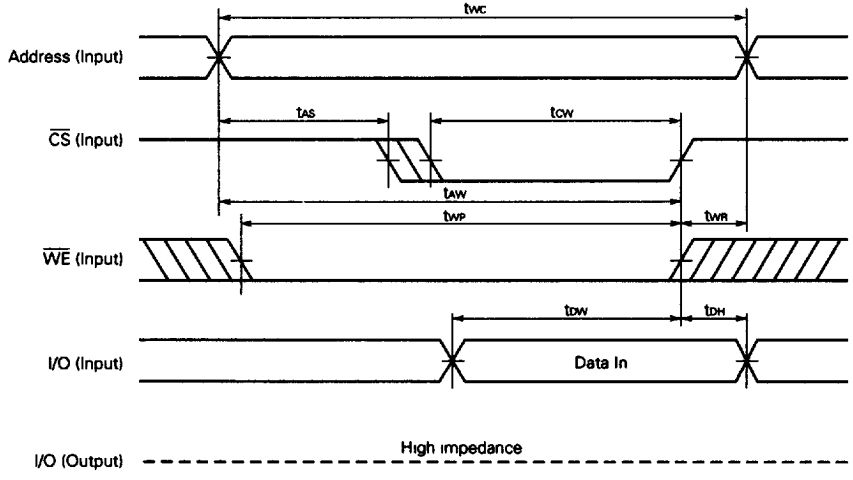
Caution $\overline{CS}$ or $\overline{WE}$ should be fixed to high level during address transition.

Remark 1. Write operation is done during the overlap time of a low level $\overline{CS}$ and a low level $\overline{WE}$.

2. During twhz, I/O pins are in the output state, therefore the input signals of opposite phase to the output must not be applied.

3. When $\overline{WE}$ is at low level, the I/O pins are always High impedance. When $\overline{WE}$ is at high level, read operation is executed. Therefore $\overline{OE}$ should be at high level to make the I/O pins high impedance.

Write Cycle Timing Chart 2 ($\overline{CS}$ Controlled)

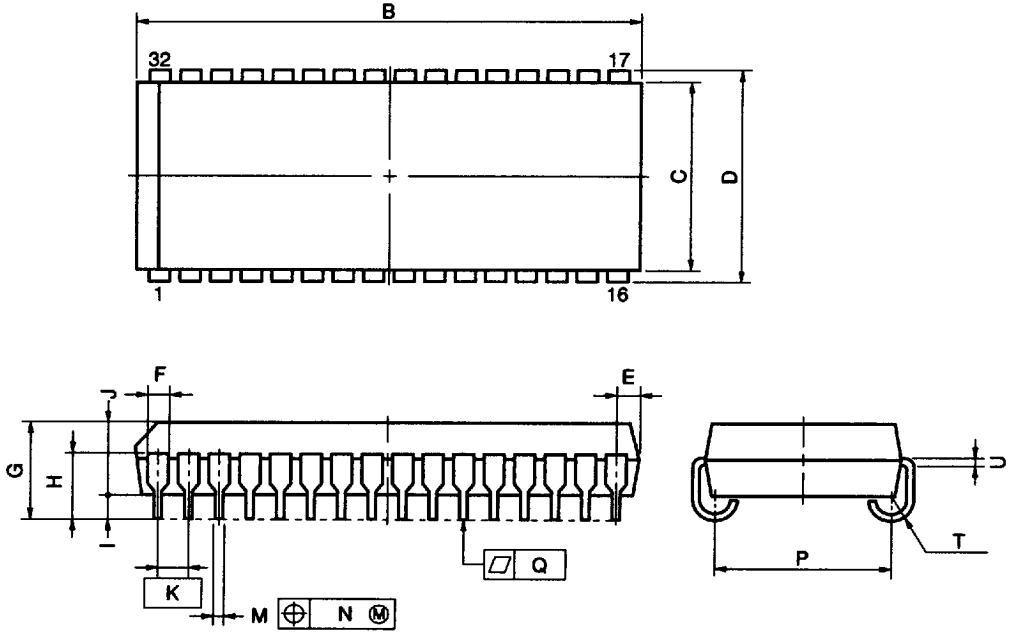


Caution $\overline{CS}$ or $\overline{WE}$ should be fixed to high level during address transition.

Remark Write operation is done during the overlap time of a low level $\overline{CS}$ and a low level $\overline{WE}$.

Package Drawing

32 PIN PLASTIC SOJ (300 mil)



NOTE
Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	$21.21^{+0.2}_{-0.35}$	$0.835^{+0.008}_{-0.014}$
C	7.57	0.298
D	8.47±0.2	$0.333^{+0.009}_{-0.008}$
E	1.08±0.15	$0.043^{+0.006}_{-0.007}$
F	0.74	0.029
G	3.5±0.2	0.138±0.008
H	2.4±0.2	$0.094^{+0.009}_{-0.008}$
I	0.8 MIN.	0.031 MIN.
J	2.55	0.1
K	1.27(T.P.)	0.050(T.P.)
M	0.40±0.10	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	6.73±0.20	0.265±0.008
Q	0.10	0.004
T	R0.85	R0.033
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

P32LA-300A-1

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μPD46258 and 46259L.

Types of Surface Mount Device

μPD46258LA : 32-pin plastic SOJ (300 mil)
μPD46259LLA: 32-pin plastic SOJ (300 mil)