NEC
NEC Electronics Inc.

μPD482444, 482445
4M Video RAM

Preliminary Information — **September 1993**

Description

The μPD482444 fast-page and μPD482445 hyper-page video RAMs have a random access port and a serial read/write port. The serial read/write port is connected to an internal 8192-bit data register through a 512 x 16-bit serial read input/output circuit. The 256K x 16-bit random access port is used by the host CPU to read or write data addressed in any desired order.

A write-per-bit capability allows each of the 16 data bits to be individually selected or masked for a write cycle. Block write cycles can also be used to write the 16 data bits to eight consecutive column addresses. Selection and masking of the 16 data bits and eight column addresses is provided. A flash-write option with write-per-bit control enables data in the color register to be written to a selected row in the random access port.

The μPD482444 and μPD482445 feature fully asynchronous dual access between the RAM and serial ports. During a data transfer, the random access port requires a special cycle using a transfer clock; the serial port continues to operate normally. Following the clock transition of a data transfer, serial output data changes from an old line to a new line, and the new starting location is addressable in the data transfer cycle.

An advanced CMOS silicon-gate process using polycide technology and stacked capacitors provides high storage cell density, high performance, and high reliability. Refreshing is by $\overline{RAS}$-only refresh cycles or by normal read or write cycles on the 512 address combinations of A_0 - A_8 during an 8-ms period. Automatic internal refreshing is by hidden refreshing, $\overline{CAS}$ before $\overline{RAS}$ timing, or self-refresh mode, which uses on-chip refresh circuitry. The transfer of a row of data from the storage array to the data register refreshes that row. Data transfer from register to RAM array also refreshes the row.

All inputs and outputs, including clocks, are TTL-compatible. All address and data inputs are latched on-chip to simplify system design. Both devices are available in a 64-pin SSOP or 70-pin TSOP (400-mil) plastic package, guaranteed for operation at 0 to +70°C.

Features

- Three functional blocks
  - 256K x 16-bit random access storage array
  - 8192-bit data register
  - 512 x 16-bit serial read/write output circuit
- Random access and serial read/write data ports
- Fast-page operation (μPD482444)
- Hyper-page operation (μPD482445)
- Addressable start of serial read and serial write operation
- Random access port
  - Two main clocks: $\overline{RAS}$ and $\overline{CAS}$
  - Multiplexed address inputs
  - Direct connection of I/O and address lines allowed by $\overline{OE}$ to simplify system design
  - 512 refresh cycles every 8 ms
  - Read, early write, late write, read-write/read-modify-write, $\overline{RAS}$-only refresh, and fast-page cycles
  - Self-refresh mode (500 μA)
  - Automatic $\overline{CAS}$ before $\overline{RAS}$ refreshing
  - $\overline{CAS}$-controlled hidden refreshing
  - Persistent and nonpersistent write-per-bit option regarding eight I/O bits
  - Write bit selection multiplexed on IO_0 - IO_{15}
- Eight-column block write option with write-per-bit control and column mask function
- Flash-write option with write-per-bit control
- Split serial data register to allow shifting from the active half while loading the inactive half
- Boundary jump function on the serial data register
- $\overline{RAS}$-activated data transfer; row data transferred to data register as specified by row address inputs
- Either full or split data register transfer to the row specified by the row address inputs. Split write transfer is always performed from inactive side of data register
  - Transfer of 8192 bits of data on one row to the data register, and the starting location of the serial read circuit, activated by a low-to-high transition of $\overline{DT}$ or $\overline{RAS}$
  - Data transfer during real-time operation or standby of serial port
- Fast serial read/write operation by means of the SC pin
- Serial data input and output on SIO_0 - SIO_{15}
- Direct connection of multiple serial outputs for extension of data length
- Fully TTL-compatible inputs, outputs, and clocks
- Three-state outputs for random and serial access
- Single +5-volt power supply
- Single power supply
  - +5 volts: μPD482444, 482445
  - +3.3 volts: μPD482444L, 482445L

Ordering Information, μPD482444; 5-Volt Power Supply

Part Number	$\overline{RAS}$ Access Time (max)	Serial Access Time (max)	Fast-Page Cycle (max)	Package
μPD482444GW-60	60 ns	15 ns	40 ns	64-pin plastic SSOP
GW-70	70 ns	17 ns	45 ns	
GW-80	80 ns	20 ns	50 ns	
μPD482444G5-60	60 ns	15 ns	40 ns	70-pin plastic TSOP (normal pinouts)
G5-70	70 ns	17 ns	45 ns	
G5-80	80 ns	20 ns	50 ns	
μPD482444G5M-60	60 ns	15 ns	40 ns	70-pin plastic TSOP (reverse pinouts)
G5M-70	70 ns	17 ns	45 ns	
G5M-80	80 ns	20 ns	50 ns	

Ordering Information, μPD482445; 5-Volt Power Supply

Part Number	$\overline{RAS}$ Access Time (max)	Serial Access Time (max)	Hyper-Page Cycle (max)	Package
μPD482445GW-60	60 ns	15 ns	30 ns	64-pin plastic SSOP
GW-70	70 ns	17 ns	35 ns	
GW-80	80 ns	20 ns	40 ns	
μPD482445G5-60	60 ns	15 ns	30 ns	70-pin plastic TSOP (normal pinouts)
G5-70	70 ns	17 ns	35 ns	
G5-80	80 ns	20 ns	40 ns	
μPD482445G5M-60	60 ns	15 ns	30 ns	70-pin plastic TSOP (reverse pinouts)
G5M-70	70 ns	17 ns	35 ns	
G5M-80	80 ns	20 ns	40 ns	

Ordering Information, μPD482444L; 3.3-Volt Power Supply

Part Number	$\overline{RAS}$ Access Time (max)	Serial Access Time (max)	Fast-Page Cycle (max)	Package
μPD482444LGW-60	60 ns	15 ns	40 ns	64-pin plastic SSOP
LGW-70	70 ns	17 ns	45 ns	
LGW-80	80 ns	20 ns	50 ns	
μPD482444LG5-60	60 ns	15 ns	40 ns	70-pin plastic TSOP (normal pinouts)
LG5-70	70 ns	17 ns	45 ns	
LG5-80	80 ns	20 ns	50 ns	
μPD482444LG5M-60	60 ns	15 ns	40 ns	70-pin plastic TSOP (reverse pinouts)
LG5M-70	70 ns	17 ns	45 ns	
LG5M-80	80 ns	20 ns	50 ns	

Ordering Information, μPD482445L; 3.3-Volt Power Supply

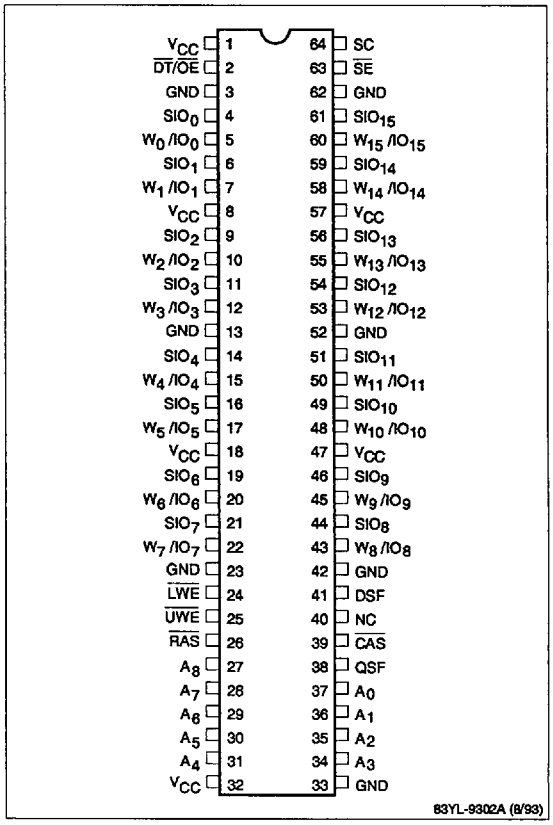
Part Number	$\overline{RAS}$ Access Time (max)	Serial Access Time (max)	Hyper-Page Cycle (max)	Package
μPD482445LGW-60	60 ns	15 ns	30 ns	64-pin plastic SSOP
LGW-70	70 ns	17 ns	35 ns	
LGW-80	80 ns	20 ns	40 ns	
μPD482445LG5-60	60 ns	15 ns	30 ns	70-pin plastic TSOP (normal pinouts)
LG5-70	70 ns	17 ns	35 ns	
LG5-80	80 ns	20 ns	40 ns	
μPD482445LG5M-60	60 ns	15 ns	30 ns	70-pin plastic TSOP (reverse pinouts)
LG5M-70	70 ns	17 ns	35 ns	
LG5M-80	80 ns	20 ns	40 ns	

Pin Identification

Symbol	Function
A_0 - A_8	Address inputs
$\overline{CAS}$	Column address strobe
DSF	Special function enable
$\overline{DT/OE}$	Data transfer/Output enable
$\overline{LWE}$, $\overline{UWE}$	Write enable, lower byte and upper byte
QSF	Special function output
$\overline{RAS}$	Row address strobe
SC	Serial control
SIO_0 - SIO_{15}	Serial data inputs and outputs
$\overline{SE}$	Serial enable
W_0/IO_0 - W_{15}/IO_{15}	Write-per-bit selects/Data inputs and outputs
GND	Ground
V_{CC}	+5-volt or +3.3-volt power supply
NC	No connection

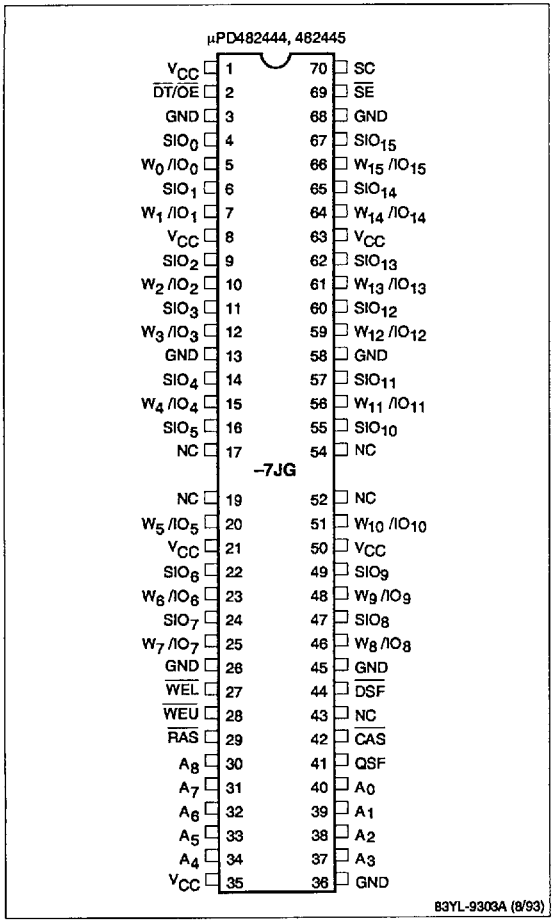
Pin Configurations

64-Pin Plastic SSOP

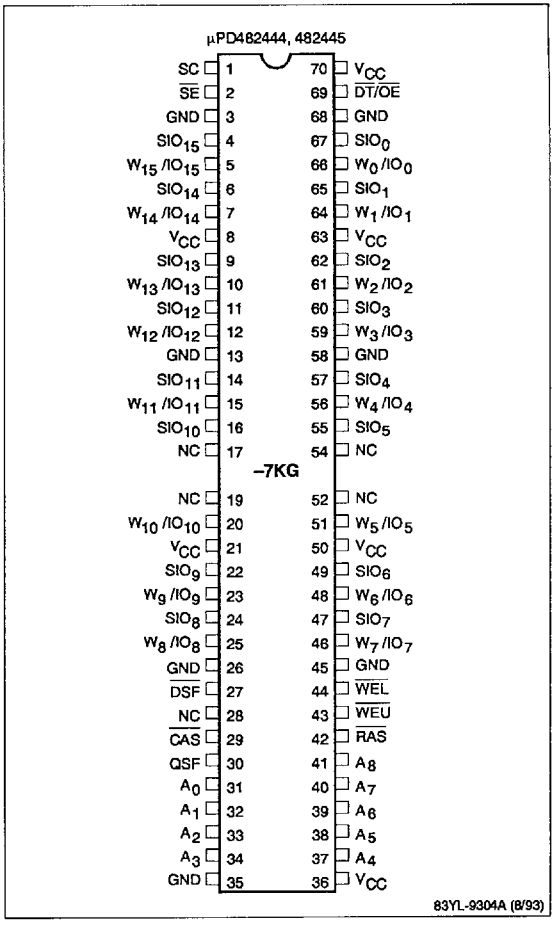


83YL-9302A (8/93)

70-Pin Plastic TSOP (Normal Pinouts)



70-Pin Plastic TSOP (Reverse Pinouts)



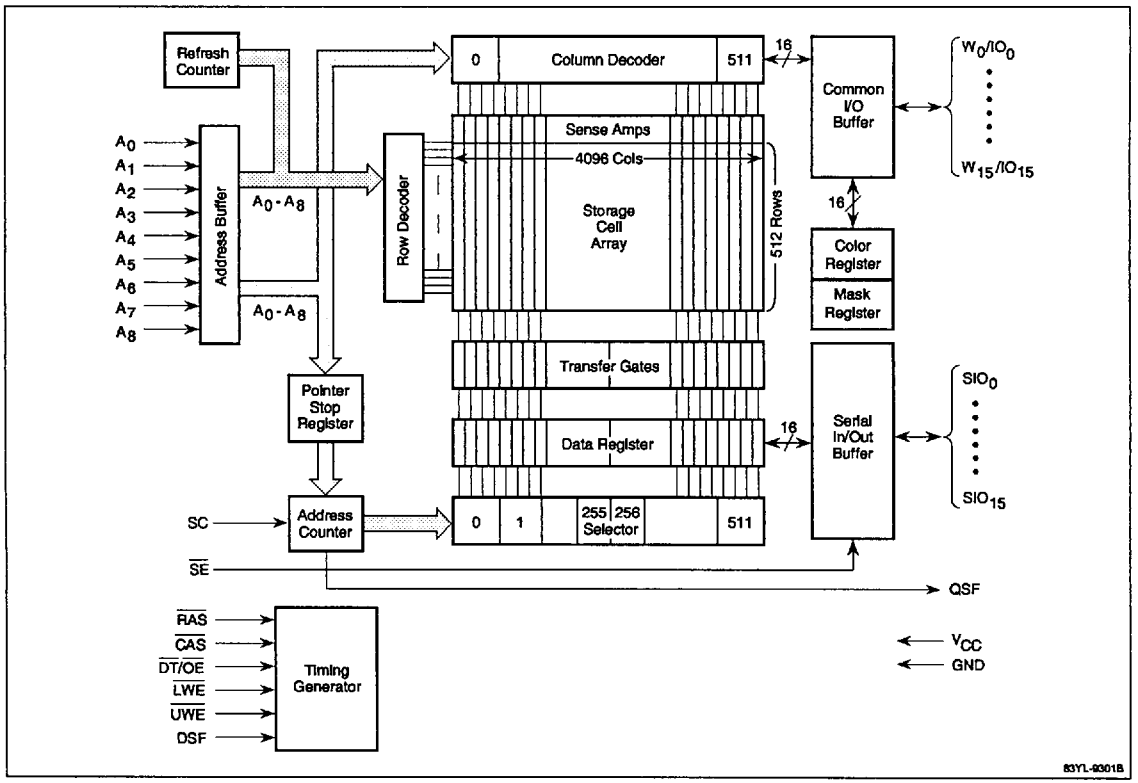
Pin Functions

A_0-A_8 (Address Inputs). These pins are multiplexed as row and column address inputs. Each of 8 data bits in the random access port corresponds to 262,144 storage cells, which means that 9-bit row addresses and 9-bit column addresses are required to decode one cell location. Row addresses are first used to select one of the 512 possible rows for a read, write, data transfer, or refresh cycle. Column addresses are then used to select the one of 512 possible column decoders for a read or write cycle or the one of 512 possible starting locations for the next serial read cycle. (Column addresses are not required in $\overline{RAS}$-only refresh cycles.)

W_0/IO_0-W_{15}/IO_{15} (Write-Per-Bit Inputs/Common Data Inputs and Outputs). Each of the 16 mask bits can be individually latched at the falling edge of $\overline{RAS}$ in any write cycle and then updated at the next falling edge of $\overline{RAS}$. In a read cycle, these pins serve as outputs for the selected storage cells. In a write cycle, data input on these pins is latched by the falling edge of $\overline{CAS}$ or $\overline{LWE}/\overline{UWE}$.

$\overline{RAS}$ (Row Address Strobe). This pin is functionally equivalent to a chip enable signal in that whenever it is activated, the 8192 storage cells of a selected row are sensed simultaneously and the sense amplifiers restore all data. The 9 row address bits are latched by this signal and must be stable on or before its falling edge. $\overline{CAS}$, $\overline{DT/OE}$, $\overline{LWE}/\overline{UWE}$, and DSF are simultaneously latched to determine device operation.

Block Diagram



$\overline{CAS}$ (Column Address Strobe). This pin serves as a chip selection signal to activate the column decoder and the input/output buffers. The 9 column address bits are latched at the falling edge of $\overline{CAS}$.

QSF (Special Function Output). This pin indicates which side of the split register is active. QSF high shows that the upper half (addresses 256 through 511) is active; QSF low indicates the lower half (addresses 0 through 255).

DSF (Special Function Control). At the leading edge of $\overline{RAS}$ and $\overline{CAS}$, the high or low level of DSF is latched to initiate one of the operations shown in table 1.

$\overline{LWE}$/$\overline{UWE}$ (Write-Per-Bit or Masked Write Control). At the falling edge of $\overline{RAS}$, the $\overline{LWE}$/$\overline{UWE}$ and DSF inputs must be low and $\overline{CAS}$ and $\overline{DT}$/$\overline{OE}$ high to enable the write- per-bit option. When $\overline{CAS}$, $\overline{DT}$/$\overline{OE}$, and DSF are high at the falling edge of $\overline{RAS}$, the level of this signal indicates either a color register set cycle or flash write cycle. A high $\overline{LWE}$/$\overline{UWE}$ can be used at the beginning of a standard write or read cycle.

$\overline{DT}$/$\overline{OE}$ (Data Transfer/Output Enable). At the $\overline{RAS}$ falling edge, $\overline{CAS}$ and $\overline{LWE}$/$\overline{UWE}$ high and $\overline{DT}$/$\overline{OE}$ low initiate a data transfer. $\overline{DT}$/$\overline{OE}$ high initiates conventional read or write cycles and controls the output buffer in the random access port. The level of DSF determines whether this is a read or split read data transfer.

SIO_0 - SIO_{15} (Serial Data Inputs/Outputs). Eight-bit data can be written or read from these pins, and during a serial read, data remains valid until the next SC signal is activated.

SC (Serial Control). Repeatedly activating this signal causes serial read/write cycles (starting from the location specified in the data transfer cycle) to be executed within the 8192 bits in the data register. The rising edge of SC activates either a serial read or write operation. In the serial read mode, 16 of the 4096 data bits are transferred to 16 serial data buses, respectively, and read out. In the serial write operation, input data is latched on the rising edge of SC. Whenever SC is low, the serial port is in standby.

$\overline{SE}$ (Serial Enable). This signal controls the serial input/output buffer.

OPERATION

The μPD482444 and μPD482445 both incorporate a random access port and a serial read or write port. The random access port executes standard read and write cycles as well as data transfer, block write, and flash write cycles, all of which are based on conventional $\overline{RAS}$/$\overline{CAS}$ timing.

In a data transfer, data in each storage cell on the selected row is transferred simultaneously through a transfer gate to its corresponding register location. The serial read port shows the contents of the data register in serial order. The random access and serial ports can operate asynchronously when split read or split write operation is used.

Addressing

The storage array is arranged in a 512-row by 8192-column matrix, whereby each of 8 data bits in the random access port corresponds to 262,144 storage cells, and 18 address bits are required to decode one cell location. Nine row address bits are set up on pins A_0 - A_8 and latched onto the chip by $\overline{RAS}$. Nine column address bits then are set up on pins A_0 - A_8 and latched onto the chip by $\overline{CAS}$.

All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. Whenever $\overline{RAS}$ is activated, 8192 cells on the selected row are sensed simultaneously, and the sense amplifiers automatically restore the data. $\overline{CAS}$ serves as a chip selection signal to activate the column decoder and the input and output buffers.

Through one of 512 column decoders, eight storage cells on the row are connected to eight data buses, respectively. In a data transfer cycle, 9 row address bits are used to select one of the 512 possible rows involved in the transfer of data to the data register. Nine column address bits are then used to select the one of 512 possible serial decoders that corresponds to the starting location of the next serial read cycle.

In the serial read port, when SC is activated, 16 data bits in the 8192-bit data register are transferred to 16 serial data buses and read out. Activating SC repeatedly causes serial read or serial write cycles (starting from the location specified in the previous data transfer cycle) to be executed within the 8192 bits in the data register.

Random Access Port

An operation in the random access port begins with a negative transition of $\overline{RAS}$. Both $\overline{RAS}$ and $\overline{CAS}$ have minimum pulse widths, as specified in the timing table, which must be maintained for proper device operation and data integrity. Once begun, a cycle must meet all specifications, including minimum cycle time. To reduce the number of pins, the following are multiplexed: $\overline{DT}$/$\overline{OE}$, $\overline{LWE}$/$\overline{UWE}$, W_n/IO_n (n = 0 through 15).

The $\overline{OE}$, $\overline{WE}$, and IO_n functions represent standard operations; $\overline{DT}$, $\overline{WB}$, and W_n are special inputs to be applied in the same way as row address inputs with setup and hold times referenced to the negative transition of $\overline{RAS}$.

The level of $\overline{DT}$ determines whether a cycle is a random access operation or a data transfer operation. $\overline{WB}$ affects only write cycles and determines whether or not the write-per-bit capability is used. W_n defines data bits to be written with the write-per-bit option. In the following discussions, these multiplexed pins are designated as $\overline{DT}$(/$\overline{OE}$), for example, depending on the function being described.

To use the μPD482244/5 for random access, $\overline{DT}$(/$\overline{OE}$) must be high as $\overline{RAS}$ falls. Holding $\overline{DT}$(/$\overline{OE}$) high disconnects the 8192-bit register from the corresponding 8192 digit lines of the storage array. Conversely, to execute a data transfer, $\overline{DT}$(/$\overline{OE}$) must be low as $\overline{RAS}$ falls to open the 8192 transfer gates and transfer data from one of the rows to the register.

Read Cycle. A read cycle is executed by activating $\overline{RAS}$, $\overline{CAS}$, and $\overline{OE}$ and by maintaining ($\overline{WB}$/)$\overline{WE}$ while $\overline{CAS}$ is active. The (W_n/)IO_n pin remains in high impedance until valid data appears at the output at access time. Device access time, t_{ACC}, will be the longest of the following four calculated intervals:

- t_{RAC}
- $\overline{RAS}$ to $\overline{CAS}$ delay (t_{RCD}) + t_{CAC}
- $\overline{RAS}$ to column address delay (t_{RAD}) + t_{AA}
- $\overline{RAS}$ to $\overline{OE}$ delay + t_{OEA}

Access times from $\overline{RAS}$ (t_{RAC}), from $\overline{CAS}$ (t_{CAC}), from the column addresses (t_{AA}), and from $\overline{OE}$ (t_{OEA}) are device parameters. The $\overline{RAS}$-to-$\overline{CAS}$, $\overline{RAS}$-to-column address, and $\overline{RAS}$-to-$\overline{OE}$ delays are system-dependent timing parameters. Output becomes valid after the access time has elapsed and it remains valid while both $\overline{CAS}$ and $\overline{OE}$ are low. Either $\overline{CAS}$ or $\overline{OE}$ high returns the output pins to high impedance (μPD482444 only). See explanation of "Extended Data Output."

Write Cycle. A write cycle is executed by bringing ($\overline{WB}$/)$\overline{WE}$ low during the $\overline{RAS}$/$\overline{CAS}$ cycle. The falling

edge of $\overline{CAS}$ or ($\overline{WB}$/)$\overline{WE}$ strobes the data on (W_n/)IO_n into the on-chip data latch. To make use of the write-per-bit option, $\overline{WB}$/($\overline{WE}$) must be low as $\overline{RAS}$ falls. In this case, write data bits can be specified by keeping W_n/(IO_n) high, with setup and hold times referenced to the negative transition of $\overline{RAS}$.

Write-Per-Bit-Cycle. A write-per-bit-cycle uses an I/O masking function to allow the system designer the flexibility of writing or not writing any combinations of W_0/IO_0 through W_{15}/IO_{15}. Two types of masking are possible: (1) new mask or the non-persistent mask that requires the user to provide the mask data each cycle and (2) old mask or the persistent mask. With the persistent mask option, an LMR or load mask register cycle is performed and the mask data is used during write, block write, and flash write cycles.

Early Write Cycle. An early write cycle is executed by bringing ($\overline{WB}$/)$\overline{WE}$ low before $\overline{CAS}$ falls. Data is strobed by $\overline{CAS}$, with setup and hold times referenced to this signal, and the output remains in high impedance for the entire cycle. As $\overline{RAS}$ falls, ($\overline{DT}$/)$\overline{OE}$ must meet the setup and hold times of a high $\overline{DT}$, but otherwise ($\overline{DT}$/)$\overline{OE}$ does not affect any circuit operation while $\overline{CAS}$ is active.

Read-Write/Read-Modify-Write Cycle. This cycle is executed by bringing ($\overline{WB}$/)$\overline{WE}$ low with the $\overline{RAS}$ and $\overline{CAS}$ signals low. (W_n/)IO_n shows read data at access time. Afterward, in preparation for the upcoming write cycle, (W_n/)IO_n returns to high impedance when ($\overline{DT}$/)$\overline{OE}$ goes high. The data to be written is strobed by ($\overline{WB}$/)$\overline{WE}$, with setup and hold times referenced to this signal.

Late Write Cycle. This cycle shows the timing flexibility of ($\overline{DT}$/)$\overline{OE}$, which can be activated just after ($\overline{WB}$/)$\overline{WE}$ falls, even when ($\overline{WB}$/)$\overline{WE}$ is brought low after $\overline{CAS}$.

Refresh Cycle. A cycle at each of the 512 row addresses (A_0 - A_8) will refresh all storage cells. Any cycle executed in the random access port (i.e., read, write, refresh, data transfer, color register set, flash write, or block write) refreshes the 8192 bits selected by the $\overline{RAS}$ addresses or by the on-chip address counter.

$\overline{RAS}$-Only Refresh Cycle. A cycle having only $\overline{RAS}$ active refreshes all cells in one row of the storage array. A high $\overline{CAS}$ is maintained while $\overline{RAS}$ is active to keep (W_n/)IO_n in high impedance. This method is preferred for refreshing, especially when the host system consists of multiple rows of random access devices. The data outputs may be OR-tied with no bus contention when $\overline{RAS}$-only refresh cycles are executed.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle (CBRN). This cycle executes internal refreshing using the on-chip control circuitry. Whenever $\overline{CAS}$ is low as $\overline{RAS}$ falls, this circuitry automatically refreshes the row addresses specified by the internal counter. In this cycle, the circuit operation based on $\overline{CAS}$ is maintained in a reset state. When internal refreshing is complete, the address counter automatically increments in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ cycle. CBRS and CBR also performed internal refresh, stopping column control.

Hidden Refresh Cycle. This cycle is executed after a read cycle without disturbing the read data output. Once valid, the data output is controlled by $\overline{CAS}$ and $\overline{OE}$. After the read cycle, $\overline{CAS}$ is held low while $\overline{RAS}$ goes high for precharge. A $\overline{RAS}$-only cycle is then executed (except that $\overline{CAS}$ is held at a low level instead of a high level) and the data output remains valid. Since hidden refreshing is the same as $\overline{CAS}$ before $\overline{RAS}$ refreshing, the data output remains valid during either operation.

Fast-Page Cycle. This feature allows faster data access by keeping the same row address while successive column addresses are strobed onto the chip. Maintaining $\overline{RAS}$ low while successive $\overline{CAS}$ cycles are executed causes data to be transferred at a faster rate because row addresses are maintained internally and do not have to be reapplied. In fast-page operation, read, write, and read-write/read-modify-write cycles may be executed. Additionally, the write-per-bit control specified in the entry write cycle is maintained throughout the next fast-page write cycle.

During a fast-page read cycle, the (W_n)/IO_n data pin (n = 0 - 15) remains in a state of high impedance until valid data appears at the output pin at access time. Device access time in this cycle will be the longest of the following intervals.

- t_{ACP}
- $t_{CP} + t_T + t_{CAC}$
- $\overline{CAS}$ high to column address delay + t_{AA}

Glossary of Special Functions

Table 1 is a truth table for implementing the functions described below.

Masked Write Cycle With New Mask (RWM new mask). When the write-per-bit function is enabled as shown below, mask data on the W_n/IO_n pins is latched by $\overline{RAS}$ and loaded directly into the write mask register. A masked write cycle is then executed using $\overline{CAS}$ or $\overline{WB}$/$\overline{WE}$ to strobe the W_n/IO_n data into the on-chip data latch.

Mask Register Data	Action
1	Write
0	Do not write

Load Mask Register Cycle (LMR). In this cycle, data on W_n/IO_n is written to a 16-bit write mask register, where it is retained and used by subsequent masked write and masked block write cycles.

Masked Write Cycle With Old Mask (RWM old mask). This write-per-bit cycle, commonly referred to as a persistent mask write cycle, uses the mask data previously set by the last load mask register cycle.

Table 1. μPD482444/5 Function Truth Table (JEDEC Standard) for Random Access Port

Mnemonic Code	$\overline{RAS}$				$\overline{CAS}$	Address		DQ_n Input		Write Mask	Register		Function
	$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WE}$ (Note 6)	DSF	DSF	$\overline{RAS}$	$\overline{CAS}$	$\overline{RAS}$	$\overline{CAS}/\overline{WE}$		WM	Color	
CBRS (Notes 1, 3)	0	x	0	1	—	STOP (Note 4)	—	x	—	—	—	—	CBR refresh/STOP (no reset)
CBRN (Note 1)	0	x	1	1	—	x	—	x	—	—	—	—	CBR refresh (no reset)
CBR (Note 1)	0	x	1	0	—	x	—	x	—	—	—	—	CBR refresh (option reset)
MWT	1	0	0	0	x	Row	Tap	WM1 (Note 5)	—	Yes	Load/ Use	—	Masked write transfer (new/old)
MSWT	1	0	0	1	x	Row	Tap	WM1 (Note 5)	—	Yes	Load/ Use	—	Masked split write transfer (new/old)
RT	1	0	1	0	x	Row	Tap	x	—	—	—	—	Read transfer
SRT	1	0	1	1	x	Row	Tap	x	—	—	—	—	Split read transfer
RWM	1	1	0	0	0	Row	Col	WM1 (Note 5)	Data	Yes	Load/ Use	—	Read write (new/old mask)
BWM	1	1	0	0	1	Row	Col	WM1 (Note 5)	Col	Yes	Load/ Use	Use	Block write (new/old mask)
FWM	1	1	0	1	x	Row	x	WM1 (Note 5)	—	Yes	Load/ Use	Use	Flash write (new/old mask)
RW	1	1	1	0	0	Row	Col	x	Data	No	—	—	Read write (no mask)
BW	1	1	1	0	1	Row	Col	x	Col	No	—	Use	Block write (no mask)
LMR (Note 2)	1	1	1	1	0	Row	x	x	WM1	0	Load	—	Load (old) mask register set cycle
LCR	1	1	1	1	1	Row	x	x	Color	0	—	Load	Load color register

x = Don't care

— = Not applicable

$\overline{RAS}$ only refresh does not reset STOP or LMR functions.

Notes:

(1) CBRS, CBRN, and CBR all perform $\overline{CAS}$ before $\overline{RAS}$ refresh cycles. CBR is used to reset all options and either CBRS or CBRN is used to continue to refresh the RAM without clearing any of the options.

(2) After LMR, RWM and BWM use old mask. (CBR resets to new mask. Use CBRS or CBRN to perform CAS before RAS refresh while using old mask.)

(3) With CBRS, all SAM operations use STOP register.

(4) STOP defines the column on which shift out moves to the other half of the SAM.

(5) After LMR, WM1 is only changed by LMR (CBR resets).

(6) Either write enable, $\overline{UWE}$ or $\overline{LWE}$, in active state (low level) will initiate the specified mode.

For the inactive mode, both $\overline{UWE}$ and $\overline{LWE}$ must be high level.

Table 2. Eight-Column Block Write Masking Function

Column Mask Select (Note 1)		Column Address A_2 - A_0
Lower Byte	Upper Byte	
IO_7	IO_{15}	111
IO_6	IO_{14}	110
IO_5	IO_{13}	101
IO_4	IO_{12}	100
IO_3	IO_{11}	011
IO_2	IO_{10}	010
IO_1	IO_9	001
IO_0	IO_8	000

Note 1: Write and don't write are selected by 1 and 0, respectively; for example, I/O_7 = 1 means write to the lower byte of column address 111

Flash Write Cycle (FWM old mask). This flash write cycle is the same as the FWM new mask except that the bit mask inputs are supplied by the mask register set by the previous LMR cycle.

Flash Write Cycle (FWM new mask). A flash write cycle can clear or set each of the eight 512-bit data sets on the selected one of 512 possible rows according to data stored in the previously set color register. Bit mask inputs are latched as $\overline{RAS}$ falls. This cycle is useful in graphics processing applications when the screen should be cleared or set to some uniform value as quickly as possible.

Load Color Register Cycle (LCR). This cycle is executed in the same fashion as a conventional read or write cycle, with a read or write cycle available to the color register under the control of $\overline{WE}$. In read operation, color register data is read on the common W_n/IO_n pins. In write operation, common W_n/IO_n data can be written into the color register. $\overline{RAS}$-only refreshing is internally performed on the row selected by A_0 - A_8. This setup cycle precedes the first flash write or block write cycle supplying the 8 write data bits.

Block Write Cycle (BW no mask). In a block write cycle, A_2, A_1, and A_0 are ignored and the color data stored in the previous Load Color Register cycle is written to eight consecutive column addresses. Bits IO_0 - IO_{15} are used to write or mask any combination of these eight column addresses for writing in an early write, late write, page early write, or page late write cycle. See table 2.

Block write data is previously stored in the color register using a set color register cycle. Column select data is latched by the W_n/IO_n pins at the falling edge of $\overline{CAS}$ or $\overline{WE}$. Block write cycles are useful for clearing windows and for accelerating polygon fill operations.

Block Write Cycle (BWM new mask). This cycle allows for W_0/IO_0 - W_{15}/IO_{15} masking during a block write cycle. The masking function is identical to a standard masked write cycle with new mask, except that eight consecutive columns are written.

Block Write Cycle (BWM old mask). This cycle uses the masked data previously set by the last LMR cycle to write eight consecutive columns.

Read Data Transfer Cycle (RT). In a full-row read data transfer cycle, one of the possible 512 rows, as well as the starting location of the following serial read cycle, is defined by row and column address inputs. The low-to-high transition of $\overline{DT}/(\overline{OE})$ causes the 8192 bits of cell data to be transferred to the serial data register.

Split Read Transfer Cycle. This cycle is a half-row data transfer in which one of the 512 rows, the starting location of the following serial read cycle, and either of the split registers are specified by the address inputs. On-chip control circuitry causes the previously specified half-row to be transferred to the selected upper or lower split register.

Hyper-Page Mode With Extended Data Output. In operation, hyper-page mode is the same as standard fast-page mode. As in fast-page mode, a faster data rate is possible by keeping the same row address while successive column addresses are strobed onto the chip. Maintaining $\overline{RAS}$ low while $\overline{CAS}$ cycles are executed causes data to be transferred at a faster rate because row addresses are maintained internally and do not have to be reapplied. During hyper-page mode, read, write, and read-modify-write cycles may be executed. Additionally, the write-per-bit control specified in the entry write cycle is maintained throughout the successive fast-page write cycle.

Extended Data Output

The introduction of the extended data output feature causes the output data to remain valid even after $\overline{CAS}$ goes high. This is made possible by the addition of a transparent latch to the data amplifier circuit. Extended data output eliminates the t_{OFF} parameter. The resulting longer data valid time allows for the speedup of the fast-page cycle time. Fast-page mode applications that try to run at minimum cycle times find that timing skews and propagation delays make the data valid time so narrow that reliable sampling is impossible. Extended data output is intended to solve this problem and permit faster page-mode cycle times, hence the term "hyper-page mode."

Speed Grade	Fast-Page Mode	Hyper-Page Mode
-70	t_{PC} = 45 ns	t_{HPC} = 35 ns

In this operation, data pins W_0/IO_0 through W_{15}/IO_{15} remain in the low-impedance state and the valid data appears after the device access time. Device access time, t_{PAC} (page-mode access time), is the longest of the following intervals:

- t_{ACP}
- t_{AA}
- t_{CAC}
- t_{AWE}†
- t_{ACE}†

† Page write to page read switch or continuous page RMW cycles.

Serial Read Port

The serial read port is used to serially read the previously loaded contents of the data register starting from a specified location. Other graphics buffers require very tight timing to synchronize this port with the random access port, but the μPD482444/5 has been designed with a split register to eliminate the need for synchronized timing between the two ports.

Read Data Transfer (RT). A data transfer is executed to both split registers, and the serial port direction is switched to the serial read mode. During this cycle, the row address selects the row, and the column address sets the start address of the next serial read sequence. The transfer trigger is $\overline{DT/OE}$ or $\overline{RAS}$ low-to-high transition, whichever occurs first. The read data transfer cycle disables the boundary jump function in the serial port but keeps the stop register value. QSF will change depending on the column address specified during the RT cycle.

Split Read Data Transfer (SRT). The split register means that the serial data register is composed of serial addresses 0-255 (lower half) and serial addresses 256-511 (upper half). With the serial port split in half, data transfers can be executed to the inactive side while SC clocks are input to access data from the active side. This sequence allows for a longer time window to perform the transfer, i.e., 256 x t_{SCC}. Column address bits A_0 - A_7 are latched on-chip to provide the tap address pointer for each split register. The most significant column address A_8 is a "don't care."

During a split read data transfer cycle, a half row of memory data is transferred to one of the split half serial registers. The row addresses select the half row to be transferred and the column addresses (A_7 - A_0) set the tap or pointer for the start of the serial read operation and boundary jump operation. A split read transfer does not change the direction of the serial port I/O.

Data in the data register is clocked serially by SC, starting from the first specified address of either register. After the last specified address has been transferred, QSF changes its level at the next rising edge of SC, and serial data transfer switches to the other (formerly inactive) register. Serial data output is maintained until the next SC clock.

Rising edges of the SC clock are not allowed for the last serial address (either 255 or 511) of the active register and for the first address (any address depending on current address pointer) of the next active register (figure 1).

$\overline{SE}$ controls the impedance of the serial output to allow multiplexing of more than one bank of μPD482444/5 on the same bus and has no effect on SC. When $\overline{SE}$ is low, SO_n is disabled and in a state of high impedance. During serial write, the $\overline{SE}$ level is latched by SC rising edge to control the serial input buffer. SC continues to increment serial addresses independent of $\overline{SE}$.

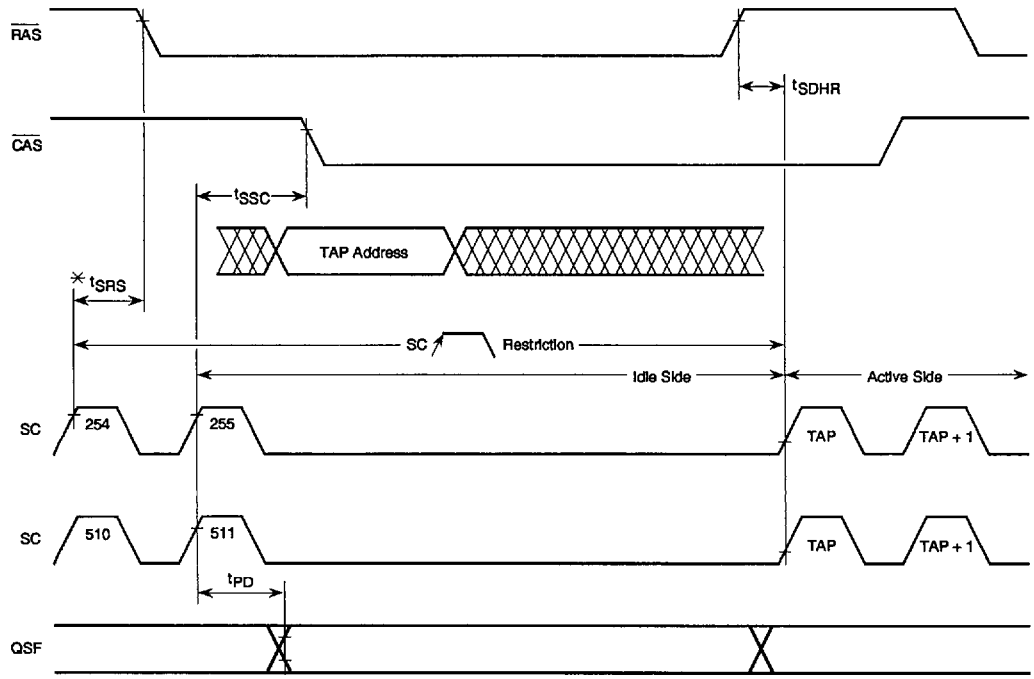
Serial Port Write Operation

Serial writes can also be performed to the serial data register starting at the location (column address) specified by the previous write or split write transfer cycle. After writing to the serial register, the contents can be transferred to the specified row address in the DRAM array. This operation provides a fast screen clear function. Both a split write and full register write transfer are possible. Refer to figure 2.

Masked Write Data Transfer (MWT). The MWT cycle, under write-per-bit control, transfers the contents of both halves of the serial data register to the selected row in the DRAM array. Row addresses are used to select the row to receive the data and the column addresses set the start location of the following serial write operation. If the previous serial port operation was a serial read, then an MWT cycle is required to change the direction of the serial I/O from serial read to serial write. During all MWT cycles, SC clocks are not allowed and system timing must meet the conditions of t_{SRS} and t_{SDHR}.

In this type of transfer, the contents of the DRAM will be changed unless the masking or write-per-bit function is employed. Keeping $\overline{WE}$ and all 16 I/Os low as $\overline{RAS}$ falls will perform a write-per-bit mask and inhibit data from being transferred to the RAM array. The MWT cycle disables the boundary jump function of the serial port but does not reset the stop register value. QSF will

Figure 1. Restrictions on Rising Edges of SC for Split Read and Split Write Data Transfer Cycles



Notes:

[1] For split register transfers, there is a restriction on the SC clocks at the transition point from the end of one half to the beginning of the other half split register. Rising edges of the SC clock for the last serial address of the idle split register (255 or 511) and the first tap address are not allowed.

[2] The restrictions apply to split read transfers, split write transfers, split read transfers with stopping column control, full read data transfers and write data transfers.

✳ The same restrictions for split write transfers except t_{SRS} apply.

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change in accordance with the value set by the column address specified during the MWT cycle.

Masked Split Write Data Transfer (MSWT). A data transfer cycle is performed from the inactive split-half serial register to the specified half row in the DRAM array. A split write transfer is always performed from the inactive half SAM. Column address CA8 is a "dont' care." The direction of the serial port I/O (serial read or write) remains unchanged. The same write-per-bit masking function is used as described in the MWT cycle.

QSF Special Function Output

This pin outputs a signal synchronized with the SC clock and indicating which half of the serial data register is active. A high level of QSF indicates that an upper half address (256 - 511) will be read from or written to by the next SC clock. Read and write addresses 0 - 255 are indicated by a low QSF level. QSF changes on the rising edge of the SC clock for serial addresses 255, 511, and BJX (boundary jump).

Advanced Serial Write Operation

If the design objective is to write data into selected blocks without disturbing the background data, the sequence of operations in figure 3 should be followed.

Figure 2. Example of Split Read and Split Write Data Transfers (Sheet 1 of 3)

		①	②	③	③	④	⑤	⑤	⑥	⑦
Power up	8 RAS Cycles	CBRS or CBR	Read Data Transfer	Split Read Data Xfer	Split Read Data Xfer	Masked Write Data Transfer	Split Write Data Transfers	Split Write Data Transfers	Read Data Transfer	Split Read Data Xfer

Notes:

(1) A CBRS or CBR is required to set up the serial register boundaries. A CBR alone or a CBRS with A_7 - A_0 set to (11111111) sets the serial register to 255 and 511 splits.

(2) A full line data transfer is required before a sequence of split read or write transfers.

(3) Rising edges of SC clocks are not allowed in this restricted window for serial addresses 255 and 511. The restricting parameters are t_{SSC} and t_{SDHR}.

(4) No SC clocks are allowed during the period specified by t_{SRS} and t_{SDHR}.

(5) Rising edges of SC clocks are not allowed in this restricted window for serial addresses 255 and 511. The restricting parameters are t_{SRS} and t_{SDHR}.

(6) No SC clocks are allowed during the period specified by t_{SSC} and t_{SDHR}.

(7) The numbers at SIO_n indicate the serial read or write address.

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Figure 2. Example of Split Read and Split Write Data Transfers (Sheet 2 of 3)

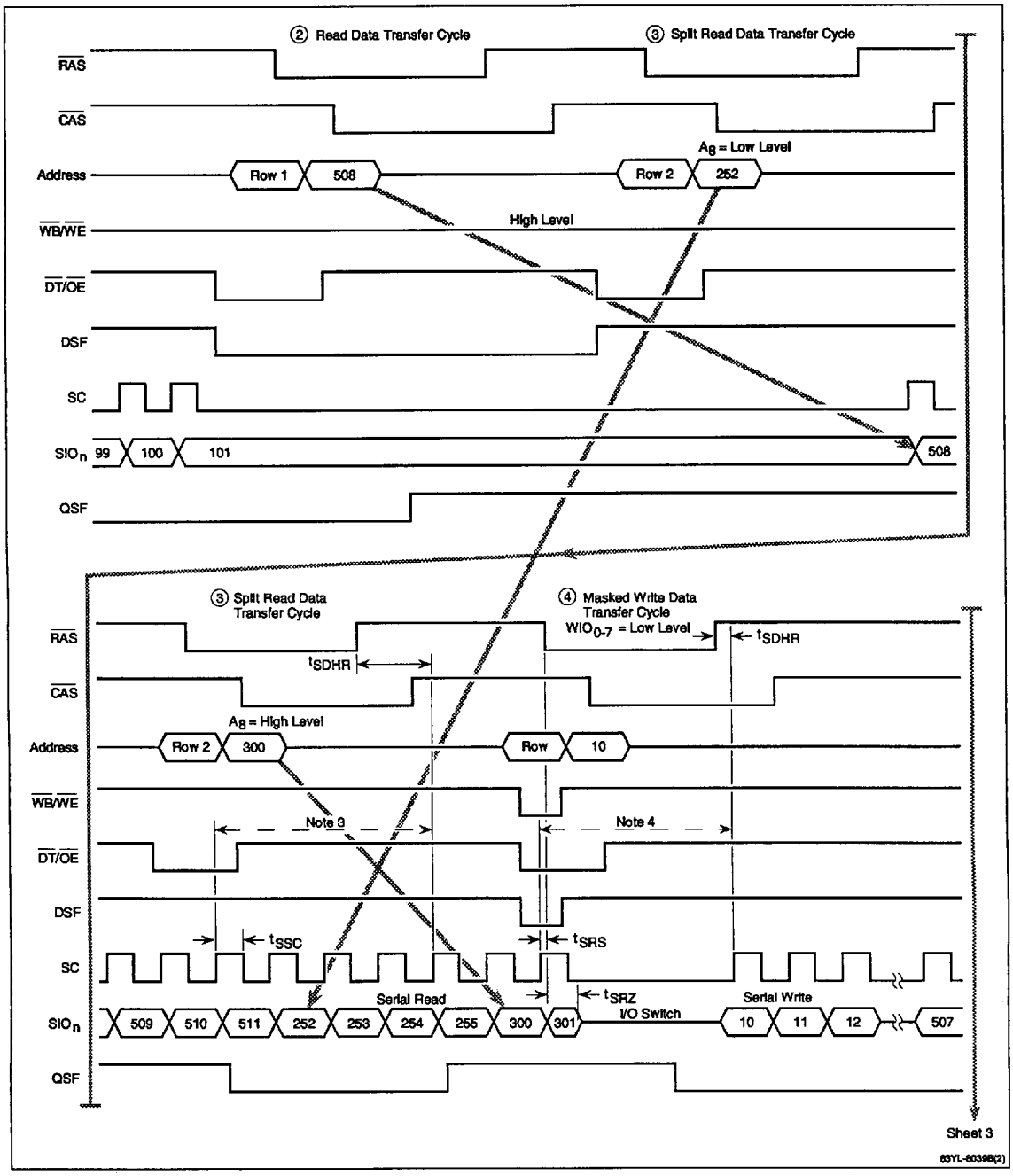


Figure 2. Example of Split Read and Split Write Data Transfers (Sheet 3 of 3)

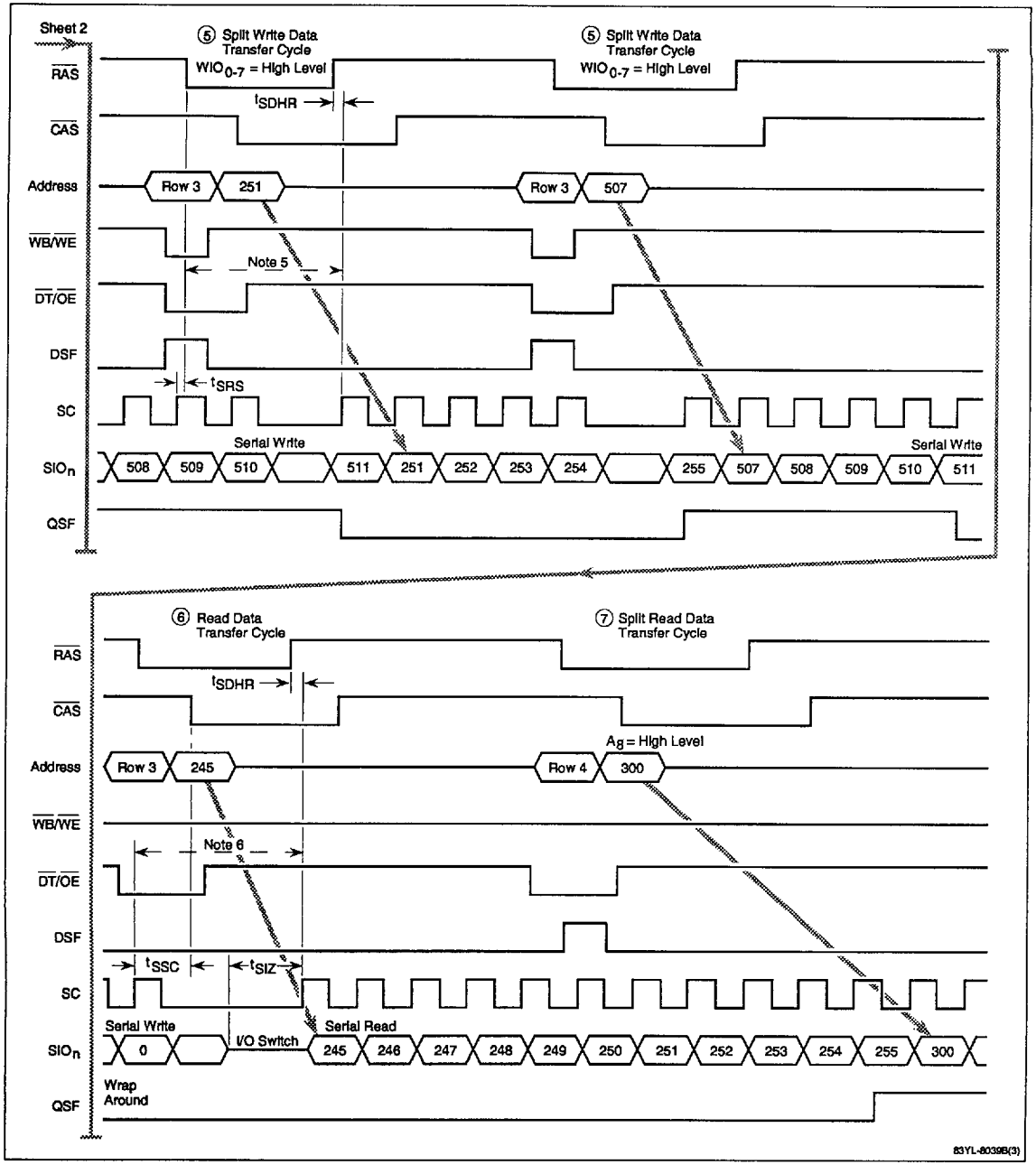


Figure 3. Advanced Serial Write Operation (Sheet 1 of 2)

Glossary

MSWT	Masked split-write transfer: half SAM to RAM	RT	Read transfer: full row in RAM to SAM
MWT	Masked write transfer: full SAM to RAM	SAM	Serial access memory
QSF	Special-function output	SRT	Split-read transfer: half row in RAM to SAM
RAM	Random access memory	Tap	Selectable start address in SAM

Background data Serial write data

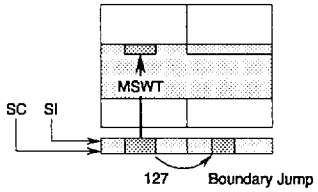
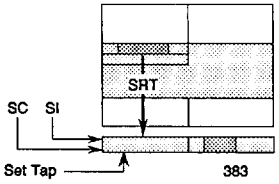
Step	Operation	
1	After power-up, perform a CBRS cycle with 0111 1111 code. This sets the SAM port to four stop addresses: 127, 255, 383, 511. When the SAM address reaches any of these four positions, the SAM pointer will jump to the opposite-half SAM address specified by the previous SRT or MSWT.	
2	Perform an MSWT after the boundary jump and the serial address moves from the lower- to the upper-half SAM. This copies the half-row back to the RAM port.	
3	During the previous serial write operation, an SRT was performed to the lower-half SAM, setting the tap. The SRT preloads the SAM with background data from the RAM.	

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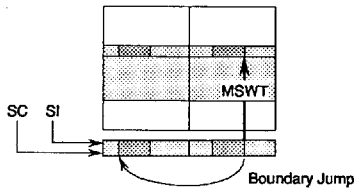
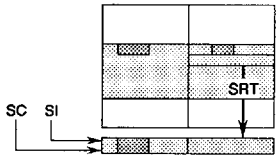
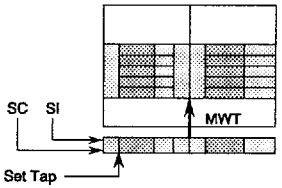
Figure 3. Advanced Serial Write Operation (Sheet 2 of 2)

Step	Operation	
4	When the serial writes to the upper-half SAM reach 383, a boundary jump to the lower-half SAM occurs, and SC clocks begin writing to the lower-half, starting at the selected tap address. An MSWT is performed from the upper-half SAM after the address jumps to the lower-half.	
5	Perform an SRT to preload the upper-half SAM. Repeat steps 6, 7, 8, and 9 until all partial rows are written to the serial port and transferred to the memory array.	
6	After the entire data set is written to RAM, an MWT is required to copy the last full SAM data to RAM.	

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Stopping Column Control

On previous dual-ported memories, after setting the pointer control (column start address in the serial register), there was no way to jump to the other half split register without serially clocking through the mid-point 255/256) of the 512-bit serial data register. Another way of stating this is that only a start position could be specified, not a stopping point.

The μPD482444/5 includes an 8-bit stop register, which corresponds to a boundary location in each split half register. The stop register value is latched during a special $\overline{CAS}$ before $\overline{RAS}$ cycle (CBRS) using address inputs A_0 - A_7. Sixteen different stop positions or boundaries can be specified for each half register using a stop register set cycle. With this feature, a mid-register to mid-register jump is possible. Refer to figure 4.

Application for Stopping Column Control. By using stopping column control, the serial port can now clock out selected pieces of data, allowing the transfer of data corresponding to sequential pixels on a scanline. This feature provides for a flexible segmentation of memory and permits an efficient transfer of these segments from the memory to the screen.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle With Stop Register Set (CBRS). This special $\overline{CAS}$ before $\overline{RAS}$ cycle writes boundary locations to a stop register. The boundary value is supplied by addresses A_7 - A_0 and is latched at the falling edge of $\overline{RAS}$. (Note: This is a real-time stop register set cycle; that is, the new stop register value is changed during this CBRS cycle.)

After power-up, initializing this register by performing a CBRS or a CBR (option reset CBR register) is required. The value in the stop register and its bit boundary location are shown in table 3. This CBRS cycle will also refresh the specified row in the DRAM.

Table 3. Stop Register Set

Stop Register Value A_7 - A_0	Boundary Location (Jumps to tap after accessing this boundary)
1111 1111	255, 511 (default)
0111 1111	127, 255, 383, 511
0011 1111	63, 127, 191, 255, 319, 383, 447, 511
0001 1111	31, 63, 95, 127, 159, 191, 223, 255, 287, 319, 351, 383, 415, 447, 479, 511
0000 1111	15, 31, 47, 63, 79, 95, 111, 127, 143, 159, 175, 191, 207, 223, 239, 255, 271, 287, 303, 319, 335, 351, 367, 383, 399, 415, 431, 447, 463, 479, 495, 511

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle With Option Reset (CBR). After executing this option reset cycle, the write-per-bit mask register and the stop register will reset to the default condition. For example, the write-per-bit masking will be new mask and the stop register will be reset to 1111 1111. This CBR cycle will refresh the specified row in the DRAM.

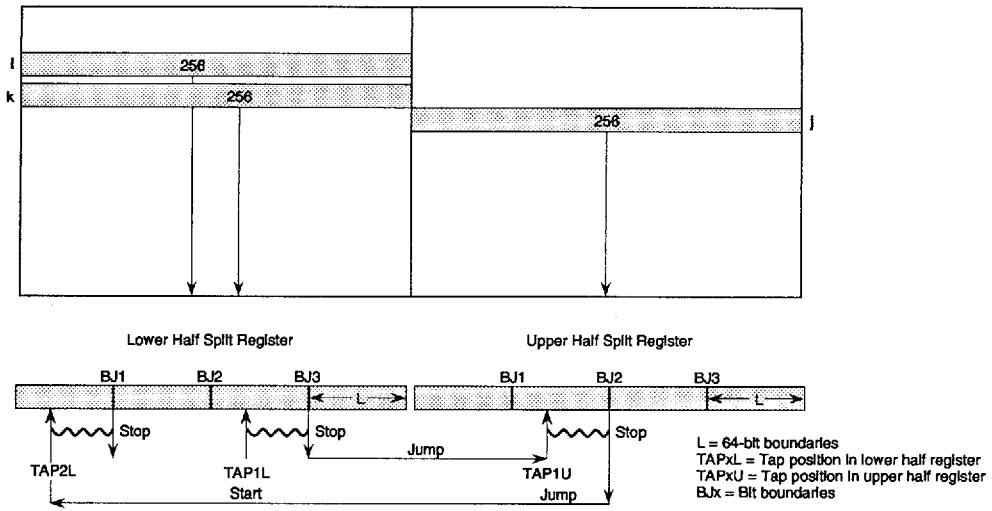
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle With No Reset (CBRN). This $\overline{CAS}$ before $\overline{RAS}$ cycle refreshes the specified row without clearing or changing any of the options and register values.

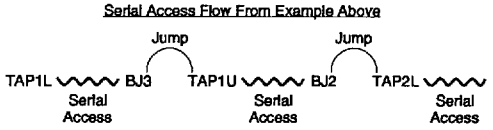
Recommended CBR, CBRS, and CBRN Cycles

To ensure that the device has not entered unwanted register modes, at least one CBR (option reset) after power has stabilized is recommended. Eight CBR cycles or combination of RAS and CBR cycles satisfies the initialization sequence.

A CBR after each vertical retrace is recommended. This fail-safe routine is for cases where a system misoperation causes entry into an unwanted mode. If the stop register function is used, then a CBRS would follow every CBR cycle. If the stop register function is not required and persistent write masking is employed, then use a CBRN. This keeps the old mask function.

Figure 4. Example of Split Read Transfer With Boundary Jump (Sheet 1 of 2)





① Perform a Stop Register Set Cycle CBRS
CBR with WE = low level and DSF = high level
A_7-A_0 = 00111111

② Split Data Transfer Cycle

③ Split Data Transfer Cycle

④ Split Data Transfer Cycle

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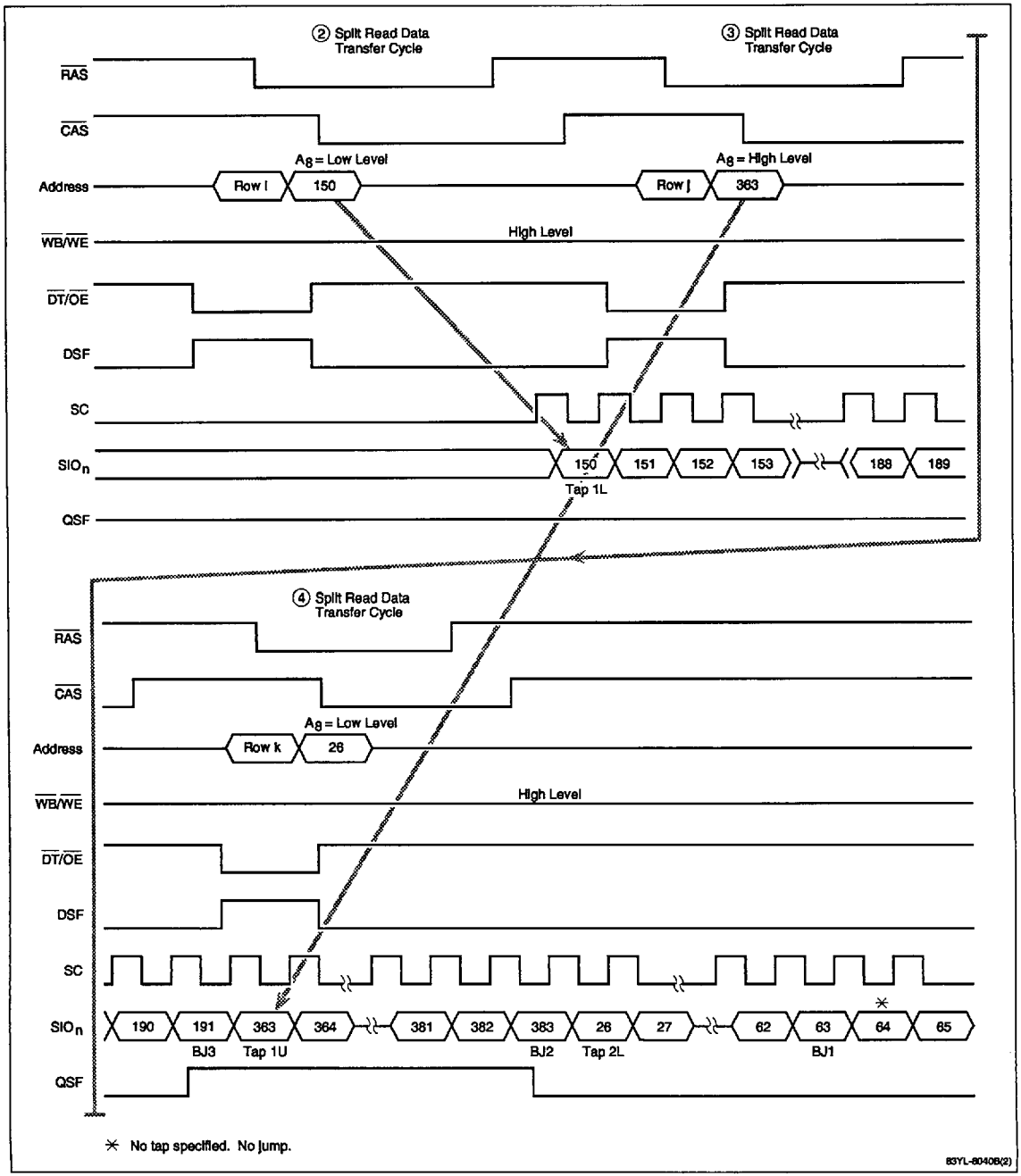
Figure 4. Example of Split Read Transfer With Boundary Jump (Sheet 2 of 2)



Absolute Maximum Ratings; 3.3-V Power

Voltage on any pin except V_{CC} relative to GND, V_{R1}	−1.0 to +4.6 V
Voltage on V_{CC} relative to GND, V_{R2}	−1.0 to +4.6 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	20 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions; 3.3-V Power

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	3.0	3.3	3.6	V
Input voltage, high	V_{IH}	2.0		V_{CC}+0.3	V
Input voltage, low	V_{IL}	−0.5		0.8	V
Ambient temp	T_A	0		+70	°C

Capacitance

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; f = 1 MHz; GND = 0 V

Parameter	Symbol	Limit (max)	Unit	Pins Under Test
Input capacitance	$C_{I(A)}$	5	pF	A_0 - A_8
	$C_{I(\overline{DT}/\overline{OE})}$	8	pF	$\overline{DT}/\overline{OE}$
	$C_{I(\overline{WE})}$	8	pF	$\overline{UWE}/\overline{LWE}$
	$C_{I(DSF)}$	8	pF	DSF
	$C_{I(\overline{RAS})}$	8	pF	$\overline{RAS}$
	$C_{I(\overline{CAS})}$	8	pF	$\overline{CAS}$
	$C_{I(\overline{SE})}$	8	pF	$\overline{SE}$
	$C_{I(SC)}$	8	pF	SC
Input/output capacitance	$C_{IO(W/IO)}$	7	pF	W_0/IO_0 - W_{15}/IO_{15}
Output capacitance	$C_{O(SIO)}$	7	pF	SIO_0 - SIO_{15}
	$C_{O(QSF)}$	7	pF	QSF

3.3-Volt Power Supply Current

T_A = 0 to +70°C; V_{CC} = +3.3. V ±0.3 V; GND = 0 V

Port Operation			−60	−70	−80		
Random Access	Serial Read	Parameter	(max)	(max)	(max)	Unit	Test Conditions
Read/write cycle	Standby	I_{CC1}	90	75	60	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; DSF low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SE}$ = V_{IH}; SC = V_{IH} or V_{IL}
Standby	Standby	I_{CC2}	7	7	7	mA	D_{OUT} = high impedance; address cycling; t_{RC} = t_{RC} min; $\overline{CAS}$ = $\overline{RAS}$ = V_{IH}; $\overline{SE}$ = V_{IH}; SC = V_{IH} or V_{IL} (Note 4)
			130	130	130	μA	$\overline{RAS}$, $\overline{CAS}$, and $\overline{SE}$ ≥ V_{CC} − 0.2 V; A_0 - A_8, $\overline{WB}/\overline{WE}$, $\overline{DT}/\overline{OE}$, DSF, SC stay at V_{IH} ≥ V_{CC} − 0.2 V or V_{IL} ≤ GND + 0.2 V
$\overline{RAS}$-only refresh cycle	Standby	I_{CC3}	90	75	60	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ = V_{IH}; DSF low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SE}$ = V_{IH}; SC = V_{IH} or V_{IL} (Note 2)
Fast-page cycle	Standby	I_{CC4}	100	85	70	mA	$\overline{RAS}$ = V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; $\overline{SE}$ = V_{IH}; SC = V_{IH} or V_{IL} (Note 3)
Hyper-page cycle	Standby	I_{CC4}	100	85	70	mA	
$\overline{CAS}$ before $\overline{RAS}$ refresh cycle	Standby	I_{CC5}	90	85	80	mA	$\overline{CAS}$ low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SE}$ = V_{IH}; SC = V_{IH} or V_{IL}
Data transfer cycle	Standby	I_{CC6}	110	95	80	mA	$\overline{DT}$ low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SE}$ = V_{IH}; SC = V_{IH} or V_{IL}
Read/write cycle	Active	I_{CC7}	120	100	80	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; DSF low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min

3.3-Volt Power Supply Current (cont)

Port Operation			-60	-70	-80		
Random Access	Serial Read	Parameter	(max)	(max)	(max)	Unit	Test Conditions
Standby	Active	I_{CC8}	30	25	20	mA	D_{OUT} = high impedance; address cycling; $t_{RC} = t_{RC}$ min; $\overline{CAS} = \overline{RAS} = V_{IH}$; $\overline{SE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min (Note 4)
$\overline{RAS}$-only refresh cycle	Active	I_{CC9}	120	100	80	mA	$\overline{RAS}$ cycling; $\overline{CAS} = V_{IH}$; DSF low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ min; $\overline{SE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min
Fast-page cycle	Active	I_{CC10}	130	110	90	mA	$\overline{RAS} = V_{IL}$; $\overline{CAS}$ cycling; $t_{PC} = t_{PC}$ min; $\overline{SE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min (Note 3)
Hyper-page cycle	Active	I_{CC10}	130	110	90	mA	
$\overline{CAS}$ before $\overline{RAS}$ refresh cycle	Active	I_{CC11}	120	110	100	mA	$\overline{CAS}$ low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ min; $\overline{SE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min
Data transfer cycle	Active	I_{CC12}	140	120	100	mA	$\overline{DT}$ low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ min; $\overline{SE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min
Color register set cycle	Standby	I_{CC13}	80	70	60	mA	$t_{RC} = t_{RC}$ min; $\overline{SE} = V_{IH}$; SC = V_{IH} or V_{IL}
Color register set cycle	Active	I_{CC14}	110	95	90	mA	$t_{RC} = t_{RC}$ min; $\overline{SE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min
Flash write cycle	Standby	I_{CC15}	80	70	60	mA	$t_{RC} = t_{RC}$ min; $\overline{SE} = V_{IH}$; SC = V_{IH} or V_{IL}
Flash write cycle	Active	I_{CC16}	110	95	80	mA	$t_{RC} = t_{RC}$ min; $\overline{SE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min
Block write cycle	Standby	I_{CC17}	100	90	80	mA	$t_{RC} = t_{RC}$ min; $\overline{SE} = V_{IH}$; SC = V_{IH} or V_{IL}
Block write cycle	Active	I_{CC18}	130	115	100	mA	$t_{RC} = t_{RC}$ min; $\overline{SE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min
Block write in fast-page cycle	Standby	I_{CC19}	115	100	85	mA	$t_{PC} = t_{PC}$ min; $\overline{SE} = V_{IH}$; SC = V_{IH} or V_{IL}
Block write in hyper-page cycle	Standby	I_{CC19}	115	100	85	mA	
Block write in fast-page cycle	Active	I_{CC20}	145	125	105	mA	$t_{PC} = t_{PC}$ min; $\overline{SE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min
Block write in hyper-page cycle	Active	I_{CC20}	145	125	105	mA	

Notes:

(1) No load on IO, SO, and QSF. Except for I_{CC2}, real values depend on output loading in addition to cycle rates.

(2) $\overline{CAS}$ is not clocked but is kept at a stable high level. The column addresses are also assumed to be kept stable at either a high or low level.

(3) A change in column addresses must not occur more than once in a fast-page cycle.

(4) A change in row addresses must not occur more than once in a read or write cycle.

DC Characteristics; 3.3-Volt Power

T_A = 0 to +70°C; V_{CC} = +3.3 V ±0.3 V; GND = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{IL}	-5		5	μA	V_{IN} = 0 to 5.5 V; all other pins not under test = 0 V
Output leakage current	I_{OL}	-5		5	μA	D_{OUT} (IO, SIO) disabled; V_{OUT} = 0 to 5.5 V
Random access port output voltage, high	$V_{OH(R)}$	2.4			V	$I_{OH(R)}$ = -1 mA
Random access port output voltage, low	$V_{OL(R)}$			0.4	V	$I_{OL(R)}$ = 2.0 mA
Serial read port output voltage, high	$V_{OH(S)}$	2.4			V	$I_{OH(S)}$ = -1 mA
Serial read port output voltage, low	$V_{OL(S)}$			0.4	V	$I_{OL(S)}$ = 2.0 mA

Absolute Maximum Ratings; 5-V Power

Voltage on any pin except V_{CC} relative to GND, V_{R1}	−1.0 to +7.0 V
Voltage on V_{CC} relative to GND, V_{R2}	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.5 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions; 5-V Power

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.4		5.5	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Ambient temp	T_A	0		+70	°C

5-Volt Power Supply Current

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; GND = 0 V

Port Operation			−60	−70	−80		
Random Access	**Serial Read**	**Parameter**	**(max)**	**(max)**	**(max)**	**Unit**	**Test Conditions**
Read/write cycle	Standby	I_{CC1}	100	85	70	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; DSF low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SE}$ = V_{IH}; SC = V_{IH} or V_{IL}
Standby	Standby	I_{CC2}	10	10	10	mA	D_{OUT} = high impedance; address cycling; t_{RC} = t_{RC} min; $\overline{CAS}$ = $\overline{RAS}$ = V_{IH}; $\overline{SE}$ = V_{IH}; SC = V_{IH} or V_{IL} (Note 4)
			200	200	200	μA	$\overline{RAS}$, $\overline{CAS}$, and $\overline{SE}$ ≥ V_{CC} − 0.2 V; A_0 - A_8, $\overline{WB/WE}$, $\overline{DT/OE}$, DSF, SC stay at V_{IH} ≥ V_{CC} − 0.2 V or V_{IL} ≤ GND + 0.2 V
$\overline{RAS}$-only refresh cycle	Standby	I_{CC3}	100	85	70	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ = V_{IH}; DSF low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SE}$ = V_{IH}; SC = V_{IH} or V_{IL} (Note 2)
Fast-page cycle	Standby	I_{CC4}	110	95	80	mA	$\overline{RAS}$ = V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; $\overline{SE}$ = V_{IH}; SC = V_{IH} or V_{IL} (Note 3)
Hyper-page cycle	Standby	I_{CC4}	110	95	80	mA	
$\overline{CAS}$ before $\overline{RAS}$ refresh cycle	Standby	I_{CC5}	100	95	90	mA	$\overline{CAS}$ low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SE}$ = V_{IH}; SC = V_{IH} or V_{IL}
Data transfer cycle	Standby	I_{CC6}	120	105	90	mA	$\overline{DT}$ low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SE}$ = V_{IH}; SC = V_{IH} or V_{IL}
Read/write cycle	Active	I_{CC7}	130	110	90	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; DSF low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min
Standby	Active	I_{CC8}	40	35	30	mA	D_{OUT} = high impedance; address cycling; t_{RC} = t_{RC} min; $\overline{CAS}$ = $\overline{RAS}$ = V_{IH}; $\overline{SE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min (Note 4)
$\overline{RAS}$-only refresh cycle	Active	I_{CC9}	130	110	90	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ = V_{IH}; DSF low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min
Fast-page cycle	Active	I_{CC10}	140	120	100	mA	$\overline{RAS}$ = V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; $\overline{SE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min (Note 3)
Hyper-page cycle	Active	I_{CC10}	140	120	100	mA	

5-Volt Power Supply Current (cont)

Port Operation			-60	-70	-80		
Random Access	Serial Read	Parameter	(max)	(max)	(max)	Unit	Test Conditions
$\overline{CAS}$ before $\overline{RAS}$ refresh cycle	Active	I_{CC11}	130	120	110	mA	$\overline{CAS}$ low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ min; $\overline{SE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min
Data transfer cycle	Active	I_{CC12}	150	130	110	mA	$\overline{DT}$ low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ min; $\overline{SE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min
Color register set cycle	Standby	I_{CC13}	90	80	70	mA	$t_{RC} = t_{RC}$ min; $\overline{SE} = V_{IH}$; SC = V_{IH} or V_{IL}
Color register set cycle	Active	I_{CC14}	120	105	90	mA	$t_{RC} = t_{RC}$ min; $\overline{SE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min
Flash write cycle	Standby	I_{CC15}	90	80	70	mA	$t_{RC} = t_{RC}$ min; $\overline{SE} = V_{IH}$; SC = V_{IH} or V_{IL}
Flash write cycle	Active	I_{CC16}	120	105	90	mA	$t_{RC} = t_{RC}$ min; $\overline{SE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min
Block write cycle	Standby	I_{CC17}	110	100	90	mA	$t_{RC} = t_{RC}$ min; $\overline{SE} = V_{IH}$; SC = V_{IH} or V_{IL}
Block write cycle	Active	I_{CC18}	140	125	110	mA	$t_{RC} = t_{RC}$ min; $\overline{SE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min
Block write in fast-page cycle	Standby	I_{CC19}	120	110	95	mA	$t_{PC} = t_{PC}$ min; $\overline{SE} = V_{IH}$; SC = V_{IH} or V_{IL}
Block write in hyper-page cycle	Standby	I_{CC19}	125	110	95	mA	
Block write in fast-page cycle	Active	I_{CC20}	155	135	115	mA	$t_{PC} = t_{PC}$ min; $\overline{SE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min
Block write in hyper-page cycle	Active	I_{CC20}	155	135	115	mA	

Notes:

(1) No load on IO, SO, and QSF. Except for I_{CC2}, real values depend on output loading in addition to cycle rates.

(2) $\overline{CAS}$ is not clocked but is kept at a stable high level. The column addresses are also assumed to be kept stable at either a high or low level.

(3) A change in column addresses must not occur more than once in a fast-page cycle.

(4) A change in row addresses must not occur more than once in a read or write cycle.

DC Characteristics; 5-Volt Power

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; GND = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{IL}	-10		10	μA	V_{IN} = 0 to 5.5 V; all other pins not under test = 0 V
Output leakage current	I_{OL}	-10		10	μA	D_{OUT} (IO, SIO) disabled; V_{OUT} = 0 to 5.5 V
Random access port output voltage, high	$V_{OH(R)}$	2.4			V	$I_{OH(R)}$ = -1 mA
Random access port output voltage, low	$V_{OL(R)}$			0.4	V	$I_{OL(R)}$ = 2.1 mA
Serial read port output voltage, high	$V_{OH(S)}$	2.4			V	$I_{OH(S)}$ = -1 mA
Serial read port output voltage, low	$V_{OL(S)}$			0.4	V	$I_{OL(S)}$ = 2.1 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10% or +3.3 V ±0.3 V; GND = 0 V

Parameter	Symbol	-60		-70		-80		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
Access time from column address	t_{AA}		30		35		40	ns	(Note 4)
Access time from previous $\overline{CAS}$	t_{ACE}		60		65		75	ns	(Note 14)
Access time from $\overline{CAS}$ trailing edge	t_{ACP}		35		40		45	ns	
$\overline{DT}$ low hold time after address	t_{ADD}	25		25		30		ns	(Note 9)
Column address setup time	t_{ASC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	55		55		65		ns	(Note 7)
Access time from previous $\overline{WE}$	t_{AWE}		55		60		70	ns	(Note 14)
Acces time from $\overline{CAS}$	t_{CAC}		18		20		25	ns	(Note 4)
Column address hold time	t_{CAH}	10		12		12		ns	
$\overline{CAS}$ pulse width	t_{CAS}	10	100,000	10	100,000	12	100,000	ns	
$\overline{DT}$ low hold time after $\overline{CAS}$ low	t_{CDH}	20		20		25		ns	(Note 9)
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CHR}	10		10		12		ns	
$\overline{CAS}$ precharge time	t_{CP}	10		10		12		ns	
$\overline{CAS}$ precharge time (non-page mode)	t_{CPN}	10		10		10		ns	
Propagation delay time from $\overline{CAS}$ to QSF	t_{CQD}	0	60	0	65	0	75	ns	
$\overline{CAS}$ high to $\overline{RAS}$ low precharge time	t_{CRP}	5		10		10		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CSR}	5		0		0		ns	
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	40		40		50		ns	(Note 7)
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		15		20		ns	
Data in hold time	t_{DH}	12		12		15		ns	(Note 8)
Output hold time from $\overline{CAS}$	t_{DHC}	3		5		5		ns	(Note 14)
$\overline{DT}$ high hold time	t_{DHH}	10		10		12		ns	
$\overline{DT}$ high setup time	t_{DHS}	0		0		0		ns	
$\overline{DT}$ low setup time	t_{DLS}	0		0		0		ns	
Propagation delay time from $\overline{DT}/\overline{OE}$ to QSF	t_{DQD}	0	30	0	30	0	35	ns	
Propagation delay time from $\overline{RAS}$ high to QSF	t_{DQR}	0	40	0	40	0	45	ns	
Data in setup time	t_{DS}	0		0		0		ns	(Note 8)
$\overline{DT}$ high pulse width	t_{DTP}	20		20		25		ns	
$\overline{DT}$ high to $\overline{RAS}$ high delay	t_{DTR}	0		0		0		ns	(Note 9)
DSF hold time from $\overline{CAS}$	t_{FCH}	12		12		15		ns	
DSF setup time from $\overline{CAS}$	t_{FCS}	0		0		0		ns	
DSF hold time from $\overline{RAS}$	t_{FRH}	10		10		12		ns	

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	Unit	Test Conditions
DSF setup time from $\overline{RAS}$	t_{FRS}	0		0		0		ns	
$\overline{CAS}$ pulse width	t_{HCAS}	10	10,000	10	10,000	12	10,000	ns	(Note 14)
Hyper-page mode cycle time	t_{HPC}	30		35		40		ns	(Note 14)
Read-write/Read-modify-write cycle time	t_{PRWC}	85		90		105		ns	
OE hold time after $\overline{CAS}$ high	t_{OCH}	10		10		25		ns	
Access time from $\overline{OE}$	t_{OEA}		18		20		20	ns	
$\overline{OE}$ high to data in setup delay	t_{OED}	15		15		20		ns	
$\overline{OE}$ high hold time after $\overline{WE}$ low	t_{OEH}	0		0		0		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	0		0		0		ns	
Output disable time from $\overline{OE}$ high	t_{OEZ}	0	15	0	15	0	20	ns	(Note 5)
Output disable time from $\overline{CAS}$ high	t_{OFC}	0	15	0	15	0	20	ns	(Notes 5, 10, 14)
Output disable time from $\overline{CAS}$ high	t_{OFF}	0	15	0	15	0	20	ns	(Notes 5, 11)
Output disable time from $\overline{RAS}$ high	t_{OFR}	0	15	0	15	0	20	ns	(Notes 5, 10, 14)
$\overline{OE}$ hold time after $\overline{RAS}$ high	t_{ORH}	10		10		10		ns	
Fast-page mode cycle	t_{PC}	40		45		50		ns	
Propagation delay time from SC to QSF	t_{PD}	0	20		20		25	ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	(Note 4)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	17	40	ns	(Note 4)
Row address hold time	t_{RAH}	10		10		12		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
$\overline{RAS}$ pulse width (non-page mode)	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ pulse width in page mode/hyper-page mode	t_{RASP}	60	125,000	70	100,000	80	100,000	ns	
Random read or write cycle time	t_{RC}	120		130		140		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	22	55	ns	(Note 4)
Read command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		0		ns	(Note 6)
Read command setup time	t_{RCS}	0		0		0		ns	
$\overline{DT}$ low hold time after $\overline{RAS}$ low	t_{RDH}	55		60		65		ns	(Note 9)
	t_{RDHS}	15		15		15		ns	(Note 9)
Refresh period	t_{REF}		8		8		8	ms	
$\overline{RAS}$ precharge time	t_{RP}	45		50		60		ns	
$\overline{RAS}$ high to $\overline{CAS}$ low precharge time	t_{RPC}	5		5		10		ns	
Propagation delay time from $\overline{RAS}$ to QSF	t_{RQD}	0	80	0	95	0	105	ns	
Read command hold time after $\overline{RAS}$ high	t_{RRH}	0		0		0		ns	(Note 6)
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	Unit	Test Conditions
Read-write/Read-modify-write cycle time	t_{RWC}	160		180		205		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	85		90		105		ns	(Note 7)
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Serial output access time from SC	t_{SCA}		15		17		20	ns	
Serial clock cycle time	t_{SCC}	20		22		25		ns	
SC pulse width	t_{SCH}	5		5		7		ns	
SC precharge time	t_{SCL}	5		5		7		ns	
SC high to $\overline{DT}$ high	t_{SDD}	0		0		0		ns	(Note 9)
SC low hold time after $\overline{DT}$ high	t_{SDH}	40		40		50		ns	(Note 9)
	t_{SDHR}	45		45		55		ns	(Note 9)
Serial output access time from $\overline{SE}$	t_{SEA}		15		17		20	ns	
$\overline{SE}$ pulse width	t_{SEE}	5		5		7		ns	
$\overline{SE}$ hold time from SC	t_{SEH}	10		10		12		ns	
$\overline{SE}$ precharge time	t_{SEP}	5		5		7		ns	
$\overline{SE}$ setup time	t_{SES}	0		0		0		ns	
Output disable time from $\overline{SE}$ high	t_{SEZ}	0	15	0	15	0	20	ns	(Note 5)
Serial data in hold time	t_{SIH}	10		10		12		ns	
Serial data in setup time	t_{SIS}	0		0		0		ns	
Serial input disable time from SC	t_{SIZ}	0		0		0		ns	
Serial output hold time after SC high	t_{SOH}	3		5		5		ns	
$\overline{SE}$ low to serial output setup delay	t_{SOO}	3		5		5		ns	
SC hold time from $\overline{RAS}$	t_{SRH}	10		10		10		ns	(Note 12)
SC setup time from $\overline{RAS}$	t_{SRS}	10		10		10		ns	(Note 12)
Serial output disable time from $\overline{RAS}$	t_{SRZ}	0		0		0		ns	
SC high to $\overline{CAS}$ low	t_{SSC}	10		10		10		ns	(Notes 9, 12)
Serial input enable time from $\overline{RAS}$	t_{SZH}	40		40		40		ns	
Transition time (rise/fall)	t_T	3	35	3	35	3	35	ns	
Write-per-bit hold time	t_{WBH}	10		10		12		ns	
Write-per-bit setup time	t_{WBS}	0		0		0		ns	
Write command hold time	t_{WCH}	10		12		12		ns	
Write command setup time	t_{WCS}	0		0		0		ns	(Note 7)
Output disable time from $\overline{WE}$ low	t_{WEZ}	0	15	0	15	0	20	ns	(Notes 5, 10)
Write bit selection hold time	t_{WH}	10		10		12		ns	
Write command pulse width	t_{WP}	10		12		12		ns	

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	Unit	Test Conditions
Write command pulse width	t_{WPZ}	10		10		15		ns	(Note 10)
Write bit selection setup time	t_{WS}	0		0		0		ns	

Notes:

(1) All applied voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up , followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved. Note: at least one of the RAS cycles must be a CBR cycle.

(3) See figures 5 for reference voltages and output loads.

(4) Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. The t_{RCD} (max) limit is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
Assumed: t_{RAD} (min) = t_{RAH} (min) + t_T.

(5) An output disable time defines the time at which the output achieves the open-circuit condition and is not referenced to output voltage levels.

(6) Either t_{RRH} (min) or t_{RCH} (min) must be satisfied for a read cycle.

(7) t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in read-write and read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle.

If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read modify-write cycle and the data output will contain data read from the selected cell. If none of the above conditions is met, the condition of the data output (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(8) These parameters are referenced to the leading edge of $\overline{CAS}$ in early write cycles and to the leading edge of (UWE/)LWE in delayed write or read-modify-write cycles.

(9) t_{RDH}, t_{CDH}, t_{ADD}, t_{SDD}, t_{SDH}, and t_{DTR} is an alternative parameter set of t_{RDHS}, t_{SSC}, t_{RSD}, t_{ASD}, t_{CSD}, and t_{SDHR} especially for real-time data transfer condition.

(10) Hyper-Page Mode Only: IO_0 - IO_{15} turn to Hi-Z state when
- Both $\overline{RAS}$ and $\overline{CAS}$ go high; later one of t_{OFR} and t_{OFC} is valid.
- $\overline{UWE}$/$\overline{LWE}$ goes low; t_{WEZ} and t_{WPZ} are valid.
- $\overline{OE}$ goes high; t_{OEZ} is valid.

(11) Fast-Page Mode Only: $\overline{CAS}$ goes high; t_{OFF} is valid.

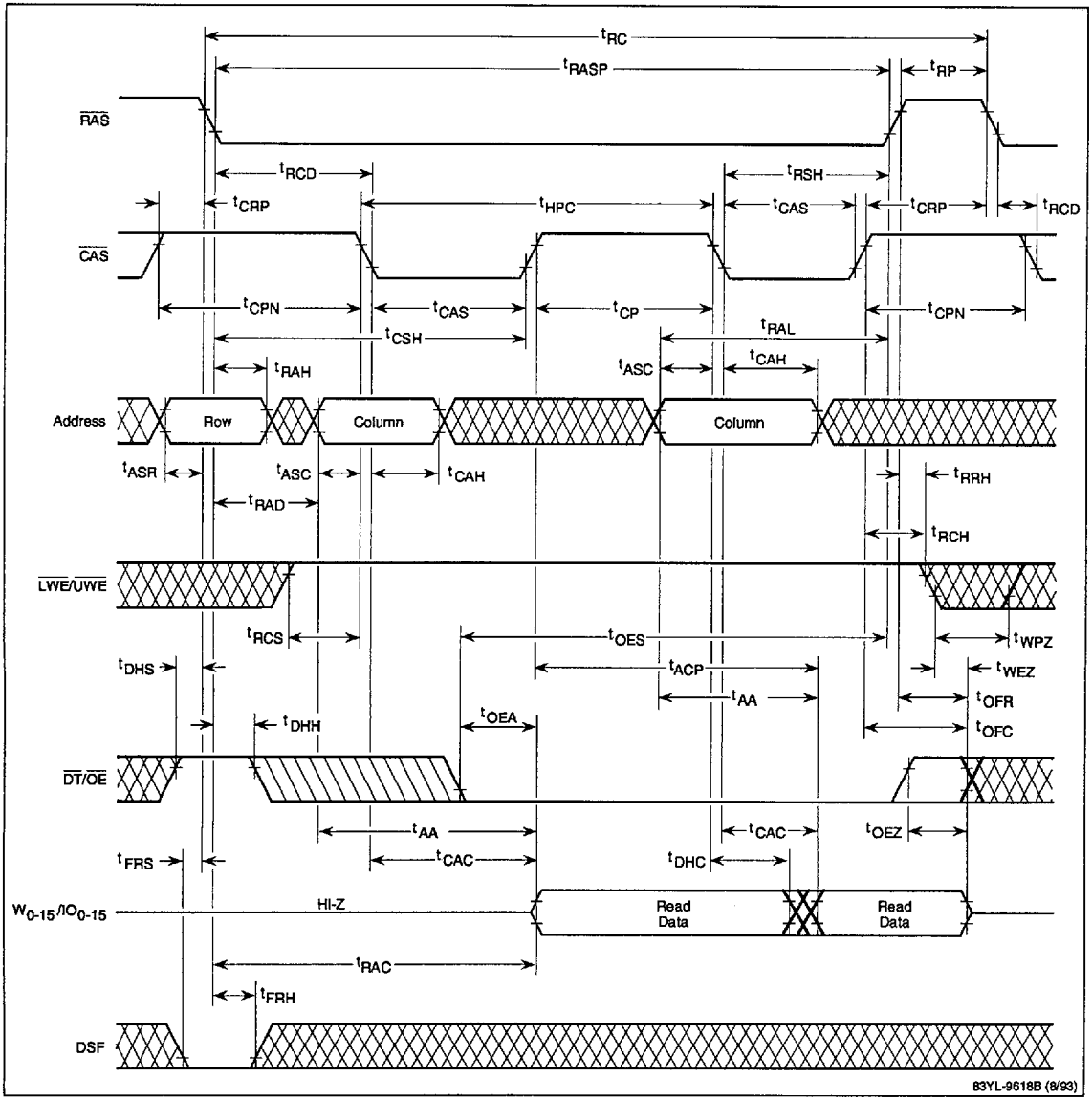
(12) If the stop register value is changed by a hidden refresh or CBRS cycle, the $\overline{CAS}$ before $\overline{RAS}$ cycle must meet t_{SRS} and t_{SRH} to guarantee a following serial port boundary jump operation. Otherwise, t_{SRS} and/or t_{SRH} are "don't care" for those cycles.

(13) In a split read data transfer cycle and split write data transfer cycle, t_{SSC}, t_{SRS}, t_{RSD}, t_{ASD}, t_{CSD}, are measured from the SC rising edge which reads/writes an address specified as boundary or tap location. These SC rising edges are not allowed during t_{SSC} through t_{RSD}, t_{ASD}, t_{CSD}, or t_{SRS} through t_{RSD}, t_{RSD}, t_{ASD}, t_{CSD}.

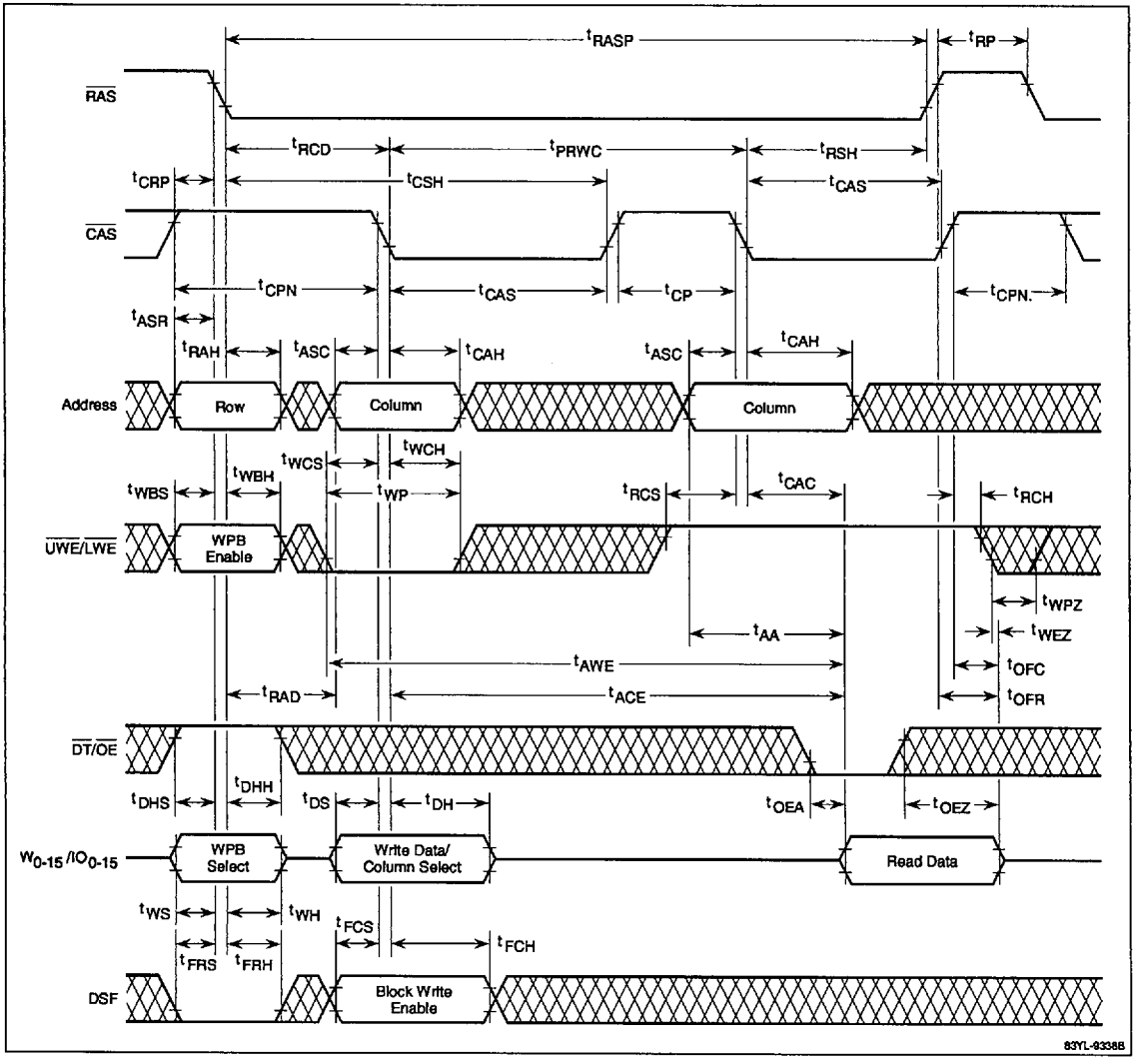
(14) These parameters apply only for the hyper-page mode devices (μPD482445).

Timing Waveforms

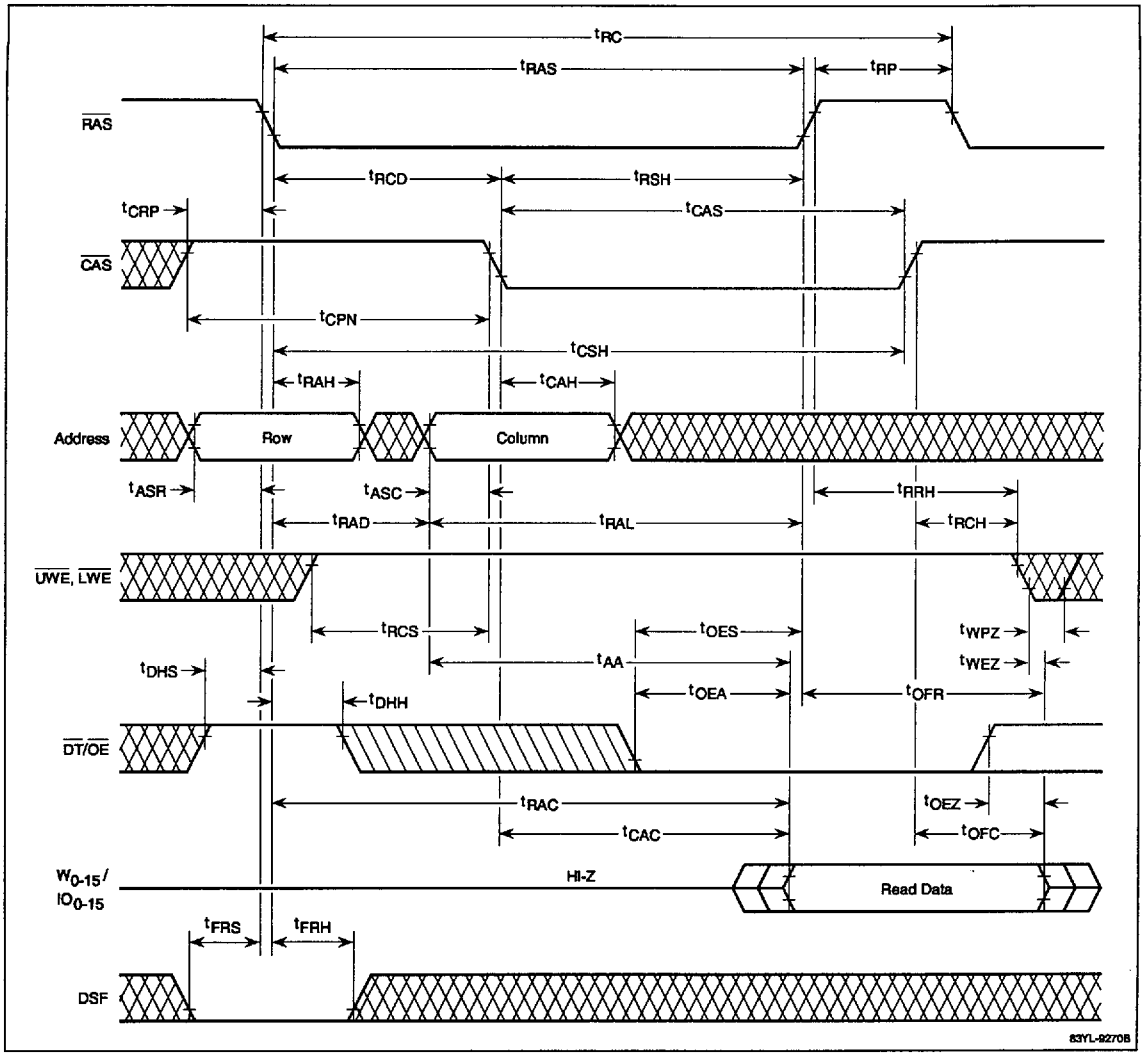
Hyper-Page Read Cycle



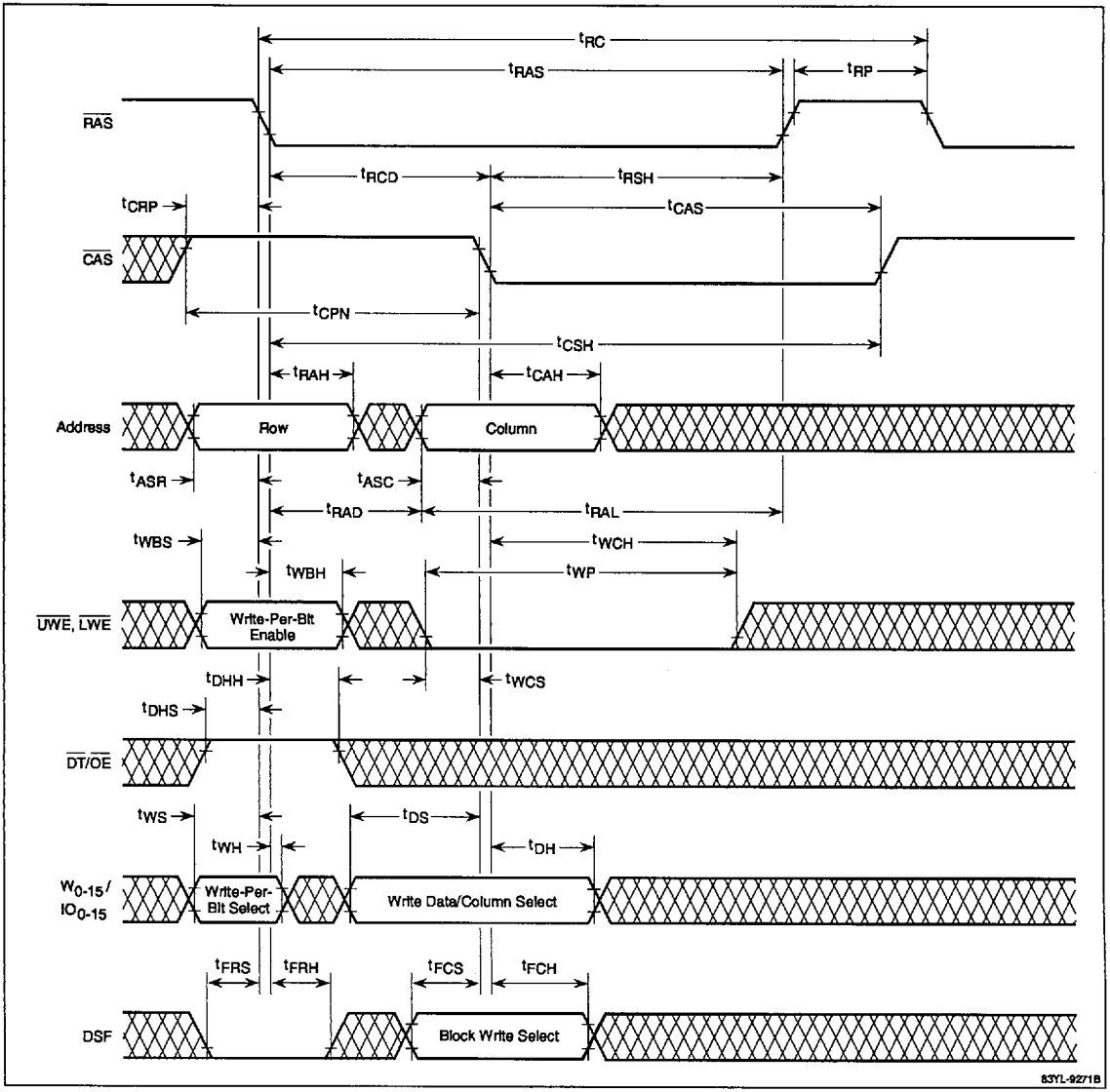
Hyper-Page Write/Read Cycle



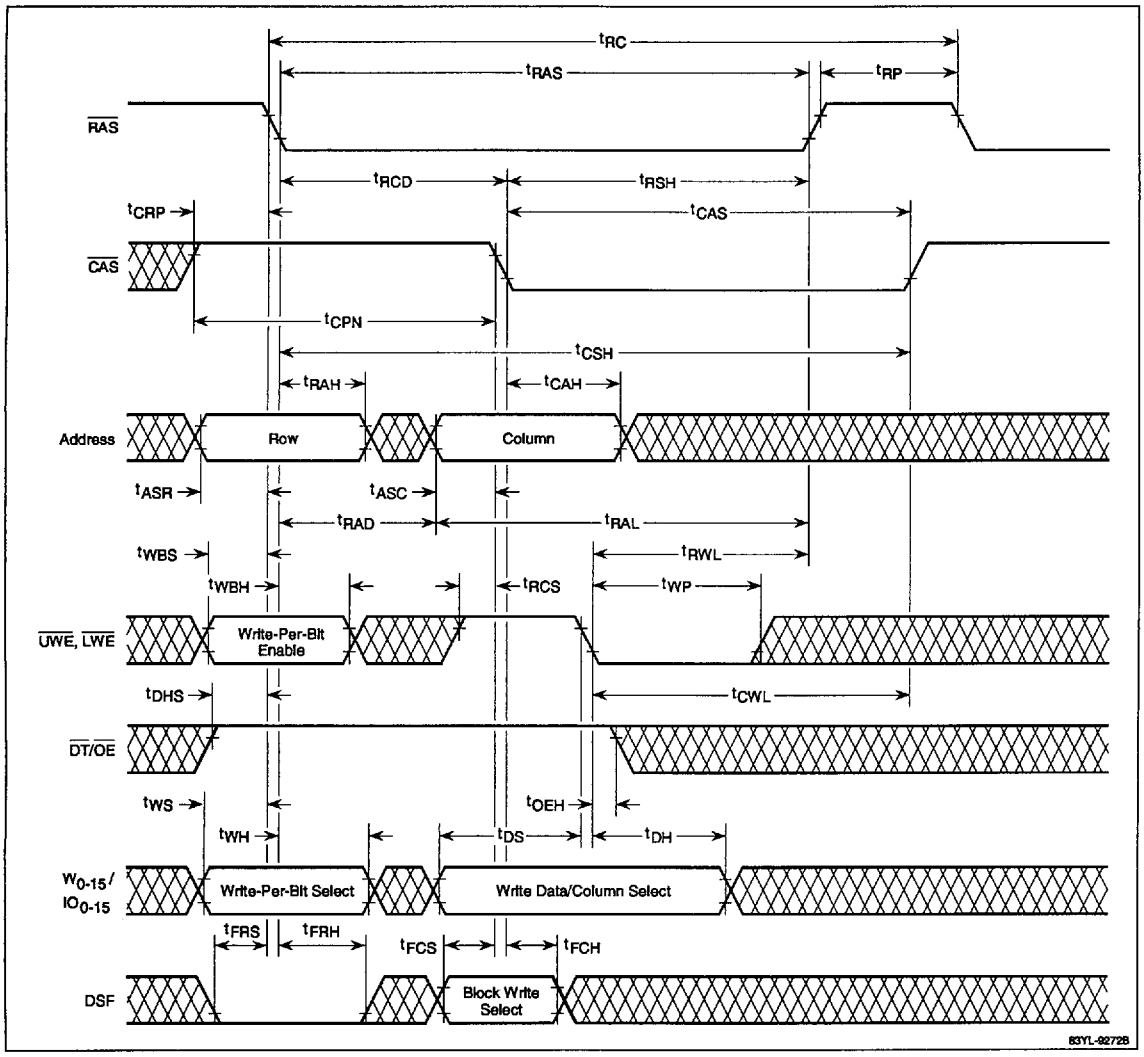
Read Cycle


tRC
tRAS
tRP
RAS
tRCD
tRSH
tCRP
tCAS
CAS
tCPN
tCSH
tRAH
tCAH
Address
Row
Column
tASR
tASC
tRRH
tRAD
tRAL
tRCH
UWE, LWE
tRCS
tOES
tWPZ
tDHS
tAA
tWEZ
tDHH
tOEA
tOFR
DT/OE
tRAC
tOEZ
tCAC
tOFC
W0-15/
IO0-15
HI-Z
Read Data
tFRS
tFRH
DSF
83YL-9270B

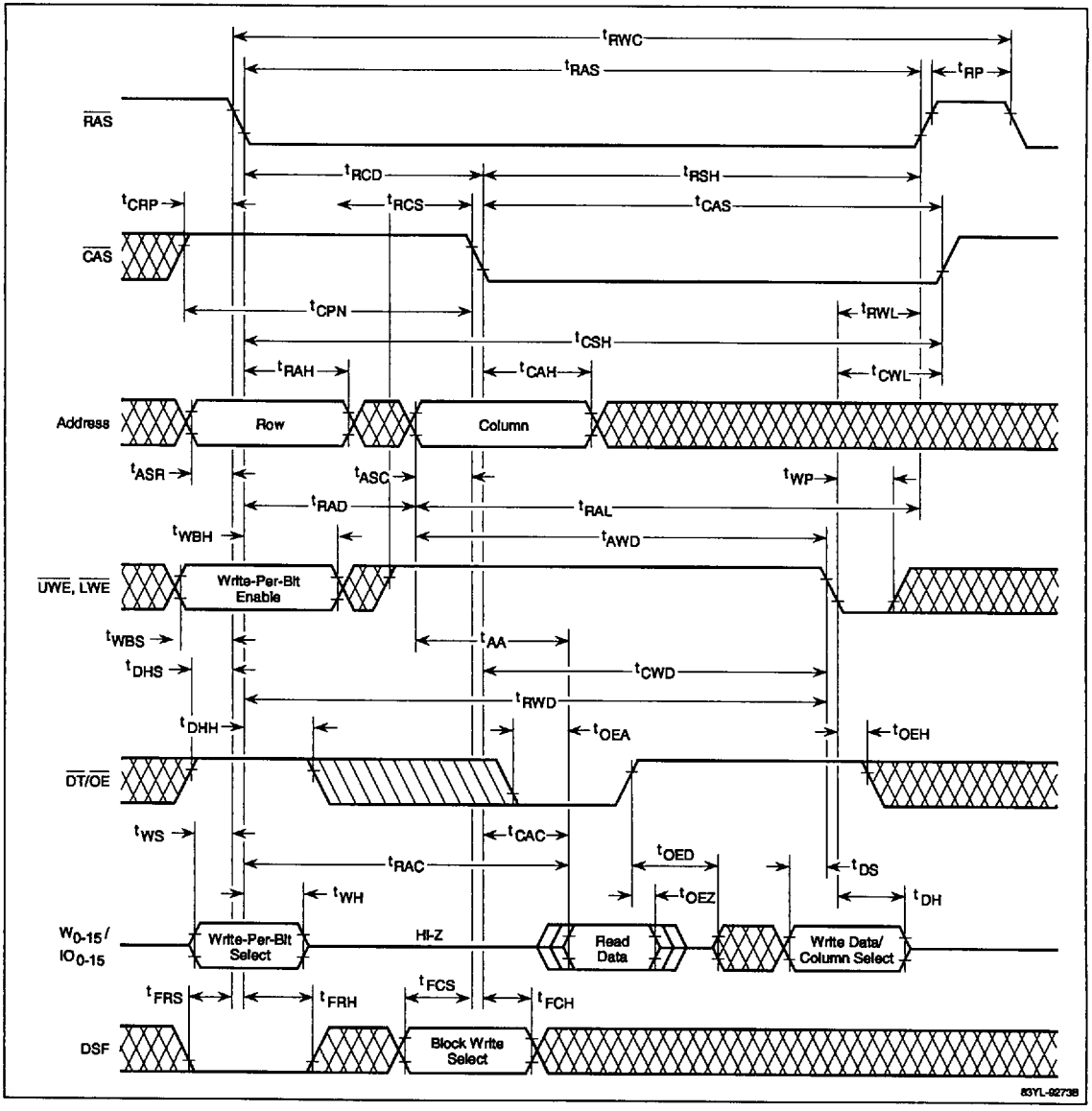
Early Write Cycle and Early Block Write Cycle



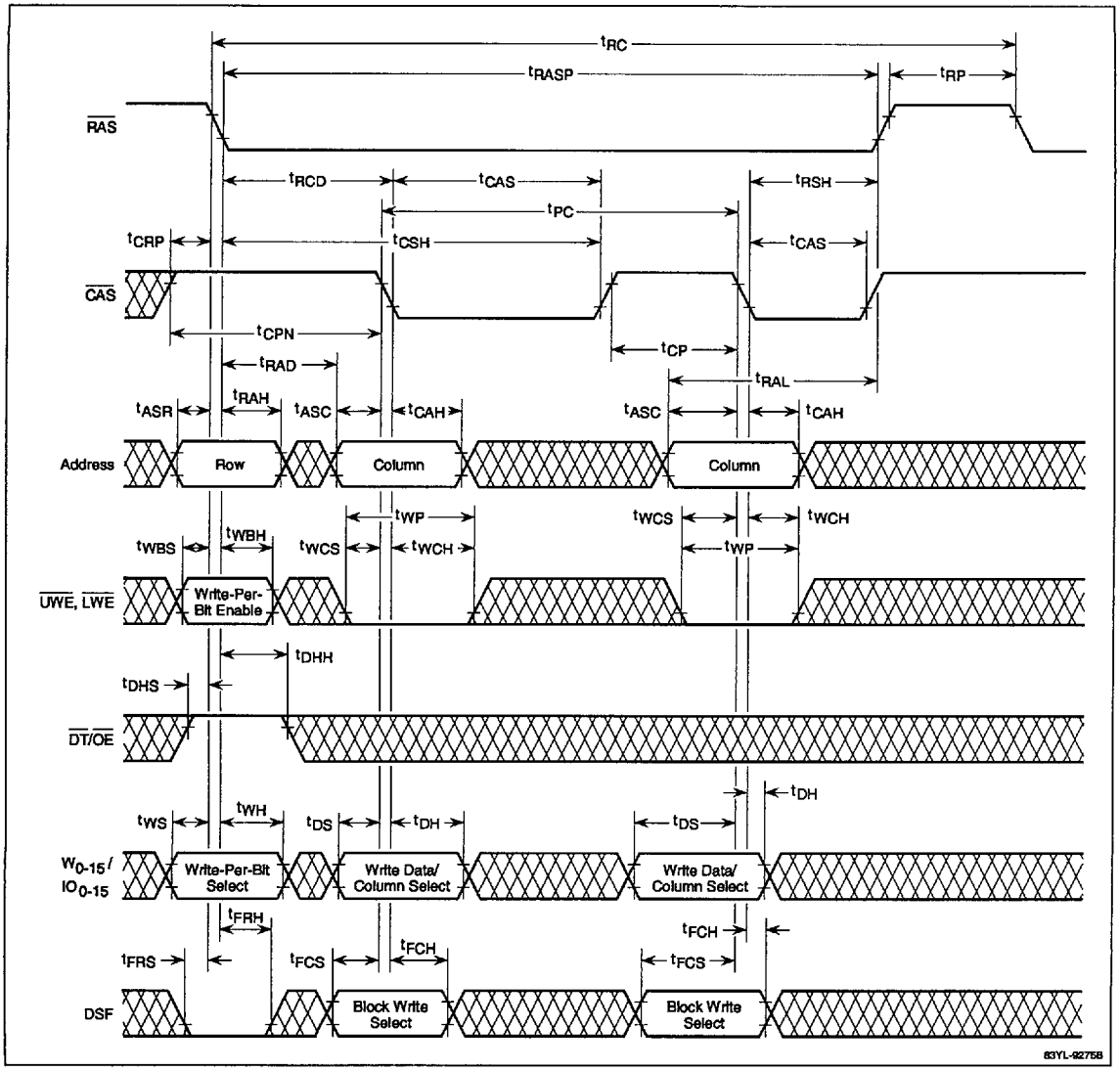
Late Write Cycle and Late Block Write Cycle



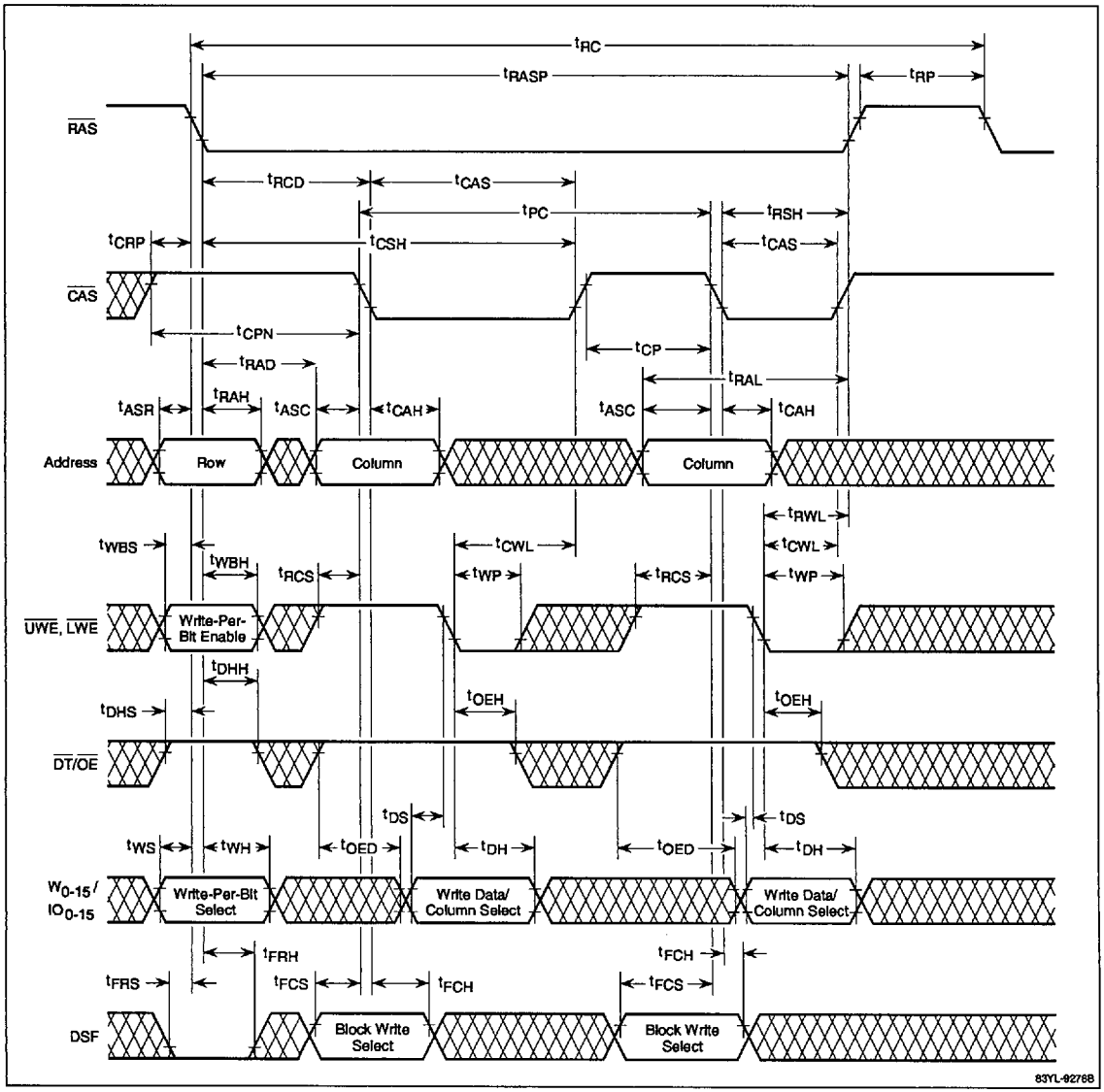
Read-Write/Read-Modify-Write Cycle



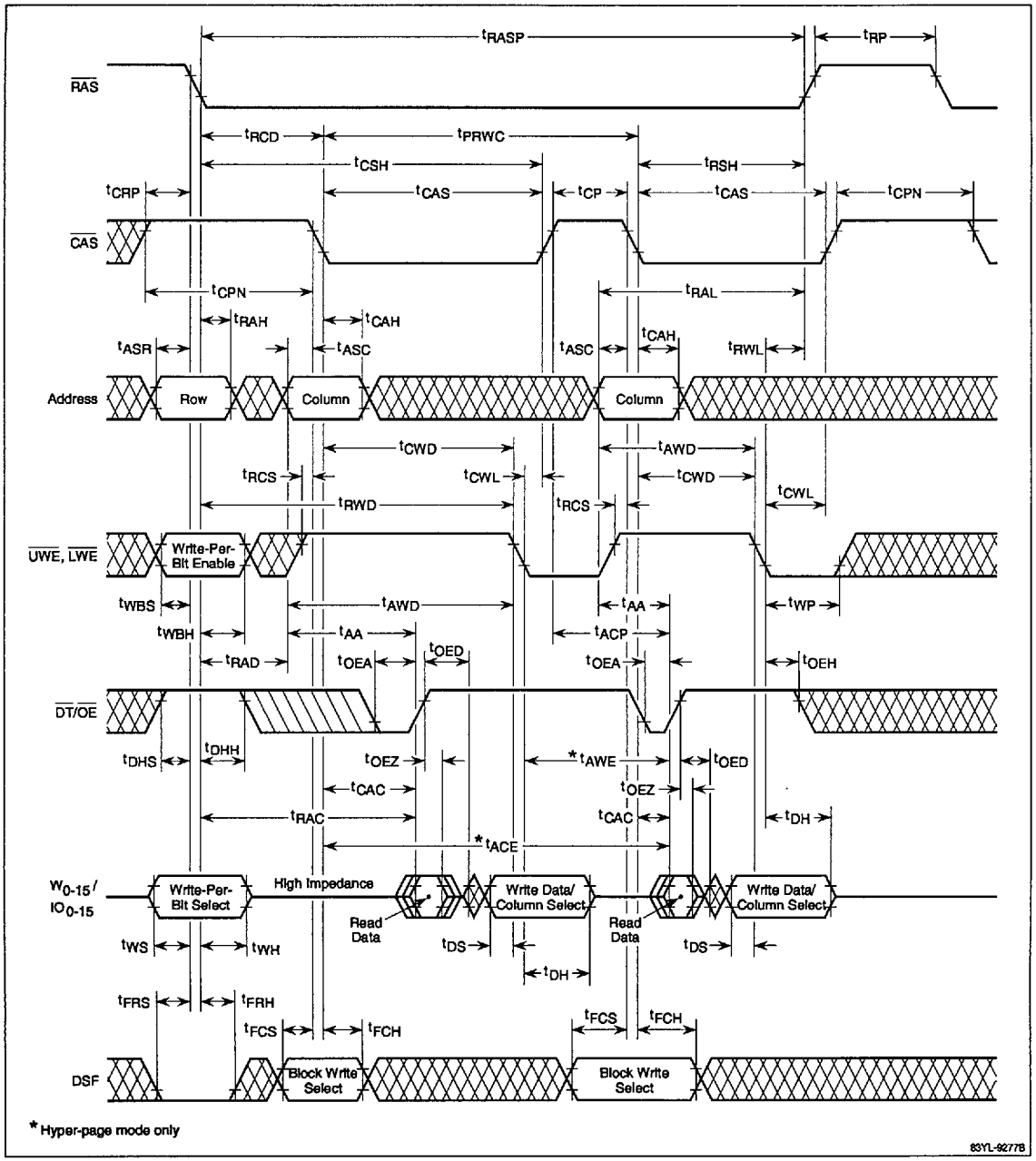
Fast-Page/Hyper-Page Early Write or Early Block Write Cycle



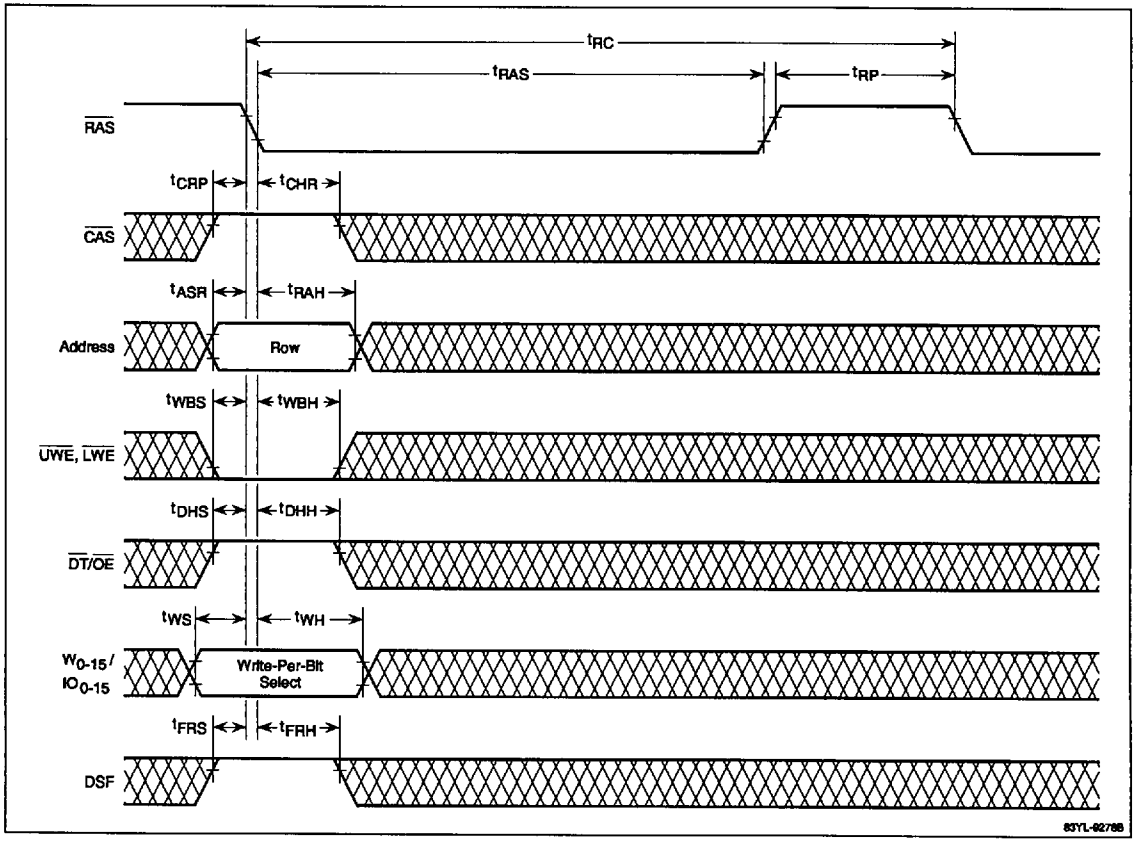
Fast-Page/Hyper-Page Late Write or Late Block Write Cycle



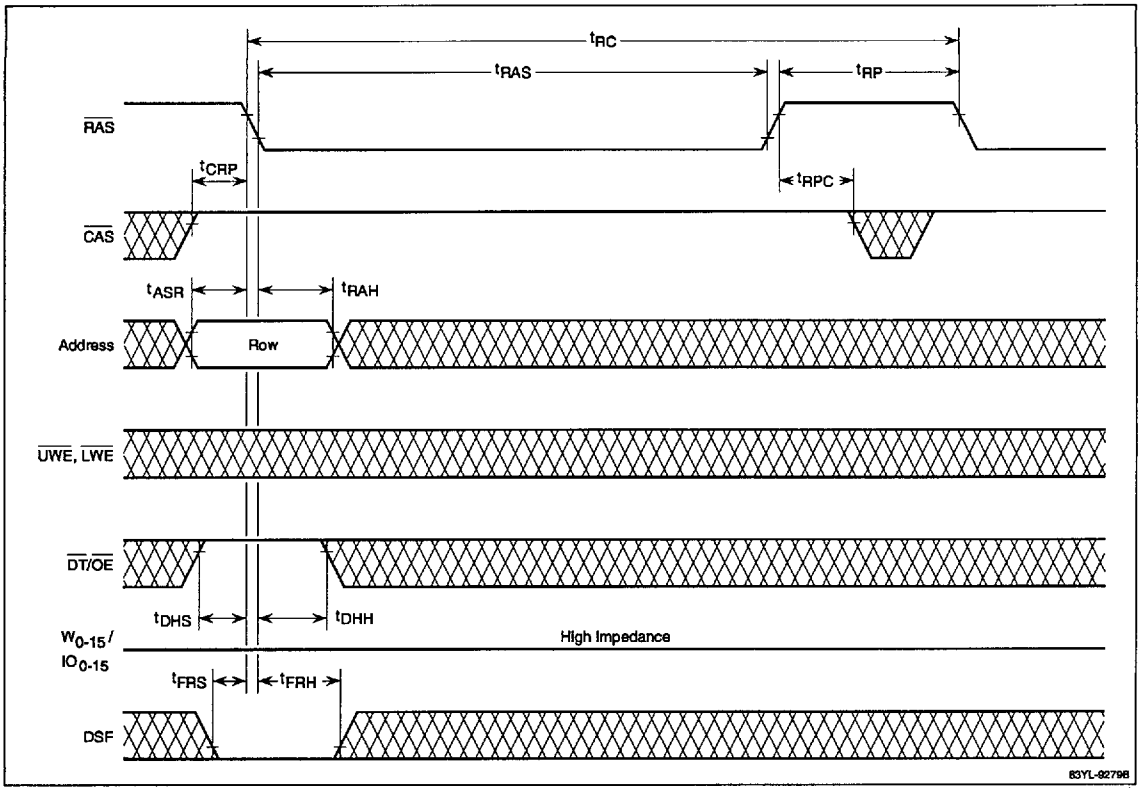
Fast-Page/Hyper-Page Read-Modify-Write Cycle



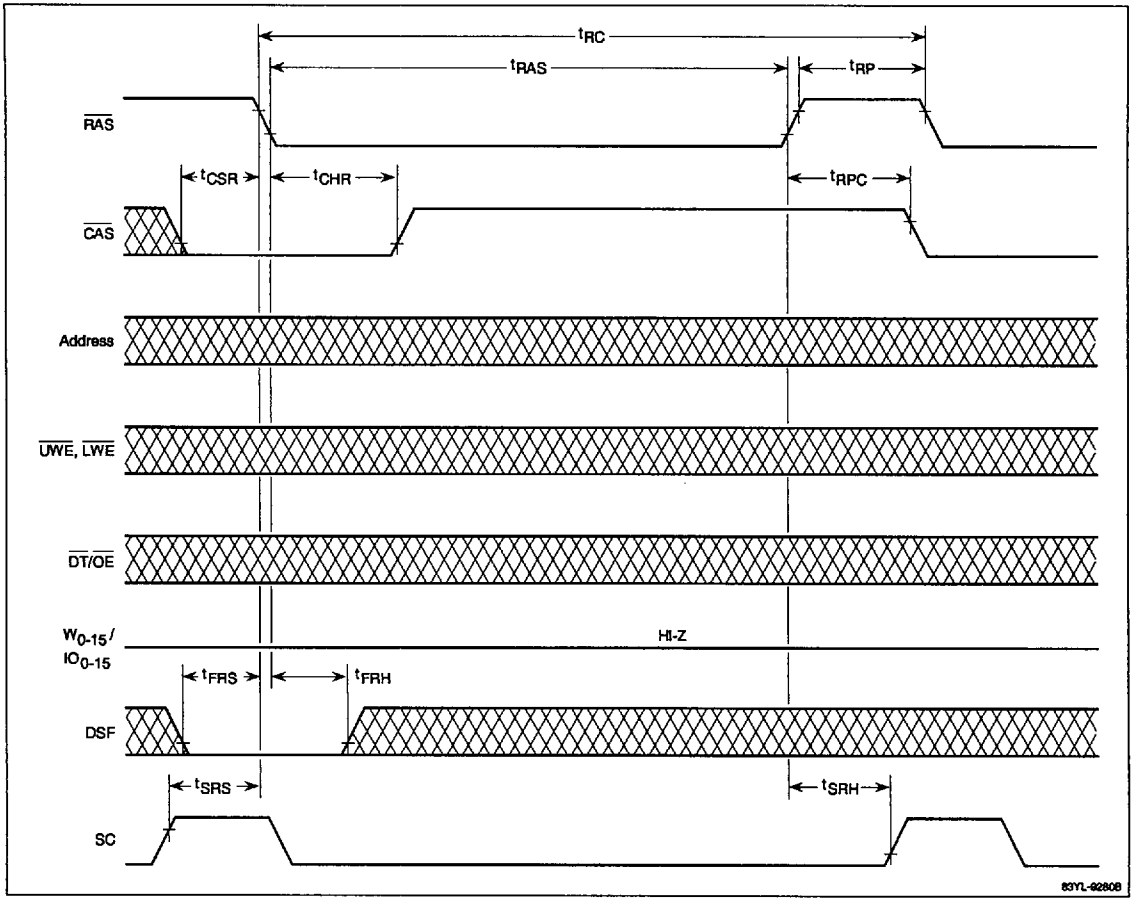
Flash Write Cycle



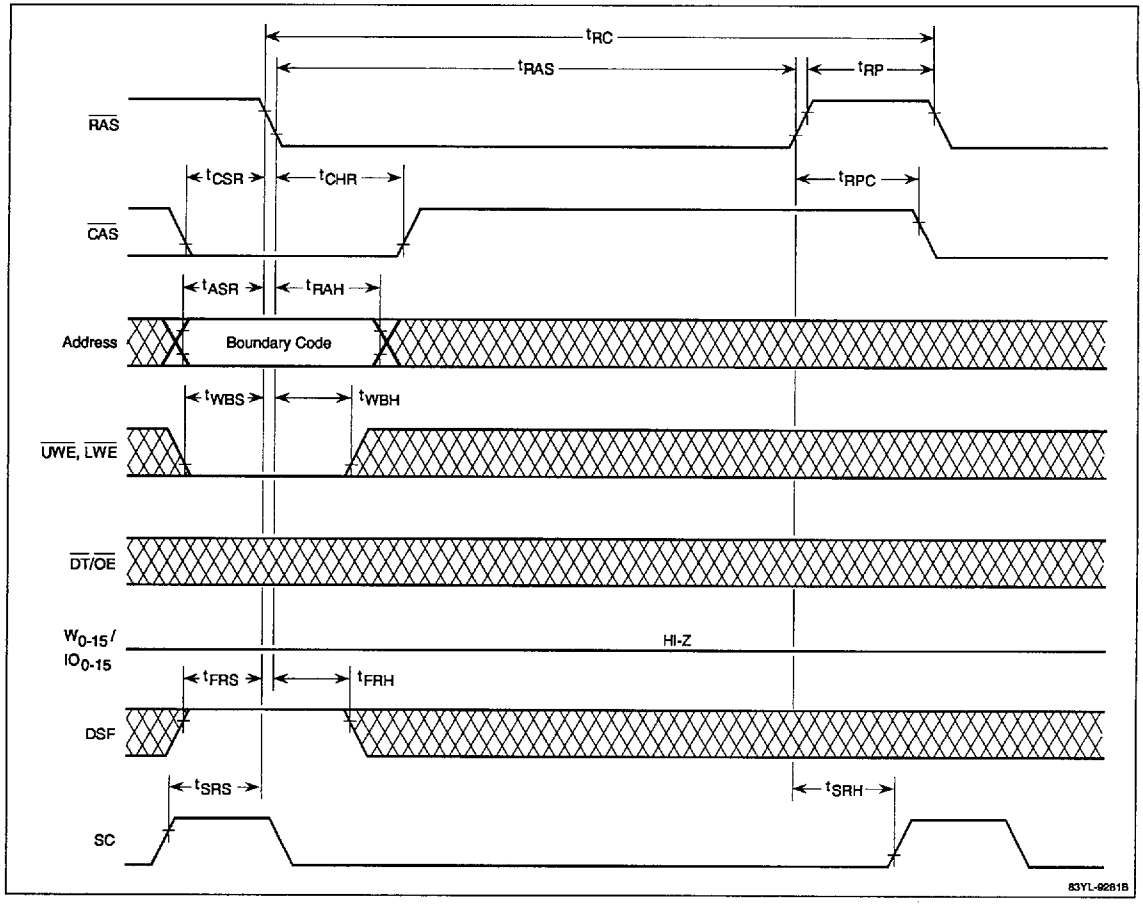
$\overline{RAS}$-Only Refresh Cycle



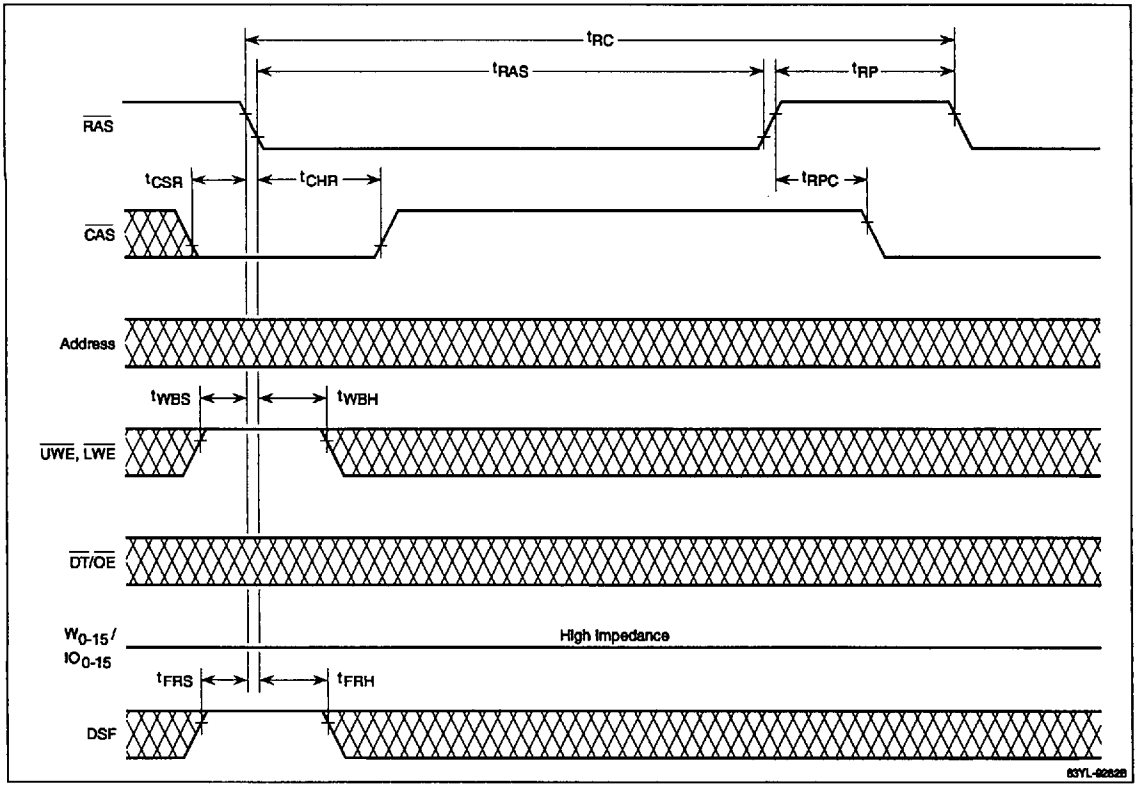
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle With Option Reset (CBR)



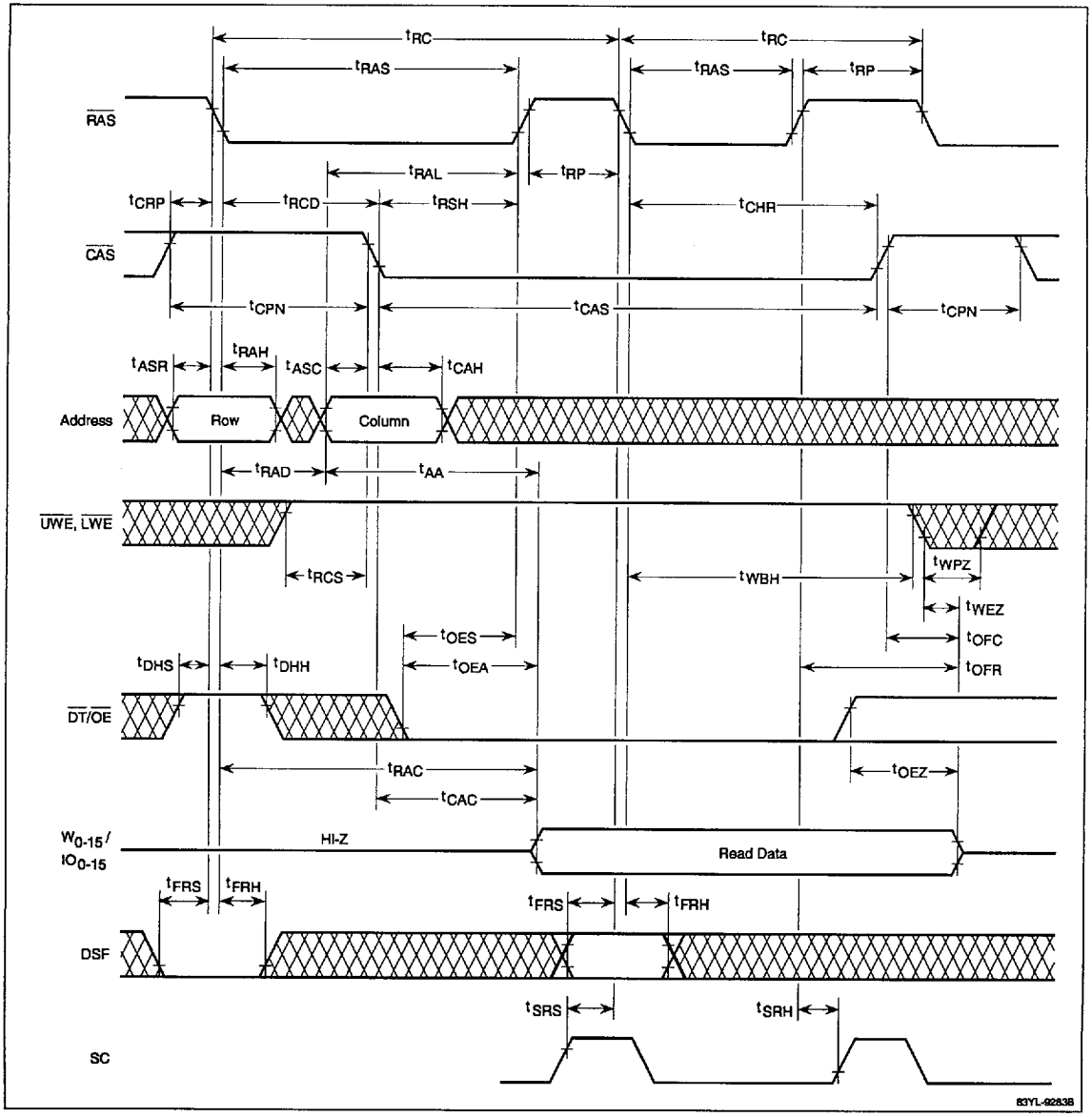
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle With Stop Register Set (CBRS)



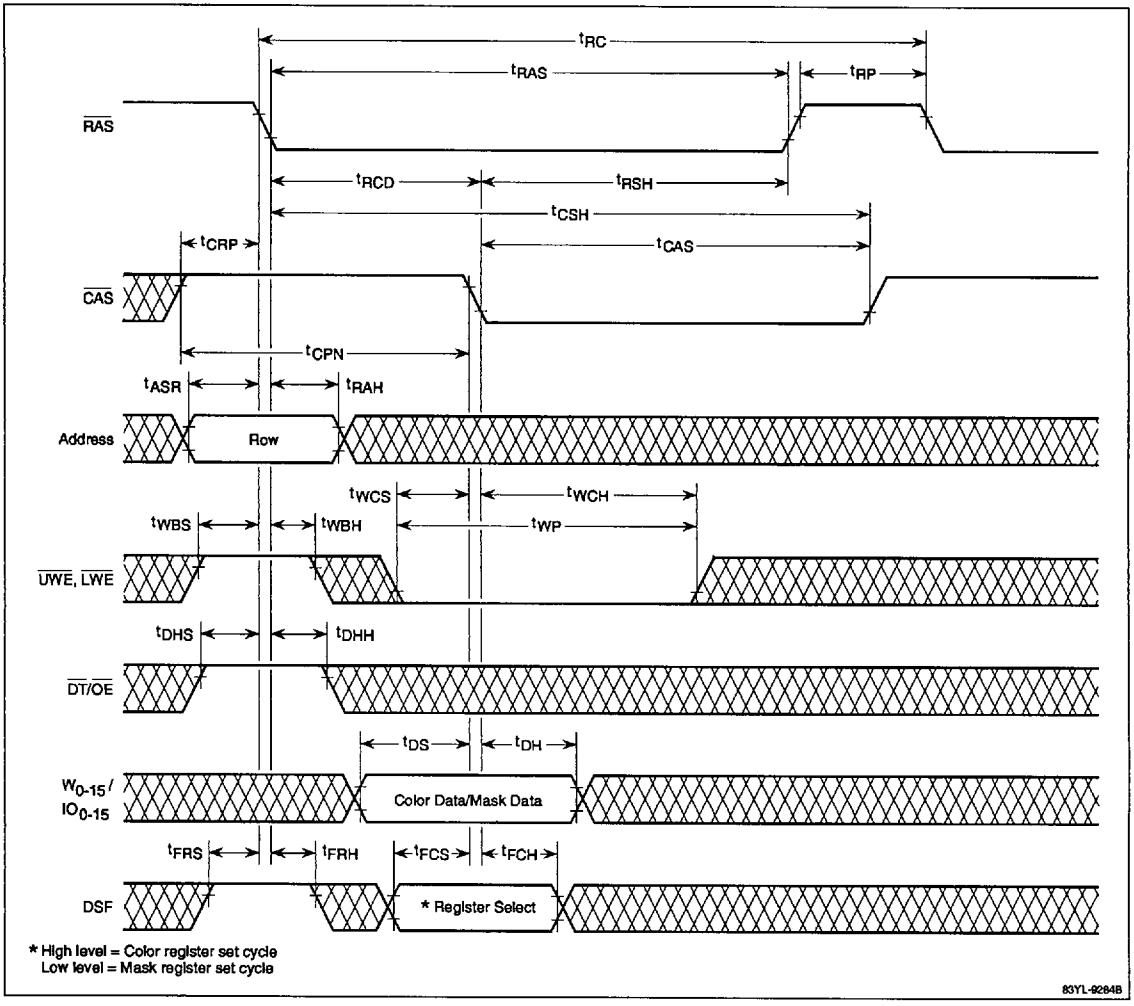
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle With No Option Reset (CBRN)



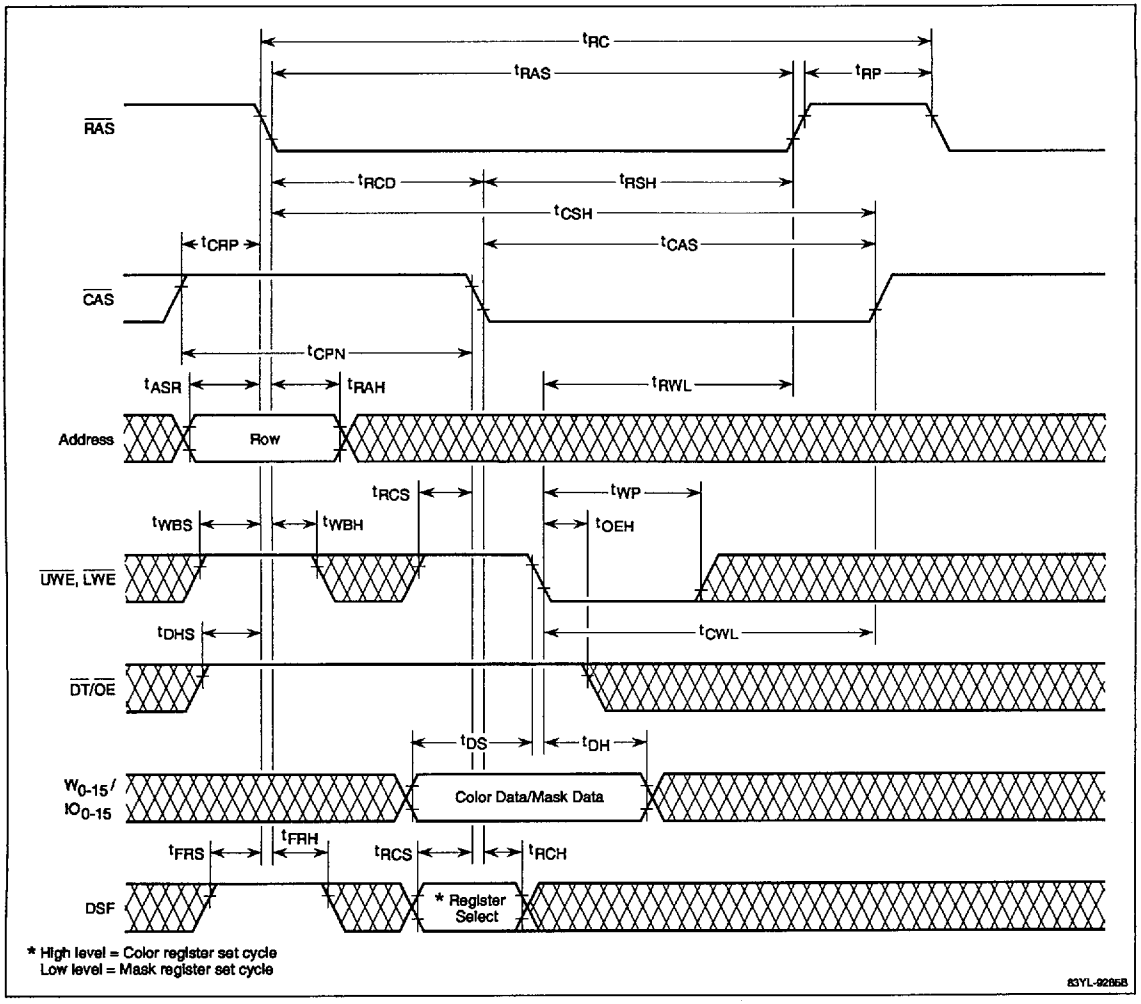
Hidden Refresh Cycle



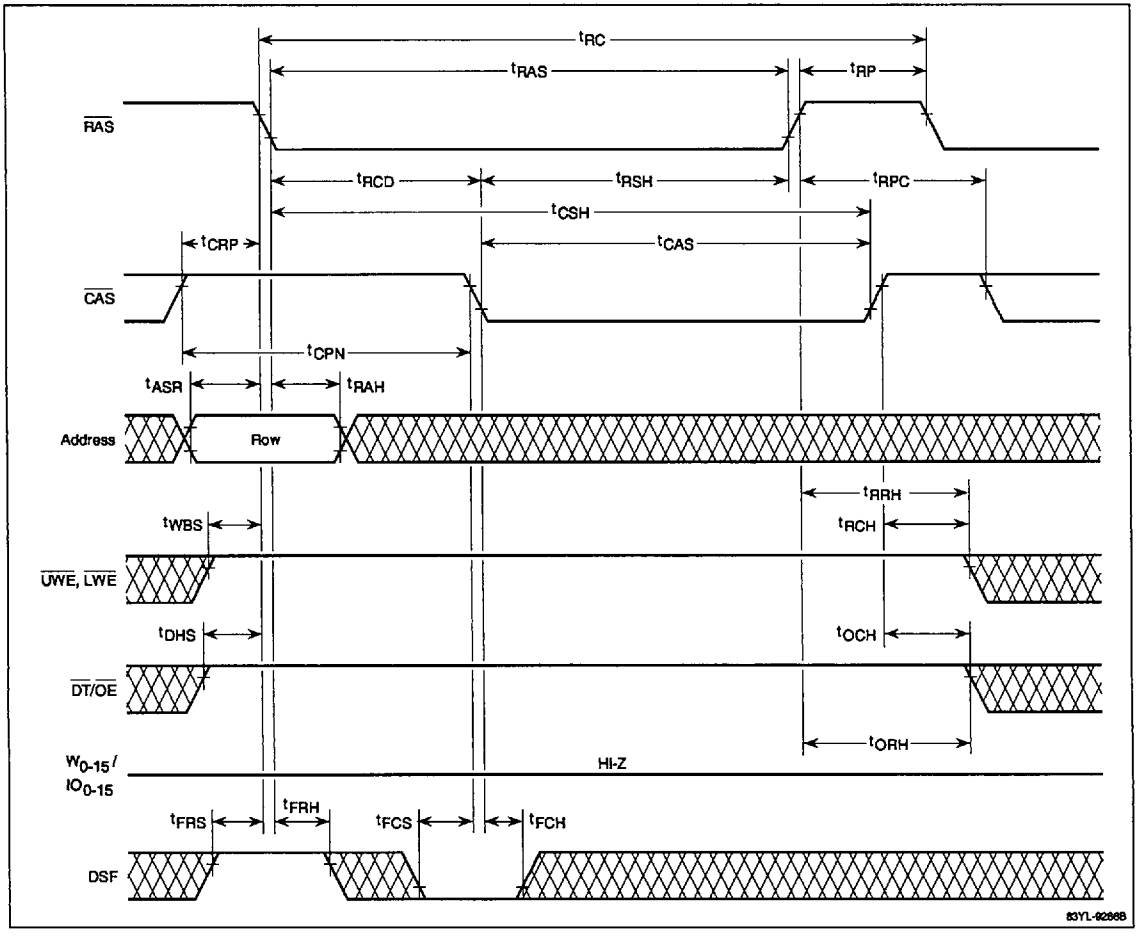
Register Set LMR and LCR Cycles (Early Write)



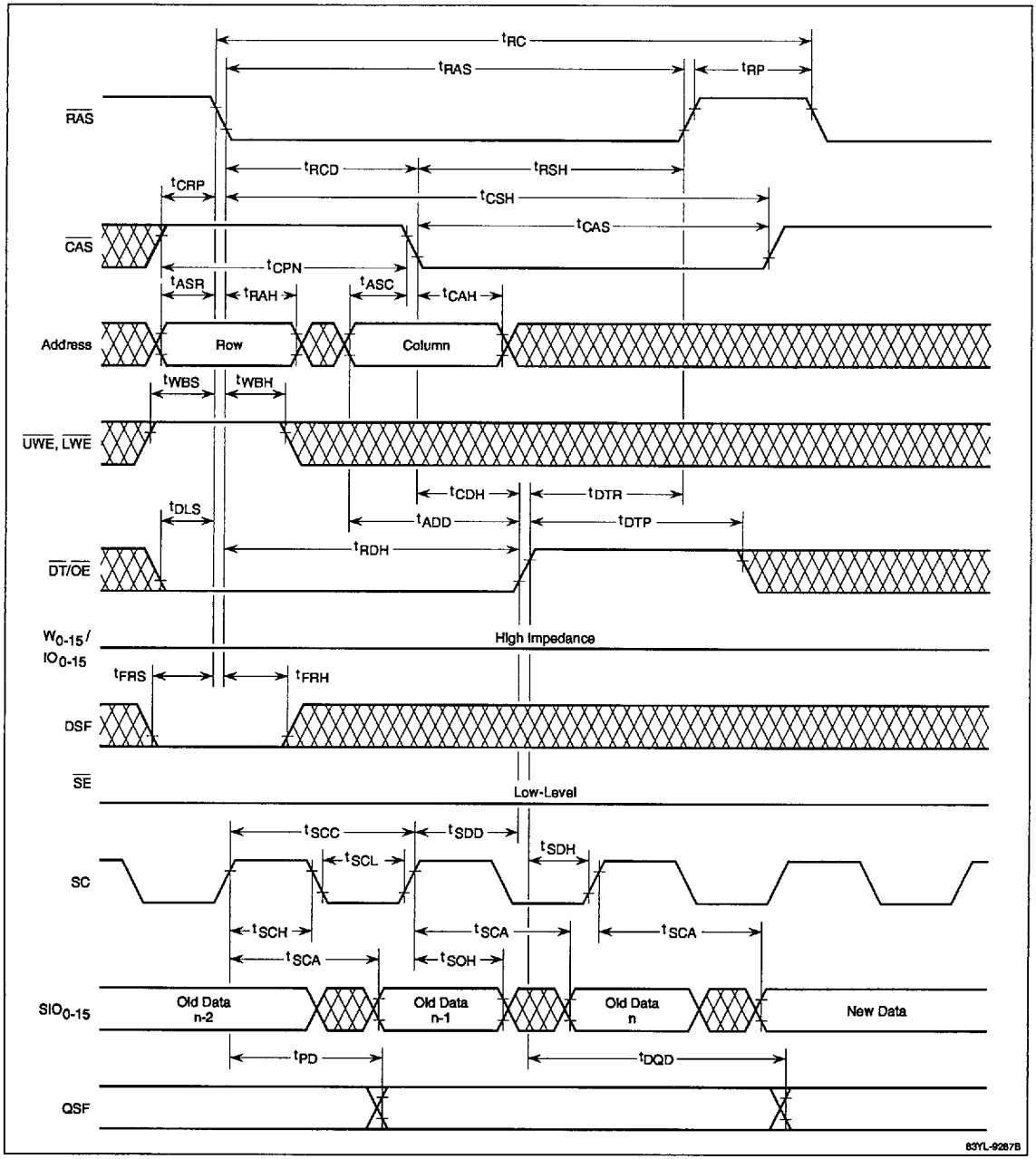
Register Set LMR and LCR Cycles (Late Write)



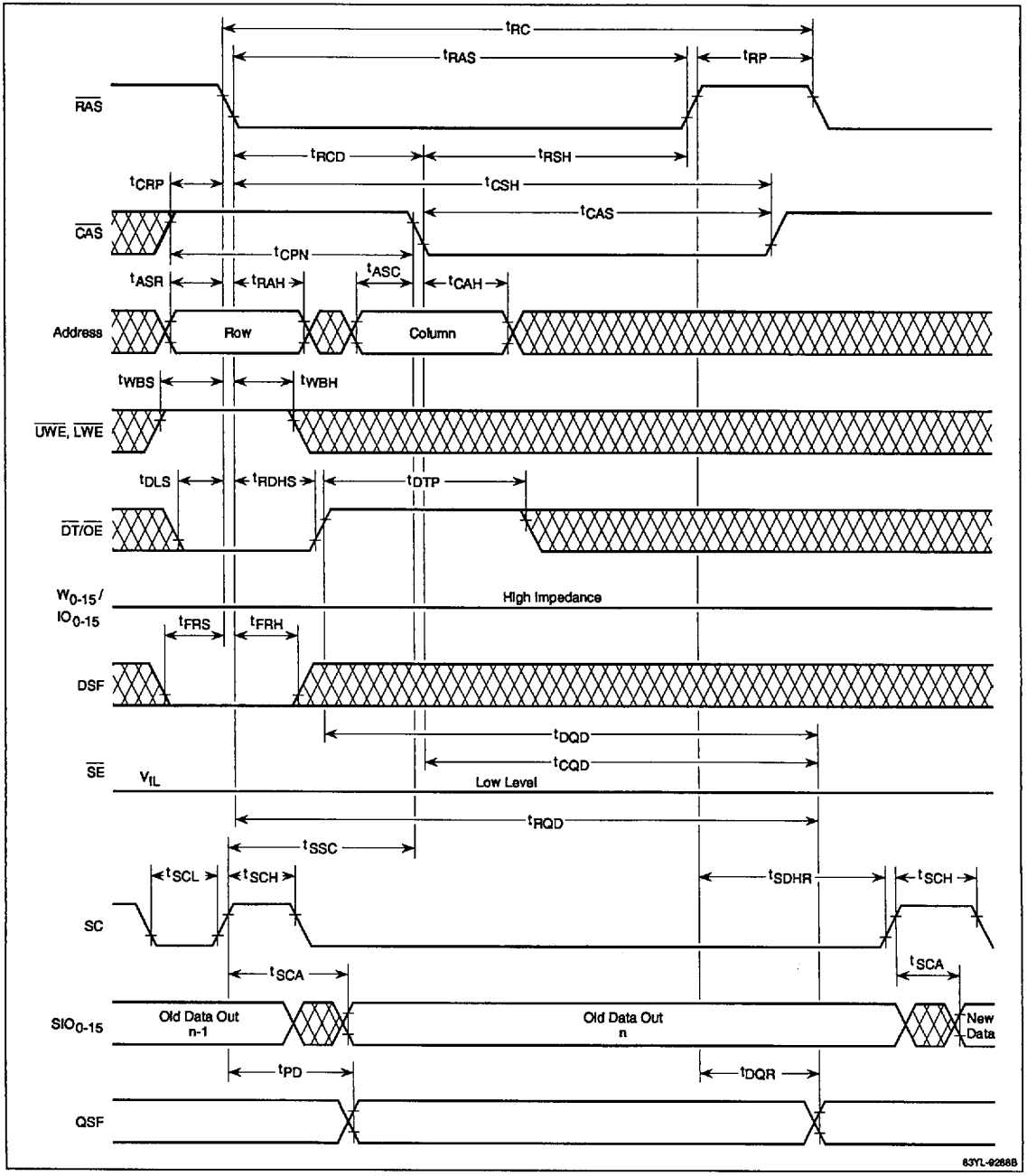
Reset Mask Register to New Mask Mode Cycle (non-JEDEC Standard)



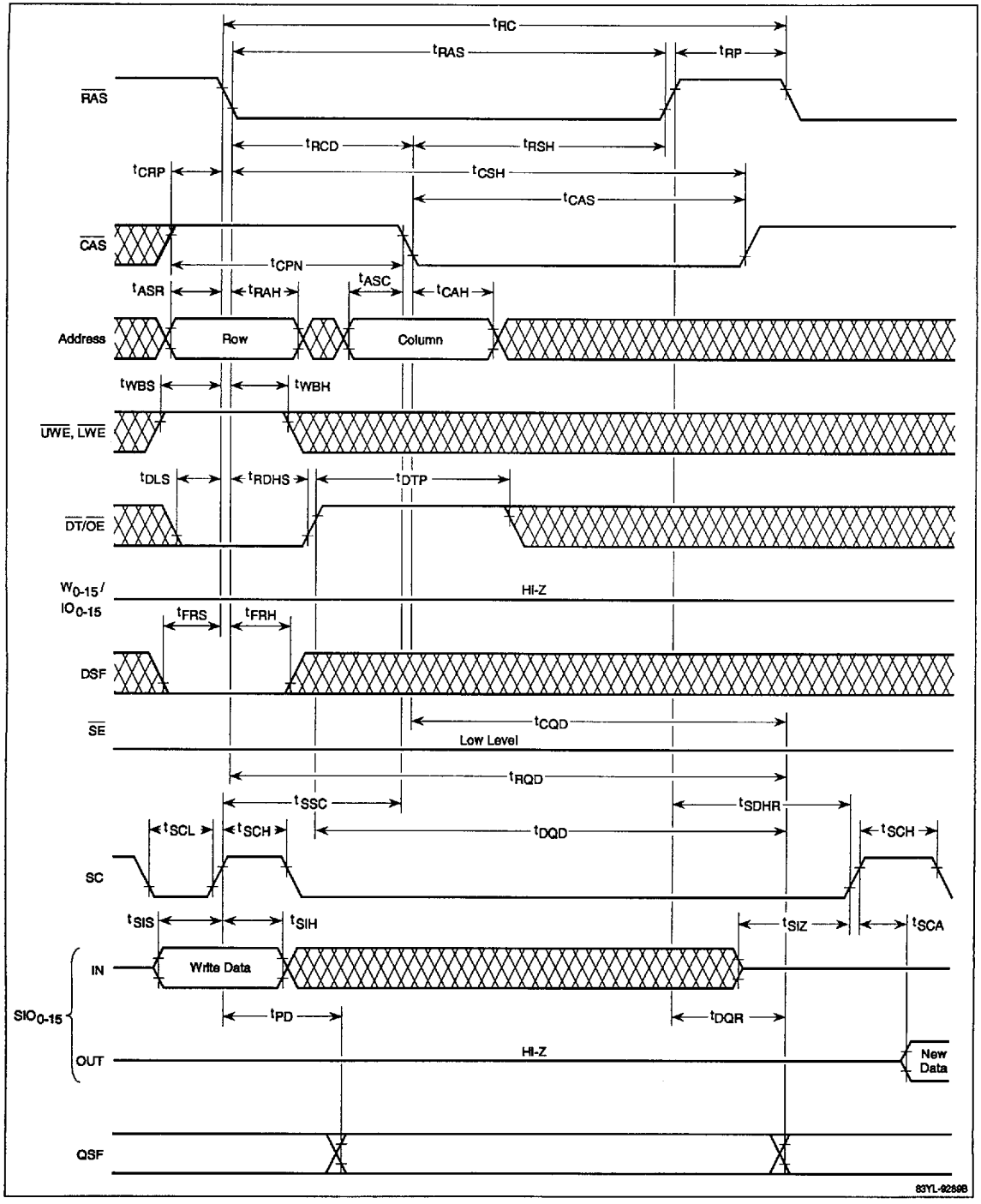
Data Transfer Cycle With Serial Port Active



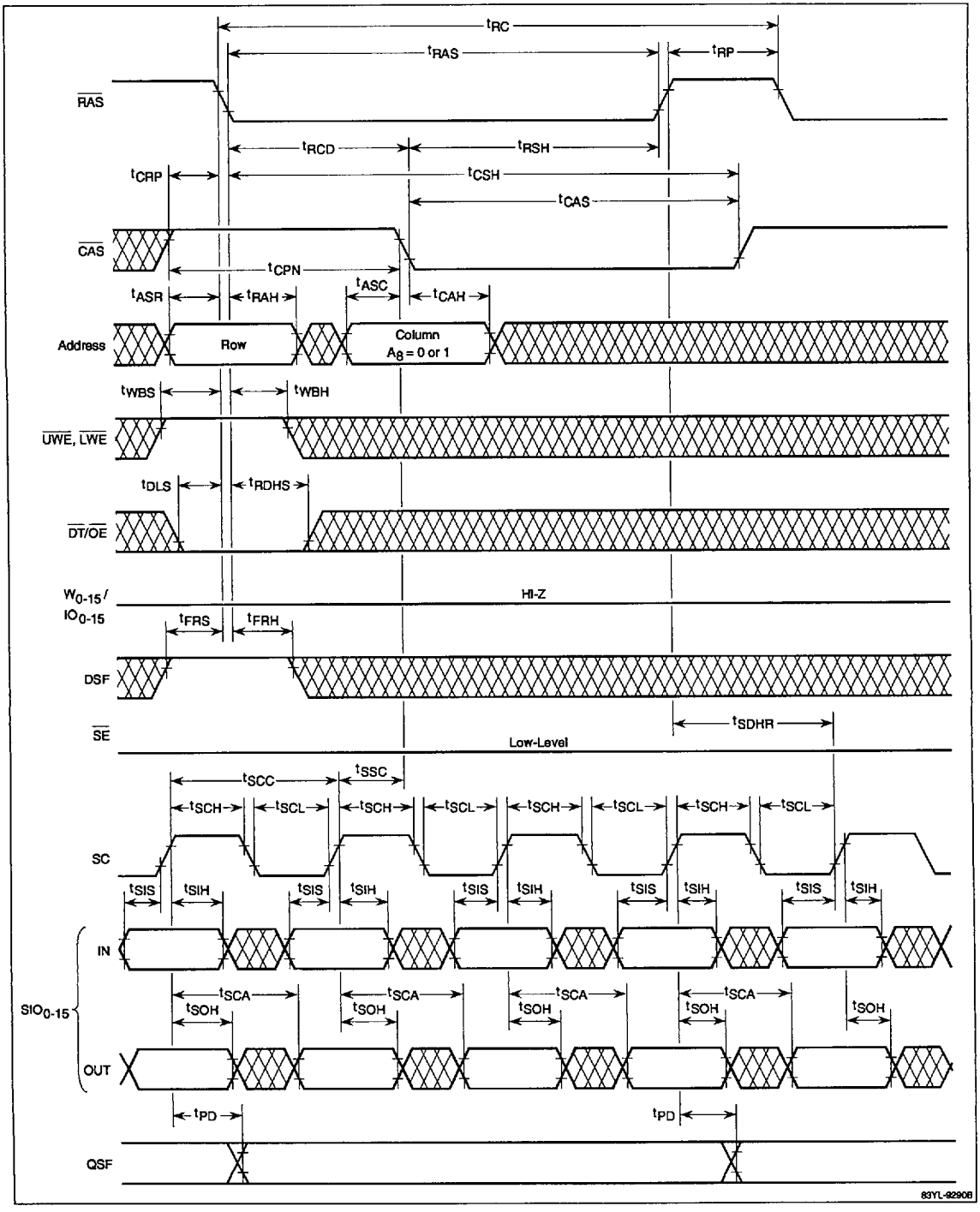
Data Transfer Cycle With Serial Port in Standby



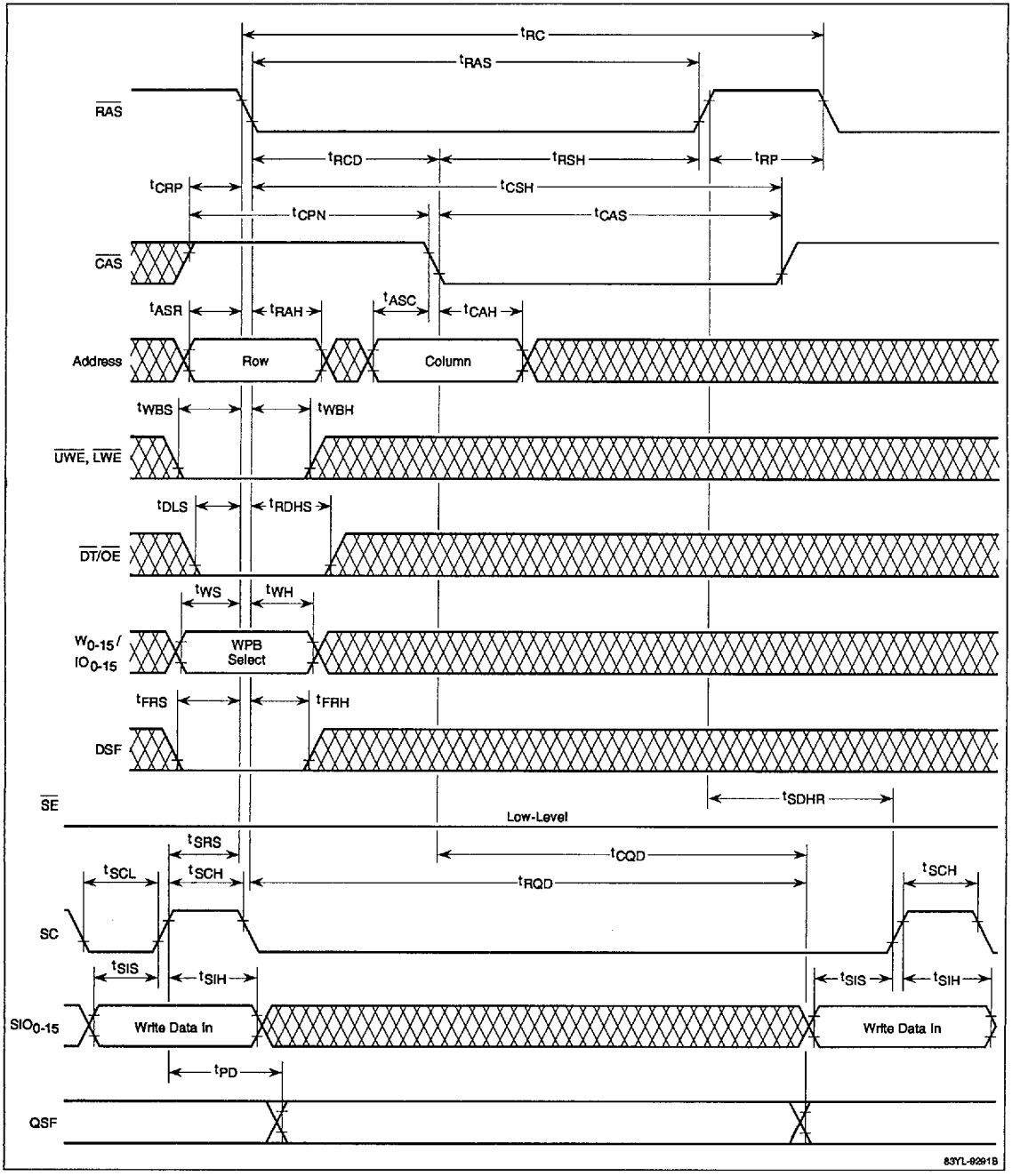
Read Data Transfer Cycle (Serial Write to Read Mode Switch)



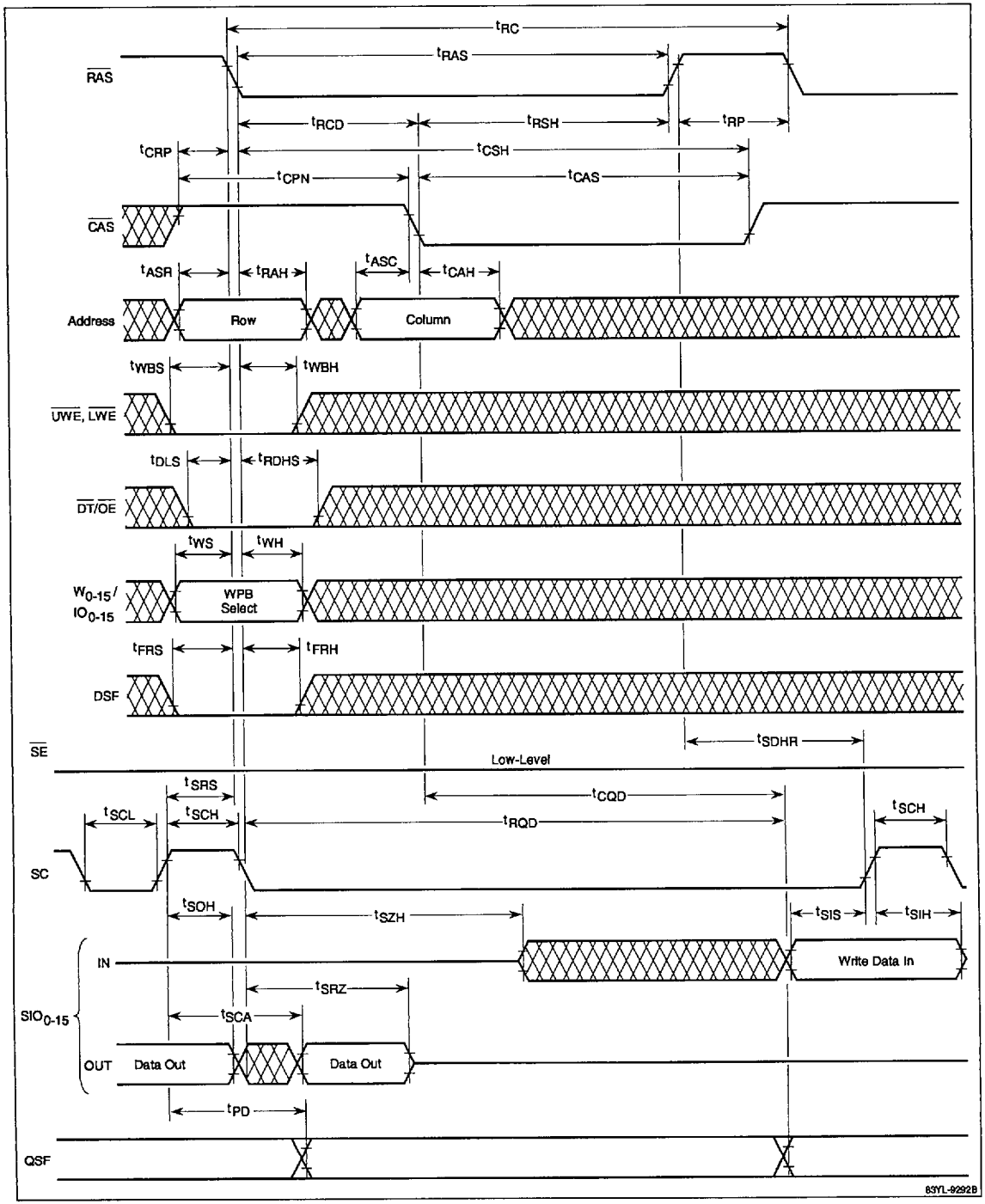
Split Read Data Transfer Cycle



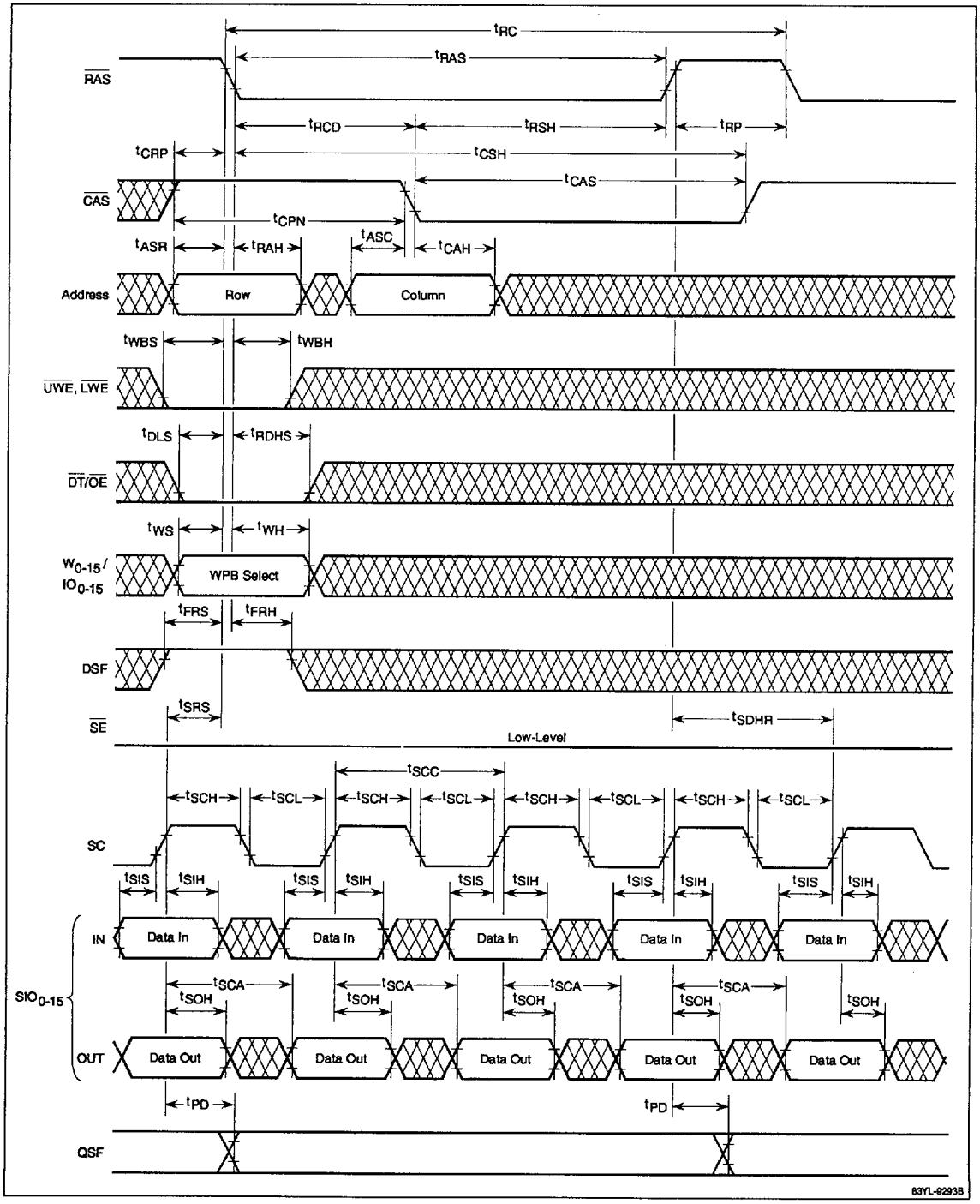
Write Data Transfer Cycle



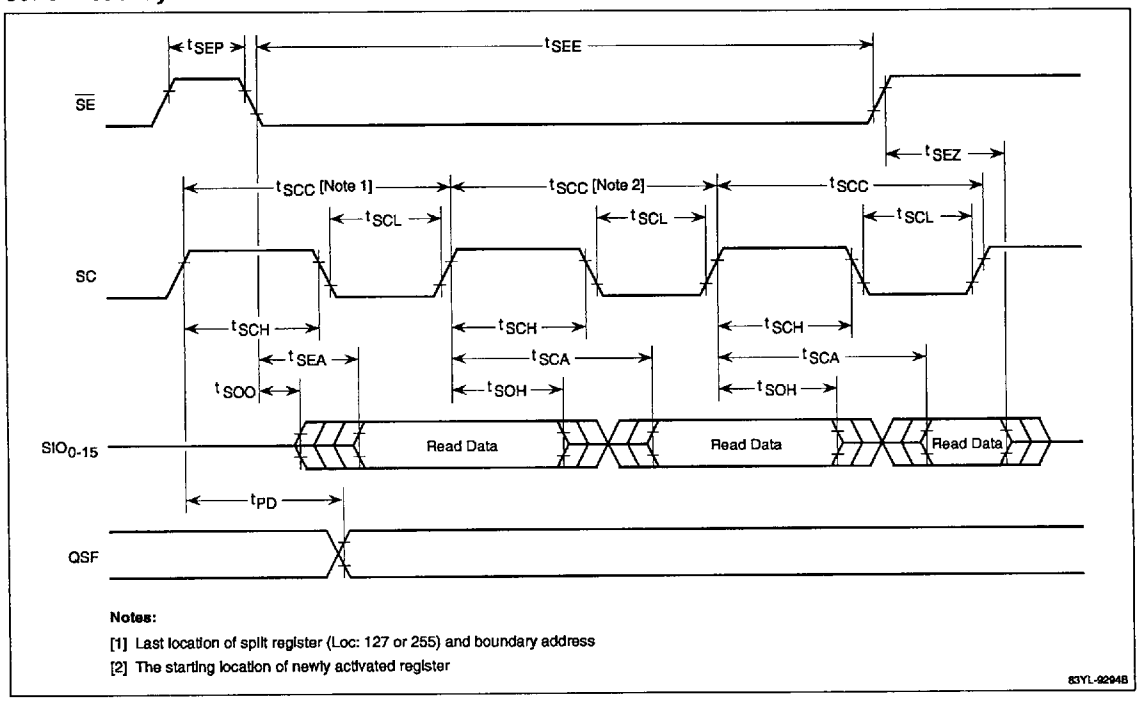
Write Data Transfer Cycle (Serial Read to Write Mode Switch)



Split Write Data Transfer Cycle



Serial Read Cycle



Notes:

[1] Last location of split register (Loc: 127 or 255) and boundary address

[2] The starting location of newly activated register

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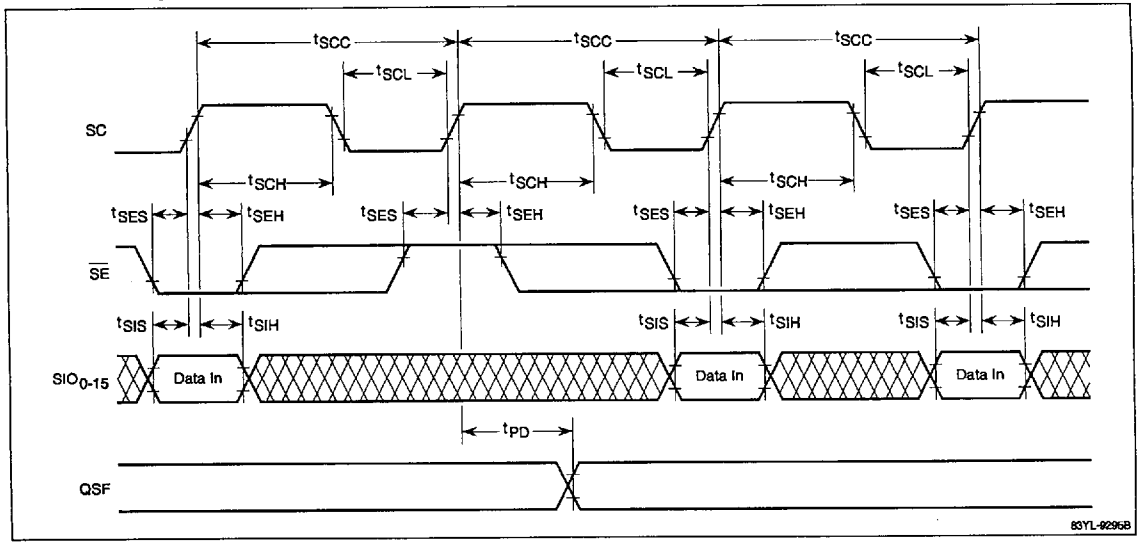
Serial Write Cycle



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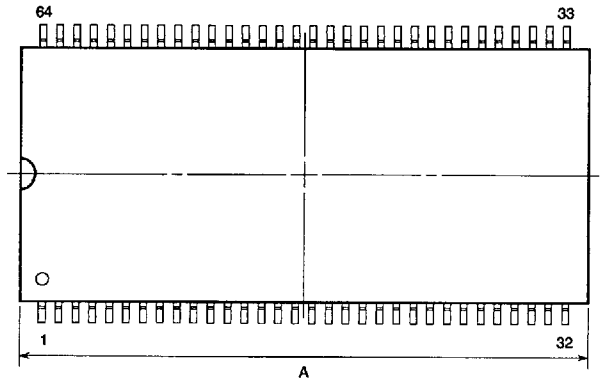
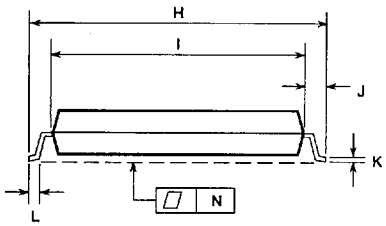
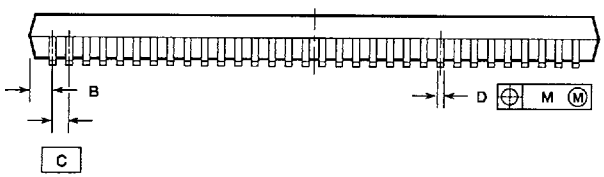
PACKAGE DRAWINGS

64-Pin Plastic SSOP

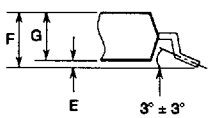
Item	Millimeters	Inches
A	26.25 max	1.033 max
B	0.73 max	.029 max
C	0.8 (TP)	.031 (TP)
D	0.35 ± 0.10	.014 ± .004
E	0.15 ± 0.05	.006 ± .002
F	2.3 max	.091 max
G	2.0 min	.079 min
H	13.8 ± 0.3	.543 ± .012
I	11.8 ± 0.1	.465 ± .004
J	1.0 ± 0.2	.039 ± .008
K	0.225 ± 0.075	.009 ± .003
L	0.5 ± 0.2	.020 ± .008
M	0.1 min	.004 min
N	0.10	.004







Enlarged detail of lead end



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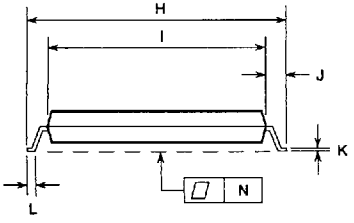
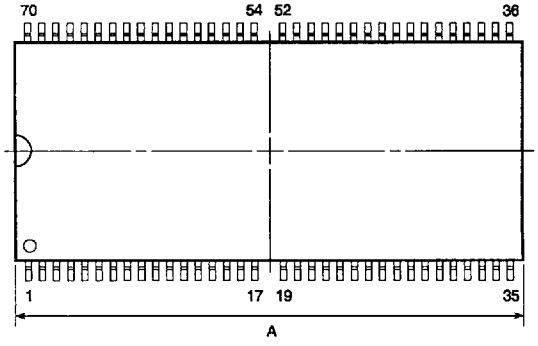
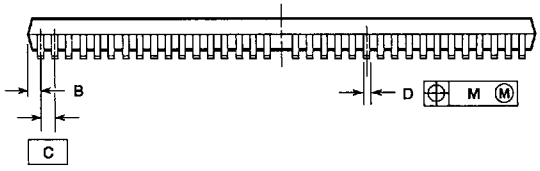
70-Pin Plastic TSOP

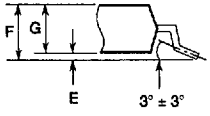
Item	Millimeters	Inches
A	23.89 max	.941
B	0.9 max	.035 max
C	0.65 (TP)	.026 (TP)
D	0.3 ± 0.1	.012 ± .004
E	0.05 ± 0.05	.002 ± .002
F	1.1 max	.043 max
G	0.97 min	.038 min
H	11.76 ± 0.2	.463 ± .008
I	10.16	.400
J	0.8 ± 0.2	.031 ± .008
K	0.150 ± 0.075	.006 ± .003
L	0.5 ± 0.1	.020 ± .004
M	0.1	.004
N	0.10	.004







Enlarged detail of lead end



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