NEC

MOS INTEGRATED CIRCUIT

μPD485506

LINE BUFFER
5K-WORD BY 16-BIT/10K-WORD BY 8-BIT

Description

The μPD485506 is a high speed FIFO (First In First Out) line buffer. Word organization can be changed either 5,048 words by 16 bits or 10,096 words by 8 bits.

Its CMOS static circuitry provides high speed access and low power consumption.

The μPD485506 can be used for one line delay and time axis conversion in high speed facsimile machines and digital copiers.

Moreover, the μPD485506 can execute read and write operations independently on an asynchronous basis. Thus the μPD485506 is suitable as a buffer for data transfer between units with different transfer rates and as a buffer for the synchronization of multiple input signals.

There are four versions, E, K, P and X. These versions operate with different specifications. Each version is identified with its lot number (refer to **7. Example of Stamping**).

Features

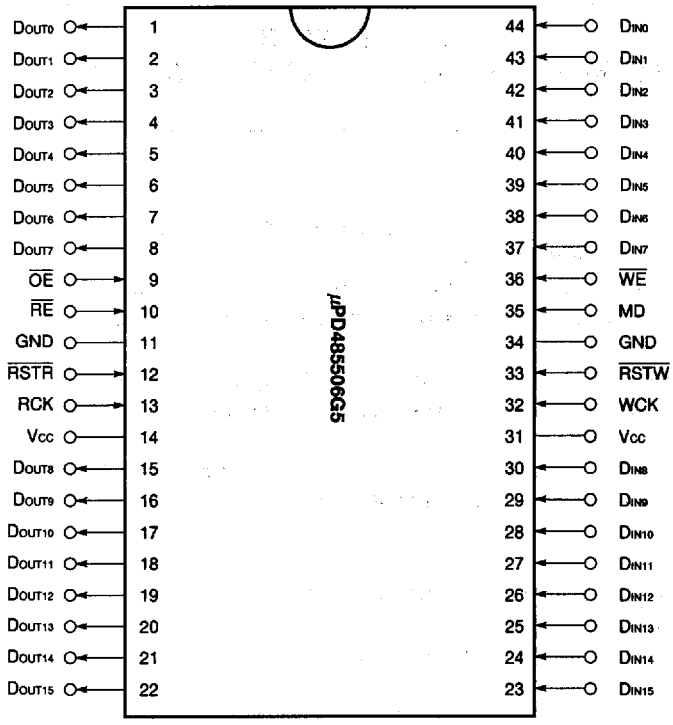
- 5,048 words by 16 bits (Word mode) /10,096 words by 8 bits (Byte mode)
- Full static operation; data hold time = infinity
- Suitable for sampling one line of A3 size paper (16 dots/mm)
- Asynchronous read/write operations available
- Variable length delay bits; 21 to 5,048 bits or 10,096 bits (Cycle time: 25 ns)
  15 to 5,048 bits or 10,096 bits (Cycle time: 35 ns)
- Power supply voltage Vcc = 5 V ± 10 %
- All input/output TTL compatible
- 3-state output

Ordering Information

Part Number	R/W Cycle Time	Package
μPD485506G5-25	25 ns	44-pin plastic TSOP (II) (400 mil)
μPD485506G5-35	35 ns	

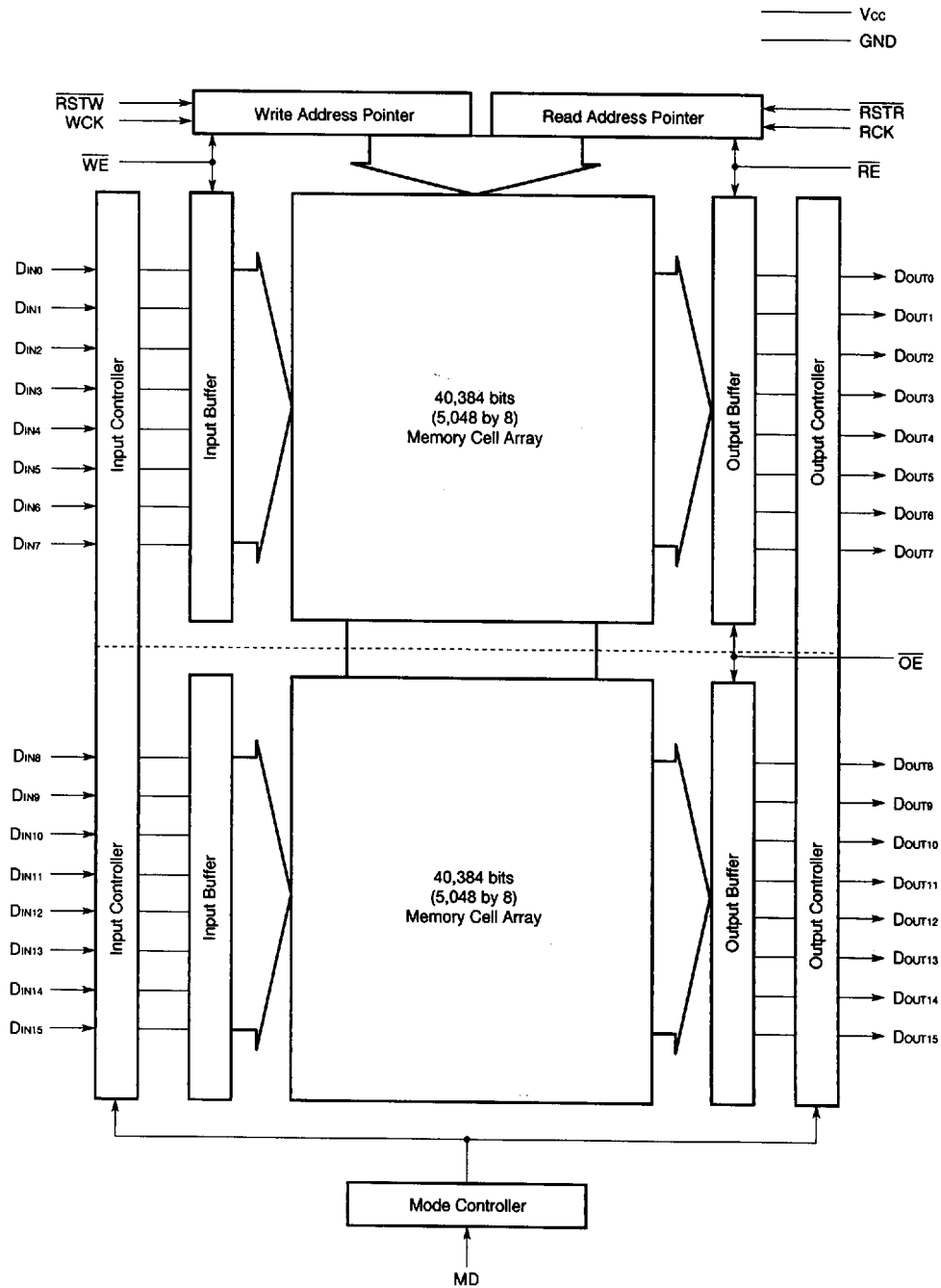
Pin Configuration (Marking side)

44-pin plastic TSOP (II) (400 mil)



DIN0 to DIN15	:	Data Inputs
DOUT0 to DOUT15	:	Data Outputs
WCK	:	Write Clock Input
RCK	:	Read Clock Input
$\overline{WE}$	:	Write Enable Input
$\overline{RE}$	:	Read Enable Input
$\overline{OE}$	:	Output Enable Input
$\overline{RSTW}$	:	Reset Write Input
$\overline{RSTR}$	:	Reset Read Input
MD	:	Mode Set Input
VCC	:	+5 V Power Supply
GND	:	Ground

Block Diagram



1. Pin Function

Pin Number	Pin Symbol	Pin Name	I/O	Function
23 - 30 37 - 44	D_{IN0} I D_{IN15}	Data Input	In	Write data input pins. The data inputs are strobed by the rising edge of WCK at the end of a cycle and the setup and hold times (t_{DS}, t_{DH}) are defined at this point.
1 - 8 15 - 22	D_{OUT0} I D_{OUT15}	Data Output	Out	Read data output pins. The access time is regulated from the rising edge of RCK at the beginning of a cycle and defined by t_{AC}.
33	$\overline{RSTW}$	Reset Write Input	In	Reset input pin for the initialization of the write address pointer. The state of $\overline{RSTW}$ is strobed by the rising edge of WCK at the beginning of a cycle and the setup and hold times (t_{RS}, t_{RH}) are defined.
12	$\overline{RSTR}$	Reset Read Input	In	Reset input pin for the initialization of the read address pointer. The state of $\overline{RSTR}$ is strobed by the rising edge of RCK at the beginning of a cycle and the setup and hold times (t_{RS}, t_{RH}) are defined.
36	$\overline{WE}$	Write Enable Input	In	Write operation control signal input pin. When $\overline{WE}$ is in the disable mode ("H" level), the internal write operation is inhibited and the write address pointer stops at the current position.
10	$\overline{RE}$	Read Enable Input	In	Read operation control signal input pin. When $\overline{RE}$ is in the disable mode ("H" level), the internal read operation is inhibited and the read address pointer stops at the current position. The data outputs remain valid for that address.
9	$\overline{OE}$	Output Enable Input	In	Output operation control signal input pin. When $\overline{OE}$ is in the disable mode ("H" level), the data out is inhibited and the output changes to high impedance. The internal read operation is executed at that time and the read address pointer incremented in synchronization with the read clock.
32	WCK	Write Clock Input	In	Write clock input pin. When $\overline{WE}$ is enabled ("L" level), the write operation is executed in synchronization with the write clock. The write address pointer is incremented simultaneously.
13	RCK	Read Clock Input	In	Read clock input pin. When $\overline{RE}$ is enabled ("L" level), the read operation is executed in synchronization with the read clock. The read address pointer is incremented simultaneously.
35	MD	Mode Set Input	In	Mode set input pin. The level of MD gives the operation mode. When MD is in "L" level, 5,048 words by 16 bits configuration with D_{IN0} - D_{IN15}, D_{OUT0} - D_{OUT15} is enabled. When MD is in "H" level, 10,096 words by 8 bits configuration with D_{IN0} - D_{IN7}, D_{OUT0} - D_{OUT7} is enabled.

2. Operation Mode

μPD485506 is a synchronous memory. All signals are strobed at the rising edge of the clock (RCK, WCK). For this reason, setup time and hold time are specified for the rising edge of the clock (RCK, WCK).

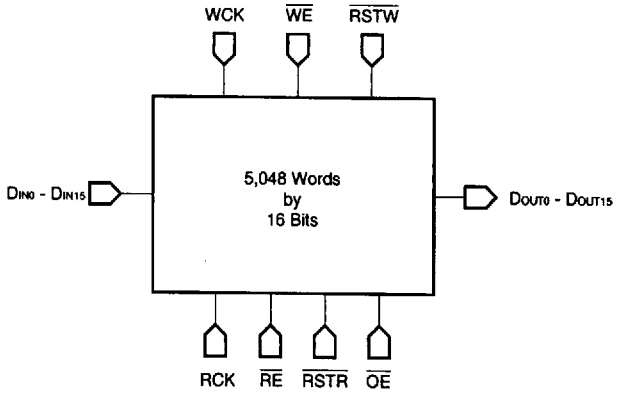
(1) Mode Set Cycle (5,048 words by 16 bits or 10,096 words by 8 bits organization)

μPD485506 has a capability of selecting from two operation modes by judging the MD level when $\overline{RSTW}$ or $\overline{RSTR}$ is enabled in the reset cycle.

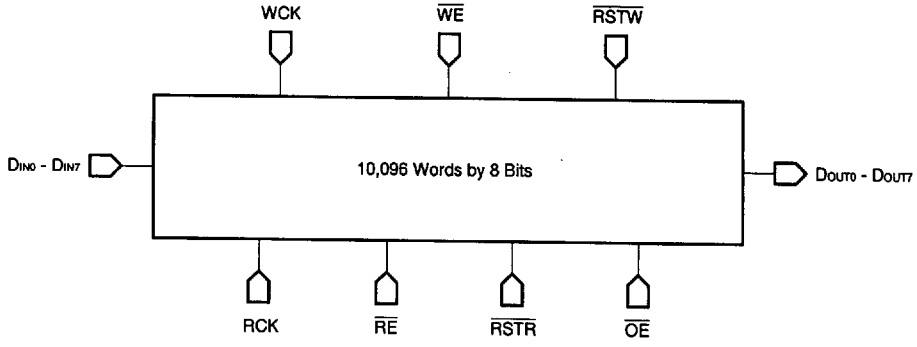
MD Level	Bit Configuration	Data Inputs/Outputs	Control Signal
"L"	5,048 words by 16 bits	D_{IN0} - D_{IN15}	WCK, $\overline{WE}$, $\overline{RSTW}$
		D_{OUT0} - D_{OUT15}	RCK, $\overline{RE}$, $\overline{RSTR}$
"H"	10,096 words by 8 bits	D_{IN0} - D_{IN7}	WCK, $\overline{WE}$, $\overline{RSTW}$
		D_{OUT0} - D_{OUT7}	RCK, $\overline{RE}$, $\overline{RSTR}$

Caution Don't change the MD level during a reset cycle.

5,048 Words by 16 Bits FIFO



10,096 Words by 8 Bits FIFO



Remark Fix D_{IN8} - D_{IN15} to "L" or "H" level in the 10,096 words by 8 bits mode.

(2) Write Cycle

When the $\overline{WE}$ input is enabled ("L" level), a write cycle is executed in synchronization with the WCK clock input. The data inputs are strobed by the rising edge of the clock at the end of a cycle so that read data after a one-line (5,048 bits or 10,096 bits) delay and write data can be processed with the same clock.

When creating a variable length delay line by controlling $\overline{WE}$ or $\overline{RSTW}$, delay bits are as follows.

Part Number	Cycle Time	Delay Bits
μPD485506-25	25 ns	21 to 5,048 bits/21 to 10,096 bits
μPD485506-35	35 ns	15 to 5,048 bits/15 to 10,096 bits

Unless inhibited by $\overline{WE}$, the internal write address will automatically wrap around from 5,047 to 0 and begin incrementing again.

(3) Read Cycle

When the $\overline{RE}$ input is enabled ("L" level), a read cycle is executed in synchronization with the RCK clock input. When the $\overline{OE}$ input is also enabled ("L" level) at that time, data is output at t_{AC}.

When creating a variable length delay line by controlling $\overline{RE}$ or $\overline{RSTR}$, delay bits are as follows.

Part Number	Cycle Time	Delay Bits
μPD485506-25	25 ns	21 to 5,048 bits/21 to 10,096 bits
μPD485506-35	35 ns	15 to 5,048 bits/15 to 10,096 bits

When read and write cycles contend for the same line for a time axis conversion, etc., the old data (previous line) may be output for the last 21 bits in the case of 25 ns read cycle time, and the last 15 bits in the case of 35 ns read cycle time.

Unless inhibited by $\overline{RE}$, the internal read address will automatically wrap around from 5,047 to 0 and begin incrementing again.

(4) Write Reset Cycle/Read Reset Cycle

After power up, the μPD485506 requires the initialization of internal circuits because the read and write address pointers are not defined at that time.

It is necessary to satisfy setup requirements and hold times as measured from the rising edge of WCK and RCK, and then input the $\overline{RSTW}$ and $\overline{RSTR}$ signals to initialize the circuit.

Caution Write and read reset cycles can be executed asynchronously. However, 1/2 cycle and 500 ns is required after a write cycle to read the data written in a cycle.

Remark Write and read reset cycles can be executed at any time and do not depend on the state of $\overline{RE}$, $\overline{WE}$ or $\overline{OE}$.

3. Electrical Specifications

- All voltages are referenced to GND.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−0.5[Note] to V_{CC} + 0.5	V
Supply voltage	V_{CC}		−0.5 to +7.0	V
Output current	I_O		20	mA
Power dissipation	P_D		1	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Note −3.0 V MIN. (Pulse width = 10 ns)

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.5	5.0	5.5	V
High level input voltage	V_{IH}		2.4		V_{CC} + 0.5	V
Low level input voltage	V_{IL}		−0.3[Note]		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Note −3.0 V MIN. (Pulse width = 10 ns)

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Operating current	I_{CC}				140	mA
Input leakage current	I_I	V_I = 0 to V_{CC}, Other Input 0 V	−10		+10	μA
Output leakage current	I_O	V_O = 0 to V_{CC}, D_{OUT}: High Impedance	−10		+10	μA
High level output voltage	V_{OH}	I_{OH} = −1 mA	2.4			V
Low level output voltage	V_{OL}	I_{OL} = 2 mA			0.4	V

Capacitance (T_A = +25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I				10	pF
Output capacitance	C_O				10	pF

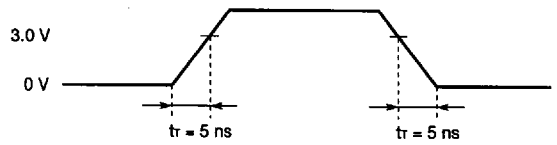
AC Characteristics (Recommended Operating Conditions unless otherwise noted)[Notes 1, 2, 3]

Parameter	Symbol	μPD485506-25		μPD485506-35		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Write clock cycle time	t_{WCK}	25		35		ns	
Write clock pulse width	t_{WCW}	11		12		ns	
Write clock precharge time	t_{WCP}	11		12		ns	
Read clock cycle time	t_{RCK}	25		35		ns	
Read clock pulse width	t_{RCW}	11		12		ns	
Read clock precharge time	t_{RCP}	11		12		ns	
Access time	t_{AC}		18		25	ns	
Output hold time	t_{OH}	5		5		ns	
Output low-impedance time	t_{LZ}	5	18	5	25	ns	4
Output high-impedance time	t_{HZ}	5	18	5	25	ns	4
Input data setup time	t_{DS}	7		10		ns	
Input data hold time	t_{DH}	3		3		ns	
MD Set setup time	t_{MS}	20		20		ns	
MD Set hold time	t_{MH}	10		10		ns	
MD Set time	t_{MD}	0		0		ns	5
Output low-impedance time (Mode change)	t_{LZM}	5	18	5	25	ns	4
Output high-impedance time (Mode change)	t_{HZM}	5	18	5	25	ns	4
$\overline{RSTW}/\overline{RSTR}$ Setup time	t_{RS}	7		10		ns	6
$\overline{RSTW}/\overline{RSTR}$ Hold time	t_{RH}	3		3		ns	6
$\overline{RSTW}/\overline{RSTR}$ Deselected time (1)	t_{RN1}	3		3		ns	7
$\overline{RSTW}/\overline{RSTR}$ Deselected time (2)	t_{RN2}	7		10		ns	7
$\overline{WE}$ Setup time	t_{WES}	7		10		ns	8
$\overline{WE}$ Hold time	t_{WEH}	3		3		ns	8
$\overline{WE}$ Deselected time (1)	t_{WEN1}	3		3		ns	9
$\overline{WE}$ Deselected time (2)	t_{WEN2}	7		10		ns	9
$\overline{RE}$ Setup time	t_{RES}	7		10		ns	10
$\overline{RE}$ Hold time	t_{REH}	3		3		ns	10
$\overline{RE}$ Deselected time (1)	t_{REN1}	3		3		ns	11
$\overline{RE}$ Deselected time (2)	t_{REN2}	7		10		ns	11
$\overline{OE}$ Setup time	t_{OES}	7		10		ns	10
$\overline{OE}$ Hold time	t_{OEH}	3		3		ns	10
$\overline{OE}$ Deselected time (1)	t_{OEN1}	3		3		ns	11
$\overline{OE}$ Deselected time (2)	t_{OEN2}	7		10		ns	11
$\overline{WE}$ Disable time	t_{WEW}	0		0		ms	
$\overline{RE}$ Disable time	t_{REW}	0		0		ms	
$\overline{OE}$ Disable time	t_{OEW}	0		0		ms	
Write reset time	t_{RSTW}	0		0		ms	
Read reset time	t_{RSTR}	0		0		ms	
Transition time	t_T	3	35	3	35	ns	

Notes 1. AC measurements assume t_T = 5 ns.

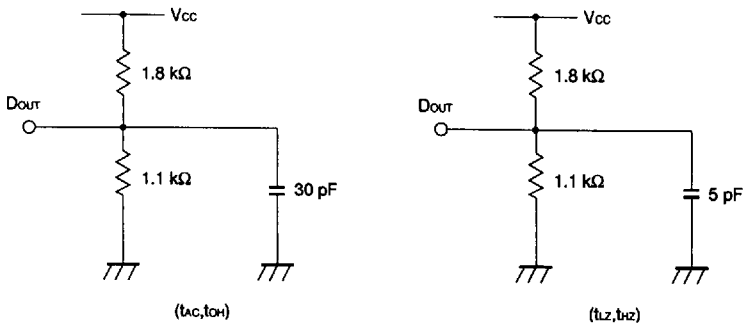
2. AC Characteristics test condition

Input Timing Specification



Output Timing Specification

Output Loads for Timing



3. Input timing reference levels = 1.5 V.

4. t_{LZ}, t_{HZ}, t_{LZM} and t_{HZM} are measured at ±200 mV from the steady state voltage. Under any conditions, $t_{LZ} \geq t_{HZ}$ and $t_{LZM} \geq t_{HZM}$.

5. Mode set signal (MD) must be input synchronously with write reset signal (t_{RSTW} period) or read reset signal (t_{RSTR} period). Under this condition, $t_{RSTW} = t_{MD}$ ($t_{RSTR} = t_{MD}$).

6. If either t_{RS} or t_{RH} is less than the specified value, reset operations are not guaranteed.

7. If either t_{RN1} or t_{RN2} is less than the specified value, reset operations may extend to cycles preceding or following the period of reset operations.

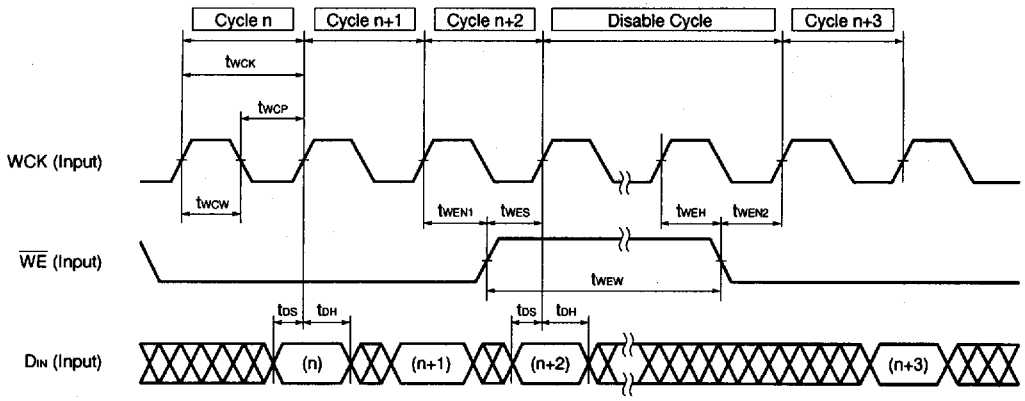
8. If either t_{WES} or t_{WEH} is less than the specified value, write disable operations are not guaranteed.

9. If either t_{WEN1} or t_{WEN2} is less than the specified value, internal write disable operations may extend to cycles preceding or following the period of write disable operations.

10. If either t_{RES} or t_{REH}, t_{OES} or t_{OEH} is less than the specified value, read disable operations are not guaranteed.

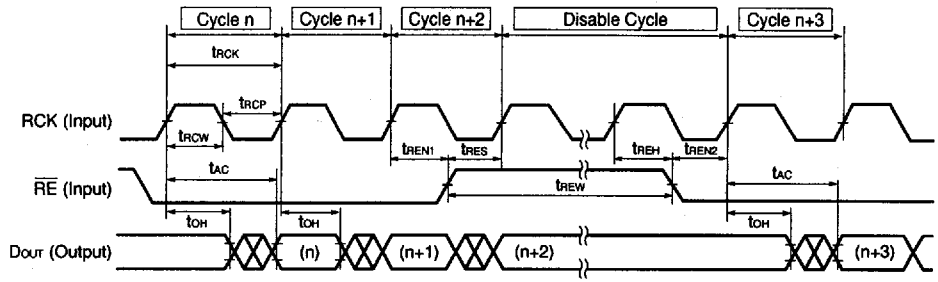
11. If either t_{REN1} or t_{REN2}, t_{OEN1} or t_{OEN2} is less than the specified value, internal read disable operations may extend to cycles preceding or following the period of read disable operations.

Write Cycle



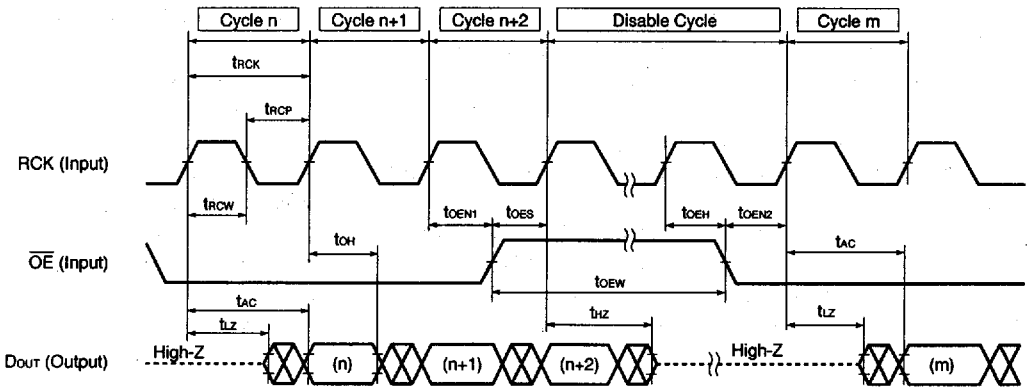
Remark $\overline{RSTW}$ = "H" level

Read Cycle ($\overline{RE}$ Control)



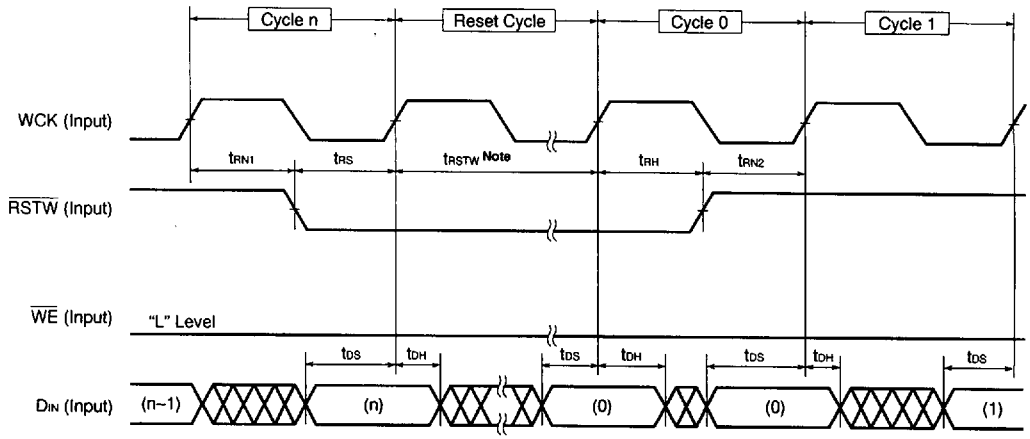
Remark $\overline{OE}$ = "L" level, $\overline{RSTR}$ = "H" level

Read Cycle ($\overline{OE}$ Control)



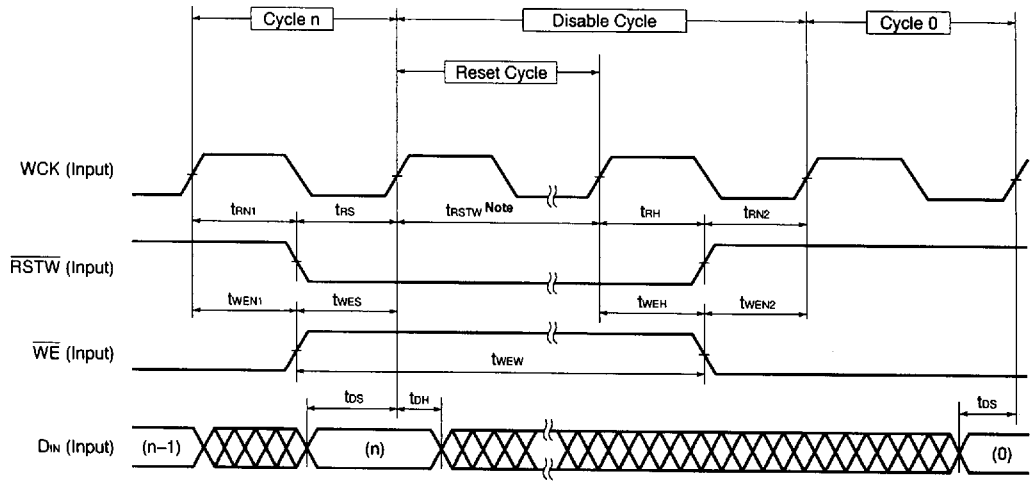
Remark $\overline{RE}$ = "L" level, $\overline{RSTR}$ = "H" level

Write Reset Cycle ($\overline{WE}$ Controlled 1) (Versions E, K and P)



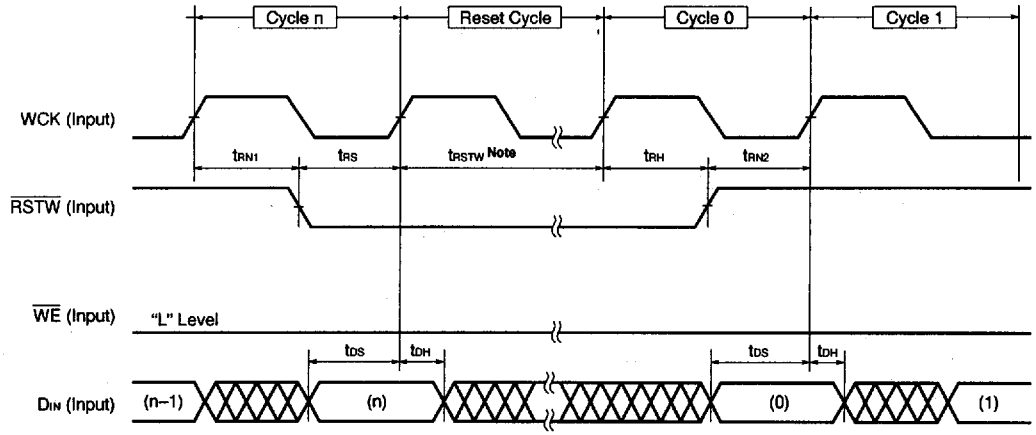
Note In write reset cycle, reset operation is executed even without a reset cycle (t_{RSTW}).
WCK can be input any number of times in a reset cycle.

Write Reset Cycle ($\overline{WE}$ Controlled 2) (Versions E, K, P and X)



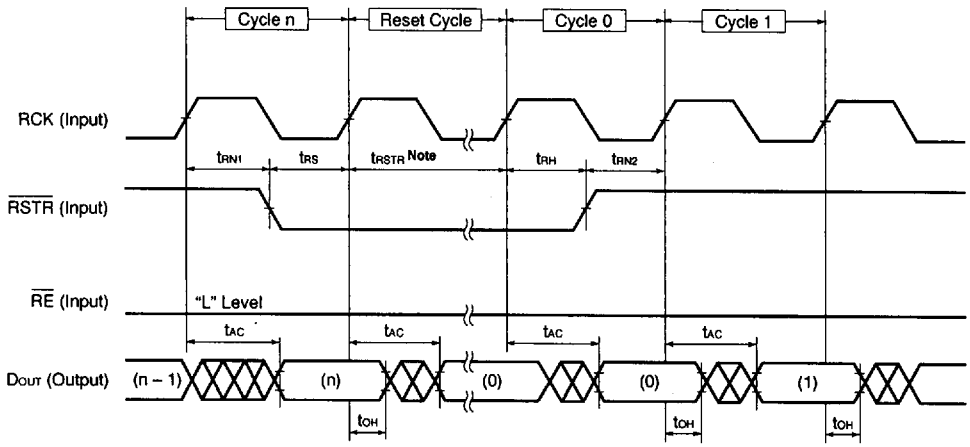
Note In write reset cycle, reset operation is executed even without a reset cycle (t_{RSTW}).
WCK can be input any number of times in a reset cycle.

Write Reset Cycle ($\overline{WE}$ Controlled 3) (Version X)



Note In write reset cycle, reset operation is executed even without a reset cycle (t_{RSTW}). WCK can be input any number of times in a reset cycle.

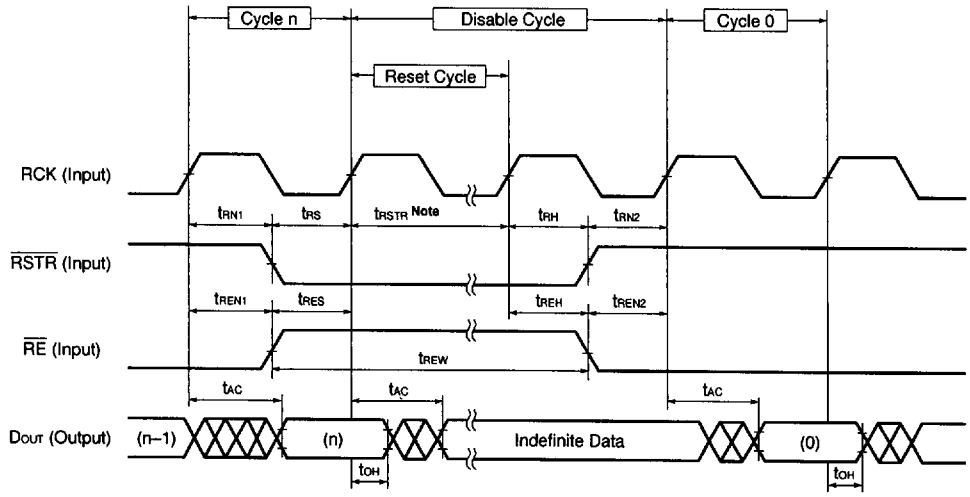
Read Reset Cycle ($\overline{RE}$ Controlled 1)



Note In read reset cycle, reset operation is executed even without a reset cycle (t_{RSTR}). RCK can be input any number of times in a reset cycle.

Remark $\overline{OE}$ = "L" level

Read Reset Cycle ($\overline{RE}$ Controlled 2)



Note In read reset cycle, reset operation is executed even without a reset cycle (t_{RSTR}). RCK can be input any number of times in a reset cycle.

Remark $\overline{OE}$ = "L" level

4. Application

- **1 H Delay Line**

  μPD485506 easily allows a 1 H (5,048 bits/10,096 bits) delay line (see Figure 1, 2).
  It is also possible to change the number of delay bits depending on the cycle time as follows.

Part Number	Cycle Time	Delay Bits
μPD485506-25	25 ns	21 to 5,048 bits/21 to 10,096 bits
μPD485506-35	35 ns	15 to 5,048 bits/15 to 10,096 bits

To change the number of delay bits, you can choose the one of the following methods.

Adjustments of the number of delay bits

(1) Reset the cycle proportionate to the delay length (Figure 3).
(2) Shift the input timing of write reset ($\overline{RSTW}$) and read reset signals ($\overline{RSTR}$) according to the delay length (Figure 4).
(3) Shift the address by disabling $\overline{WE}$ or $\overline{RE}$ for the period proportionate to the delay length (Figure 5).

Caution After power up, the μPD485506 requires the initialization of internal circuits because the read and write address pointers are not defined at that time.

Figure 1 1 H Delay Line Circuit

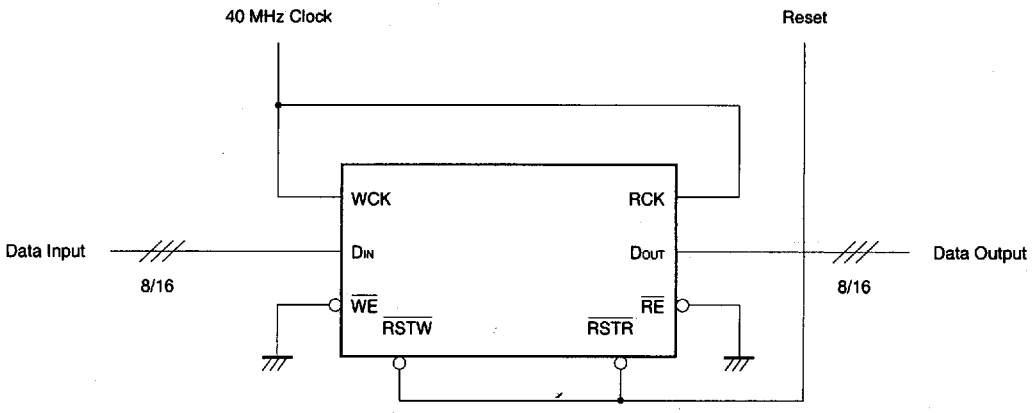
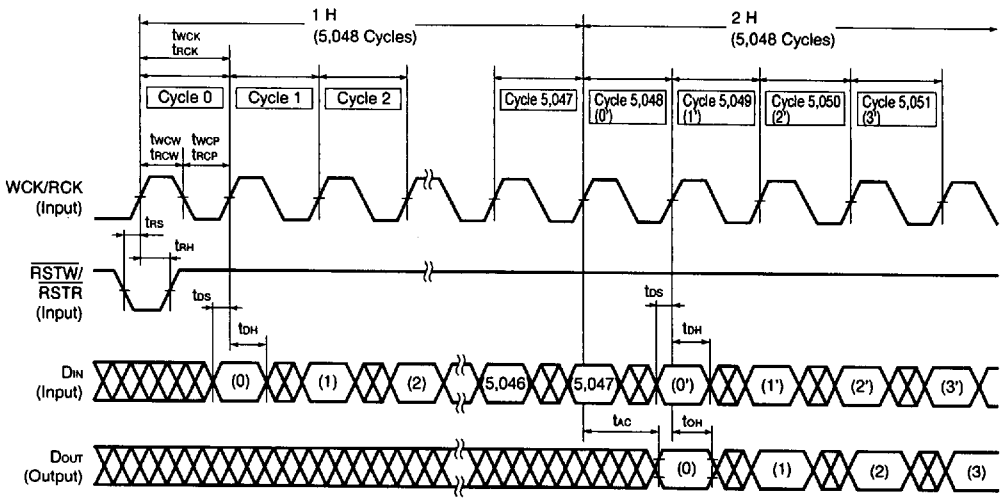
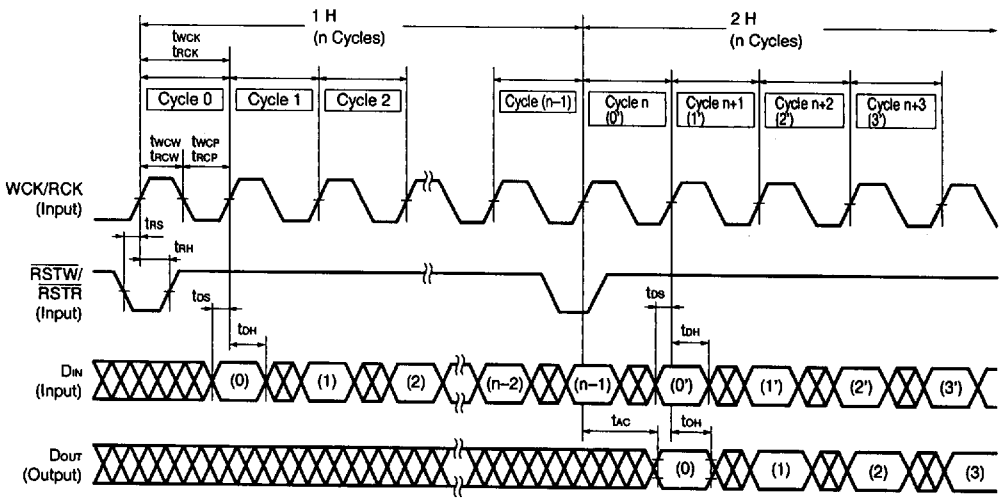


Figure 2 1 H Delay Line Timing



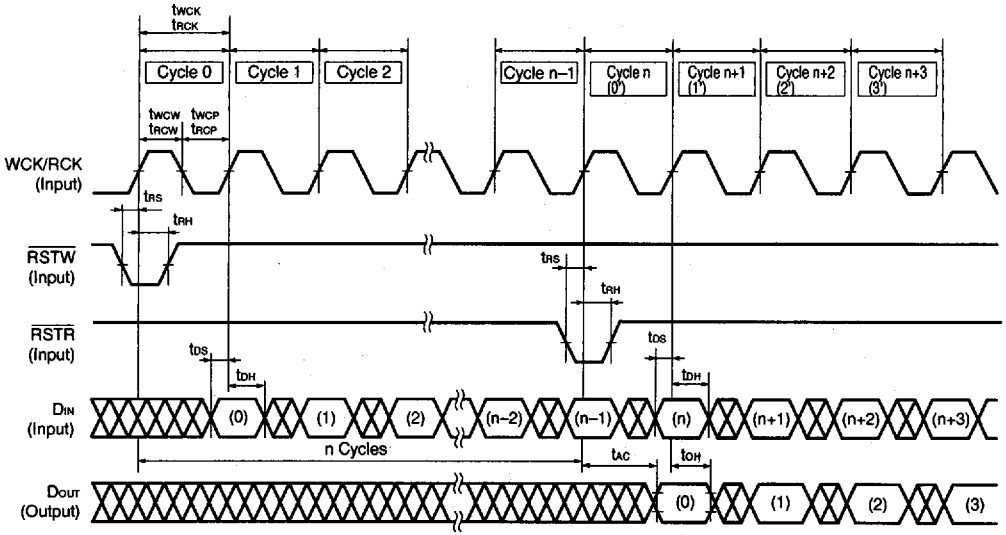
Remark $\overline{RE}$, $\overline{WE}$, $\overline{OE}$ = "L" level

Figure 3 n-Bit Delay Line Timing (1)



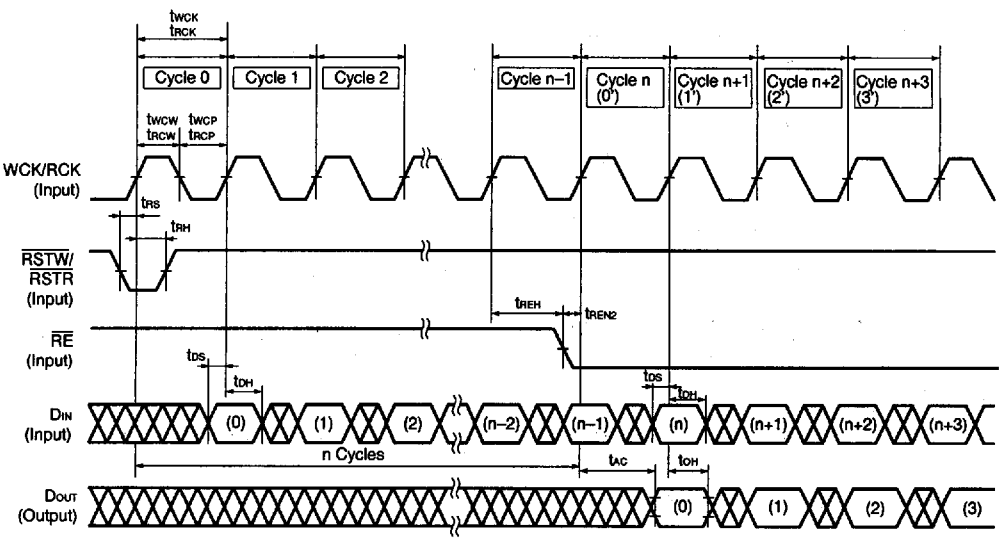
Remark $\overline{RE}$, $\overline{WE}$, $\overline{OE}$ = "L" level

Figure 4 n-Bit Delay Line Timing (2)



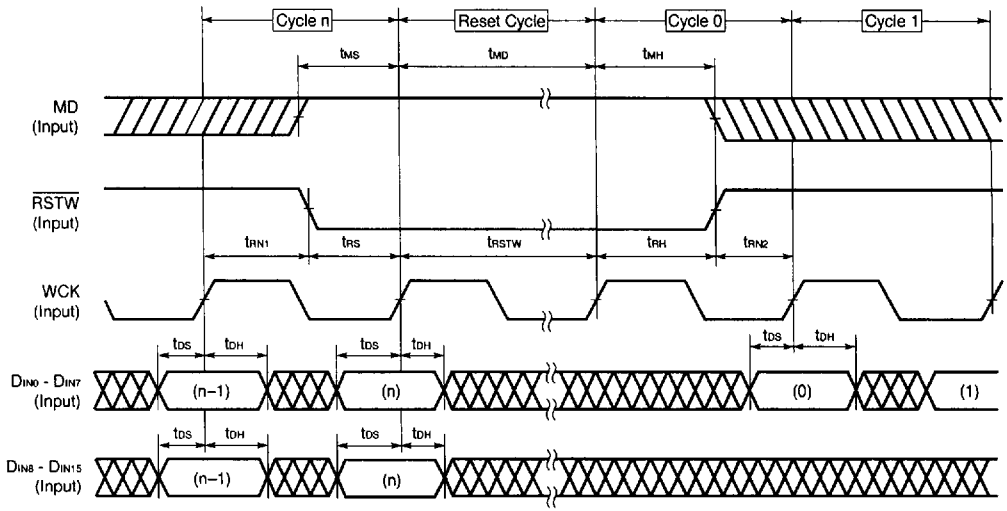
Remark $\overline{RE}$, $\overline{WE}$, $\overline{OE}$ = "L" level

Figure 5 n-Bit Delay Line Timing (3)



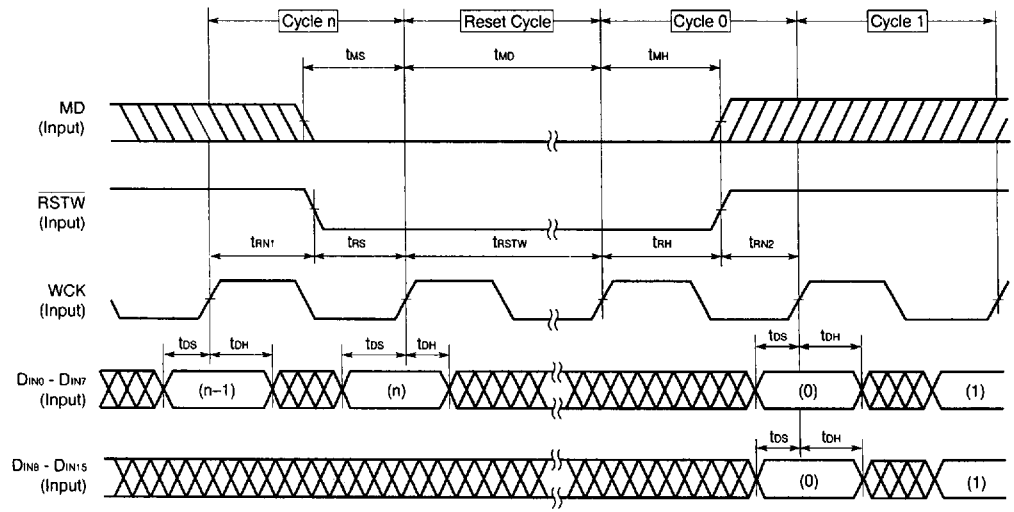
Remark $\overline{WE}$, $\overline{OE}$ = "L" level

Figure 6 Mode Set Cycle (Write) (1)



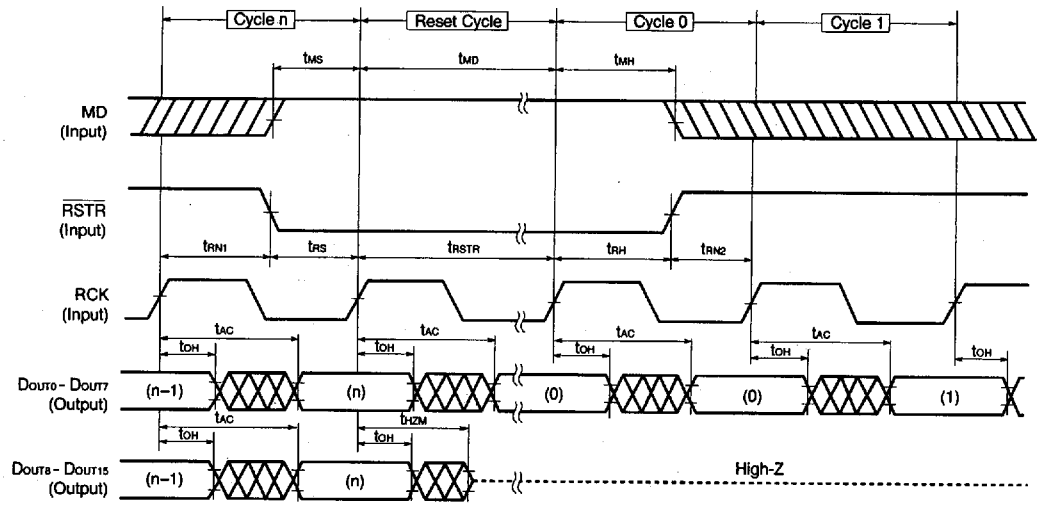
Remark $\overline{WE}$ = "L" level

Figure 7 Mode Set Cycle (Write) (2)



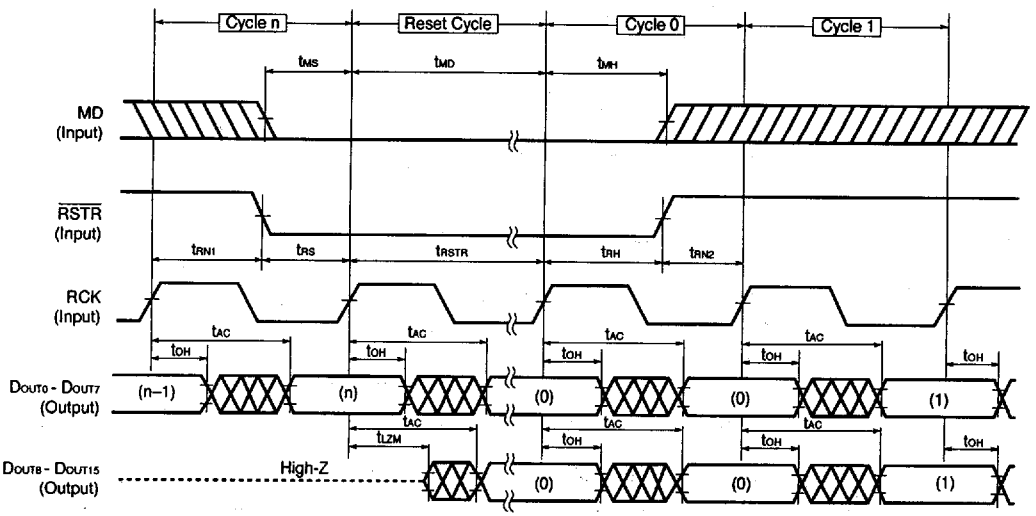
Remark $\overline{WE}$ = "L" level

Figure 8 Mode Set Cycle (Read) (1)



Remark $\overline{RE}$, $\overline{OE}$ = "L" level

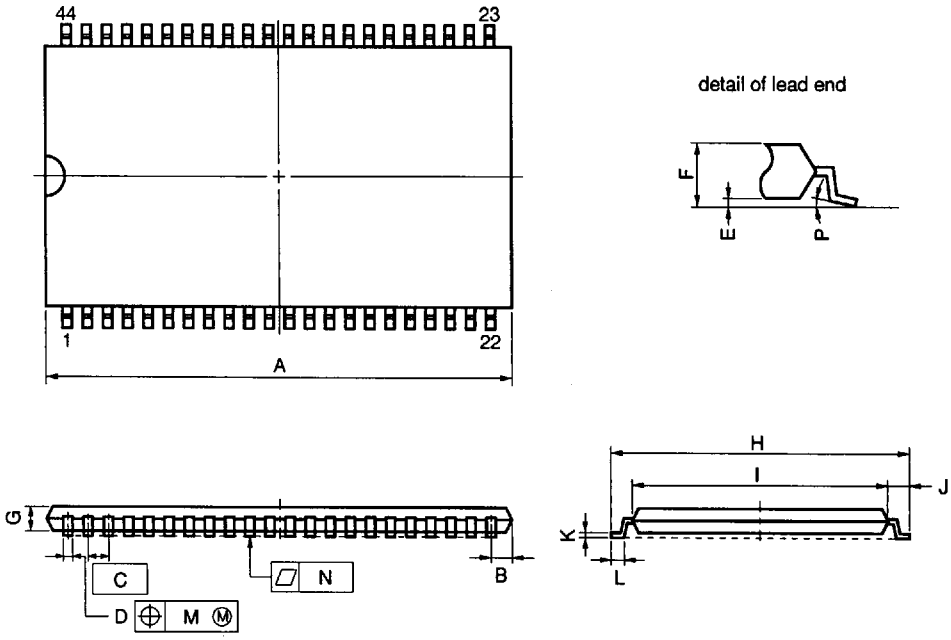
Figure 9 Mode Set Cycle (Read) (2)



Remark $\overline{RE}$, $\overline{OE}$ = "L" level.

5. Package Drawing

44 PIN PLASTIC TSOP(II) (400 mil)



NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	18.63 MAX.	0.734 MAX.
B	0.93 MAX.	0.037 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	$0.32^{+0.08}_{-0.07}$	0.013±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	$0.145^{+0.025}_{-0.015}$	0.006±0.001
L	0.5±0.1	$0.020^{+0.004}_{-0.005}$
M	0.13	0.005
N	0.10	0.004
P	$3°^{+7°}_{-3°}$	$3°^{+7°}_{-3°}$

S44G5-80-7JF5

6. Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μPD485506.

Type of Surface Mount Device

μPD485506G5: 44-pin plastic TSOP (II) (400 mil)

7. Example of Stamping

Letter E in the fifth character position in a lot number signifies version E, letter K, version K, letter P, version P, and letter X, version X.