MOS INTEGRATED CIRCUIT
μPD6332C

LATCH AND DRIVER FOR LCD
CMOS LSI

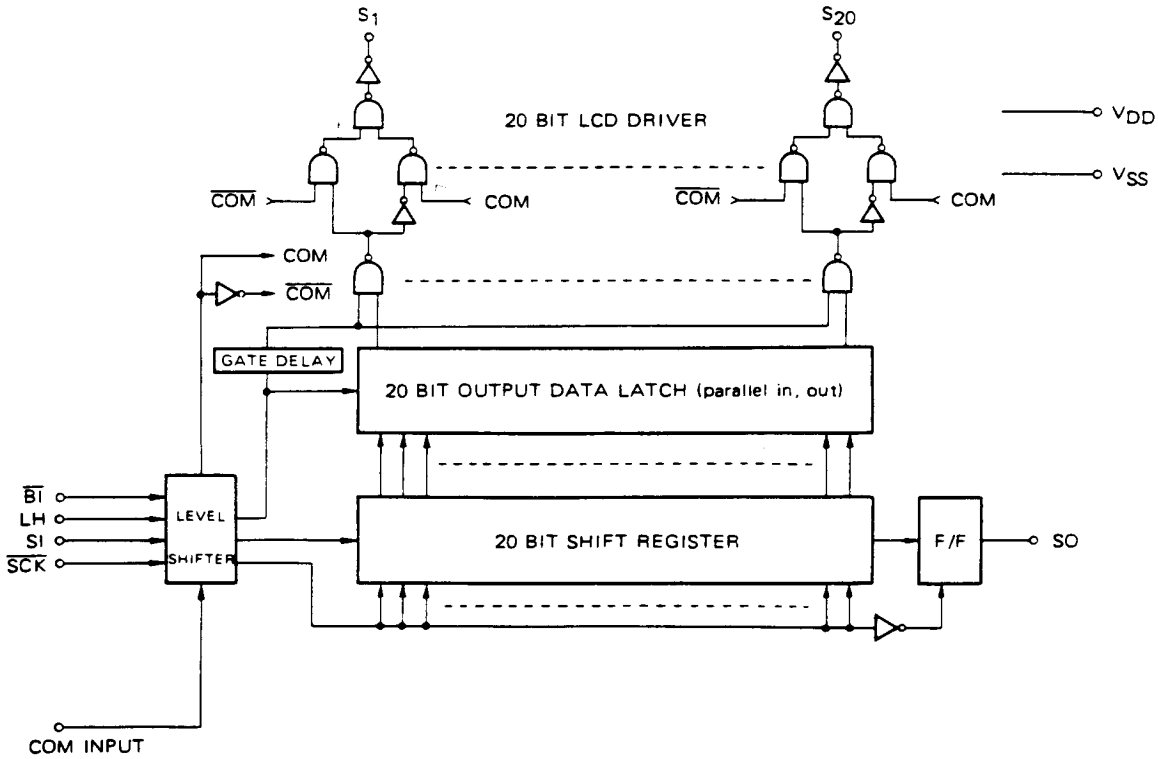
DESCRIPTION

The μPD6332C is a latch and driver CMOS IC for LCD (Liquid Crystal Display). For multiplex wiring, the μPD6332C is supplied with the serial interface circuit, 20 bit shift register, 20 bit data latch and 20 bit drivers. The serial data transfer from the data source to the μPD6332C is accomplished with 3 signals.

FEATURES

- Serial Input 20 bit Shift Register Incorporated.
- Data Control by Clock transfer (external) and Latch.
- Capable of Flashing Display by Blanking Terminal.
- Capable of Color LCD Drive Owing to High Circuit Voltage (18 V MAX.).
- Input Level Shifter Enables Direct Connection with Microcomputer.
- Wide Supply Voltage V_{DD} = 4 to 12 V (18 V MAX.)
- 28 Pin Plastic Molded DIP (Dual In-line Package).
- C-MOS

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C ±2 °C)

Supply Voltage at V_{DD} terminal	V_{DD}	18	V
Input Voltage	V_{IN}	−0.3 to V_{DD}	V
SO Output Current	I_{SO}	±5	mA
Operating Temperature Range	$T_{opt.}$	−40 to +85	°C
Storage Temperature Range	$T_{stg.}$	−55 to +125	°C

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC		SYMBOL	MIN.	TYP.	MAX.	UNIT
Operating Temperature Range		$T_{opt.}$	−40		+85	°C
Operating Supply Voltage		V_{DD}	4	8	12	V
Input Voltage High		V_{IH}	3.0		V_{DD}	V
Input Voltage Low		V_{IL}	0		1.0	V
SO Output Current		I_{SO}			1.0	mA
$\overline{SCK}$ Frequency		$f_{\overline{SCK}}$		200	500	kHz
$\overline{SCK}$ Cycle Time	(*1)	t_{KCY}	2.0			μs
$\overline{SCK}$ High Level Pulse Width	(*1)	t_{KHW}	0.9			μs
$\overline{SCK}$ Low Level Pulse Width	(*1)	t_{KLW}	0.9			μs
SI Setup Time to $\overline{SCK}$ ↑	(*1)	t_{SIK}	0.4			μs
SI Hold Time	(*1)	t_{KSI}	0.4			μs
$\overline{SCK}$ → LH Valid Time	(*2)	t_{CLL}	10			μs
LH Low Level Pulse Width	(*2)	t_{LLW}	10			μs
$\overline{BI}$ Low Level Pulse Width	(*3)	t_{BLW}	0.4			μs

Notes: (*1) ; See Fig. 1

(*2) ; See Fig. 2

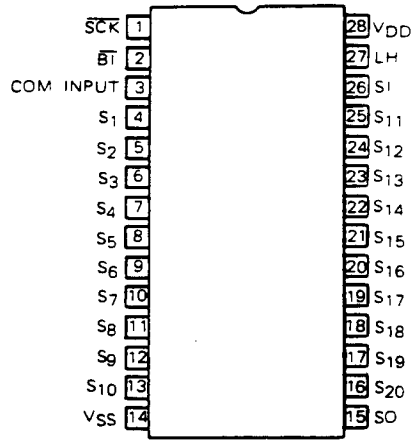
(*3) ; See Fig. 3

ELECTRICAL CHARACTERISTICS (Recommended operating conditions)

CHARACTERISTIC	SYMBOL	MAX.	TYP.	MIN.	UNIT	CONDITION
Input Leakage Current	I_{IL}			±10	μA	$V_{IH}=V_{SS}$ or $V_{IN}=V_{DD}$
SO Output Voltage High	V_{SOH}	$V_{DD}-1$		V_{DD}	V	$I_{SOH}=-1$ mA
SO Output Voltage Low	V_{SOL}	V_{SS}		0.4	V	$I_{SOL}=1$ mA
Output Voltage High	V_{OH}	$V_{DD}-1$			V	$I_{OH}=-1$ mA
Output Voltage Low	V_{OL}			1.0	V	$I_{OL}=1$ mA
Supply Current at V_{DD} Terminal	I_{DD}			1.0	mA	
Supply Voltage at V_{DD} Terminal to Keep DATA	$V_{DD}(H)$	3.0			V	
Input Capacitance	C_{IN}			15	pF	f=1 MHz
$\overline{SCK}\downarrow\rightarrow$ SO Valid Time (*4)	t_{KSO}			0.8	μs	
$\overline{BI}\rightarrow$Sn Valid Time (*3)	t_{BKQ}			1.8	μs	

Note: (*4) ; See Fig. 4

PIN CONNECTION (Top View)



TIMING CHART

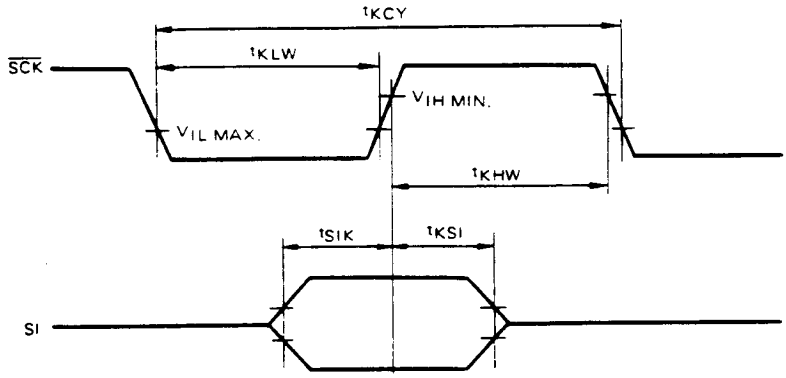


Fig. 1

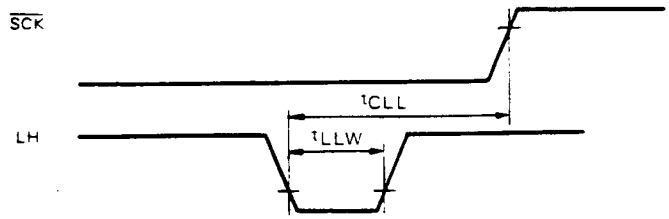


Fig. 2

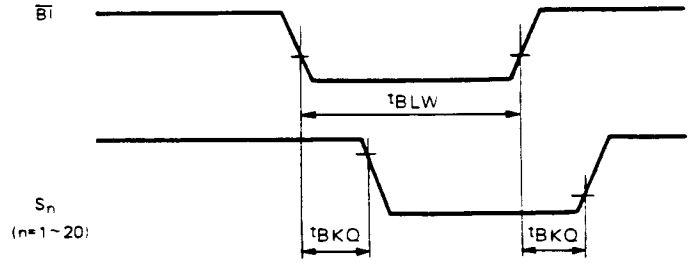


Fig. 3

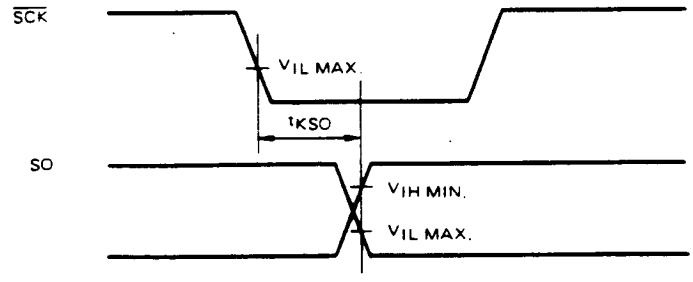
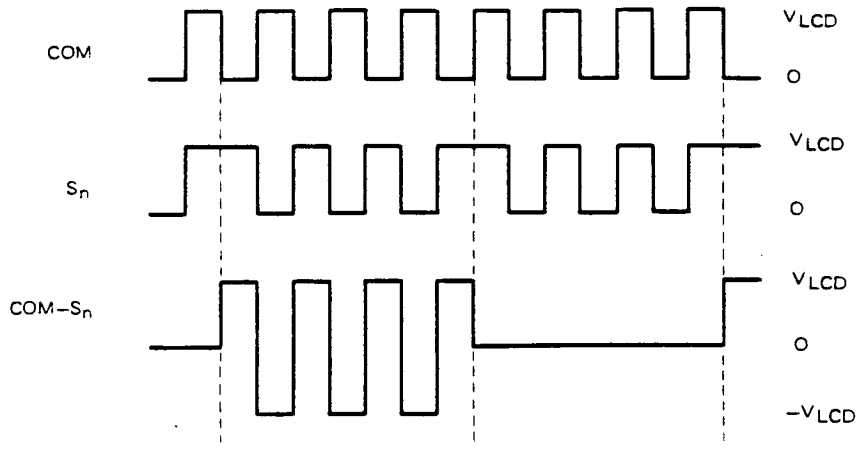


Fig. 4

TIMING CHART

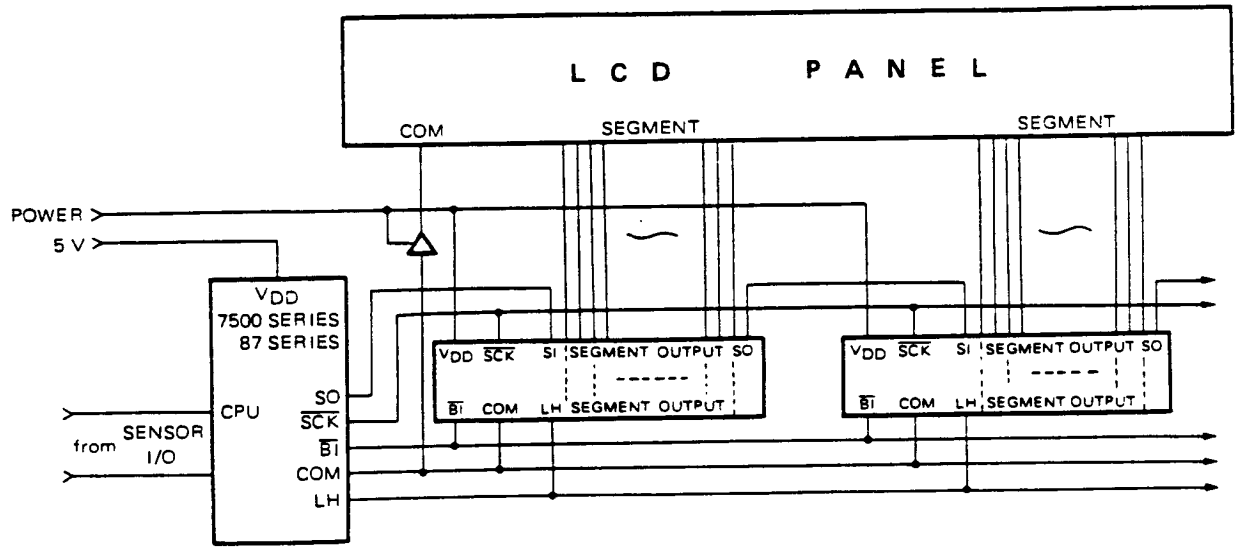


* V_{LCD}: LCD BIAS VOLTAGE

FUNCTION

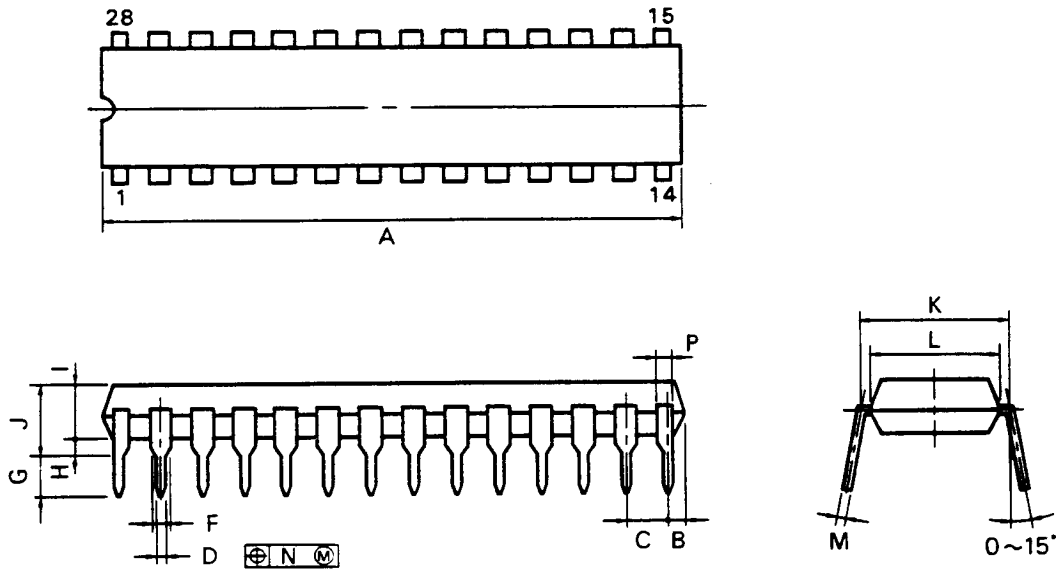
PIN NUMBER	SYMBOL	FUNCTION	INPUT/OUTPUT	EXPLANATION
1	$\overline{SCK}$	Serial Clock Input	INPUT	The SI data are read and stored in the 20 bit shift register at the rising edge of $\overline{SCK}$. DATA output from SO at the dropping edge of $\overline{SCK}$.
2	$\overline{BI}$	Blanking Input	INPUT	When "H" level signal is supplied to the $\overline{BI}$, S_1 to S_{20} are active. Flashing function is possible by external control.
3	COM INPUT	COM Input	INPUT	Input Common signal.
4 5 6 7 8 9 10 11 12 13	S_1 S_2 S_3 S_4 S_5 S_6 S_7 S_8 S_9 S_{10}	Segment and Driver for LCD	OUTPUT	These 10 Outputs are the Outputs of 10 bit output data latch, which can drive LCD directly.
14	V_{SS}	GND		Connection to GND.
15	SO	Serial data Output	OUTPUT	Serial data output at the dropping edge of $\overline{SCK}$. In case of "n" pieces of μPD6332C are serial connected, so it is possible to connect one to next SI.
16 17 18 19 20 21 22 23 24 25	S_{20} S_{19} S_{18} S_{17} S_{16} S_{15} S_{14} S_{13} S_{12} S_{11}	Segment and Driver for LCD	OUTPUT	These 10 Outputs are the Outputs of 10 bit output data latch, which can drive LCD directly.
26	SI	Serial data Input	INPUT	Serial Data Input. The SI data are read and stored in the 20 bit shift register at the rising edge of $\overline{SCK}$.
27	LH	Latch and Hold Input	INPUT	When "L" level signal is supplied to the LH, the data of 20 bit shift register are normally transferred the 20 bit output data latch. At the time of the rising edge of LH; the data of 20 bit output data latch are hold. "H"; The data of 20 bit output data latch are protected.
28	V_{DD}	Supply Voltage at V_{DD} Terminal		4 to 12 V

APPLICATION CIRCUIT



In case of no output COM, 2 Pieces of CMOS 4000 series are necessary externally.

28PIN PLASTIC DIP (400 mil)



P28C-100-400

NOTES

1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	35.56 MAX.	1.400 MAX.
B	1.27 MAX.	0.050 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	$0.50^{+0.10}$	$0.020^{+0.004}_{-0.005}$
F	1.1 MIN.	0.043 MIN.
G	$3.5^{+0.3}$	$0.138^{+0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.72 MAX.	0.226 MAX.
K	10.16 (T.P.)	0.400 (T.P.)
L	8.6	0.339
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.25	0.01
P	0.9 MIN.	0.035 MIN.

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