NEC

MOS INTEGRATED CIRCUIT

μPD6454

12-LINE 24-DIGIT ON-SCREEN DISPLAY LSI FOR STATIONARY TYPE VCR CMOS LSI

The μPD6454 is an on-screen display CMOS LSI performing, in combination with a microcomputer, various displays such as program reservation screens (tape counters, etc.) for stationary type VCRs.

The characters on the display are formed by 12 (width) × 18 (height) dots.

Symbols (Chinese characters, etc.) and figures can be displayed by combining two or more characters. The μPD6454 is internally equipped with a synchronization separation circuit and AFC circuit which have been required as IC peripheral circuits, so that the mounting area on a printed wiring board can be saved.

The μPD6454 also incorporates a power-ON clear function and a video RAM batch clear command to reduce the load on the microcomputer. It is also equipped with synchronization detection output that detects the status of the video signal, so that the timing at which blue back is selected can be notified to the microcomputer.

FEATURES

- Video signal I/O: Composite video signal
- Number of display characters: 288 (12 lines × 24 digits)
- Kinds of characters: 256 (ROM). Can be changed by mask code option
- Character size: 1 dot/1H, 2H, 3H, 4H (field)
- Character color: White (single color)
- Background: One of the following per screen: None, Fringed, Square, or Solid
- Dot matrix: 12 (width) × 18 (height) dots, without space between adjacent characters
- Blinking: Blinking ON/OFF can be specified for each character. The blinking ratio is 1:1 and there are three choices for the blinking cycle set for each screen: 0.5 Hz, 1 Hz, or 2 Hz.
- Half-tone display: Background can be displayed in half tones by command.
- Character signal output: VCR with S-pin can also be used if an external mixing circuit is connected because a character signal and blinking signal output pins are provided.
- Video RAM data clear: Executed by video RAM clear command and clear function at power on
- Applicable video signal mode: NTSC/PAL
- Other incorporated circuits: Synchronization separation circuit and AFC circuit
- Interface with microcomputer: 8-bit serial input of variable word length
- Supply voltage: +5 V (single power source)

ORDERING INFORMATION

Part Number	Package	Quality Grade
μPD6454CS-001	24-pin plastic shrink DIP (300 mil)	Standard
μPD6454GT-101	24-pin plastic SOP (375 mil)	Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

The information in this document is subject to change without notice.

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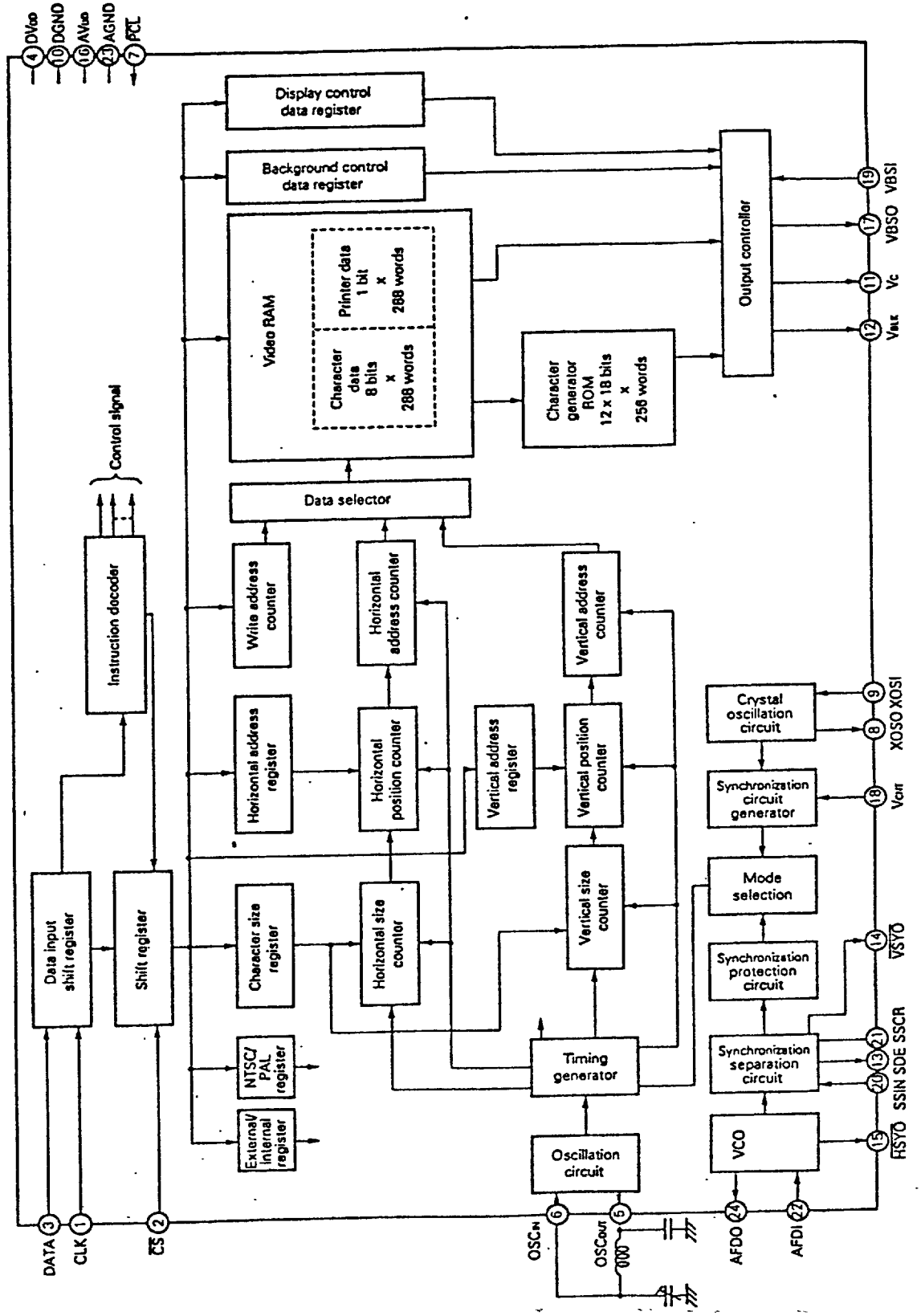
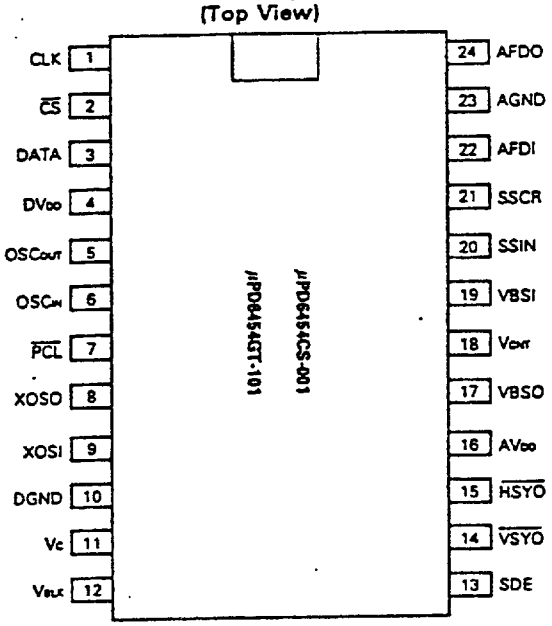
BLOCK DIAGRAM



PIN CONFIGURATION

(Top View)



Pin Functions

No.	Symbol	Name	Function
1	CLK	Clock input	Inputs clock for reading data. Data input to DATA pin is read at rising edge of clock.
2	$\overline{CS}$	Chip select input	Serial transfer can be accepted when this pin goes low.
3	DATA	Serial data input	Inputs control data. Reads data in synchronization with clock to be input to CLK pin.
4	DVDD	Power supply	Supplies power to digital circuits.
5,6	OSCOUT OSCIN	LC oscillation I/O	I/O pins of oscillator circuit for dot clock generation. Connect coil and capacitor for oscillation.
7	$\overline{PCL}$	Power-ON clear	Power-ON clear pin. Make this pin high at power on (Internal initialization is executed while PCL pin is low).
8,9	XOSO XOSI	Crystal oscillator I/O	Connect a crystal resonator for internal video signal generation.
10	DGND	Ground	Ground pin for digital circuits.
11	Vc	Character signal output	Active-high character signal output pin.
12	VBLK	Blanking signal output	Outputs blanking signal that cuts video signal. This active-high pin corresponds to output of Vc.
13	SDE	Synchronization detection output	Outputs results of synchronization detection.
14	$\overline{VSYO}$	Vertical sync. signal output	Outputs synchronization-separated composite sync. signal in the external video mode, and vertical sync. signal for internal video signal in the internal video signal mode.
15	$\overline{HSYO}$	Horizontal sync signal output	Outputs horizontal sync signal from AFC circuit.
16	AVDD	Power supply	Supplies power to analog circuits.
17	VBSO	Composite video signal output	Outputs composite video signal mixed with character signal.
18	VCNT	Video signal output level control	Controls output levels of composite video signal and luminance signal.
19	VBSI	Composite video signal input	Inputs composite video signal. Inputs signal with synchronization edge with negative synchronization and positive video.
20	SSIN	Synchronization separation input	Inputs composite video signal for synchronization separation.
21	SSCR	Synchronization separation time constant connection	Connects time constant (capacitor and resistor) for synchronization separation.
22	AFDI	Frequency error voltage input	Frequency error voltage input pin of VCO for AFC
23	AGND	Ground	Ground for analog circuits
24	AFDO	Frequency error voltage output	Frequency error voltage output pin of VCO for AFC

CONTENTS

1. μPD6454 COMMANDS

1.1 COMMAND FORMAT

The control command is in 8-bit serial input format of variable word length.

The μPD6454 commands are classified into three categories: 1-byte commands and 2-byte commands which respectively consists of 8 bits and 16 bits with an instruction and data combined, and 2-byte continuous commands that can be input in an abbreviated form. Input command data starting from the MSB.

1.2 COMMAND LIST

1-byte command

(MSB)

Function	D7	D6	D5	D4	D3	D2	D1	D0
Video RAM batch clear	0	0	0	0	0	0	0	0
Display control	0	0	0	1	D0	LC	BL1	BL0
Internal video signal color control	0	0	1	0	R	G	B	0
Background control	0	0	1	1	0	BS1	BS0	0
Half tone control	0	0	1	1	1	BHT	0	0
Internal/external mode control, crystal oscillation control	0	1	0	0	0	E/I	0	Xosc
Video signal mode control	0	1	0	0	1	0	0	N/P
Scanning line, crystal selection control	0	1	0	1	0	0	X_{fc}	INS
Synchronization detection control	0	1	0	1	1	SD	0	0

2-byte command

(MSB)

Function	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Display position control	1	0	0	0	0	0	V4	V3	V2	V1	V0	H4	H3	H2	H1	H0
Write address control	1	0	0	0	1	0	0	AR3	AR2	AR1	AR0	AC4	AC3	AC2	AC1	AC0
Output/background level control	1	0	0	1	0	0	0	VPD	VB3	VB2	VB1	VB0	VC3	VC2	VC1	VC0
Character size control	1	0	0	1	1	0	0	0	S1	S0	0	0	AR3	AR2	AR1	AR0
Test mode Note	1	0	1	1	0	0	0	0	T7	T6	T5	T4	T3	T2	T1	T0

Note Must not be used.

2-byte continuous command

Function	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Display character control	1	1	0	0	0	0	BL	0	C7	C6	C5	C4	C3	C2	C1	C0

1.3 POWER-ON CLEAR FUNCTION

Because the internal condition of the IC is unstable when power is turned on, perform initialization by clearing the IC by making the $\overline{PCL}$ pin high. The commands that are set through clearing are as follows:

- The test mode is cleared.
- All the character data of the video RAM (12 lines by 24 digits) is cleared (Display Off Data (FEH)) and no blinking data exists.
- The video RAM write address is (line 0, digit 0).
- The character size is set to x1 (minimum) on all lines.
- Display OFF, LC oscillation ON

The time required for power-On clear (Do not execute any command in this mode.) can be calculated using the following formula:

t (time for power-On clear) = t_{PCL} Note + video RAM clear time = 10 (μs) + 10 (μs) + 12/f_{OSC} (MHz) x 288

where, f_{OSC} (MHz): LC oscillation frequency

Note Refer to the power-On clear specifications.

2. COMMANDS DETAILS

2.1 VIDEO RAM BATCH CLEAR COMMAND

The video RAM can be cleared by one command.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0

The following parameters are set by the video RAM batch clear command:

- All character data of the video RAM is cleared (Display OFF Data (FEH), and no blinking data exists.
- The video RAM write address is (line 0, digit 0).
- The character size is x1 (minimum) on all the lines.
- Display OFF, LC oscillation ON

The time required for clearing the video RAM (Do not execute any command in this mode.) can be calculated using the following formula:

$$\text{Video RAM clear time} = 10\ (\mu s) + 12/f_{osc}\ (\text{MHz}) \times 288$$

2.2 DISPLAY CONTROL COMMAND

Controls display output, LC oscillation, and characters blinking.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	D0	LC	BL1	BL0

Blinking control bit		
BL1	BL0	Function
0	0	Blinking OFF
0	1	Blinking freq.:about 2 Hz
1	0	Blinking freq.:about 1 Hz
1	1	Blinking freq.:about 0.5 Hz

LC oscillation control bit	
LC	Function
0	LC Oscillation OFF
1	LC Oscillation ON

Display ON/OFF control bit	
D0	Function
0	Display OFF
1	Display ON

- Blinking control

  The character specified to blink by the display character control command blinks. The blinking ratio is 1:1 and one of three types of blinking frequencies can be selected for a screen.
  The blinking can be specified for each character with the Display Character Control Command.

- LC oscillation control

  The oscillation circuit can be turned ON/OFF by the oscillation control bit. When characters are not displayed, oscillation can be stopped to reduce power consumption.
  Data cannot be written to the video RAM when oscillation is stopped. To write to the video RAM, be sure to turn oscillation ON.

Remark When display is ON, oscillation synchronizes with $\overline{H_{sync}}$ signal and oscillation continues while $\overline{H_{sync}}$ is low. When display is OFF, oscillation continues regardless of the $\overline{H_{sync}}$ condition.

- Display ON/OFF control

  Display output can be turned ON/OFF in synchronization with the falling edge of $\overline{H_{sync}}$.

2.3 INTERNAL VIDEO SIGNAL COLOR CONTROL COMMAND

The color of the internal video signal can be set. The internal video signal is the video signal generated inside the μPD6454 (e.g., blue back). When a video signal is not being input from an external source to the μPD6454 and characters cannot be displayed, select the internal video signal to display characters.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	R	G	B	0

Internal video signal color control bit			
R	G	B	Function
0	0	0	Black
0	0	1	Blue
0	1	0	Green
0	1	1	Cyan
1	0	0	Red
1	0	1	Magenta
1	1	0	Yellow
1	1	1	White

- Internal video signal color control
  Eight colors can be selected for the internal video signal (when the crystal oscillation frequency is 4 f_{sc}). When the crystal oscillation frequency is 2 f_{sc} (supported only in NTSC mode), green and magenta cannot be selected. Their selection may result in a malfunction.

Remark In the NTSC mode, the crystal oscillation frequency can be set to 4 f_{sc} (14.318180 MHz) or 2 f_{sc} (7.159090 MHz). In the PAL mode, use a crystal resonator of 4 fsc (17.734476 MHz).

2.4 BACKGROUND CONTROL COMMAND

This command sets the background condition and black fringe of characters displayed in the external video signal mode. Available background color in this mode is black.

In the internal video signal mode, specify a background type other than the Solid.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	0	BS1	BS0	0

Background control bit		
BS1	BS0	Function
0	0	None
0	1	Fringed
1	0	Square
1	1	Solid

- Background control
  Either of None, Fringed, Square, or Solid can be selected for a screen. The color of background and fringe is black.

None: A character is output as is.

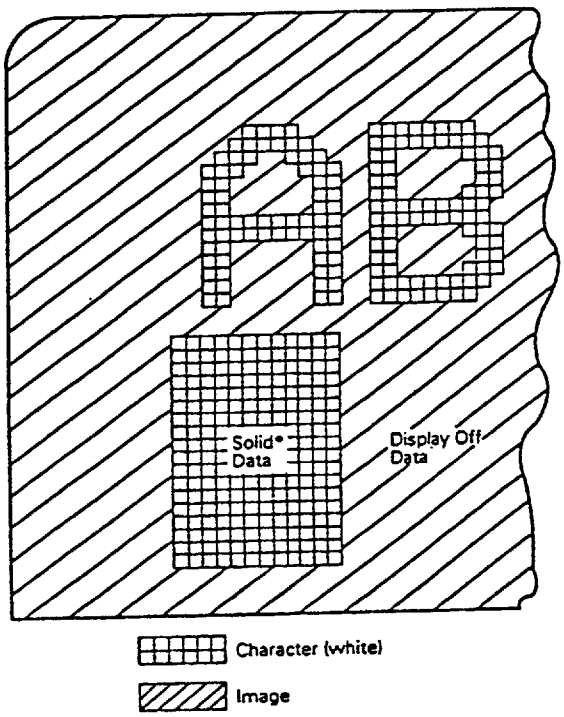
Fringed: When the left and right edges or top and bottom edges of the dot matrix are not used, characters are fringed in left, right, top, and diagonal sides. When the right- or left-edge dots of the dot matrix forming a character are used, the adjacent character display area is fringed.
Fringe is not displayed, however, on the top and bottom of a character if the top- or bottom-edge dots are used.
Even when the character size is changed, fringe size is fixed to 1 dot of the minimum character size.

Square: A character is backgrounded in black to the extent of one character display area and more 1 bit of the minimum character size than the area in both sides.

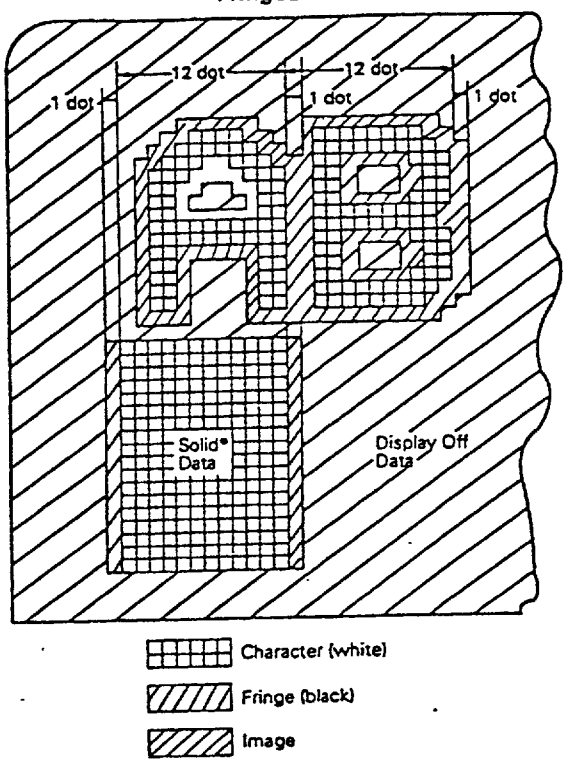
Solid: The black background is displayed on the entire screen.

Display format of each background mode

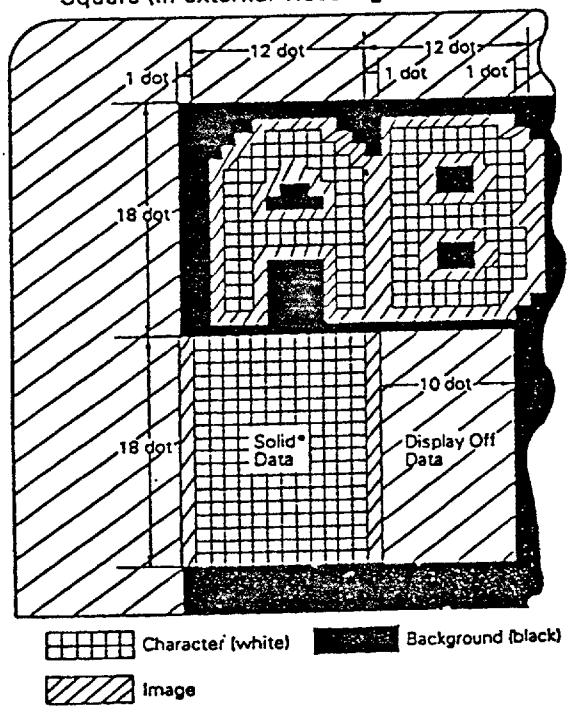
None



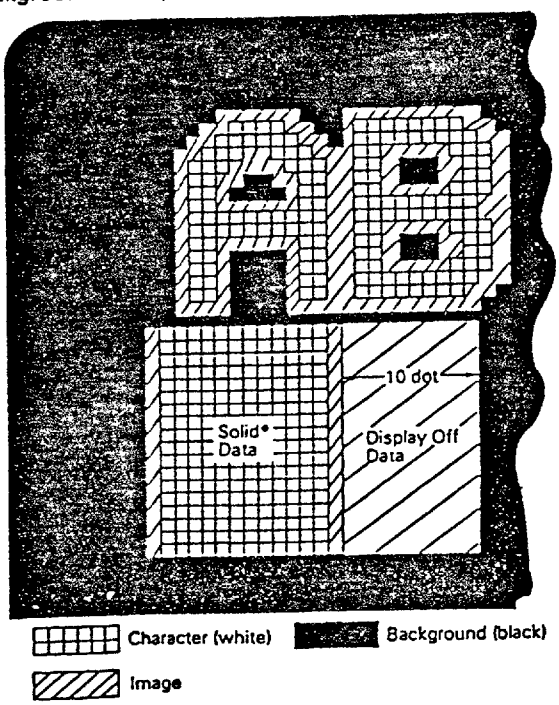
Fringed



Square (in external video signal mode only)



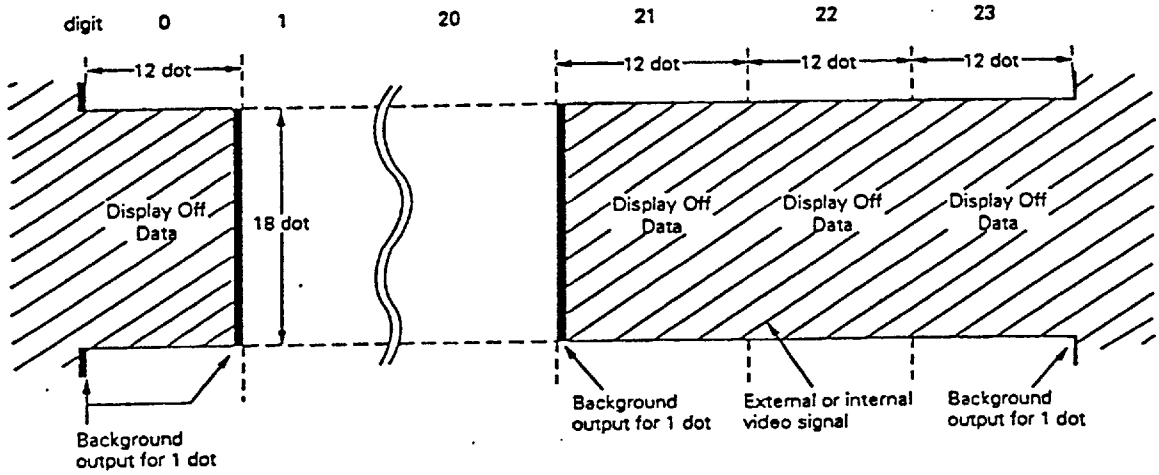
Background solid (in external video signal mode only)



Note Solid Data means 18H of NEC standard character.

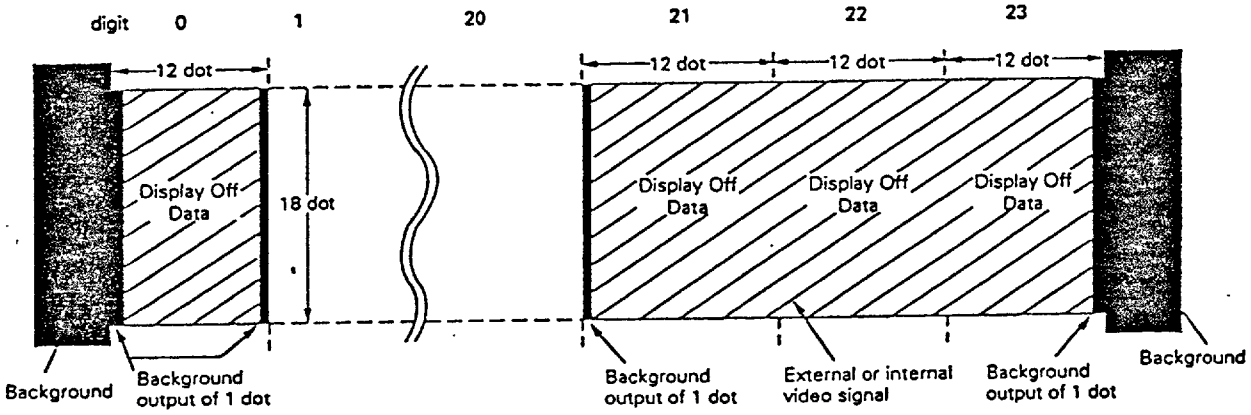
Example of Display when Display Off Data is Used

- Square



When Display Off Data is used, one bit of Display Off Data fronting on a character in both sides are displayed as background.

- Solid



When Display Off Data is used, one bit of Display Off Data fronting on a character in both sides are displayed as background.

Remark Even when the character size is changed, "background output of 1 dot" is always 1 dot of the minimum character size.

2.5 HALF TONE CONTROL COMMAND

With this command, the background in the external video signal mode is displayed in half tone (the image behind seen vague). The character does not become vague.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	BHT	0	0

Half tone control bit	
BS1	Function
0	Half tone OFF (background color: black)
1	Half tone ON

- Half tone control

When this command is turned ON, the section specified as background by the background control command is displayed in half tones. The half tone control command is valid only in the external video signal mode.

2.6 INTERNAL/EXTERNAL MODE CONTROL AND CRYSTAL OSCILLATION CONTROL COMMANDS

These commands select a video signal mode in which a character signal is superimposed (internal mode/external mode) and turns ON/OFF crystal oscillation.

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	E/I	0	Xosc

Crystal oscillation control bit	
Xosc	Function
0	Oscillation OFF
1	Oscillation ON

Internal/external mode control bit	
E/I	Function
0	External video signal mode
1	Internal video signal mode

- Crystal oscillation control

This command controls oscillation of the crystal generating the internal video signal. When the oscillation ON is selected, and the video signal mode is changed from the external to the internal mode without disturbing the screen.

- Internal/external mode selection

Internal video signal mode: Characters are superimposed on the video signal (e.g., blue back) internally created by the μPD6454 for display.

External video mode: Characters are superimposed on a video signal input from an external source to the μPD6454 for display.

If no character is superimposed, turn OFF display with the display ON/OFF control bit of the display control command.

2.7 VIDEO SIGNAL MODE CONTROL COMMAND

The μPD6454 allows reception of video signals in the NTSC or PAL mode as internal video signals by selecting a control bit.

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	0	0	N/P

Video signal mode control bit	
N/P	Function
0	NTSC
1	PAL

- Video signal mode control

An internal video signal in the NTSC or PAL mode can be generated.

The internal video signal is generated by an external crystal.

The frequency of the crystal must be 4 f_{sc} for each mode of video signal (i.e., NTSC: 14.31818 MHz/PAL: 17.734476 MHz). In the NTSC mode, 2 f_{sc} can also be used (note, however, that eight colors can be selected at 4 f_{sc} and six colors at 2 f_{sc}. NTSC: 2 f_{sc} (7.15909 MHz)).

2.8 SCANNING MODE AND CRYSTAL SELECTION CONTROL COMMANDS

The μPD6454 allows selection of a scanning mode (non-interlace/interlace) in the internal video signal mode, and of a crystal for internal video signal generation in the NTSC mode (only 4 f_{sc} in the PAL mode).

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	Xfc	INS

Scanning mode control bit	
INS	Function
0	Non-interlace
1	Interlace

Crystal selection control bit	
Xfc	Function
0	4 f_{sc}
1	2 f_{sc}

- Scanning mode control

Two types of scanning modes can be selected in the internal video signal mode: non-interlace and interlace modes.

The number of scanning lines in this mode are 263 for NTSC and 312 for PAL signal.

- Crystal control mode

Two types of crystals for internal video signal generation can be selected in the NTSC mode: 4 f_{sc} and 2 f_{sc}. When 2 f_{sc} is selected, however, only six colors can be set for the internal video signals (eight colors can be selected with 4 f_{sc}, of which green and magenta cannot be selected with 2 f_{sc}).

In the PAL mode, only a crystal of 4 f_{sc} can be used.

2.9 SYNCHRONIZATION DETECTION CONTROL COMMAND

This command turns ON/OFF the synchronization detection output.

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	SD	0	0

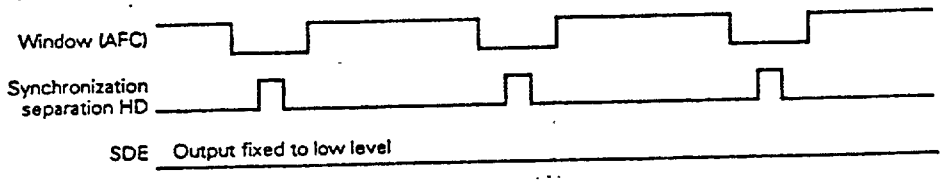
Synchronization detection control bit	
SD	Function
0	Synchronization detection output OFF
1	Synchronization detection output ON

- Synchronization detection control

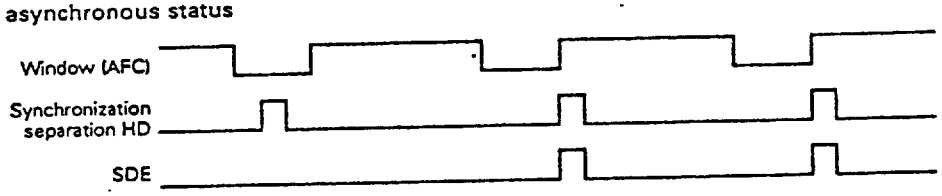
When synchronization detection output is ON, the SDE pin (pin 13) outputs the logical product (AND) of the AFC non-$\overline{H_{sync}}$ (synchronization negative) portion and H_{sync} (synchronization positive) separated from the video signal. When synchronization detection output is OFF, the SDE pin is fixed to the high level.

Synchronization detection output condition of μPD6454 (SDE pin)

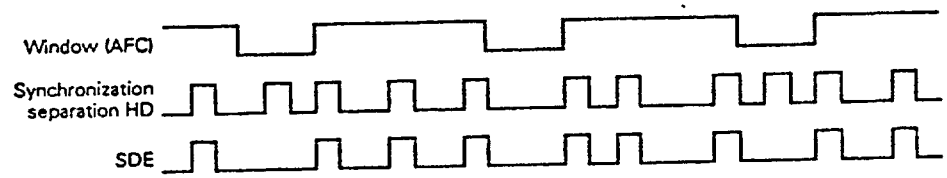
(1) In synchronized status



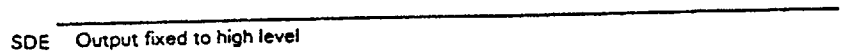
(2) In asynchronous status



(3) In weak electric field, or with signal with much noise



(4) When synchronization detection is OFF (set by command)



The SDE output is integrated by an external circuit. This signal is used by the microcomputer to identify the status of the video signal (high level: signal not output, low level: signal output), and a command is transferred to the μPD6454 so that the internal (blue back display) or external video signal mode is set. Note that, when synchronization detection is OFF, output (4) in the above figure is fixed to the high level.

2.10 DISPLAY POSITION CONTROL COMMAND

This command can set the display start position horizontally in 12-dot intervals in 32 stages, and vertically in 9-line intervals in 32 stages (because this is a 2-byte command, 16 bits must be input when the command is continuously input).

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	V4	V3	V2	V1	V0	H4	H3	H2	H1	H0

Horizontal display start position control bit

H4	H3	H2	H1	H0	Function
0	0	0	0	0	Time from rising of $\overline{H_{sync}}$ (μs) $(12 \times 1)/f_{osc}$ (MHz) + $4/f_{osc}$ (MHz)
0	0	0	0	1	Time from rising of $\overline{H_{sync}}$ (μs) $(12 \times 2)/f_{osc}$ (MHz) + $4/f_{osc}$ (MHz)
≈	≈	≈	≈	≈	≈
1	1	1	1	1	Time from rising of $\overline{H_{sync}}$ (μs) $(12 \times 3)/f_{osc}$ (MHz) + $4/f_{osc}$ (MHz)

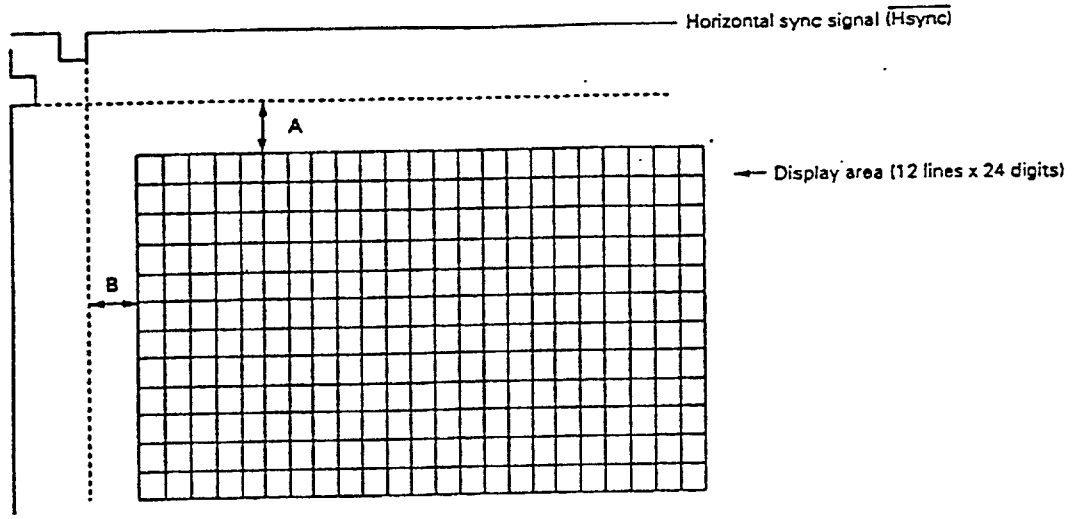
f_{osc} (MHz): LC oscillation frequency

Vertical display start position control bit

V4	V3	V2	V1	V0	Function
0	0	0	0	0	9 lines × 0 from rising of $\overline{V_{sync}}$
0	0	0	0	1	9 lines × 1 from rising of $\overline{V_{sync}}$
≈	≈	≈	≈	≈	≈
1	1	1	1	1	9 lines × 31 from rising of $\overline{V_{sync}}$

- Horizontal display start position control
  The horizontal display start position can be set after 16 clocks ($16/f_{osc}$ (MHz)), from the rising of the horizontal sync. signal ($\overline{H_{sync}}$) in 12-dot intervals and 32 stages. (f_{osc} (MHz): LC oscillation frequency)

- Vertical display start position control
  The vertical display start position can be set from the rising of the vertical sync signal ($\overline{V_{sync}}$) in 9-line intervals and 32 stages.



Vertical sync signal ($\overline{V_{sync}}$)

A: $9H \times (2^4V4 + 2^3V3 + 2^2V2 + 2^1V1 + 2^0V0)$

B: $\frac{12}{f_{osc}\,(MHz)} \times (2^4H4 + 2^3H3 + 2^2H2 + 2^1H1 + 2^0H0 + 1) + \frac{4}{f_{osc}\,(MHz)}$

The character position is determined by $\overline{H_{sync}}$ and $\overline{V_{sync}}$ that are generated as follows:

$\overline{H_{sync}}$: Generated by the internal AFC circuit

$\overline{V_{sync}}$: Generated by being synchronization-separated inside the device

2.11 WRITE ADDRESS CONTROL COMMAND

This command specifies a write address when a character is written to the 12-line × 24-digit display area (video RAM) (Because this is a 2-byte command, 16 bits must be input even when the command is continuously input.).

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	0	AR3	AR2	AR1	AR0	AC4	AC3	AC2	AC1	AC0

Write digit address control bit					
AC4	AC3	AC2	AC1	AC0	Function
0	0	0	0	0	Sets first digit
0	0	0	0	1	Sets second digit
≈	≈	≈	≈	≈	≈
1	0	1	1	1	Sets 24th digit
Inhibited					

Write line address control bit				
AR3	AR2	AR1	AR0	Function
0	0	0	0	Set first line
0	0	0	1	Set second line
≈	≈	≈	≈	≈
1	0	1	1	Set 12th line
Inhibited				

- Write digit address control
  One line consists of 24 digits in the horizontal direction.
  A digit to be written must be specified.

- Write line address control
  A display area consists of 12 lines in the vertical direction.
  A line to be written must be specified.

Video RAM configuration

The video RAM is configured with 12 lines by 24 digits as shown below.
The number of display characters is 12 lines by 24 digits (in minimum size).

AC4, AC3, AC2, AC1, AC0		0000	0001	00010	≈	10110	10111
AR3, AR2, AR1, AR0	0000				≈		
	0001				≈		
	0010				≈		
	0011				≈		
	0100				≈		
	0101				≈		
	0110				≈		
	0111				≈		
	1000				≈		
	1001				≈		
	1010				≈		
	1011				≈		

2.12 CHARACTER/BACKGROUND LUMINANCE LEVEL CONTROL COMMAND

The μPD6454 allows the luminance level of characters and background (including fringes) to be set by a command (Because this is a 2-byte command, 16 bits must be input when the command is input continuously.).

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	0	0	VPD	VB3	VB2	VB1	VB0	VC3	VC2	VC1	VC0

Character level control bit

VC3	VC2	VC1	VC0	Function
0	0	0	0	0 I.R.E.
0	0	0	1	10 I.R.E.
0	0	1	0	20 I.R.E.
0	0	1	1	30 I.R.E.
0	1	0	0	40 I.R.E.
0	1	0	1	70 I.R.E.
0	1	1	0	80 I.R.E.
0	1	1	1	90 I.R.E.
1	0	0	0	100 I.R.E.
Inhibited				

Background level control bit

VB3	VB2	VB1	VB0	Function
0	0	0	0	0 I.R.E.
0	0	0	1	10 I.R.E.
0	0	1	0	20 I.R.E.
0	0	1	1	30 I.R.E.
0	1	0	0	40 I.R.E.
0	1	0	1	70 I.R.E.
0	1	1	0	80 I.R.E.
0	1	1	1	90 I.R.E.
1	0	0	0	100 I.R.E.
Inhibited				

Internal video signal amplitude control bit

VPD	Function
0	$1V_{P-P}$ amplitude
1	$2V_{P-P}$ amplitude

- Character level control
  The luminance level of a character can be set in 9 stages.

- Background (fringe) level control
  The luminance level of the background (fringe) can be set in 9 stages.

- Internal video signal amplitude control
  The amplitude of the internal video signal can be set to $1V_{P-P}$ or $2V_{P-P}$ (must match the amplitude of the video signal input in the external video signal mode). When $1V_{P-P}$ is set, apply 2.5 V to the V_{CNT} pin. To set $1V_{P-P}$, apply 5 V to the V_{CNT} pin.

2.13 CHARACTER SIZE CONTROL COMMAND

This command can set character size in line units (simultaneously set in the vertical and horizontal directions). Because this is a 2-byte command, 16 bits must be input when the command is continuously input.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	1	0	0	0	S1	S0	0	0	AR3	AR2	AR1	AR0

Line specification control bit

AR3	AR2	AR1	AR0	Function
0	0	0	0	Set first line
0	0	0	1	Set second line
≈	≈	≈	≈	≈
1	0	1	1	Set 12th line
Inhibited				

Character size control bit

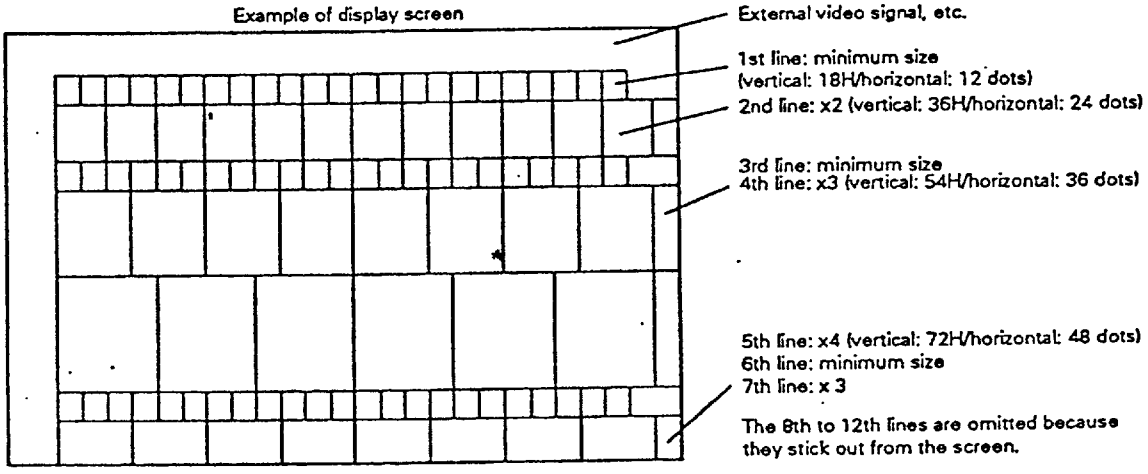
S1	S0	Function
0	0	Vertical 1 dot: 1H, horizontal 1 dot: 1t dot (minimum size)
0	1	Vertical 1 dot: 2H, horizontal 1 dot: 2t dots
1	0	Vertical 1 dot: 3H, horizontal 1 dot: 3t dots
1	1	Vertical 1 dot: 4H, horizontal 1 dot: 4t dots

$$1t\ dot = \frac{1}{f_{osc}\,(MHz)}\ \mu s$$

where, f_{osc} (MHz): LC oscillation frequency

- Line specification control
  The character size is specified in line units. A line to be specified is controlled.
- Character size control
  The character size can be selected in 4 stages.

Display with different character sizes mixed



The size in the vertical direction (the number of horizontal scanning lines) is per field.

2.14 TEST MODE

This command is to test the IC. Do not use it for any other purposes.

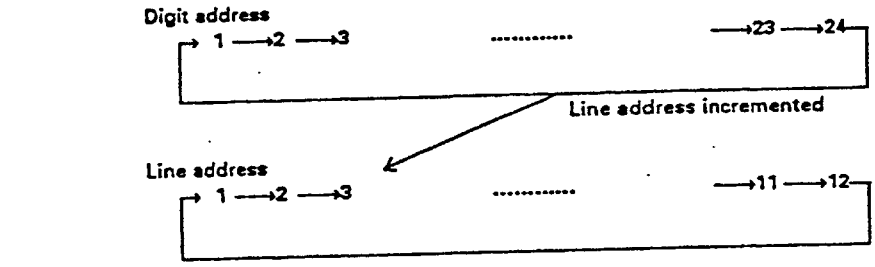
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	0	0	0	0	T7	T6	T5	T4	T3	T2	T1	T0

2.15 DISPLAY CHARACTER CONTROL COMMAND

This command specifies the character data and blinking data to be written to the video RAM. When this command is to be input, turn ON the LC oscillation (when oscillation is OFF, characters cannot be written to the video RAM).

Because this is a 2-byte continuous command, when character data are continuously written without changing the blinking data, abbreviated input by which only the lower 8 bits (D7 to D0) are input can be made for the second character and those that follow.

In this case, the write digit address is automatically incremented (when data is written to the 24th digit at the leftmost position, the next write address is automatically incremented to the first digit (leftmost position) of the next line).



D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	0	0	BL	0	C7	C6	C5	C4	C3	C2	C1	C0

Character specification bit

D7	D6	D5	D4	D3	D2	D1	D0	Function
0	0	0	0	0	0	0	0	Outputs data at 00H
0	0	0	0	0	0	0	1	Outputs data at 01H
≈	≈	≈	≈	≈	≈	≈	≈	≈
1	1	1	1	1	1	1	0	Outputs data at FEH (DISPLAY OFF)
1	1	1	1	1	1	1	1	Outputs data at FFH (2-byte continuous command end code)

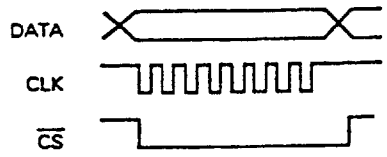
Blinking control bit	
BL	Function
0	Character does not blink
1	Character blinks

- Character specification
  Specifies the address of 256 types of characters. However, address FEH and FFH are respectively reserved for the Display Off Data and the end code of the 2-byte continuous command (these addresses are also fixed when the character is changed by mask code option and characters cannot be input).
  The design of the character can be changed by mask code option.

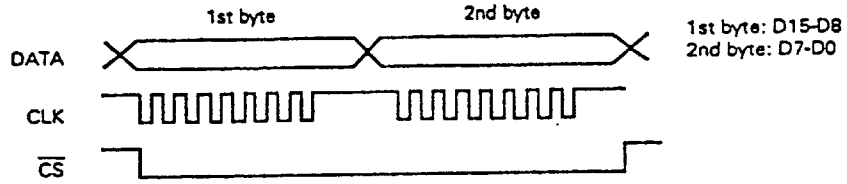
- Blink control
  Whether a character written to the video RAM blinks is specified for each character. For details on blinking ON/OFF control in screen units, refer to 2.2 DISPLAY CONTROL COMMAND.

3. COMMAND TRANSFER

3.1 1-BYTE COMMAND

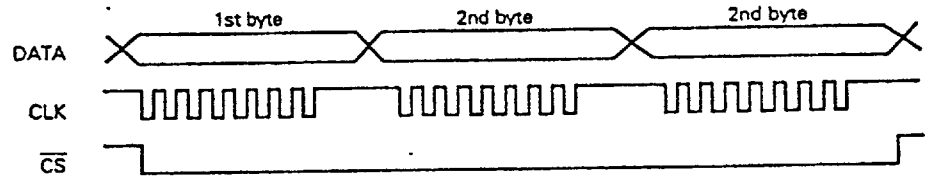


3.2 2-BYTE COMMAND



To use the 2-byte command, do not make $\overline{CS}$ high (keep it low) during the first and second bytes.

3.3 2-BYTE CONTINUOUS COMMAND



The 2-byte continuous command writes characters to the video RAM. To write characters continuously without changing the blink data, first transfer the first byte and then continuously transfer the second byte (character address).

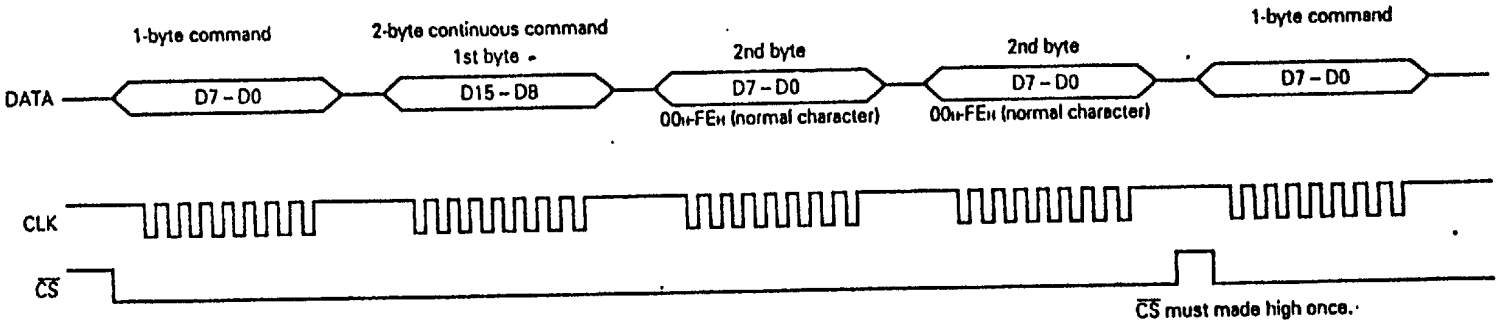
3.4 CONTINUOUS COMMAND INPUT

Transfer each of the 1-byte, 2-byte, and 2-byte continuous commands from the microcomputer to the μPD6454 as follows.

To transfer a 1-byte, 2-byte, or 2-byte continuous command with the blink data changed after a 2-byte continuous command has been transferred, either make $\overline{CS}$ high once, or transfer FFH (2-byte continuous command end code) at the end of the 2-byte continuous command. In the latter case, the $\overline{CS}$ needs not to be made high.

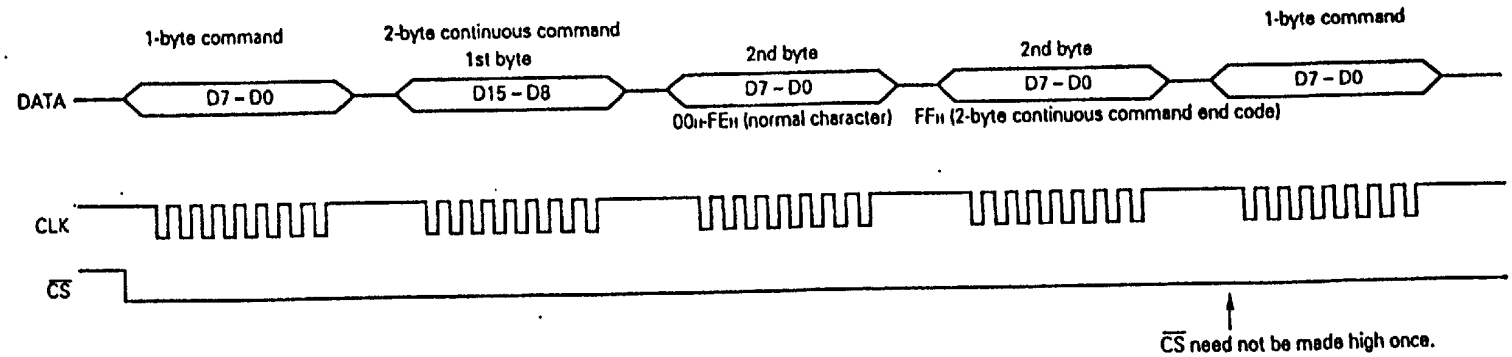
3.4.1 When 2-byte Continuous Command End Code Is not Used

Example: 1-byte command → 2-byte continuous command → 1-byte command



3.4.2 When 2-byte Continuous Command End Code Is Used

Example: 1-byte command → 2-byte continuous command → 1-byte command



Remark Although the $\overline{CS}$ pin can be low when the 2-byte continuous command end code is used, we recommended you make the pin high, unless especially required, to improve noise immunity.

4. ADJUSTING μPD6454

The μPD6454 is equipped with a synchronization separation circuit and an AFC circuit. Adjust each circuit as follows:

4.1 SYNCHRONIZATION SEPARATION CIRCUIT

The characteristics of the synchronization separation circuit are determined by the resistor or capacitor (1) in 8. APPLICATION CIRCUIT. The resistance and capacitance described in the figure are measured with NEC's jigs and to be used for reference only.

The resistor and capacitor connected to the synchronization separation time constant connection pin (SSCR) have the following tendency:

- Resistance

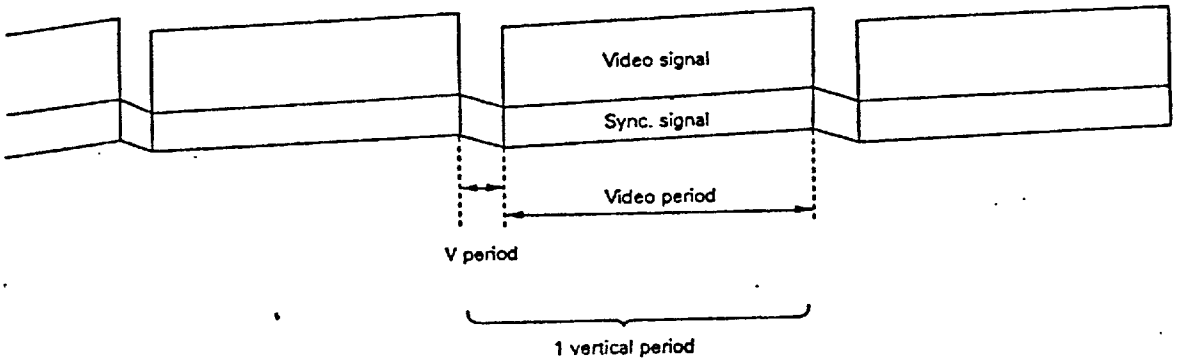
Resistance: low	Sync. signal slice level: low (pedestal side)
Resistance: high	Sync. signal slice level: high (synchronization end side)

- Capacitance

Capacitance: low	Voltage fluctuation of SSCR pin during vertical period of video signal: large (slice level: low)
Capacitance: high	Voltage fluctuation of SSCR pin during vertical period of video signal: small (slice level: high)

As for capacitance, sufficiently evaluate the follow-up of the video signal to the DC level fluctuation.

- Evaluation: Follow up of video signal to DC level fluctuation
  Check to see if the character display is not disturbed when the input signal to the μPD6454 has been changed from "a black signal to a white signal" (or vice versa).
  Also evaluate sufficiently when the vertical sync. signal is in the following status:

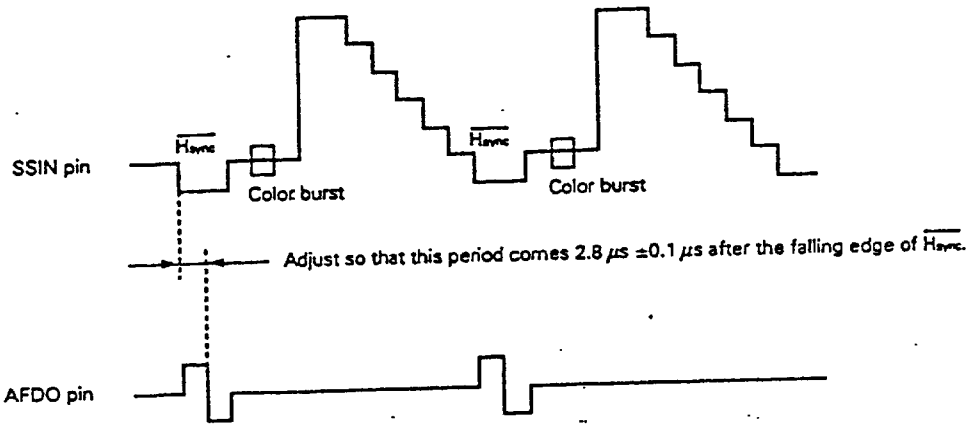


4.2 AFC CIRCUIT

The μPD6454 is equipped with an AFC circuit ($\overline{H_{sync}}$). In addition, it is also equipped with VCO used for the AFC circuit. The oscillation frequency (free run) of this VCO must match the frequency of $\overline{H_{sync}}$.

Adjustment method

- The waveforms of the following two pins are used:



Adjust the variable resistor ② in the application circuit diagram.

4.3 OSCILLATION FREQUENCY ADJUSTMENT

4.3.1 Adjusting Crystal Oscillation Frequency

The μPD6454 generates the internal video signal through 4 f_{sc} or 2 f_{sc} (NTSC) crystal oscillation. The oscillation frequency of the crystal can also be output from the $\overline{VSYO}$ pin by the test mode command.

Adjustment

- The crystal oscillation frequency is output from the $\overline{VSYO}$ pin by inputting the following command. Because the μPD6454 enters the test mode with this command input, execute the test mode clear command after the adjustment is finished.
- In this case, this pin does not function as the $\overline{VSYO}$ pin (vertical synchronization signal output pin).
- Adjust the trimmer (3) in 8. APPLICATION CIRCUIT DIAGRAM, watching a frequency counter.

Crystal oscillation frequency output command (2-byte command)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	0	0	0	0	0	0	0	0	1	1	1	1

4.3.2 Adjusting LC Oscillation Frequency (Dot clock)

The μPD6454 creates the character dots through LC oscillation.
The LC oscillation frequency can be output from the SDE pin by the test mode command in the similar manner as when the crystal oscillation frequency is adjusted as described in 4.3.1.

Adjustment

- The LC oscillation frequency is output from the SDE pin when the following command is input. (Adjust the LC oscillation frequency in the display OFF status. In the display ON status, oscillation stops during the LOW period of $\overline{H_{SYNC}}$ and therefore the accurate oscillation frequency cannot be measured with devices like a frequency counter).
  Because the μPD6454 enters the test mode with this command input, execute the test mode clear command after the judgement is finished.
- In this case, this pin does not function as SDE (synchronization detection output) pin.
- Adjust the coil (4) (or trimmer) in 8. APPLICATION CIRCUIT DIAGRAM, watching a frequency counter.

LC oscillation frequency output command (2-byte command)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	0	0	0	0	0	0	0	0	1	1	1	1

4.4 TEST MODE CLEAR COMMAND

The test mode clear command is in the following format:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0

4.5 CLAMP LEVEL OF VIDEO SIGNAL

The clamp level of the composite video signal input to the μPD6454 must match the internal video signal level of the μPD6454; otherwise, the luminance level of character and background in the external video signal mode becomes different from that in the internal video mode.

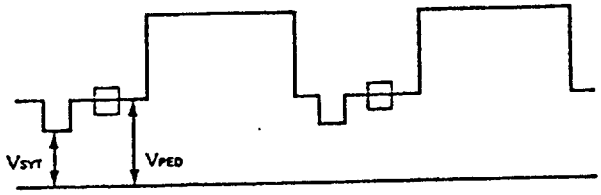
Adjustment

- The internal video signal level of the μPD6454 is set by the applied voltage to the V_{CNT} pin and "Character/Background Luminance Level Control Command". The amplitude level, sync. chip level, and pedestal level of the internal video signal are set as follows:

V_{CNT} pin voltage	Specification by output level control command	Internal video signal amplitude level (V_{DD} = 5.0 typ.)	Sync. chip level (V_{DD} = 5.0 typ.) (V_{SYT})	Pedestal level (V_{DD} = 5.0 typ.) (V_{PED})
2.5 V	Selects 1 V_{P-P}	1 V_{P-P}	1 V	1.29 V
5.0 V	Selects 1 V_{P-P}	2 V_{P-P}	2 V	2.58 V
2.5 V	Selects 2 V_{P-P}	1 V_{P-P}	0.5 V	0.79 V
5.0 V	Selects 2 V_{P-P}	2 V_{P-P}	1 V	1.58 V

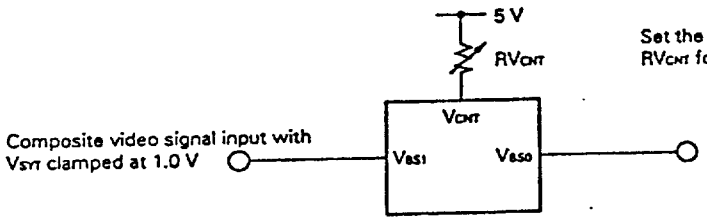
- Adjust the sync. chip level and pedestal level of the external video signal to the same levels as those of the internal video signal by using the variable resistor (5) in 8. APPLICATION CIRCUIT DIAGRAM. To set the video amplitude level to 1 V_{P-P}, we recommend you connect a variable resistor to the V_{CNT} pin to adjust the internal video signal level (To use the video signal at amplitude of 2 V_{P-P}, connect the V_{CNT} pin to the power supply (5 V)).

V_{SYT} and V_{PED} levels of composite video signal



Match the level output from the V_{BSI} pin in the external video signal mode with that in the internal video signal mode.

Input level in external video signal mode (with video signal of 1 V_{P-P} input)



Set the voltage applied to V_{CNT} pin at 2.5 V by connecting RV_{CNT} for adjustment.

When external video signal is to be input with amplitude of 2 V_{P-P}, clamp the V_{SYT} of composite video signal at 1 V, apply 5.0 V(power supply) to the V_{CNT} pin, and set the VPD bit of the Character/Background Luminance Level Control Command to 1 (2 V_{P-P} amplitude).

5. CHARACTER PATTERN DATA

The only difference between the μPD6454CS-001 and μPD6454GT-101 is the package. The character patterns of the character ROM are the same and both the models can display 256 types of characters such as alphanumeric characters and symbols shown on the following pages.

The contents of the character ROM (character design) can be changed by mask code option. However, the addresses FEH and FFH are respectively reserved for [Display Off Data] and [2-byte continuous command end code] and character patterns cannot be written to these addresses.

FBH (Blank Data) and FEH (Display Off Data) of NEC's standard products are expressed in the same manner on the page showing character patterns (as characters without dots), but they are different in the following ways:

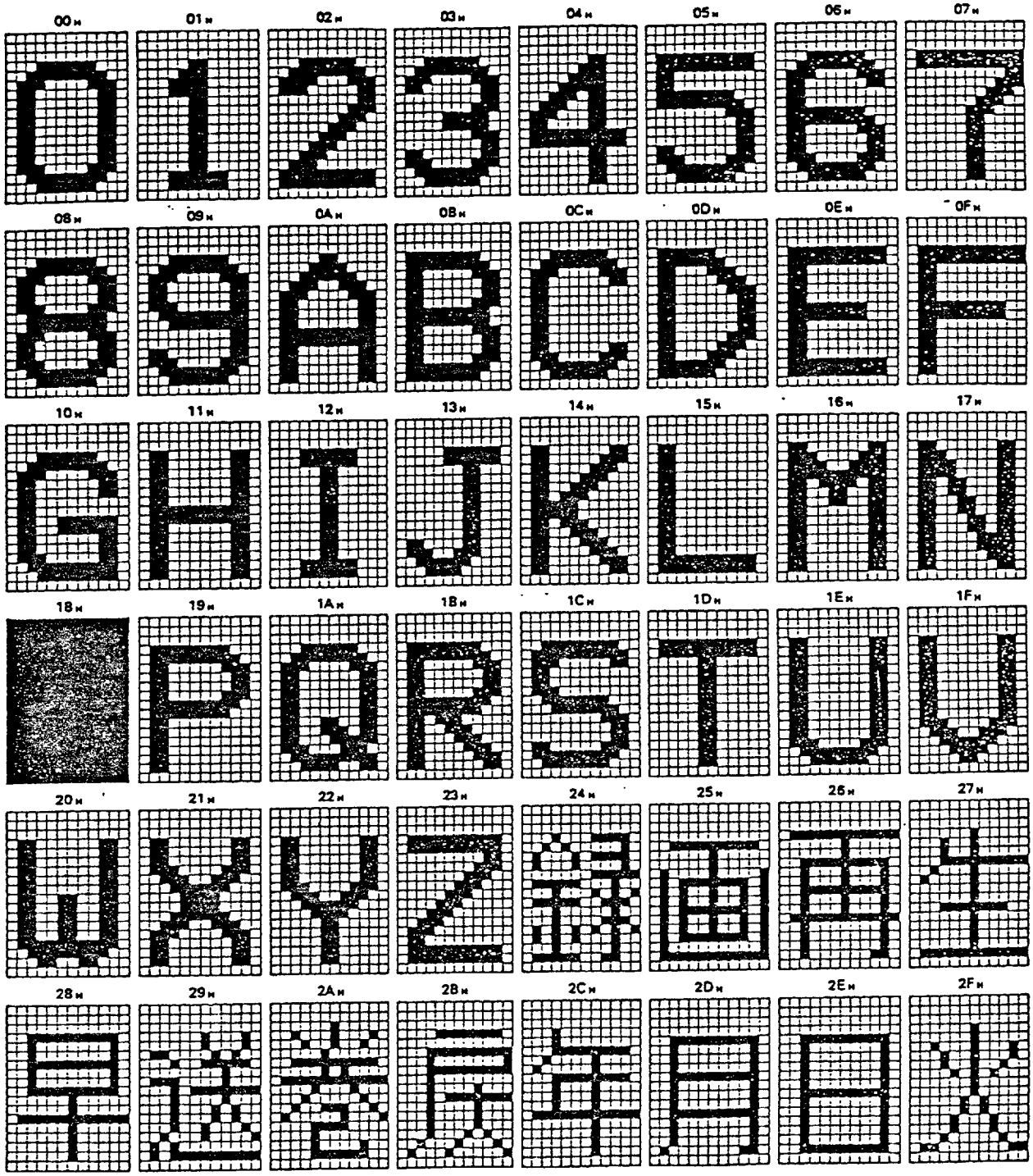
Video signal mode	Character code Note 2	Display of portion to which character is written in each mode		
		Background		
		None	Square	Solid
External video signal mode	Blank Data	Displays video signal	Displays background	Displays background
	Display Off Data	Displays external video signal	Displays external video signal (w/o background)	Displays external video signal (w/o background)
Internal video signal mode Note 1	Blank Data	Displays internal video signal color	Displays internal video signal color	Displays internal video signal color
	Display Off Data	Displays internal video signal color	Displays internal video signal color	Displays internal video signal color

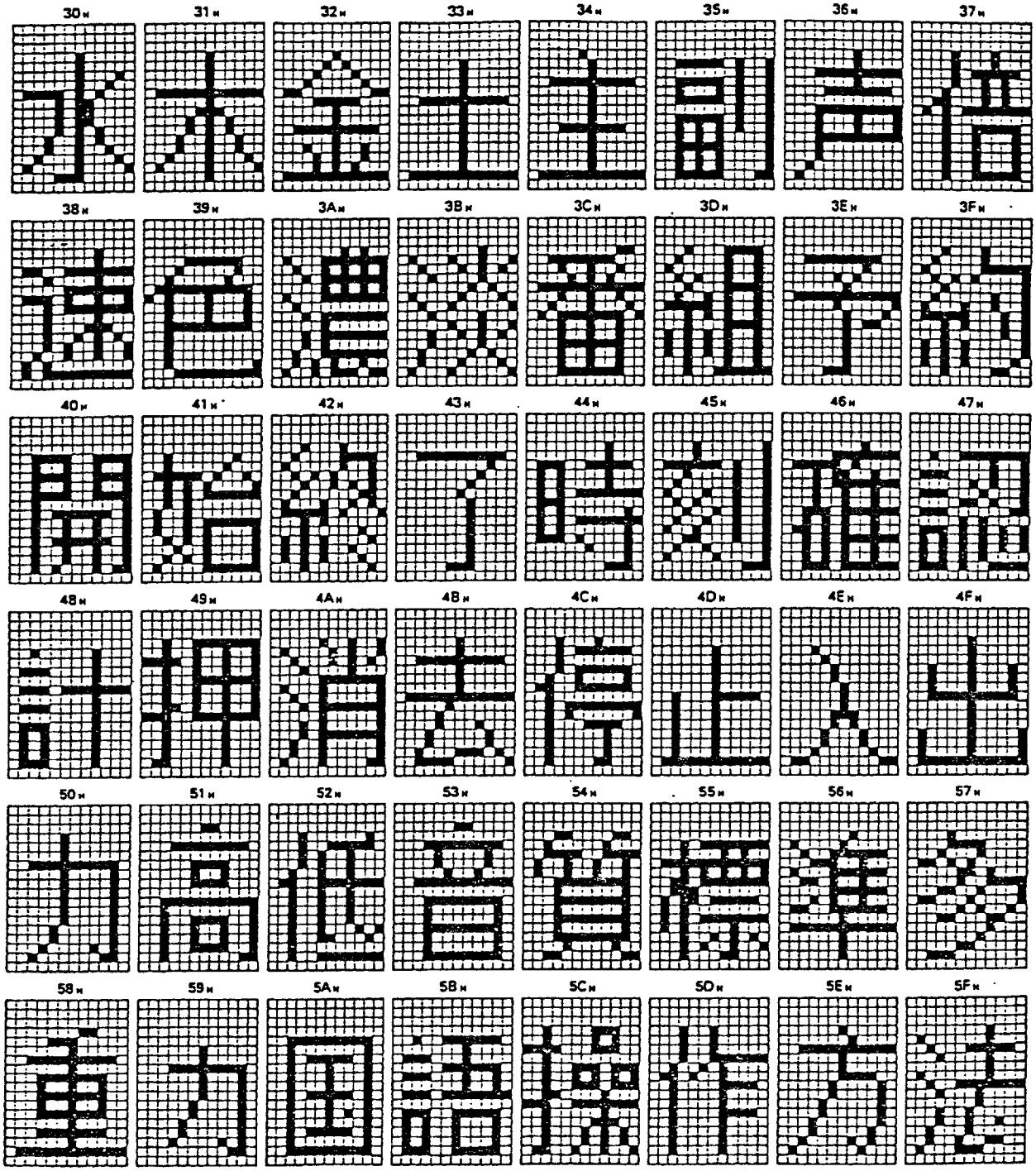
To create a character by mask code option, the address of Display Off Data is fixed to FEH, but the address of Blank Data is not fixed.

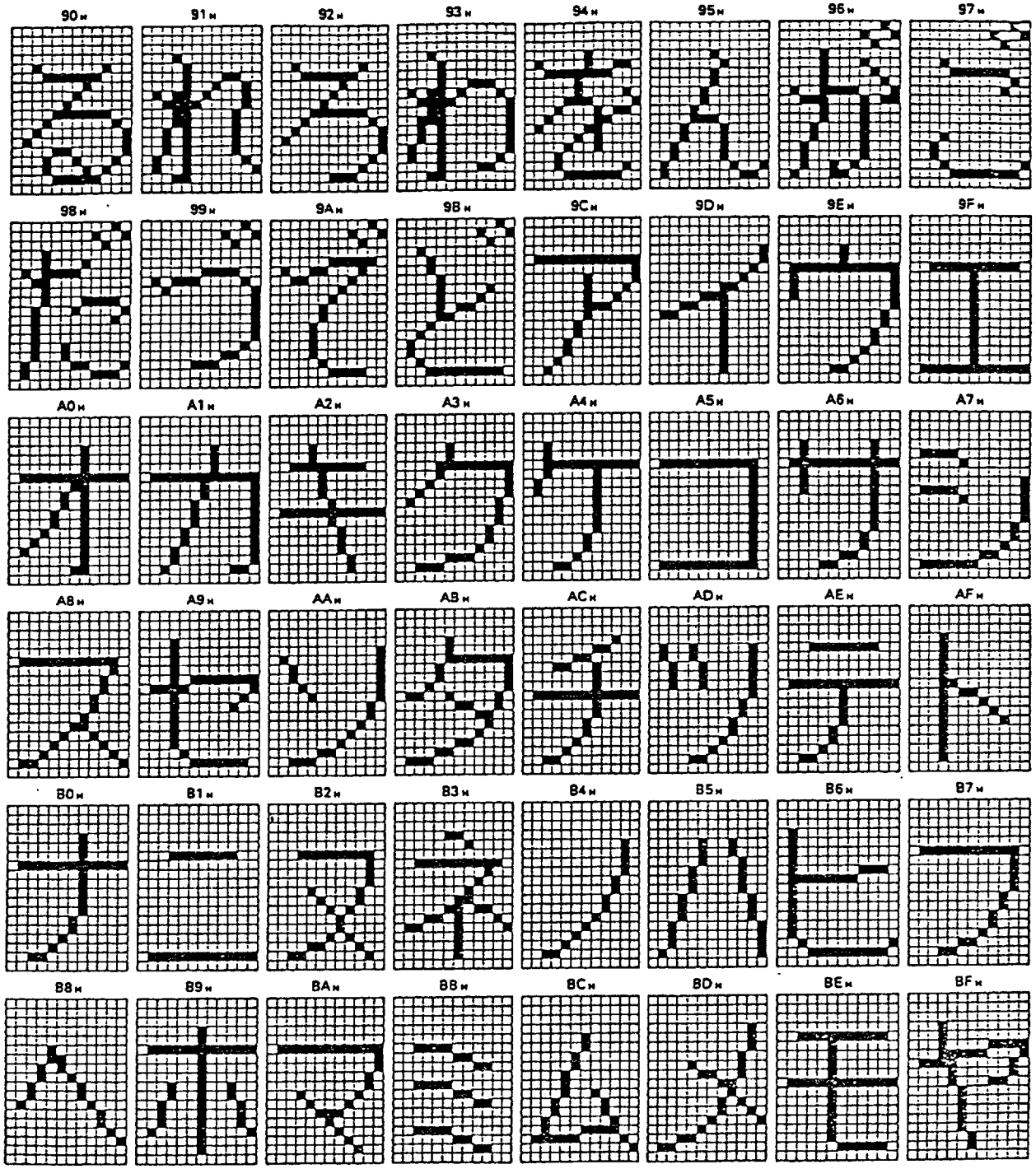
Note 1 In the internal video signal mode, the internal video signal is used as background. Therefore, the same display as background solid is performed in this mode (background specification is invalid).

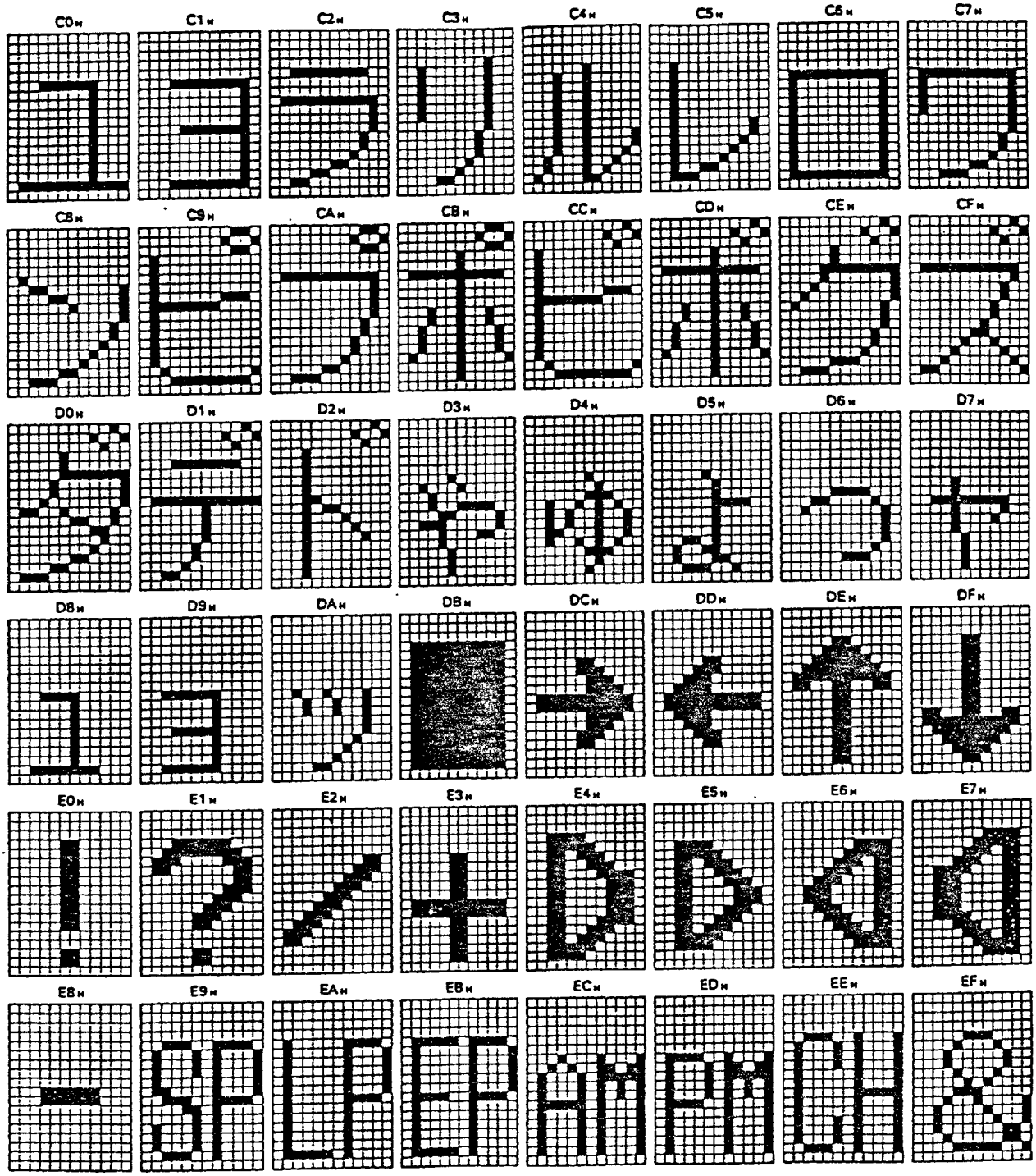
Note 2 Blank Data and Display Off Data are displayed in the same manner when the None is specified as background in the internal video signal mode and external video signal mode. When the Square or Solid is specified as background in the external video signal, Blank Data and Display Off Data are displayed in a different manner.

6. CHARACTER PATTERNS OF μPD6454CS-001 AND μPD6454GT-101









7. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	7	V
Input pin voltage	V_{IN}	−0.3 to V_{DD} +0.3	V
Output pin voltage	V_{OUT}	−0.3 to V_{DD} +0.3	V
Operating ambient temperature	T_{opt}	−20 to +75	°C
Storage temperature	T_{stg}	−40 to +125	°C
Output current	I_O	±5	mA

Recommended Operating Conditions

Parameter	Symbol	Conditions	MIN.	TYP.	MAX	Unit
Supply voltage	V_{DD}		4.5	5.0	5.5	V
Operating ambient temperature	T_{opt}		−20		+75	°C
LC oscillation frequency	fosc		4	7	8	MHz

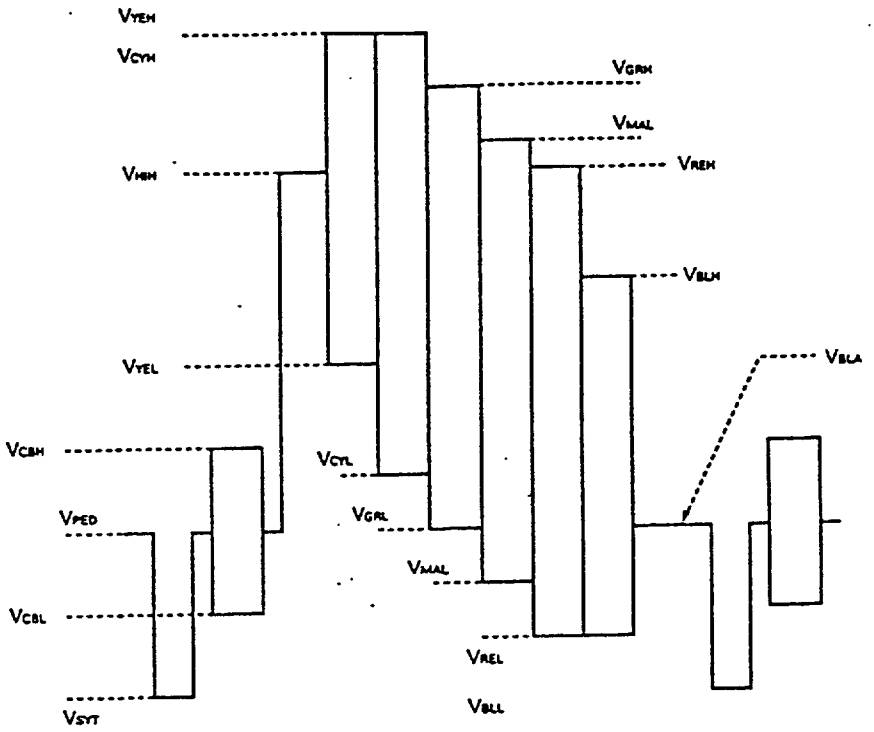
Electrical Characteristics (Unless otherwise specified, T_a = +25°C, V_{DD} = 5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX	Unit
Supply voltage	V_{DD}	V_{DD} = 4.5 to 5.5 V Note	4.5	5.0	5.5	V
Current consumption	I_{DD}	f_{OSC} = 8MHz, V_{CNT} = 2.5 V Note			20	mA
Signal output high-level voltage	V_{SOH}	I_{SOH} = −1 mA Note (VC, V_{BLK}, HSYO, $\overline{VSYO}$, SDE)	4.5			V
Signal output low-level voltage	V_{SOL}	I_{SOL} = 1 mA Note (VC, V_{BLK}, HSYO, VSYO, SDE)			0.5	V
Control input high-level voltage	V_{CIH}	DATA, CLK, $\overline{CS}$, $\overline{PCL}$ Note	2.4			V
Control input low-level voltage	V_{CIL}	DATA, CLK, $\overline{CS}$, $\overline{PCL}$ Note			0.8	V
Internal signal level set voltage	V_{VL}	V_{CNT} Note	2.5		V_{DD}	V
External video signal input voltage	V_I	VBSI Note	0		V_{DD}	V
AFC VCO control sensitivity	β_{AFC}	Horizontal sync. input = −300 mV_P		360		Hz/mV
Horizontal AFC sync. pull-in range	f_{PAFC}	Horizontal sync. input = −300 mV_P, f_H	(f_H) −0.7		(f_H) +0.7	kHz
Horizontal sync. signal input level	V_{HSI}	Horizontal sync. pulse width = 4.7 μs	−210			mV
Horizontal sync. signal input pulse width	V_{HST}	Horizontal sync. input = −300 mV_P	4.0			μs
Pedestal level voltage	V_{PED}	VBS0, internal mode, V_{CNT} = 2.5 V, V_{SYT} = 1.0 V		1.29		V
Sync. chip level voltage	V_{SYT}	VBS0, internal mode, V_{CNT} = 2.5 V, V_{SYT} = 1.0 V		1.00		V
Sync. signal width	V_{SW}	VBS0, internal mode, V_{CNT} = 2.5 V, V_{SYT} = 1.0 V	3.7			μs
Color burst high-level voltage	V_{CBH}	VBS0, internal mode, V_{CNT} = 2.5 V, V_{SYT} = 1.0 V	1.24	1.44	1.54	V
Color burst low-level voltage	V_{CBL}		0.94	1.14	1.24	V
Black level voltage	V_{BLA}		1.09	1.29	1.39	V
Blue VBS high-level voltage	V_{BLH}		1.41	1.61	1.71	V
Blue VBS low-level voltage	V_{BLL}		0.91	1.11	1.21	V
Green VBS high-level voltage	V_{GRH}		1.72	1.92	2.02	V
Green VBS low-level voltage	V_{GRL}		1.09	1.29	1.39	V
Cyan VBS high-level voltage	V_{CYH}		1.80	2.00	2.10	V
Cyan VBS low-level voltage	V_{CYL}		1.13	1.33	1.43	V
Red VBS high-level voltage	V_{REH}		1.59	1.79	1.89	V
Red VBS low-level voltage	V_{REL}		0.91	1.11	1.21	V
Magenta VBS high-level voltage	V_{MAH}		1.62	1.82	1.92	V
Magenta VBS low-level voltage	V_{MAL}		0.99	1.19	1.29	V
Yellow VBS high-level voltage	V_{YEH}		1.80	2.00	2.10	V
Yellow VBS low-level voltage	V_{YEL}		1.30	1.50	1.60	V
White level voltage	V_{WH}		1.58	1.79	1.89	V
Burst phase angle	ϕ_{BGN}	NTSC, internal mode	170	180	190	deg
Yellow phase angle	ϕ_Y		170	180	190	deg
Magenta phase angle	ϕ_M		35	45	55	deg
Red phase angle	ϕ_R		80	90	100	deg
Cyan phase angle	ϕ_C		260	270	280	deg
Green phase angle	ϕ_G		215	225	235	deg
Blue phase angle	ϕ_B		350	0	10	deg
Burst phase angle	ϕ_{BGN1}	PAL 1, internal mode	125	135	145	deg
Yellow phase angle	ϕ_{Y1}		170	180	190	deg
Magenta phase angle	ϕ_{M1}		35	45	55	deg
Red phase angle	ϕ_{R1}		80	90	100	deg
Cyan phase angle	ϕ_{C1}		260	270	280	deg
Green phase angle	ϕ_{G1}		215	225	235	deg
Blue phase angle	ϕ_{B1}		350	0	10	deg
Burst phase angle	ϕ_{BGN2}	PAL 2, internal mode	245	225	265	deg
Yellow phase angle	ϕ_{Y2}		170	180	190	deg
Magenta phase angle	ϕ_{M2}		305	315	325	deg
Red phase angle	ϕ_{R2}		260	270	280	deg
Cyan phase angle	ϕ_{C2}		80	90	100	deg
Green phase angle	ϕ_{G2}		125	135	145	deg
Blue phase angle	ϕ_{B2}		350	0	10	deg
Crystal oscillation frequency 1	f_{XON1}	NTSC, 4 f_{sc} mode		14.31818		MHz
Crystal oscillation frequency 2	f_{XON2}	NTSC, 2 f_{sc} mode		7.15909		MHz
Crystal oscillation frequency 3	f_{XON3}	PAL, (4 f_{sc})		17.7344		MHz

Note T_a = −20 to +75°C

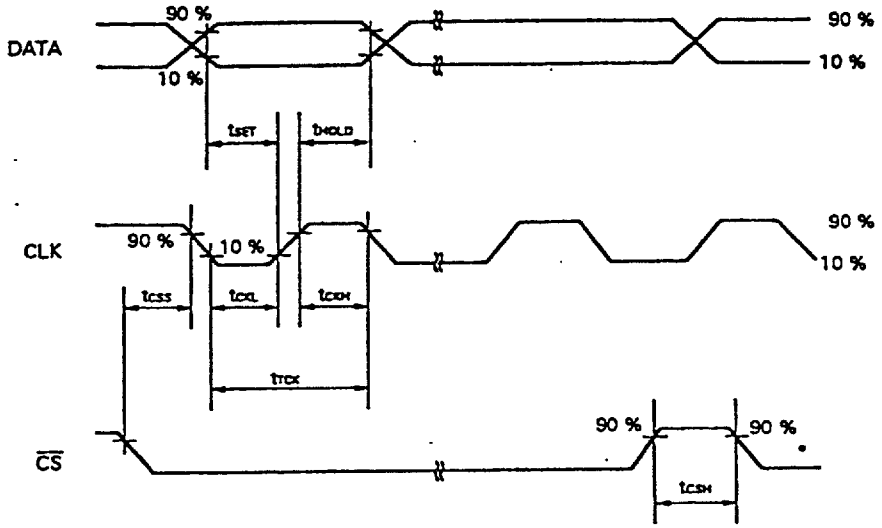
Parameter	Symbol	Conditions	MIN.	TYP.	MAX	Unit
Character/background 100% level voltage	V100	V_{OUT} = 2.5 V, V_{SYT} = 1.0 V,	1.80	2.00	2.10	V
Character/background 90% level voltage	V90		1.72	1.92	2.02	V
Character/background 80% level voltage	V80		1.66	1.86	1.96	V
Character/background 70% level voltage	V70		1.59	1.79	1.89	V
Character/background 40% level voltage	V40		1.37	1.57	1.67	V
Character/background 30% level voltage	V30		1.30	1.50	1.60	V
Character/background 20% level voltage	V20		1.24	1.44	1.54	V
Character/background 10% level voltage	V10		1.16	1.36	1.46	V
Character/background 0% level voltage	V0		1.09	1.29	1.39	V

μPD6454 internal video signal level



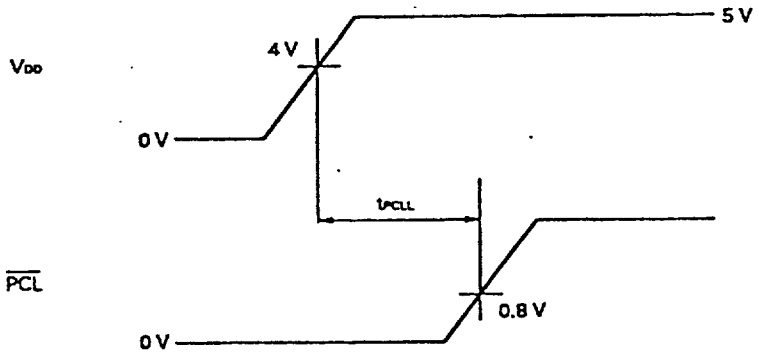
Recommended Operating Timing (T_a = −20 to +75°C, V_{DD} = 4.5 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX	Unit
Setup time	t_{SET}		200			ns
Hold time	t_{HOLD}		200			ns
Minimum clock low level width	t_{CCL}		400			ns
Minimum clock high level width	t_{CCH}		400			ns
Clock cycle	t_{TCK}		1.0			μs
$\overline{CS}$ setup time	t_{CSS}		400			ns
$\overline{CS}$ hold time	t_{CSH}		400			ns

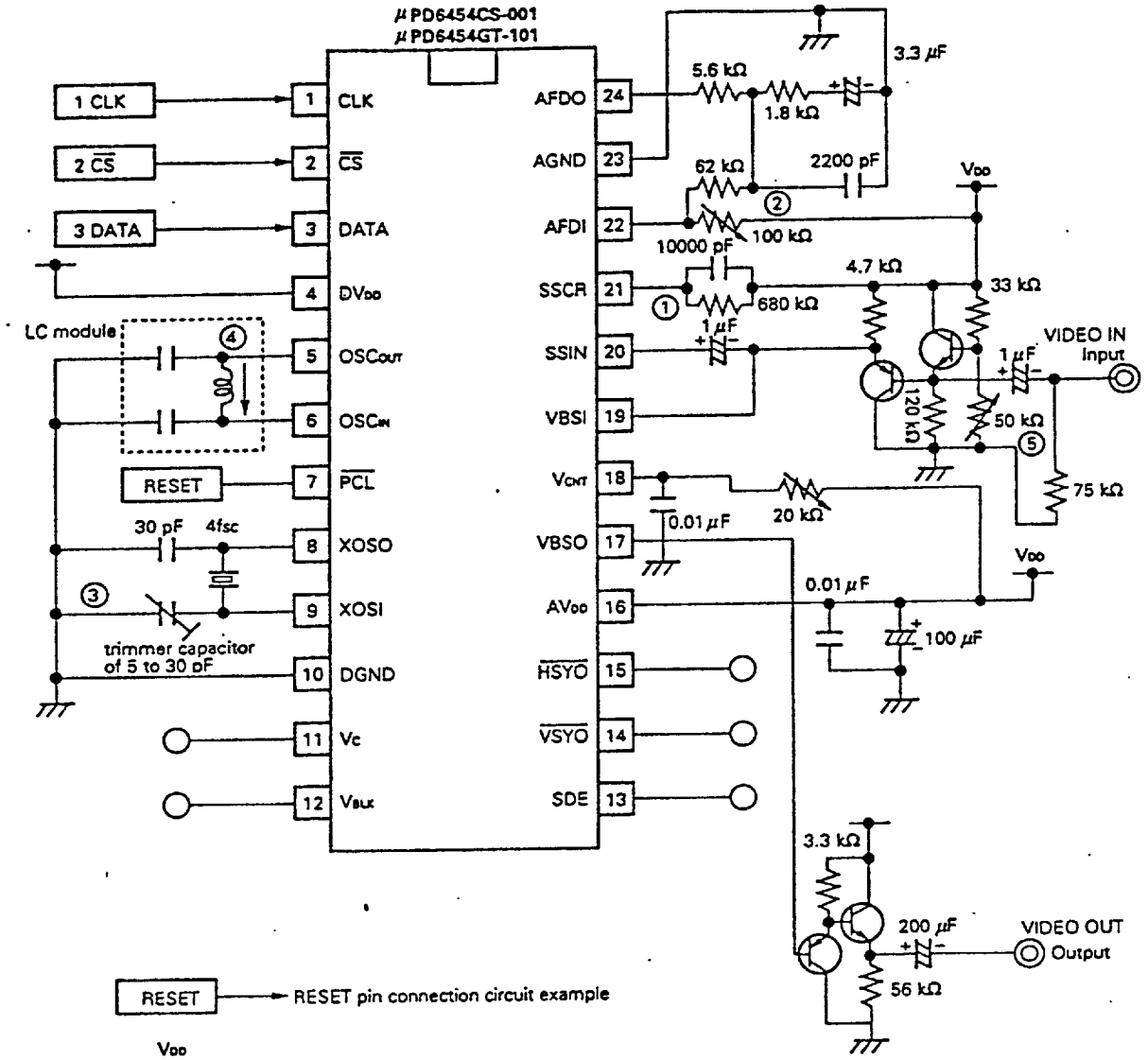


Power-on Clear Specification

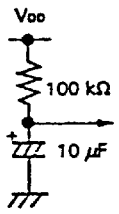
Parameter	Symbol	Conditions	MIN.	TYP.	MAX	Unit
$\overline{PCL}$ pin low hold time	t_{PCLL}		10			μs



8. APPLICATION CIRCUIT DIAGRAM



RESET → RESET pin connection circuit example

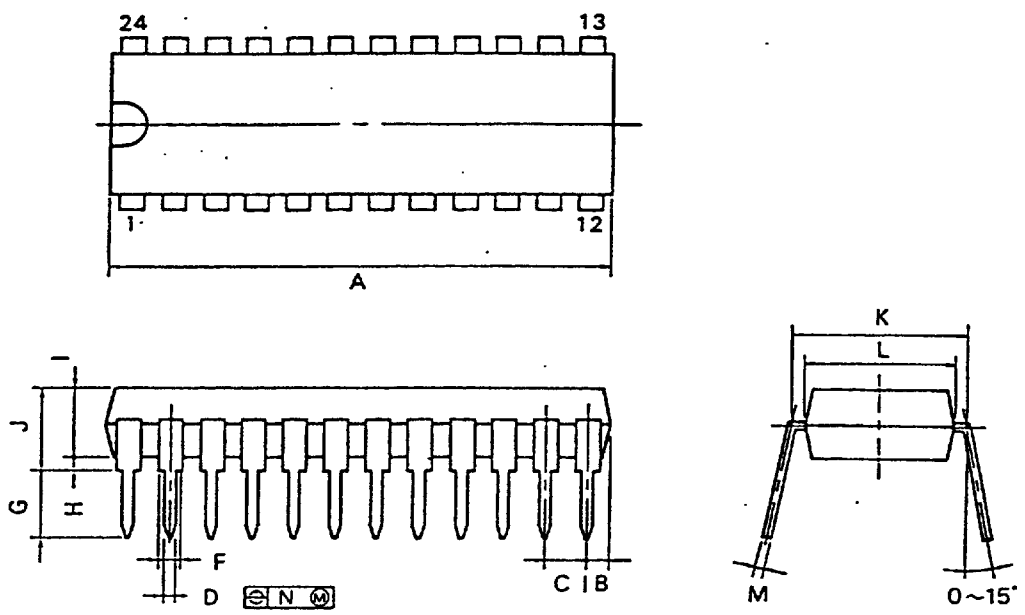


(Other constant may be used if the Power-on Clear Specification shown in the previous page is satisfied.)

The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

9. PACKAGE DRAWINGS (in mm)

24PIN PLASTIC SHRINK DIP (300 mil)



S24C-70-3008

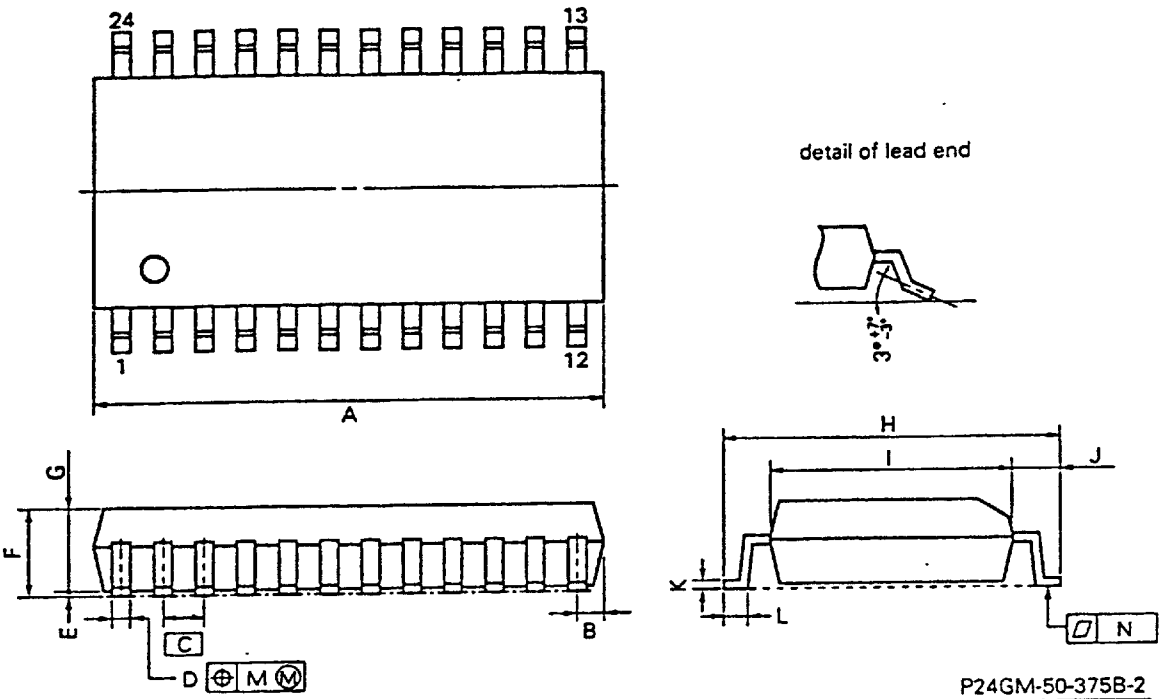
NOTES

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	23.12 MAX.	0.911 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	$0.50^{-0.10}$	$0.020^{+0.004}_{-0.005}$
F	0.85 MIN.	0.033 MIN.
G	$3.2^{-0.3}$	$0.126^{-0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.5	0.256
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007

24 PIN PLASTIC SOP (375 mil)



P24GM-50-375B-2

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	15.54 MAX.	0.612 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.1±0.1	0.004±0.004
F	2.9 MAX.	0.115 MAX.
G	2.50	0.098
H	10.3±0.3	$0.406^{+0.012}_{-0.013}$
I	7.2	0.283
J	1.6	0.063
K	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.002}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	0.12	0.005
N	0.15	0.006

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIAIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.