T-45-23-17

HARRIS

CD40102B, CD40103B Types

CMOS 8-Stage Presettable Synchronous Down Counters

High-Voltage Types (20-Volt Rating)

CD40102B – 2-Decade BCD Type
CD40103B – 8-Bit Binary Type

■ CD40102B, and CD40103B consist of an 8-stage synchronous down counter with a single output which is active when the internal count is zero. The CD40102B is configured as two cascaded 4-bit BCD counters, and the CD40103B contains a single 8-bit binary counter. Each type has control inputs for enabling or disabling the clock, for clearing the counter to its maximum count, and for presetting the counter either synchronously or asynchronously. All control inputs and the CARRY-OUT/ZERO-DETECT output are active-low logic.

In normal operation, the counter is decremented by one count on each positive transition of the CLOCK. Counting is inhibited when the CARRY-IN/COUNTER ENABLE ($\overline{CI/CE}$) input is high. The CARRY-OUT/ZERO-DETECT ($\overline{CO/ZD}$) output goes low when the count reaches zero if the $\overline{CI/CE}$ input is low, and remains low for one full clock period.

When the SYNCHRONOUS PRESET-ENABLE ($\overline{SPE}$) input is low, data at the JAM input is clocked into the counter on the next positive clock transition regardless of the state of the $\overline{CI/CE}$ input. When the ASYNCHRONOUS PRESET-ENABLE ($\overline{APE}$) input is low, data at the JAM inputs is asynchronously forced into the counter regardless of the state of the $\overline{SPE}$, $\overline{CI/CE}$, or CLOCK inputs. JAM inputs JO-J7 represent two 4-bit BCD words for the CD40102B and a single 8-bit binary word for the CD40103B.

When the CLEAR ($\overline{CLR}$) input is low, the counter is asynchronously cleared to its maximum count (99_{10} for the CD40102B and 255_{10} for the CD40103B) regardless of the state of any other input. The precedence relationship between control inputs is indicated in the truth table.

If all control inputs except $\overline{CI/CE}$ are high at the time of zero count, the counters will jump to the maximum count, giving a counting sequence of 100 or 256 clock pulses long.

This causes the $\overline{CO/ZD}$ output to go low to enable the clock on each succeeding clock pulse.

The CD40102B and CD40103B may be cascaded using the $\overline{CI/CE}$ input and the $\overline{CO/ZD}$ output, in either a synchronous or ripple mode as shown in Figs.21 and 22.

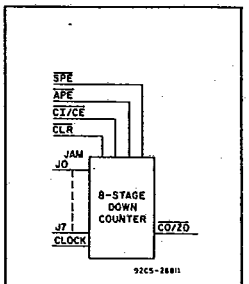
The CD40102B and CD40103B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

Features:

- Synchronous or asynchronous preset
- Medium-speed operation: f_{CL} = 3.6 MHz (typ.) @ V_{DD} = 10 V
- Cascadable
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) = 1 V at V_{DD} = 5 V, 2 V at V_{DD} = 10 V, 2.5 V at V_{DD} = 15 V
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Divide-by-"N" counters
- Programmable timers
- Interrupt timers
- Cycle/program counter



CD40102B, CD40103B FUNCTIONAL DIAGRAM

RECOMMENDED OPERATING CONDITIONS AT T_A = 25°C, Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	V_{DD}	LIMITS Min.	LIMITS Max.	Units
Supply Voltage Range (At T_A = Full Package-Temperature Range)		3	18	V
Clock Pulse Width, t_W	5	300	–	ns
	10	180	–	
	15	80	–	
$\overline{Clear}$ Pulse Width, t_W	5	320	–	ns
	10	160	–	
	15	100	–	
$\overline{APE}$ Pulse Width, t_W	5	360	–	ns
	10	160	–	
	15	120	–	
Clock Input Frequency, f_{CL}	5	–	0.7	MHz
	10	–	1.8	
	15	–	2.4	
Clock Rise and Fall Time, t_rCL, t_fCL	5	–	15	μs
	10	–		
	15	–		
$\overline{SPE}$ Setup Time, t_{SU}	5	280	–	ns
	10	140	–	
	15	100	–	
Jam Setup Time, t_{SU}	5	200	–	ns
	10	80	–	
	15	60	–	
$\overline{CI/CE}$ Setup Time, t_{SU}	5	500	–	ns
	10	250	–	
	15	150	–	

T-45-23-17

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
Voltages referenced to V_{SS} Terminal) ..... -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55°C to +100°C 500mW
For T_A = +100°C to +125°C ..... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C

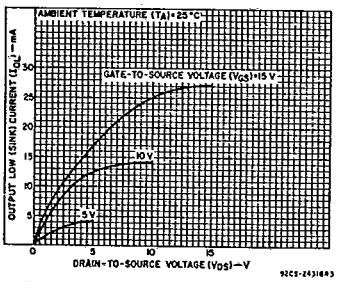


Fig. 1 — Typical output low (sink) current characteristics.

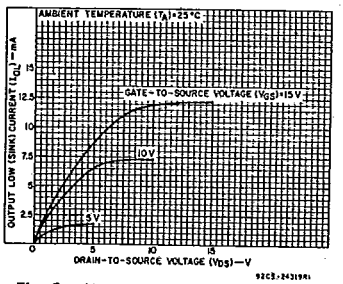


Fig. 2 — Minimum output low (sink) current characteristics.

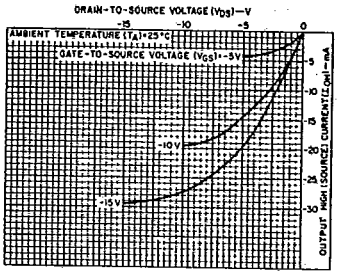


Fig. 3 — Typical output high (source) current characteristics.

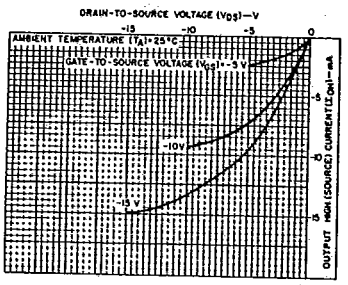


Fig. 4 — Minimum output high (source) current characteristics.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	-40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	µA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	–	
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	–	
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	–	
	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5,13.5	-	15	11				11	—	—	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$±10^{-5}$	±0.1	µA

Note 1: These parameters and limits also apply to the Synchronous Preset Mode should a Preset condition of JAM Zero on J_0 to J_7 exist.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, C_L = 50 pF, Input t_r, t_f = 20 ns, R_L = 200 kΩ

Characteristic	Conditions V_{DD} (V)	Limits All Packages Min.	Typ.	Max.	Units
Propagation Delay Time (t_{PHL}, t_{PLH}):					
Clock-to-Output (See Fig. 6)	5	–	300	600	ns
Note 1	10	–	130	260	
	15	–	95	190	
Carry In/Counter Enable-to-Output	5	–	200	400	
	10	–	90	180	
	15	–	65	130	
Asynchronous Preset Enable-to-Output	5	–	650	1300	
Note 1	10	–	300	600	
	15	–	200	400	
$\overline{\text{Clear}}$-to-Output	5	–	375	750	
	10	–	180	360	
	15	–	100	200	
Transition Time (t_{THL}, t_{TLH})	5	–	100	200	ns
	10	–	50	100	
	15	–	40	80	
Minimum Clock Pulse Width, (t_W)	5	–	150	300	ns
	10	–	90	180	
	15	–	40	80	
Minimum $\overline{\text{CLR}}$ Pulse Width (t_W)	5	–	160	320	
	10	–	80	160	
	15	–	50	100	
Minimum $\overline{\text{APE}}$ Pulse Width (t_W)	5	–	180	360	
	10	–	80	160	
	15	–	60	120	
Minimum $\overline{\text{APE}}$ Removal Time (t_{RM})	5	—	110	220	
	10	—	50	100	
	15	—	35	70	
Minimum $\overline{\text{SPE}}$ Set-Up Time (t_{SU})	5	–	140	280	
	10	–	70	140	
	15	–	50	100	
Minimum $\overline{\text{CI/CE}}$ Setup Time (t_{SU})	5	–	250	500	
	10	–	125	250	
	15	–	75	150	
Minimum JAM Set-Up Time (t_{SU}) *(Synchronous presetting)*	5	–	100	200	
	10	–	40	80	
	15	–	30	60	
Maximum Clock Input Frequency (f_{CL}) *(See Fig. 7)*	5	0.7	1.4	–	MHz
	10	1.8	3.6	–	
	15	2.4	4.8	–	
Input Capacitance (C_{IN})		–	5	7.5	pF

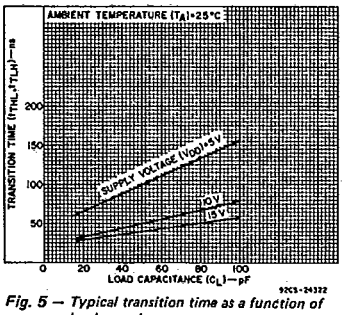


Fig. 5 — Typical transition time as a function of load capacitance.

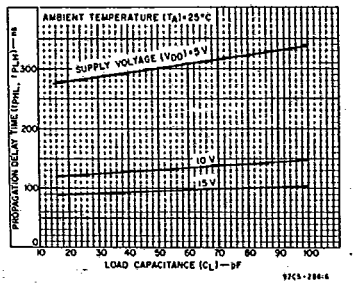


Fig. 6 — Typical propagation delay time as a function of load capacitance (clock to CO/ZD).

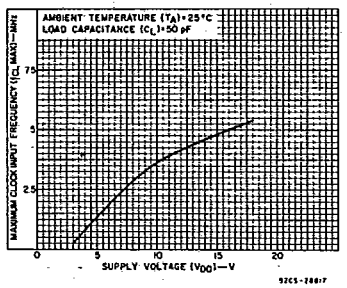


Fig. 7 — Typical maximum clock input frequency as a function of supply voltage.

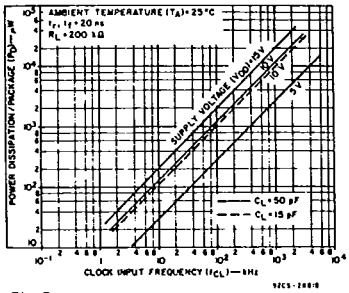


Fig. 8 — Typical dynamic power dissipation as a function of frequency.

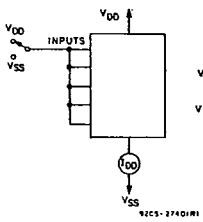


Fig. 9 — Quiescent device current test circuit.

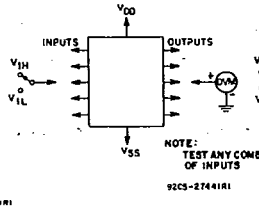


Fig. 10 — Input voltage test circuit.

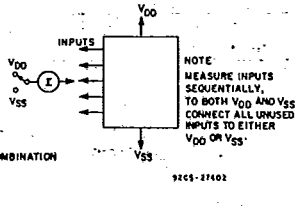


Fig. 11 — Input current test circuit.

T-45-23-17

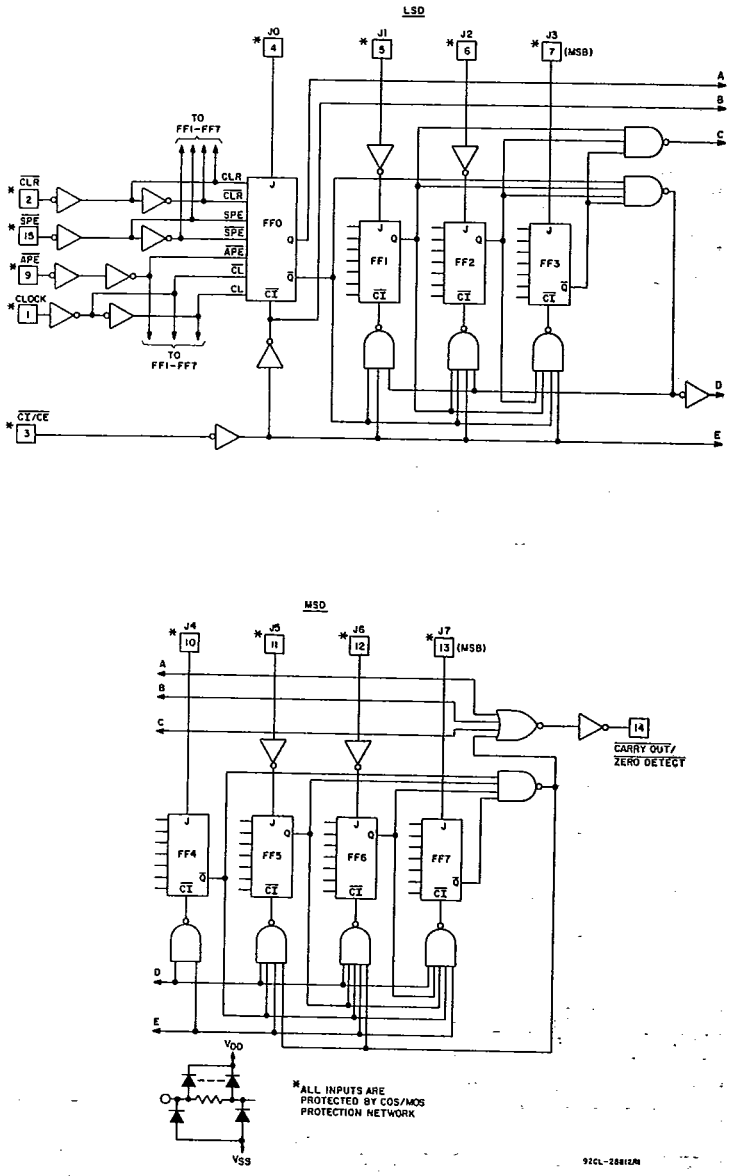


Fig. 12 – Logic diagram for CD40102B.

T-45-23-17

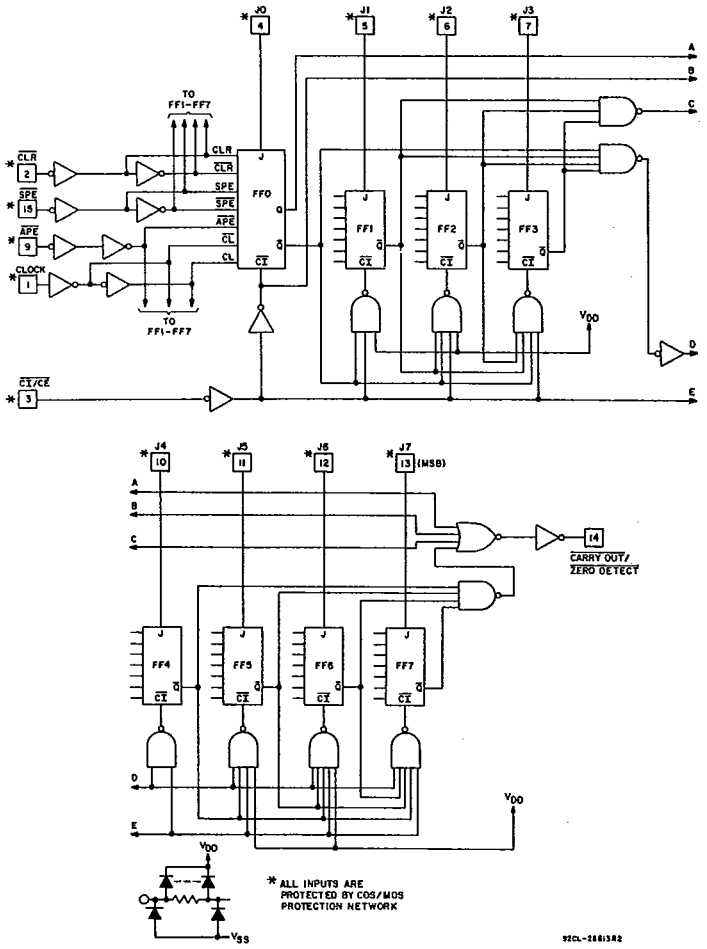


Fig. 13 – Logic diagram for CD40103B.

TRUTH TABLE

CONTROL INPUTS				PRESET MODE	ACTION
$\overline{CLR}$	$\overline{APE}$	$\overline{SPE}$	$\overline{CI/CE}$		
1	1	1	1	Synchronous	Inhibit counter
1	1	1	0		Count down*
1	1	0	X		Preset on next positive clock transition
1	0	X	X	Asynchronous	Preset asynchronously
0	X	X	X		Clear to maximum count

Notes: 1. 0 = Low level
1 = High level
X = Don't care

2. Clock connected to clock input
3. Synchronous operation: changes occur on negative-to-positive clock transitions
4. JAM inputs: CD40102B BCD; MSD = J7,J6,J5,J4 (J7 is MSB)
LSD = J3,J2,J1,J0 (J3 is MSB)
CD40103B Binary; MSB = J7, LSB = J0

*At zero count, the counters will jump to the maximum count on the next clock transition to "High."

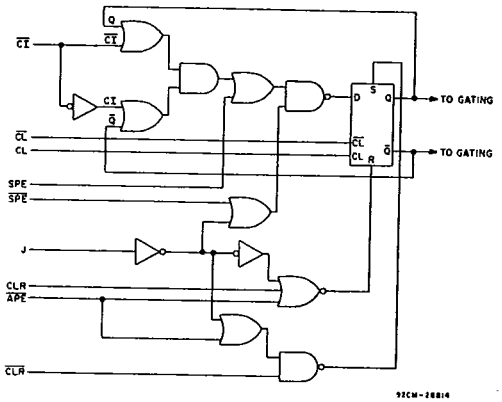


Fig. 14 – Detail logic diagram for flip-flops, FF0 – FF7, used in logic diagrams for CD40102B and CD40103B.

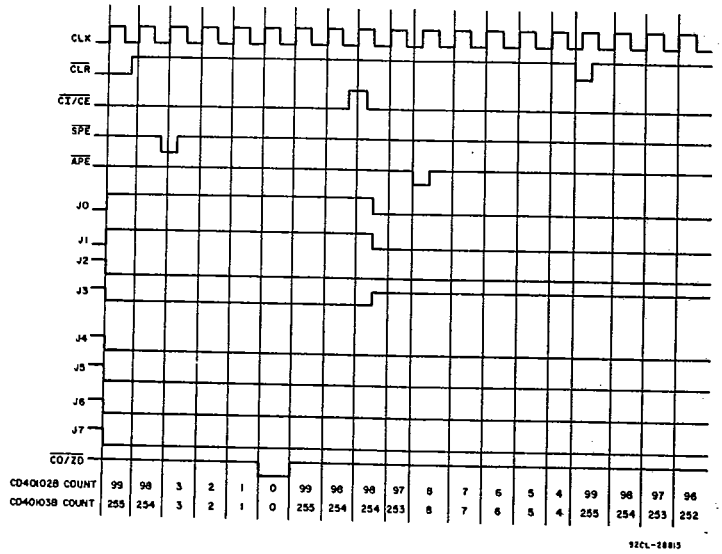
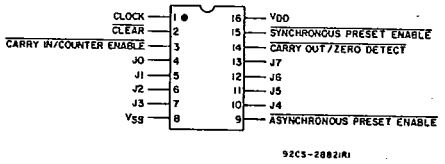


Fig. 15 – Timing diagram for CD40102B and CD40103B.



CD40102B, CD40103B
TERMINAL ASSIGNMENT

T-45-23-17

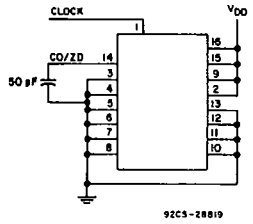


Fig.16 – Maximum clock frequency test circuit.

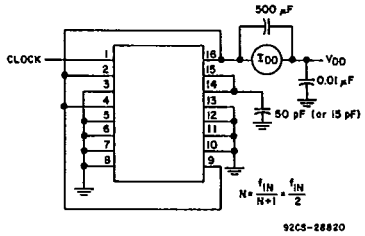


Fig.17 – Dynamic power dissipation test circuit (÷2 mode).

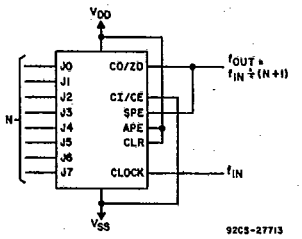


Fig.18 – Divide-by-"N" counter.

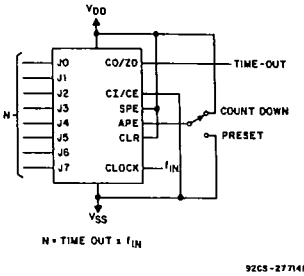


Fig.19 – Programmable timer.

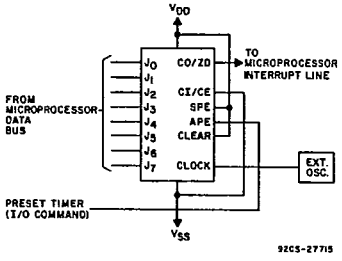
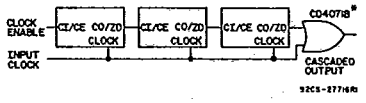


Fig.20 – Microprocessor interrupt timer.



* An output spike (160 ns @ V_{DD} = 5 V) occurs whenever two or more devices are cascaded in the parallel-clocked mode because the clock-to-carry out delay is greater than the carry-in-to-carry out delay. This spike is eliminated by gating the output of the last device with the clock as shown.

Fig.21 – Synchronous cascading.

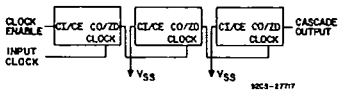
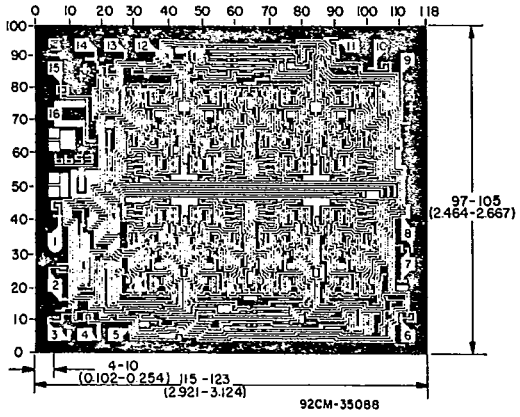


Fig.22 – Ripple cascading.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Dimensions and pad layout for CD40102B.



Dimensions and pad layout for CD40103B.