Empowered by Innovation NEC

## 0.35 µm CMOS Embedded Array

# EA-9HD Family


*Second-generation highly integrated*
*Multifarious macro support*
*Considerable cost reduction*

New Products

# WHAT IS AN EMBEDDED ARRAY?

An embedded array is a high-performance semi-custom LSI that uses in its internal area the basic cell of a gate array, and can integrate a large variety of macros, including the same type of RAM as a cell-based IC.
With an embedded array, a highly functional, high-performance LSI of the cell-based IC class can be realized.
Because it is possible to manufacture wafers and perform simulation in parallel, the end of simulation leaves only the wiring process to be completed, thus enabling the TAT up until sample completion to be reduced to the same level as for gate arrays.
By using an embedded array as the initial mass-produced product of cell-based ICs, it is possible to construct a system in express time.
Moreover, if the macro structure and gate scale levels are the same, the embedded array can be put to common use as a master wafer. Because of this, the cost of embedded arrays is lower than cell-based ICs, and it is possible to develop a variety of derivative products.
Furthermore, because the circuitry is easier to modify, embedded arrays aid in risk reduction.

# FEATURES

## Highly Integrated, Super High-Speed, Low Power Consumption-Type Embedded Array Using 0.35 μm Process

- Realizes the high-level function, high performance LSI of the cell-based IC class
- TAT reduced to gate array level
- Easy derivative-product development or reworking
- Macro common to cell-based IC (CB-9/9VX) provided

| Family Name | | EA-9HD |
|---|---|---|
| Supply voltage | | 3.3 V ±0.3 V |
| Delay time | Internal gates[Note 1] | 131 ps |
| | Input buffers[Note 2] | 229 ps |
| | Output buffers[Note 3] | 1396 ps |
| Power consumption | | 0.524 μW/MHz/cell (internal gates) |

**Notes 1.** 2NAND power gate, fanout = 1, standard wiring length value
**2.** The value when fanout = 1, standard wiring length value
**3.** The value when load capacitance 15 pF

**3-metal layer**

| Part Number | μPD65443 | μPD65444 | μPD65445 | μPD65446 | μPD65448 | μPD65449 | μPD65451 | μPD65454 | μPD65456 | μPD65458 |
|---|---|---|---|---|---|---|---|---|---|---|
| Number of I/O pads | 172 | 196 | 216 | 268 | 327 | 380 | 436 | 516 | 588 | 708 |
| Number of raw gates | 76720 | 103032 | 128872 | 207000 | 314104 | 440832 | 592020 | 840768 | 1104432 | 1626628 |
| Number of usable gates | 42196 | 56667 | 70879 | 113850 | 172757 | 220416 | 296010 | 420384 | 552216 | 731982 |

**4-metal layer**

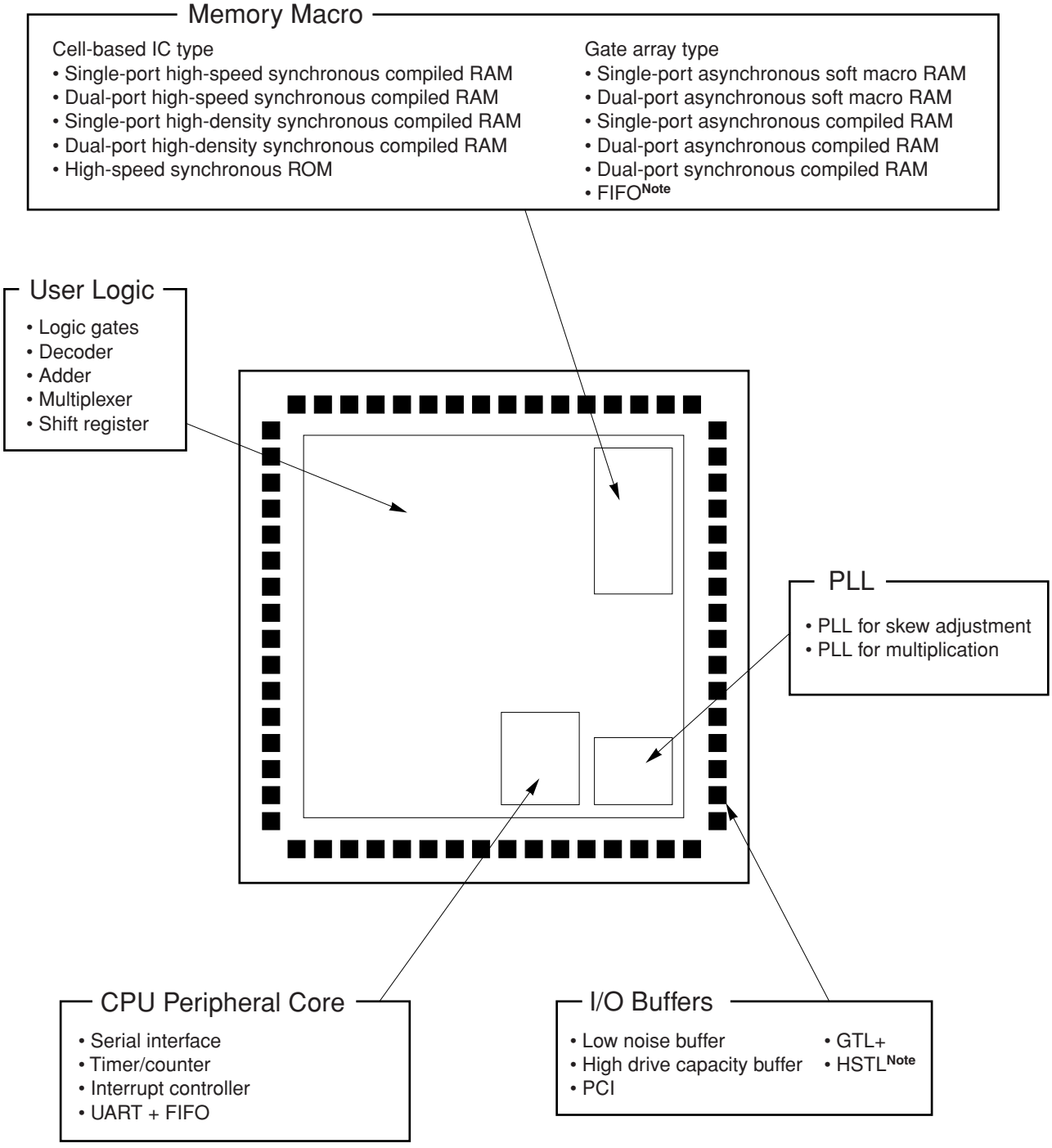
| Part Number | μPD65461 | μPD65464 | μPD65466 | μPD65468 | μPD65469 | μPD65470 | μPD65471 |
|---|---|---|---|---|---|---|---|
| Number of I/O pads | 436 | 516 | 588 | 708 | 764 | 820 | 876 |
| Number of raw gates | 592020 | 840768 | 1104432 | 1626628 | 1906800 | 2203360 | 2521344 |
| Number of usable gates | 355212 | 504460 | 662659 | 894645 | 1048740 | 1211848 | 1386739 |

**Remark** The actual number of usable signal lines depends on the package and the number of power supply and GND pins used.

## Support of Variety of Pin Count Packages

- 100- to 304-pin plastic QFP (fine-pitch)
- 48- to 120-pin plastic TQFP
- 144-pin plastic LQFP
- 225- to 352-pin plastic BGA
- 256- to 696-pin tape BGA

## Abundance of Macro Libraries




**Note** Macros that are under development or under investigation.

# ELECTRICAL SPECIFICATIONS

## Absolute Maximum Ratings

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | | –0.5 to +4.6 | V |
| Input voltage | | | | |
| LVTTL interface buffer | $V_I$ | $V_I < V_{DD}$ +0.5 V | –0.5 to +4.6 | V |
| LVTTL interface buffer with fail safe function | $V_I$ | $V_I < V_{DD}$ +0.5 V | –0.5 to +4.6 | V |
| TTL 5-V tolerant voltage interface buffer | $V_I$ | $V_I < V_{DD}$ +3.0 V | –0.5 to +6.6 | V |
| Output voltage | | | | |
| LVTTL output buffer | $V_O$ | $V_O < V_{DD}$ +0.5 V | –0.5 to +4.6 | V |
| TTL 5-V output buffer | $V_O$ | $V_O < V_{DD}$ +3.0 V | –0.5 to +6.6 | V |
| 5-V output buffer for CMOS | $V_O$ | $V_O < V_{DD}$ +3.0 V | –0.5 to +6.6 | V |
| Output current[Note] | $I_O$ | $I_{OL}$ = 1 mA (FV0A) | 3 | mA |
| | | $I_{OL}$ = 2 mA (FV0B) | 7 | mA |
| | | $I_{OL}$ = 3 mA (FO09) | 10 | mA |
| | | $I_{OL}$ = 6 mA (FO04) | 20 | mA |
| | | $I_{OL}$ = 9 mA (FO01) | 30 | mA |
| | | $I_{OL}$ = 12 mA (FO02) | 40 | mA |
| | | $I_{OL}$ = 18 mA (FO03) | 60 | mA |
| | | $I_{OL}$ = 24 mA (FO06) | 75 | mA |
| Operating ambient temperature | $T_A$ | | –40 to +85 | °C |
| Storage temperature | $T_{stg}$ | | –65 to +150 | °C |

**Note** Output current: Indicates the maximum value of the direct current that is allowed to flow through this output pin.

**Remark** With the exception of the buffer with fail safe function, be sure to apply voltage to the I/O pins only after the supply voltage has been fixed.

**Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

## Recommended Operating Range

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | LVTTL interface | | 3.00 | 3.30 | 3.60 | V |
| High-level input voltage | $V_{IH}$ | (LVTTL input buffer with | | 2.0 | | $V_{DD}$ | V |
| Low-level input voltage | $V_{IL}$ | fail-safe function) | | 0 | | 0.8 | V |
| Positive trigger voltage | $V_P$ | | Schmitt input | 1.4 | | 2.4 | V |
| Negative trigger voltage | $V_N$ | | | 0.8 | | 1.6 | V |
| Hysteresis voltage | $V_H$ | | | 0.3 | | 1.5 | V |
| High-level input voltage | $V_{IH}$ | TTL 5-V tolerant voltage | | 2.0 | | 5.5 | V |
| Low-level input voltage | $V_{IL}$ | interface | | 0 | | 0.8 | V |
| Positive trigger voltage | $V_P$ | | Schmitt input | 1.4 | | 2.4 | V |
| Negative trigger voltage | $V_N$ | | | 0.8 | | 1.6 | V |
| Hysteresis voltage | $V_H$ | | | 0.3 | | 1.5 | V |
| Input rise time | $t_{ri}$ | Normal input | | 0 | | 200 | ns |
| Input fall time | $t_{fi}$ | | | 0 | | 200 | ns |
| Input rise time | $t_{ri}$ | Schmitt input | | 0 | | 10 | ms |
| Input fall time | $t_{fi}$ | | | 0 | | 10 | ms |

**Remark** When inputting a slow signal with a long rise/fall time, noise on a signal line may affect the operation.
Therefore, use a Schmitt trigger input buffer.
Because fluctuation on the power supply line due to simultaneous operation of output buffers reduces the capability of the Schmitt trigger input buffer, carefully determine pin placement.

## DC Characteristics ($V_{DD}$ = 3.3 V ±0.3 V)

(1/3)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Static current consumption[Note1] | | | | | | |
| μPD65443, μPD65444, μPD65445, μPD65446, μPD65448, μPD65449, | $I_{DDS}$ | $V_I$ = $V_{DD}$ or GND | | 2.0 | 300 | μA |
| μPD65451, μPD65454, μPD65456 | $I_{DDS}$ | $V_I$ = $V_{DD}$ or GND | | 3.0 | 400 | μA |
| μPD65458 | $I_{DDS}$ | $V_I$ = $V_{DD}$ or GND | | 4.0 | 800 | μA |
| Off-state output current[Note2] | | | | | | |
| LVTTL output | $I_{OZ}$ | $V_O$ = $V_{DD}$ or GND | | | ±10 | μA |
| TTL 5-V tolerant voltage output | $I_{OZ}$ | $V_O$ = $V_{DD}$ or GND | | | ±10 | μA |
| 5-V tolerant voltage for CMOS | $I_{OZ}$ | $V_O$ = $V_{DD}$ or GND | | | ±10 | μA |
| Output flow current[Note3] 5-V tolerant output for CMOS | $I_R$ | $V_{PU}$ = 5.5 V, $R_{PU}$ = 2 kΩ, $V_O$ = 3.0 V | | | 0.1 | μA |
| Output short-circuit current[Note4] | $I_{OS}$ | $V_O$ = GND | | | –250 | mA |
| Input leakage current | | | | | | |
| Normal input | $I_I$ | $V_I$ = $V_{DD}$ or GND | | | ±1.0 | μA |
| With pull-up resistor (50 kΩ) | $I_I$ | $V_I$ = GND | –28 | –83 | –190 | μA |
| With pull-up resistor (5 kΩ) | $I_I$ | $V_I$ = GND | –280 | –700 | –1900 | μA |
| With pull-down resistor (50 kΩ) | $I_I$ | $V_I$ = $V_{DD}$ | 28 | 83 | 190 | μA |
| Pull-up resistor 50 kΩ[Note5] | $R_{PU}$ | $V_I$ = GND | 18.9 | 39.8 | 107.1 | kΩ |
| Pull-up resistor 5 kΩ[Note5] | $R_{PU}$ | $V_I$ = GND | 1.9 | 4.7 | 10.7 | kΩ |
| Pull-down resistor 50 kΩ[Note5] | $R_{PD}$ | $V_I$ = $V_{DD}$ | 18.9 | 39.8 | 107.1 | kΩ |

## DC Characteristics ($V_{DD}$ = 3.3 V ±0.3 V)

(2/3)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Low-level output current[Note6] | | | | | | |
| 3 mA buffer (FO09) | $I_{OL}$ | LVTTL output type | 3.00[Note7] | | | mA |
| 6 mA buffer (FO04) | $I_{OL}$ | $V_{OL}$ = 0.4 V | 6.00 | | | mA |
| 9 mA buffer (FO01) | $I_{OL}$ | | 9.00 | | | mA |
| 12 mA buffer (FO02) | $I_{OL}$ | | 12.00 | | | mA |
| 18 mA buffer (FO03) | $I_{OL}$ | | 18.00 | | | mA |
| 24 mA buffer (FO06) | $I_{OL}$ | | 24.00 | | | mA |
| 1 mA buffer (FV0A) | $I_{OL}$ | TTL 5-V tolerant voltage | 1.00 | | | mA |
| 2 mA buffer (FV0B) | $I_{OL}$ | output type | 2.00 | | | mA |
| 3 mA buffer (FV09) | $I_{OL}$ | $V_{OL}$ = 0.4 V | 3.00 | | | mA |
| 6 mA buffer (FV04) | $I_{OL}$ | | 6.00 | | | mA |
| 9 mA buffer (FV01) | $I_{OL}$ | | 9.00 | | | mA |
| 12 mA buffer (FV02) | $I_{OL}$ | | 12.00 | | | mA |
| 18 mA buffer (FV03) | $I_{OL}$ | | 18.00 | | | mA |
| 24 mA buffer (FV06) | $I_{OL}$ | | 24.00 | | | mA |
| 3 mA buffer (FY09) | $I_{OL}$ | 5-V tolerant voltage output | 3.00 | | | mA |
| 6 mA buffer (FY04) | $I_{OL}$ | type for CMOS | 6.00 | | | mA |
| 9 mA buffer (FY01) | $I_{OL}$ | $V_{OL}$ = 0.4 V | 9.00 | | | mA |
| 12 mA buffer (FY02) | $I_{OL}$ | | 12.00 | | | mA |
| 18 mA buffer (FY03) | $I_{OL}$ | | 18.00 | | | mA |
| 24 mA buffer (FY06) | $I_{OL}$ | | 24.00 | | | mA |

## DC Characteristics ($V_{DD}$ = 3.3 V ±0.3 V)

(3/3)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| High-level output current[Note6] | | | | | | |
| 3 mA buffer (FO09) | $I_{OH}$ | LVTTL output type | –3.00 | | | mA |
| 6 mA buffer (FO04) | $I_{OH}$ | $V_{OH}$ = 2.4 V | –6.00 | | | mA |
| 9 mA buffer (FO01) | $I_{OH}$ | | –9.00 | | | mA |
| 12 mA buffer (FO02) | $I_{OH}$ | | –12.00 | | | mA |
| 18 mA buffer (FO03) | $I_{OH}$ | | –18.00 | | | mA |
| 24 mA buffer (FO06) | $I_{OH}$ | | –24.00 | | | mA |
| 1 mA buffer (FV0A) | $I_{OH}$ | TTL 5-V tolerant voltage | –1.00 | | | mA |
| 2 mA buffer (FV0B) | $I_{OH}$ | output type | –1.00 | | | mA |
| 3 mA buffer (FV09) | $I_{OH}$ | $V_{OH}$ = 2.4 V | –3.00 | | | mA |
| 6 mA buffer (FV04) | $I_{OH}$ | | –3.00 | | | mA |
| 9 mA buffer (FV01) | $I_{OH}$ | | –3.00 | | | mA |
| 12 mA buffer (FV02) | $I_{OH}$ | | –3.00 | | | mA |
| 18 mA buffer (FV03) | $I_{OH}$ | | –6.00 | | | mA |
| 24 mA buffer (FV06) | $I_{OH}$ | | –6.00 | | | mA |
| Low-level output voltage | | | | | | |
| LVTTL output type | $V_{OL}$ | $I_{OL}$ = 0 mA | | | 0.1 | V |
| LVTTL output type (with 5 kΩ pull-up resistor) | $V_{OL}$ | $I_{OL}$ = 0 mA | | | 0.2 | V |
| TTL 5-V tolerant voltage output type | $V_{OL}$ | $I_{OL}$ = 0 mA | | | 0.1 | V |
| 5-V tolerant voltage output type for CMOS | $V_{OL}$ | $I_{OL}$ = 0 mA | | | 0.1 | V |
| High-level output voltage | | | | | | |
| LVTTL output type | $V_{OH}$ | $I_{OH}$ = 0 mA | $V_{DD}$ – 0.1 | | | V |
| TTL 5-V tolerant voltage output type | $V_{OH}$ | $I_{OH}$ = 0 mA | $V_{DD}$ – 0.2 | | | V |

**Notes 1.** When using I/O blocks (etc.) with pull-up/pull-down resistors incorporated, the static current consumption increases.

**2.** Because there is a bias toward the 5-V protection circuit in the TTL 5-V tolerant voltage and 5-V tolerant voltage for CMOS 3-state or I/O buffers, the output off-state current increases slightly.

**3.** When the LSI supply current is pulled up to a higher voltage in the CMOS I/O buffers, a flow current from the output pin to inside the LSI is generated.

**4.** The output short-circuit time is less than 1 second and for 1 LSI pin only.

**5.** The pull-up and pull-down resistances vary depending on the input and output voltages.

**6.** All the buffers with the same output drive capability have the same specifications.

**7.** 2.00 mA for a buffer with a 5 kΩ pull-up resistor.

**Remarks 1.** The + and – symbols attached to the current values in the table indicate the direction of the current. The symbol is + when the current is flowing into the device, and – when flowing out of the device.

**2.** Blanks in the table indicate that the values are undergoing evaluation.

# AC Characteristics

The values in the table below refer to when the supply voltage of the internal gate array block is 3.3 V.

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Toggle frequency | $f_{tog}$ | Internal toggle F/F (fanout = 2) | | 670 | | | MHz |
| Transfer delay time | $t_{PD}$ | Internal gates | Fanout = 1, wiring length 0 mm | | 94 | | ps |
| | | | Fanout = 1, standard wiring length | | 131 | | ps |
| | | | Standard load | | 108 | | ps |
| | | Internal gates, power gates, 2NAND | Fanout = 1, standard wiring length | | 107 | | ps |
| | | | Standard load | | 94 | | ps |
| | | Input buffers | Fanout = 1, standard wiring length | | 229 | | ps |
| | | | Standard load | | 222 | | ps |
| | | Output buffer (FO01) $C_L$ = 15 pF | | | 1396 | | ps |
| Output rise time | $t_r$ | Output buffer (FO01) $C_L$ = 15 pF | | | 2391 | | ps |
| Output fall time | $t_f$ | Output buffer (FO01) $C_L$ = 15 pF | | | 1872 | | ps |

**Remark** Standard load: Fanout = 2, wiring length 0 mm
Standard wiring length: 145 $\mu$m/1 pin pair

# DEVELOPMENT TOOLS

## Easy interface with your EWS or PC

Users can choose the following tools to their environment.

**Caution Some functions may not be supported. Make it sure before use.**

**OPENCAD™ V5.5 Configuration Tool**

| Function | NEC Tool | Interface Data | Commercially Available Tool Interface |
|---|---|---|---|
| Function simulator | – | • Net list PWC/EDIF (2.0.0)/ Verilog™ HDL<br>• Test pattern ALBA<br>• Delay data file<br>• Timing limit | ModelSim™/Verilog-XL™/ NC-Verilog™/VCS™ |
| Schmatic editor | Vdraw™ | | – |
| Logic synthesis | – | | Design Compiler® |
| Gate-level simulator Note 1 | V. sim™ | | ModelSim/Verilog-XL/NC-Verilog/VCS |
| Formal verifier | – | | Formality®/Tuxedo™-LEC/ Conformal™-LEC |
| STA Note 1 | Tiara | | PrimeTime® |
| Fault simulation Note 2 | C. FGRADE™ | | – |
| Design for test | TESTACT/NEC_SCAN/ NEC_BSCAN/NEC_BIST/ TESTBUS | | DFT Compiler/TetraMAX™ |
| Floor planner Note 3 | CBIC : ace_floorplan G/A : Galet | | – |
| Layout and wiring Note 3 | Galet | | Silicon Ensemble™ (Only CBIC) |

**Notes 1.** Sign-off tool
**2.** Tool not supported in the HP™ version
**3.** Individually supported tool

**Remark** Platform : SUN™ (Solaris™)/HP (HP-UX™)
GUI : X11R5/Motif™ 1.2

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