TEXAS INSTRUMENTS
Data sheet acquired from Harris Semiconductor
SCHS104A – Revised March 2002

CD40174B Types

CMOS Hex 'D'-Type Flip-Flop

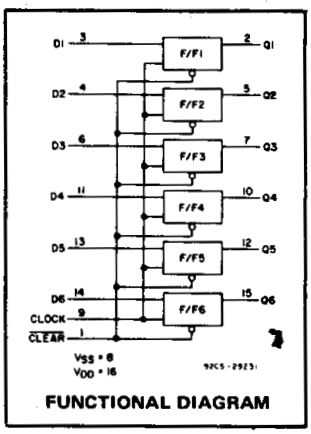
High-Voltage Types (20-Volt Rating)

■ CD40174B consists of six identical 'D'-type flip-flops having independent DATA inputs. The CLOCK and $\overline{\text{CLEAR}}$ inputs are common to all six units. Data is transferred to the Q outputs on the positive-going transition of the clock pulse. All six flip-flops are simultaneously reset by a low level on the $\overline{\text{CLEAR}}$ input.

The CD40174B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline package (NSR suffix), and in chip form (H suffix).

Features:

- 5-V, 10-V, and 15-V parametric rating
- Standardized symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package-temperature range): 1 V at V_{DD} = 5 V; 2 V at V_{DD} = 10 V; 2.5 V at V_{DD} = 15 V
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"



FUNCTIONAL DIAGRAM

Applications:

- Shift Registers
- Buffer/Storage Registers
- Pattern Generators

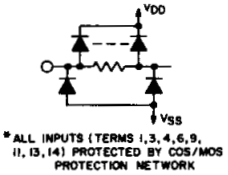
MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
Voltages referenced to V_{SS} Terminal) ..... −0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS ..... −0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −55°C to +100°C 500mW
For T_A = +100°C to +125°C ..... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)..... 100mW
OPERATING-TEMPERATURE RANGE (T_A) .....−55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) .....−65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C

TRUTH TABLE FOR 1 OF 6 FLIP-FLOPS

INPUTS			OUTPUT
CLOCK	DATA	$\overline{\text{CLEAR}}$	Q
⌒	0	1	0
⌒	1	1	1
⌣	X	1	NC
X	X	0	0

1 = High Level X = Don't Care
0 = Low Level NC = No Change



*ALL INPUTS (TERMS 1,3,4,6,9, 11, 13, 14) PROTECTED BY COS/MOS PROTECTION NETWORK

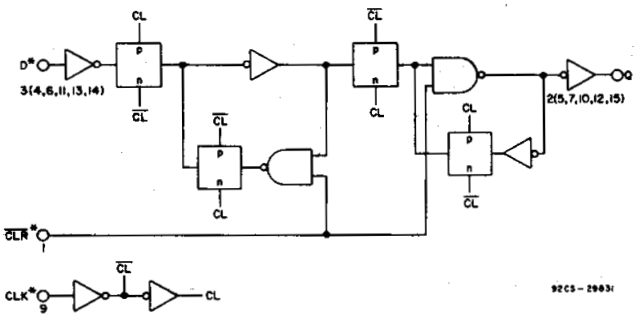


Fig. 1 – Logic diagram (1 of 6 flip-flops).

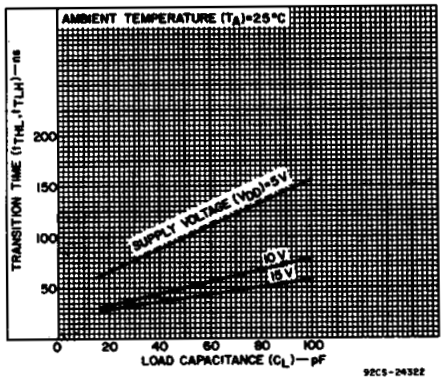
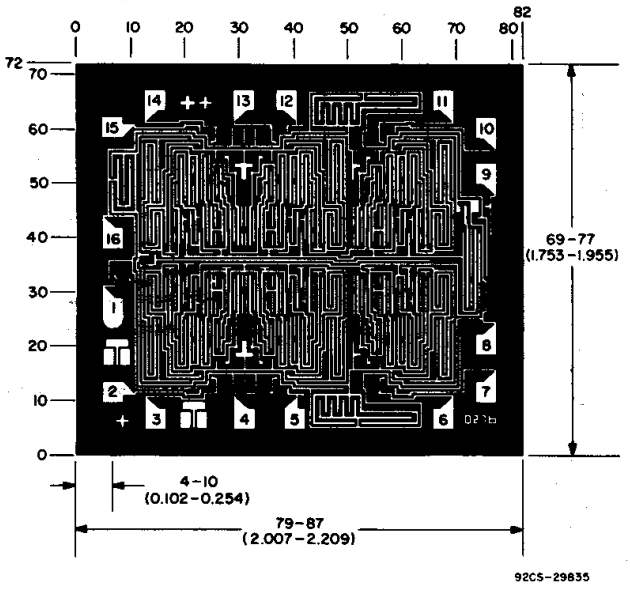


Fig. 2– Typical transition time as a function of load capacitance.

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS		UNITS
		Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	–	3	18	V
Data Setup Time, t_{SU}	5	40	–	ns
	10	20	–	
	15	10	–	
Data Hold Time, t_H	5	80	–	ns
	10	40	–	
	15	30	–	
Clock Input Frequency, f_{CL}	5	–	3.5	MHz
	10	dc	6	
	15		8	
Clock Input Rise or Fall Time, t_rCL, t_fCL	5	–	15	μs
	10	–	15	
	15	–	15	
Clock Input Pulse Width, t_{WL}, t_{WH}	5	130	–	ns
	10	60	–	
	15	40	–	
$\overline{\text{Clear}}$ Pulse Width, t_{WL}	5	100	–	ns
	10	50	–	
	15	40	–	
$\overline{\text{Clear}}$ Removal Time, t_{REM}	5	0	–	ns
	10	0	–	
	15	0	–	



Dimensions and pad layout for CD40174BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of −3 mils to +16 mils applicable to the nominal dimensions shown.

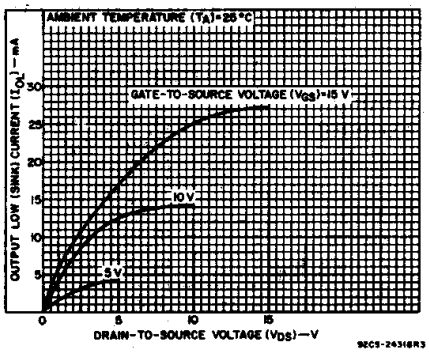


Fig. 3— Typical output low (sink) current characteristics.

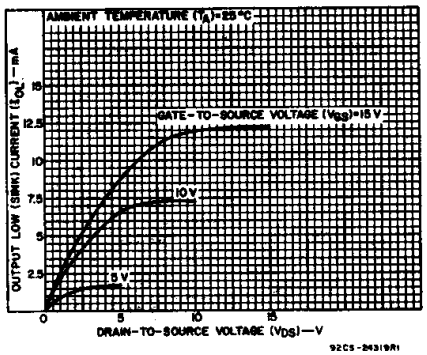


Fig. 4— Minimum output low (sink) current characteristics.

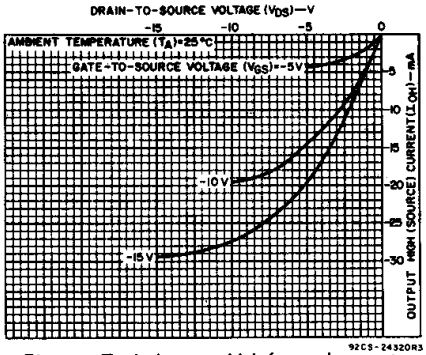


Fig. 5— Typical output high (source) current characteristics.

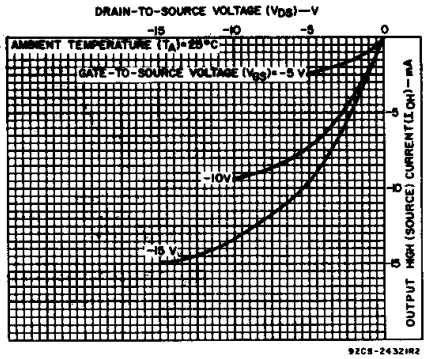


Fig. 6— Minimum output high (source) current characteristics.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	μA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6		
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8		
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–		0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$±10^{-5}$	±0.1	μA

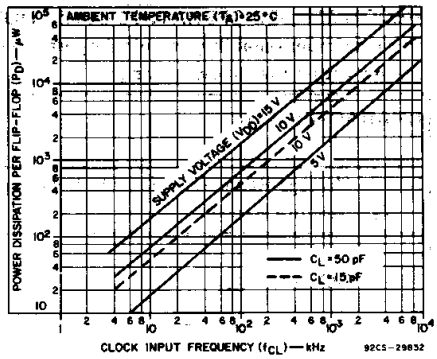


Fig. 7— Typical dynamic power dissipation as a function of CLOCK frequency.

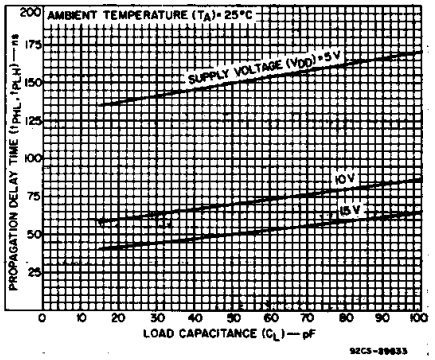


Fig. 8— Typical propagation delay time (CLOCK to OUTPUT) as a function of load capacitance.

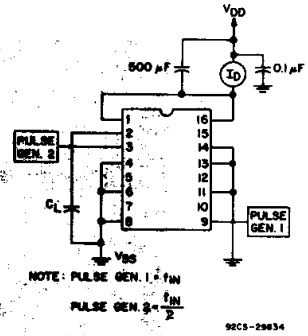


Fig. 9— Dynamic power dissipation test circuit.

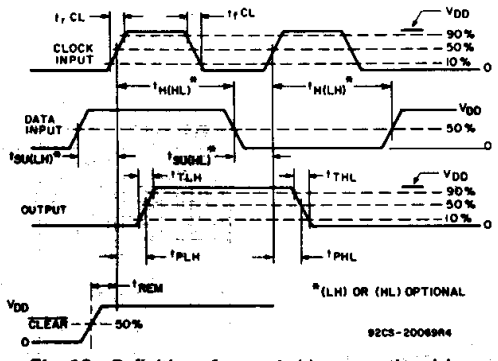


Fig. 10— Definition of setup, hold, propagation delay, and removal times.

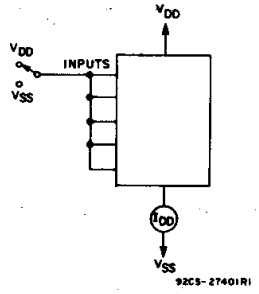


Fig. 11 — Quiescent device current test circuit.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C;
Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS			UNITS
		Min.	Typ.	Max.	
Propagation Delay Time Clock to Output, t_{PHL}, t_{PLH}	5	–	150	300	ns
	10	–	70	140	
	15	–	50	100	
$\overline{\text{Clear}}$ to Output, t_{PHL}	5	–	100	200	ns
	10	–	50	100	
	15	–	40	80	
Transition Time, t_{THL}, t_{TLH}	5	–	100	200	ns
	10	–	50	100	
	15	–	40	80	
Minimum Pulse Width, Clock, t_{WL}, t_{WH}	5	–	65	130	ns
	10	–	30	60	
	15	–	20	40	
$\overline{\text{Clear}}$, t_{WL}	5	–	50	100	ns
	10	–	25	50	
	15	–	20	40	
Minimum Data Setup Time, t_{SU}	5	–	20	40	ns
	10	–	10	20	
	15	–	0	10	
Minimum Data Hold Time, t_H	5	–	40	80	ns
	10	–	20	40	
	15	–	15	30	
Maximum Clock Frequency, f_{CL}	5	3.5	7	–	MHz
	10	6	12	–	
	15	8	16	–	
Maximum Clock Rise or Fall Time, t_rCL, t_fCL	5	15	–	–	μs
	10	15	–	–	
	15	15	–	–	
Input Capacitance, C_{IN} $\overline{\text{Clear}}$	–	–	25	40	pF
All other	–	–	5	7.5	
Minimum $\overline{\text{Clear}}$ Removal Time, t_{REM}	5	–	–40	0	ns
	10	–	–15	0	
	15	–	–10	0	

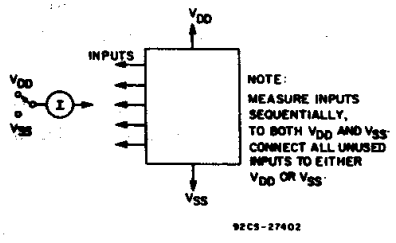


Fig. 12 – Input current test circuit.

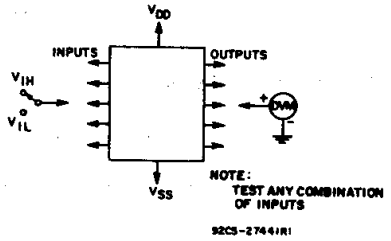
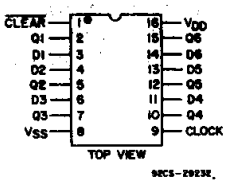


Fig. 13 – Input voltage test circuit.

TERMINAL ASSIGNMENT



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