BiCMOS-4, -4A, -5

Device	Integration (Gate)	Delay Time: Gate (ns)	Delay Time: Output Buffer (ns)	Delay Time: Input Buffer (ns)	Number of Buffers: Output	Number of Buffers: Input	Power Dissipation
BiCMOS-4 (1.5-micron CMOS and Bipolar with $f_T = 4$ GHz)							
μPD67001	624	0.8	3	1.2	64	64	18 μW/MHz/cell (F/O = 3, L = 3 mm)
μPD67010	1124	0.8	3	1.2	84	84	
μPD67020	2248	0.8	3	1.2	120	120	
μPD67030	3140	0.8	3	1.2	140	140	
BiCMOS-4A (1.5-micron CMOS and Bipolar with $f_T = 4$ GHz)							
μPD67060	6372	0.8	3.0	1.2	180	180	18 μW/MHz/gate (F/O = 3, L = 3 mm)
μPD67100	10,348	0.8	3.0	1.2	228	228	
BiCMOS-5 (1.2-micron CMOS and Bipolar with $f_T = 8$ GHz)							
μPD67021	2208	0.3	1.3 (ECL) 1.9 (TTL)	1.8 (ECL) 0.9 (TTL)	80	80	48 μW/MHz/gate
μPD67031	3240	0.3	1.3 (ECL) 1.9 (TTL)	1.8 (ECL) 0.9 (TTL)	96	96	
μPD67050	5320	0.3	1.3 (ECL) 1.9 (TTL)	1.8 (ECL) 0.9 (TTL)	124	124	
μPD67070	7216	0.3	1.3 (ECL) 1.9 (TTL)	1.8 (ECL) 0.9 (TTL)	148	148	
μPD67101	10,152	0.3	1.3 (ECL) 1.9(TTL)	1.8 (ECL) 0.9 (TTL)	176	176	
μPD67240	24,528	0.3	1.3 (ECL) 1.9 (TTL)	1.8 (ECL) 0.9 (TTL)	272	272	

Notes: (1) Number of macros: 146; 180 (BiCMOS-5)
(2) Ambient temperature: 0 to 85°C; 0 to 70°C (BiCMOS-5)
(3) Power source: 5 V ±0.5 V; BiCMOS-5: 5 V ±5% CMOS/TTL; -5.2 V ±5% ECL-10KH; -4.5 V ± 0.3 V ECL-100K
(4) Input/output interface: CMOS, ALS-TTL (input/output) and ECL-10KH, -100K for BiCMOS-5

Standard Cell-4, -5

Device	Integration (Gate)	Delay Time: Gate (ns)	Delay Time: Output Buffer (ns)	Delay Time: Input Buffer (ns)	Number of Buffers: Input/Output Total	Power Dissipation	RAM	ROM
SC-4 (1.5-micron CMOS)								
μPD91000	Up to 17,000	1.4	4	2	256	15 μW/gate	1 port: 64 Kb max; 2 port: 16 Kb max	None
μPD92000	Up to 17,000	1.4	4	2	256	15 μW/MHz/gate	1 port: 64 Kb max; 2 port: 16 Kb max	256 Kb max
SC-5 (1.2-micron CMOS)								
μPD93000	Up to 60,000	1.0	2.5	2.0	280	18 μW/MHz/gate	128 Kb max	1 Mb max

Notes: (1) Number of macros: 180
(2) Ambient temperature: -40 to +85°C
(3) Power source: 5 V ±10% for CMOS; 5 V ±5% for TTL
(4) Input/output interface: TTL, CMOS compatible
(5) Technology: silicon-gate CMOS, two-layer Al metallization