

# MOS INTEGRATED CIRCUIT

## $\mu$ PD6900

### 8 bit D/A Converter for Video Signal Processing

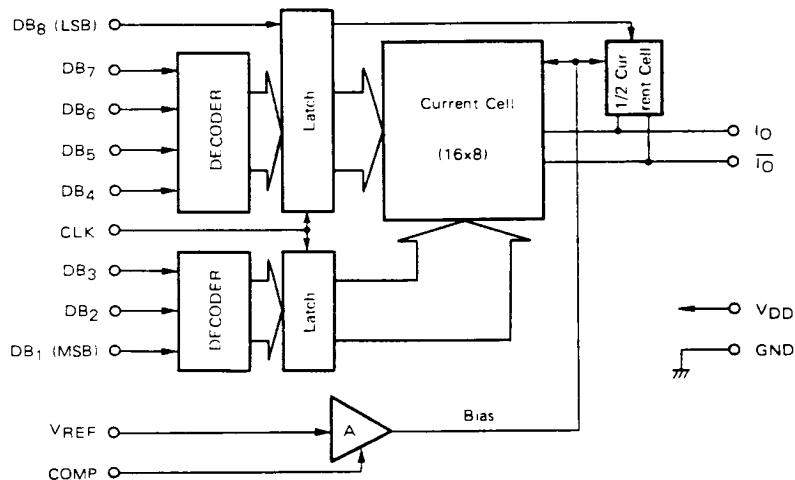
#### CMOS LSI

The  $\mu$ PD6900 is an 8 bit D/A converter for use in video applications. The high-speed CMOS processing technology and the matrix current cell method adopted for this CMOS device have enabled fast conversion rates to be achieved. Conversion rates of up to 20 Msp/s can be attained while operating at low power consumption, making this device ideal for a wide range of applications including digital TV systems and video systems. ★

#### FEATURES

- Resolution : 8 bits
- Conversion rate : 20 Msp/s
- Linearity :  $\pm 1/2$  LSB TYP.
- Reference voltage : 2.0 V TYP.
- Power supply voltage : +5 V single
- Low power consumption (150 mW TYP.)
- TTL compatible (Digital inputs)
- 22 pin plastic DIP, and 24 pin plastic SOP (375 mil)

#### BLOCK DIAGRAM



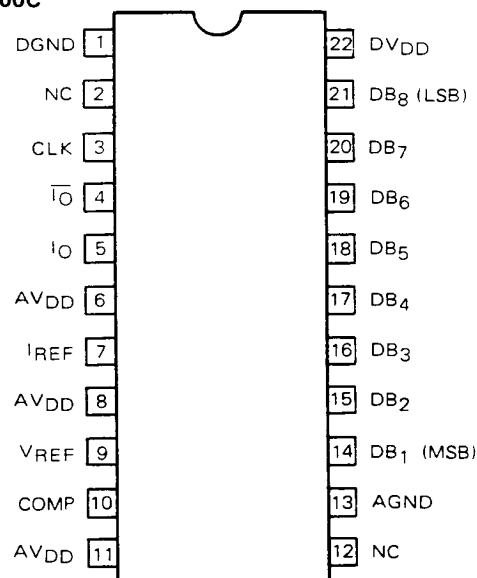
#### ORDERING INFORMATION

| ORDERING CODE | PACKAGE                      |
|---------------|------------------------------|
| $\mu$ PD6900C | 22 pin plastic DIP (400 mil) |
| $\mu$ PD6900G | 24 pin plastic SOJ (375 mil) |

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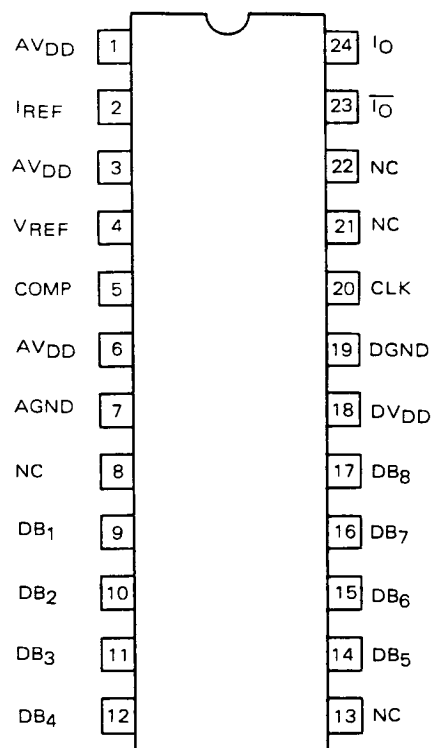
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**CONNECTION DIAGRAM (Top View)****μPD6900C**

|    |                  |                               |
|----|------------------|-------------------------------|
| 1  | DGND             | Digital GND                   |
| 2  | NC               | No connection                 |
| 3  | CLK              | Sampling clock input          |
| 4  | $\overline{I_O}$ | Complementary current output  |
| 5  | $I_O$            | Current output                |
| 6  | AV <sub>DD</sub> | Analog power supply           |
| 7  | I <sub>REF</sub> | Full-scale current adjustment |
| 8  | AV <sub>DD</sub> | Analog power supply           |
| 9  | V <sub>REF</sub> | Reference voltage input       |
| 10 | COMP             | Amp compensation              |
| 11 | AV <sub>DD</sub> | Analog power supply           |
| 12 | NC               | No connection                 |
| 13 | AGND             | Analog GND                    |
| 14 | DB <sub>1</sub>  | Digital input (MSB)           |
| 15 | DB <sub>2</sub>  | Digital input (2nd)           |
| 16 | DB <sub>3</sub>  | Digital input (3rd)           |
| 17 | DB <sub>4</sub>  | Digital input (4th)           |
| 18 | DB <sub>5</sub>  | Digital input (5th)           |
| 19 | DB <sub>6</sub>  | Digital input (6th)           |
| 20 | DB <sub>7</sub>  | Digital input (7th)           |
| 21 | DB <sub>8</sub>  | Digital input (LSB)           |
| 22 | DV <sub>DD</sub> | Digital power supply          |

**μPD6900G**



|    |                  |                               |
|----|------------------|-------------------------------|
| 1  | AV <sub>DD</sub> | Analog power supply           |
| 2  | I <sub>REF</sub> | Full-Scale current adjustment |
| 3  | AV <sub>DD</sub> | Analog power supply           |
| 4  | V <sub>REF</sub> | Reference voltage input       |
| 5  | COMP             | Amp phase compensation        |
| 6  | AV <sub>DD</sub> | Analog power supply           |
| 7  | AGND             | Analog GND                    |
| 8  | NC               | No connection                 |
| 9  | DB <sub>1</sub>  | Digital input (MSB)           |
| 10 | DB <sub>2</sub>  | Digital input (2nd)           |
| 11 | DB <sub>3</sub>  | Digital input (3rd)           |
| 12 | DB <sub>4</sub>  | Digital input (4th)           |
| 13 | NC               | No connection                 |
| 14 | DB <sub>5</sub>  | Digital input (5th)           |
| 15 | DB <sub>6</sub>  | Digital input (6th)           |
| 16 | DB <sub>7</sub>  | Digital input (7th)           |
| 17 | DB <sub>8</sub>  | Digital input (LSB)           |
| 18 | DV <sub>DD</sub> | Digital power supply          |
| 19 | DGND             | Digital GND                   |
| 20 | CLK              | Sampling clock input          |
| 21 | NC               | No connection                 |
| 22 | NC               | No connection                 |
| 23 | $\overline{I_O}$ | Complementary current output  |
| 24 | I <sub>O</sub>   | Current output                |

**ABSOLUTE MAXIMUM RATINGS ( $T_a = 25\text{ }^{\circ}\text{C}$ )**

|                             |                                |                    |
|-----------------------------|--------------------------------|--------------------|
| Power supply voltage        | -0.3 to +7.0                   | V                  |
| Input terminal voltage      | -0.3 to $V_{DD}+0.3$           | V                  |
| Output terminal voltage     | -0.3 to $V_{DD}+0.3$           | V                  |
| Analog power supply voltage | $DV_{DD}-0.3$ to $DV_{DD}+0.3$ | V                  |
| Analog GND voltage          | DGND-0.3 to DGND+0.3           | V                  |
| Operating temperature range | -20 to +75                     | $^{\circ}\text{C}$ |
| Storage temperature range   | -40 to +125                    | $^{\circ}\text{C}$ |

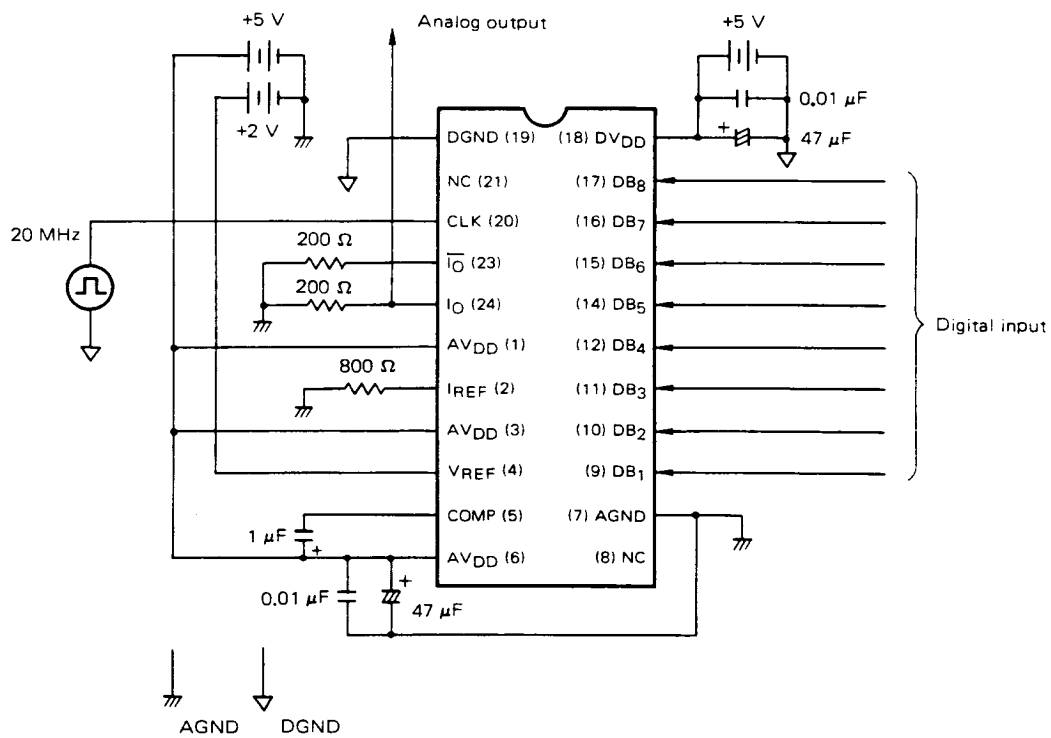
**RECOMMENDED OPERATING CONDITIONS ( $T_a = -20$  to  $+75\text{ }^{\circ}\text{C}$ )**

| CHARACTERISTIC                        | SYMBOL            | MIN. | TYP. | MAX. | UNIT          | TEST CONDITION |
|---------------------------------------|-------------------|------|------|------|---------------|----------------|
| Power supply voltage                  | $V_{DD}$          | 4.5  | 5.0  | 5.5  | V             |                |
| Reference voltage                     | $V_{REF}$         | 1.8  | 2.0  | 2.2  | V             |                |
| Reference resistance                  | $R_{REF}$         |      | 800  |      | $\Omega$      |                |
| Sampling clock                        | $f_{\text{samp}}$ | DC   |      | 20   | MHz           |                |
| Sampling clock low level pulse width  | $t_{\text{PWL}}$  | 10   |      |      | ns            |                |
| Sampling clock high level pulse width | $t_{\text{PWH}}$  | 10   |      |      | ns            |                |
| Data set up time                      | $t_S$             | 20   |      |      | ns            |                |
| Data hold time                        | $t_H$             | 10   |      |      | ns            |                |
| Digital input high level              | $V_{IH}$          | 2.7  |      |      | V             |                |
| Digital input low level               | $V_{IL}$          |      |      | 0.4  | V             |                |
| Compensation capacity                 | $C_{\text{COMP}}$ | 1.0  |      |      | $\mu\text{F}$ |                |

**ELECTRICAL CHARACTERISTICS ( $T_a = -20$  to  $+75\text{ }^{\circ}\text{C}$ ,  $V_{DD} = 5\text{ V} \pm 0.5\text{ V}$ ,  $f_{\text{samp}} = 20\text{ MHz}$ )**

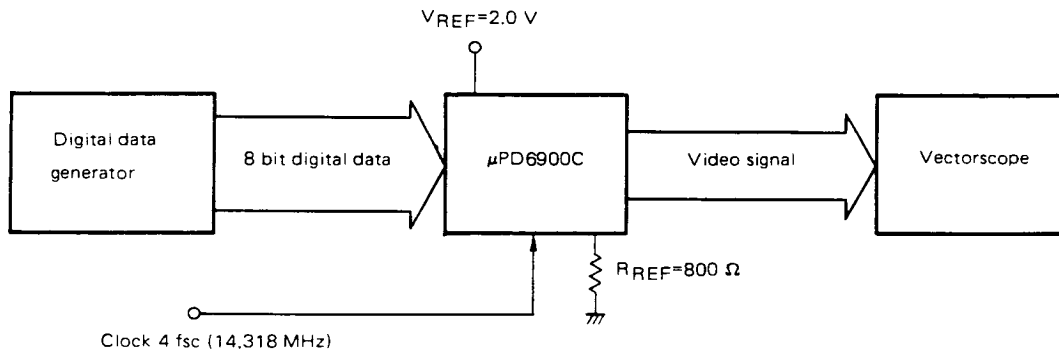
| CHARACTERISTIC             | SYMBOL           | MIN. | TYP.      | MAX.    | UNIT          | TEST CONDITION                                                                     |
|----------------------------|------------------|------|-----------|---------|---------------|------------------------------------------------------------------------------------|
| Power supply current       | $I_{DD}$         |      | 30        | 50      | mA            | $V_{DD}=5.0\text{ V}$                                                              |
| Resolution                 | RES              |      | 8         |         | bit           |                                                                                    |
| Non-linearity error        | NL               |      | $\pm 1/2$ | $\pm 1$ | LSB           | $T_a=0$ to $60\text{ }^{\circ}\text{C}$ ,<br>$V_{DD}=5\text{ V} \pm 0.25\text{ V}$ |
| Differential non-linearity | DNL              |      | $\pm 1/2$ | $\pm 1$ | LSB           | $T_a=0$ to $60\text{ }^{\circ}\text{C}$ ,<br>$V_{DD}=5\text{ V} \pm 0.25\text{ V}$ |
| Differential gain          | DG               |      | 3         | 4       | %             | $f_{\text{samp}}=14.318\text{ MHz}$ ,<br>$V_{DD}=5\text{ V} \pm 0.25\text{ V}$     |
| Differential phase         | DP               |      | 1         | 3       | deg           | $f_{\text{samp}}=14.318\text{ MHz}$ ,<br>$V_{DD}=5\text{ V} \pm 0.25\text{ V}$     |
| Output compliance          | $V_O$            | 2.5  | 3.0       |         | V             | $V_{DD}=5.0\text{ V}$                                                              |
| Analog output delay time   | $t_D$            |      | 40        |         | ns            |                                                                                    |
| Settling time              | $t_{\text{SET}}$ |      | 40        |         | ns            |                                                                                    |
| Full-scale current         | $I_{FS}$         | 9    | 10        | 11      | mA            | $V_{REF}=2.0\text{ V}$ , $R_{REF}=800\text{ }\Omega$                               |
| Zero-scale offset current  | $I_{ZS}$         |      |           | 20      | $\mu\text{A}$ | $V_{REF}=2.0\text{ V}$ , $R_{REF}=800\text{ }\Omega$                               |
| Digital input capacitance  | $C_{DI}$         |      |           | 30      | pF            |                                                                                    |
| Digital input current      | $I_I$            |      |           | 10      | $\mu\text{A}$ |                                                                                    |

TEST CIRCUIT



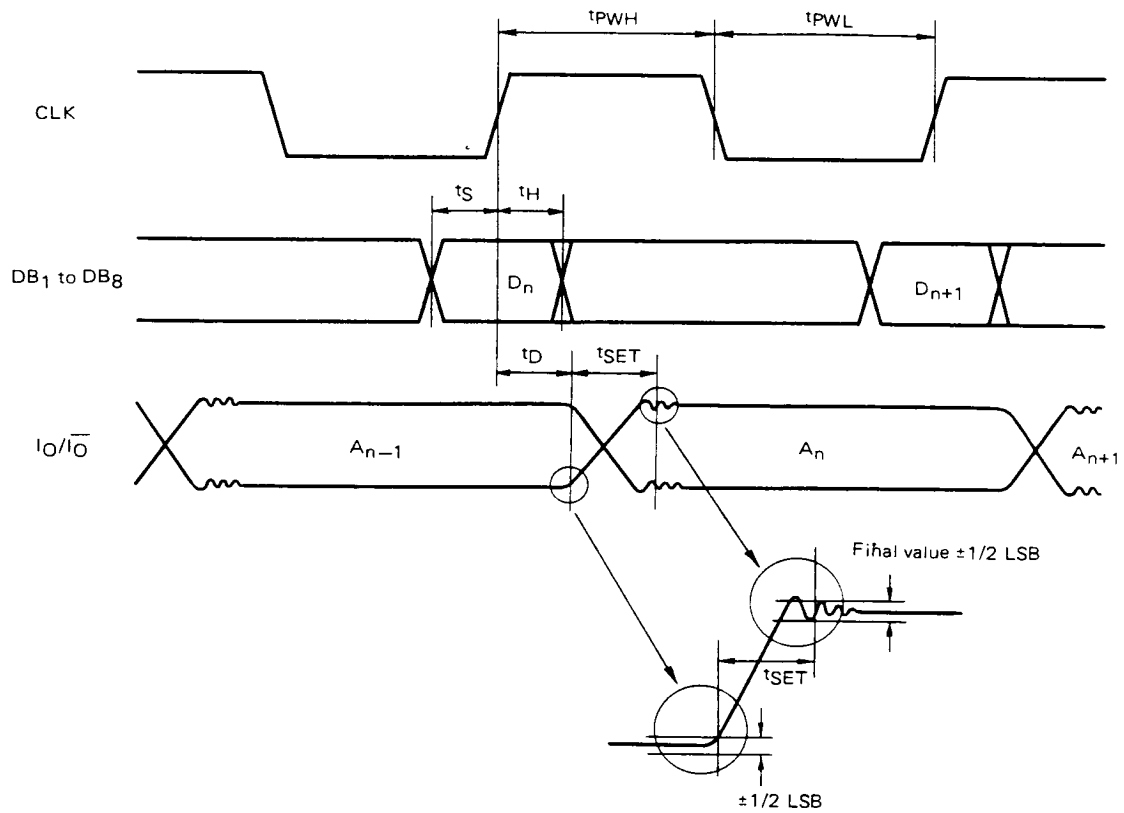
( ) shows pins number of μPD6900G.

DG AND DP MEASUREMENT BLOCK DIAGRAM



The data from the digital data generator is 40 IRE lamp signal (NTSC) digital data.

**TIMING CHART**



## PIN DESCRIPTIONS

( / ) shows pins number. RIGHT one is μPD6900G's and LEFT one is μPD6900C's terminal number.

|                              |                                    |
|------------------------------|------------------------------------|
| DGND (Pin 1/19)              | Digital system ground              |
| AGND (Pin 13/7)              | Analog system ground               |
| DVDD (Pin 22/18)             | Digital system power supply (+5 V) |
| AVDD (Pins 6, 8, 11/1, 3, 6) | Analog system power supply (+5 V)  |

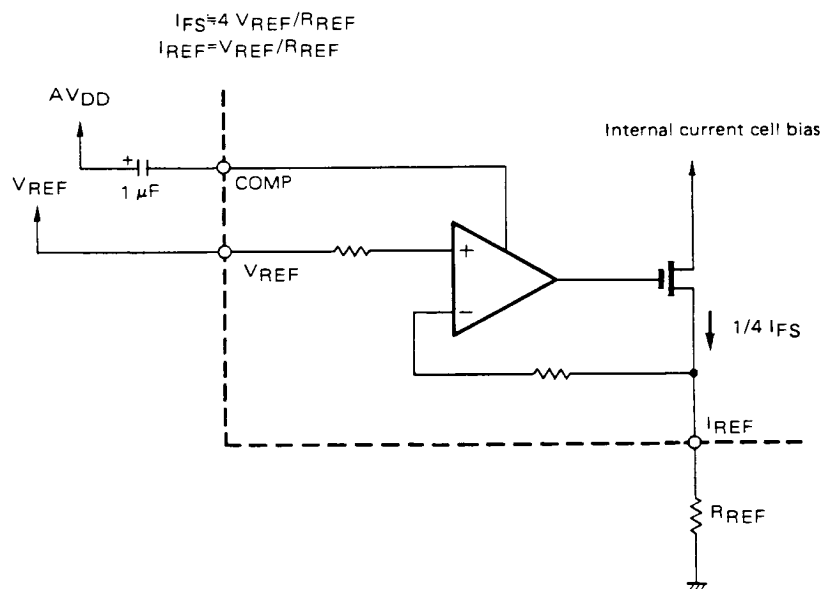
The digital system power supply and ground is isolated from the analog system power supply and ground in the IC as a precaution against noise. The ground and power supply lines are also isolated on the circuit boards, the analog ground being as wide as possible for better stability.

Insert by-pass capacitors of about 0.01 μF and 47 μF between the analog power line and analog ground, and also between the digital power line and digital ground. These capacitors should be connected as close as possible to the μPD6900C pins. Supply the digital system power from the analog power line through the low path filter to prevent from lurch up.

|                            |                                   |
|----------------------------|-----------------------------------|
| I <sub>REF</sub> (Pin 7/2) | Full-scale current adjustment pin |
| V <sub>REF</sub> (Pin 9/4) | Reference voltage input pin       |

These pins are used in adjustment of the analog output current (full-scale current).

The analog output current (full-scale current I<sub>FS</sub>) is set by the reference voltage V<sub>REF</sub> and the reference resistance R<sub>REF</sub> connected between the I<sub>REF</sub> pin and analog ground.



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The recommended reference voltage and reference resistance values are  $V_{REF} = 2.0\text{ V}$  and  $R_{REF} = 800\ \Omega$  respectively. The output analog current  $I_{FS}$  in this case will be 10 mA. Also connect by-pass capacitors of about  $0.01\ \mu\text{F}$  and  $47\ \mu\text{F}$  between the  $V_{REF}$  pin and GND in the same way as the by-pass capacitors connected to the power pins.

**COMP (Pin 10/5)** Phase compensation capacitor connection

A capacitor for phase compensation of the internal amplifier is connected to this pin. Connect a  $1.0\ \mu\text{F}$  capacitor between this pin and analog  $V_{DD}$ .

**DB<sub>1</sub> to DB<sub>8</sub> (Pins 14 thru 21/9 thru 12, 14 thru 17)** Digital data input pins

DB<sub>1</sub> to DB<sub>8</sub> are the 8 bit digital data input pins. The code format is binary, and the input voltage level is TTL compatible.

| Digital input code       |                 |                 |                 |                 |                 |                 |                          | Analog output current |
|--------------------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|--------------------------|-----------------------|
| DB <sub>1</sub><br>(MSB) | DB <sub>2</sub> | DB <sub>3</sub> | DB <sub>4</sub> | DB <sub>5</sub> | DB <sub>6</sub> | DB <sub>7</sub> | DB <sub>8</sub><br>(LSB) |                       |
| 0                        | 0               | 0               | 0               | 0               | 0               | 0               | 0                        | 0 note                |
| 0                        | 0               | 0               | 0               | 0               | 0               | 0               | 1                        | $1/256\ I_{FS}$       |
| ⋮                        | ⋮               | ⋮               | ⋮               | ⋮               | ⋮               | ⋮               | ⋮                        | ⋮                     |
| 1                        | 1               | 1               | 1               | 1               | 1               | 0               | 1                        | $253/256\ I_{FS}$     |
| 1                        | 1               | 1               | 1               | 1               | 1               | 1               | 0                        | $254/256\ I_{FS}$     |
| 1                        | 1               | 1               | 1               | 1               | 1               | 1               | 1                        | $255/256\ I_{FS}$     |

**note :** Excluding offset current

Digital data (DB<sub>1</sub> to DB<sub>8</sub>) is latched by the rising edge of the sampling clock, and converted to corresponding analog outputs.

**CLK (Pin 3/20)** Sampling clock input pin

Digital data is latched by the rising edge of the clock signal applied to the sampling clock input pin, and is subsequently converted to analog outputs. The maximum clock frequency is 20 MHz.



|                  |            |                                        |
|------------------|------------|----------------------------------------|
| $I_O$            | (Pin 5/24) | Analog signal output pin               |
| $\overline{I_O}$ | (Pin 4/23) | Analog signal complementary output pin |

★

These two pins are current output pins. The full-scale output current is determined by the reference resistance  $R_{REF}$  and reference voltage  $V_{REF}$ .

$$I_{FS} = I_O + \overline{I_O} = 4 V_{REF}/R_{REF}$$

$\overline{I_O}$  is the complementary output pin of  $I_O$ . The added output current from the  $I_O$  and  $\overline{I_O}$  pins becomes the full-scale current in accordance with the above equation. Analog output current can be easily converted to an analog output voltage by connecting a resistance between the  $I_O$  or  $\overline{I_O}$  pin and analog ground. In this case resistances must also be connected to the  $I_O$  and  $\overline{I_O}$  pins.

NC (Pins 2 and 12/8, 3, 21, 22) No connection

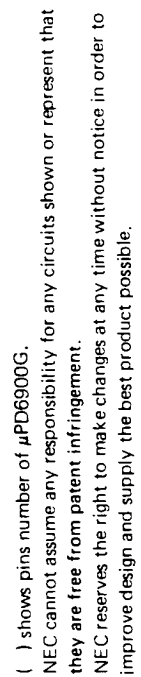
These pins may be connected to analog ground.

#### Example of an Application Circuit

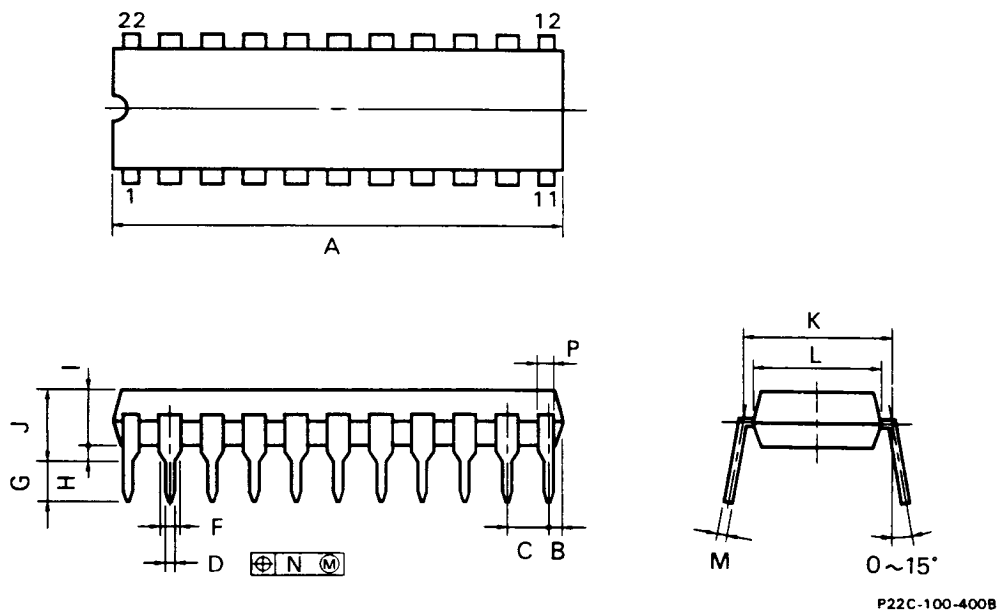
This example shows D/A conversion of video signal (NTSC) digital data at a conversion rate of four times the subcarrier frequency ( $4 f_{sc}$ ) to obtain the video output signal.

The analog output signal is passed via a low-pass filter (LPF) to a video amplifier (HA5195) to be amplified prior to output.

## 10



22PIN PLASTIC DIP (400 mil)

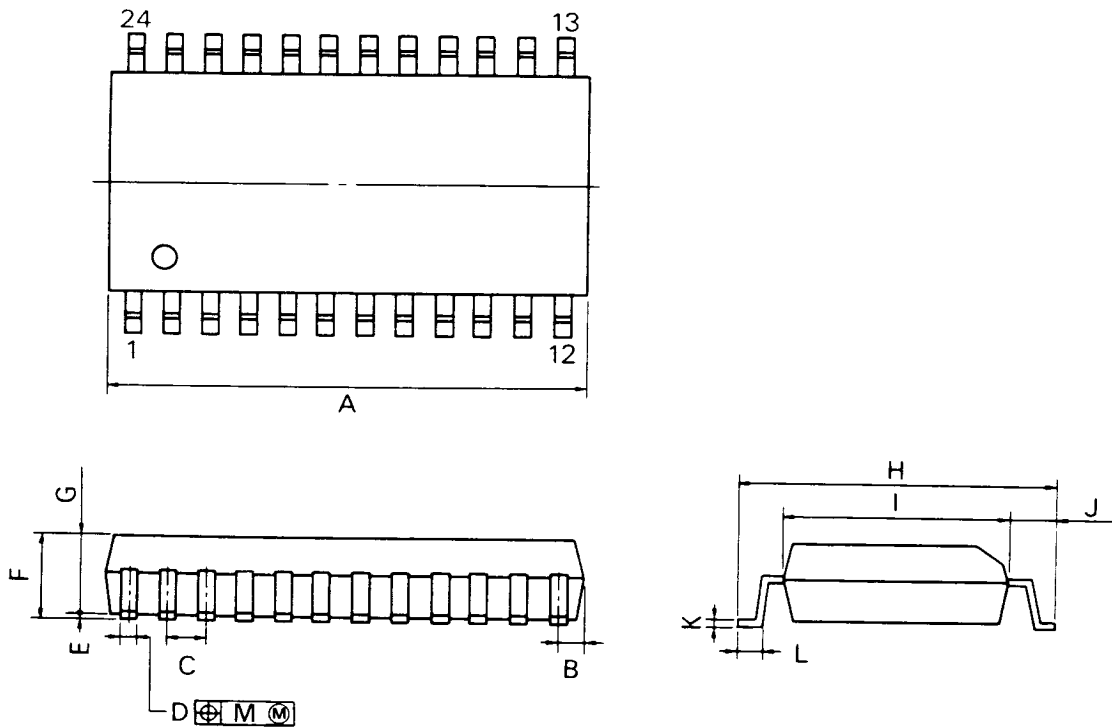


NOTES

- 1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.
- 2) Item "K" to center of leads when formed parallel.

| ITEM | MILLIMETERS     | INCHES            |
|------|-----------------|-------------------|
| A    | 27.94 MAX.      | 1.100 MAX.        |
| B    | 1.27 MAX.       | 0.050 MAX.        |
| C    | 2.54 (T.P.)     | 0.100 (T.P.)      |
| D    | 0.50 $\pm 0.10$ | 0.020 $\pm 0.004$ |
| F    | 1.2 MIN.        | 0.047 MIN.        |
| G    | 3.5 $\pm 0.3$   | 0.138 $\pm 0.012$ |
| H    | 0.51 MIN.       | 0.020 MIN.        |
| I    | 4.31 MAX.       | 0.170 MAX.        |
| J    | 5.72 MAX.       | 0.226 MAX.        |
| K    | 10.16 (T.P.)    | 0.400 (T.P.)      |
| L    | 8.6             | 0.339             |
| M    | 0.25 $\pm 0.10$ | 0.010 $\pm 0.004$ |
| N    | 0.25            | 0.01              |
| P    | 0.8 MIN.        | 0.031 MIN.        |

★ 24PIN PLASTIC SOP (375 mil)



P24GM-50-375B

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS                            | INCHES                                    |
|------|----------------------------------------|-------------------------------------------|
| A    | 15.54 MAX.                             | 0.612 MAX.                                |
| B    | 0.78 MAX.                              | 0.031 MAX.                                |
| C    | 1.27 (T.P.)                            | 0.050 (T.P.)                              |
| D    | 0.40 <sup>+0.10</sup> <sub>-0.05</sub> | 0.016 <sup>+0.004</sup> <sub>-0.003</sub> |
| E    | 0.1 <sup>+0.1</sup>                    | 0.004 <sup>+0.004</sup>                   |
| F    | 2.9 MAX.                               | 0.115 MAX.                                |
| G    | 2.50                                   | 0.098                                     |
| H    | 10.3 <sup>+0.3</sup>                   | 0.406 <sup>+0.013</sup> <sub>-0.012</sub> |
| I    | 7.2                                    | 0.283                                     |
| J    | 1.6                                    | 0.063                                     |
| K    | 0.15 <sup>+0.10</sup> <sub>-0.05</sub> | 0.006 <sup>+0.004</sup> <sub>-0.002</sub> |
| L    | 0.8 <sup>+0.2</sup>                    | 0.031 <sup>+0.009</sup> <sub>-0.008</sub> |
| M    | 0.12                                   | 0.005                                     |