

V853™
32-/16-BIT SINGLE-CHIP MICROCONTROLLER**DESCRIPTION**

The μPD70F3003 has a flash memory instead of the internal mask ROM of the μPD703003. This model is useful for small-scale production of a variety of application sets or early start of production since the program can be written and erased by the user even with the μPD70F3003 mounted on the board.

Functions in detail are described in the following user's manuals. Be sure to read these manuals when you design your systems.

V853 User's Manual-Hardware : U10913E

V850 Family™ User's Manual-Architecture: U10243E

FEATURES

- Compatible with μPD703003
 - Can be replaced with mask ROM model for mass production of application set
μPD70F3003 → μPD703003
- Internal flash memory: 128K bytes

Remark For differences among the products, refer to **1. DIFFERENCES AMONG PRODUCTS.**

ORDERING INFORMATION

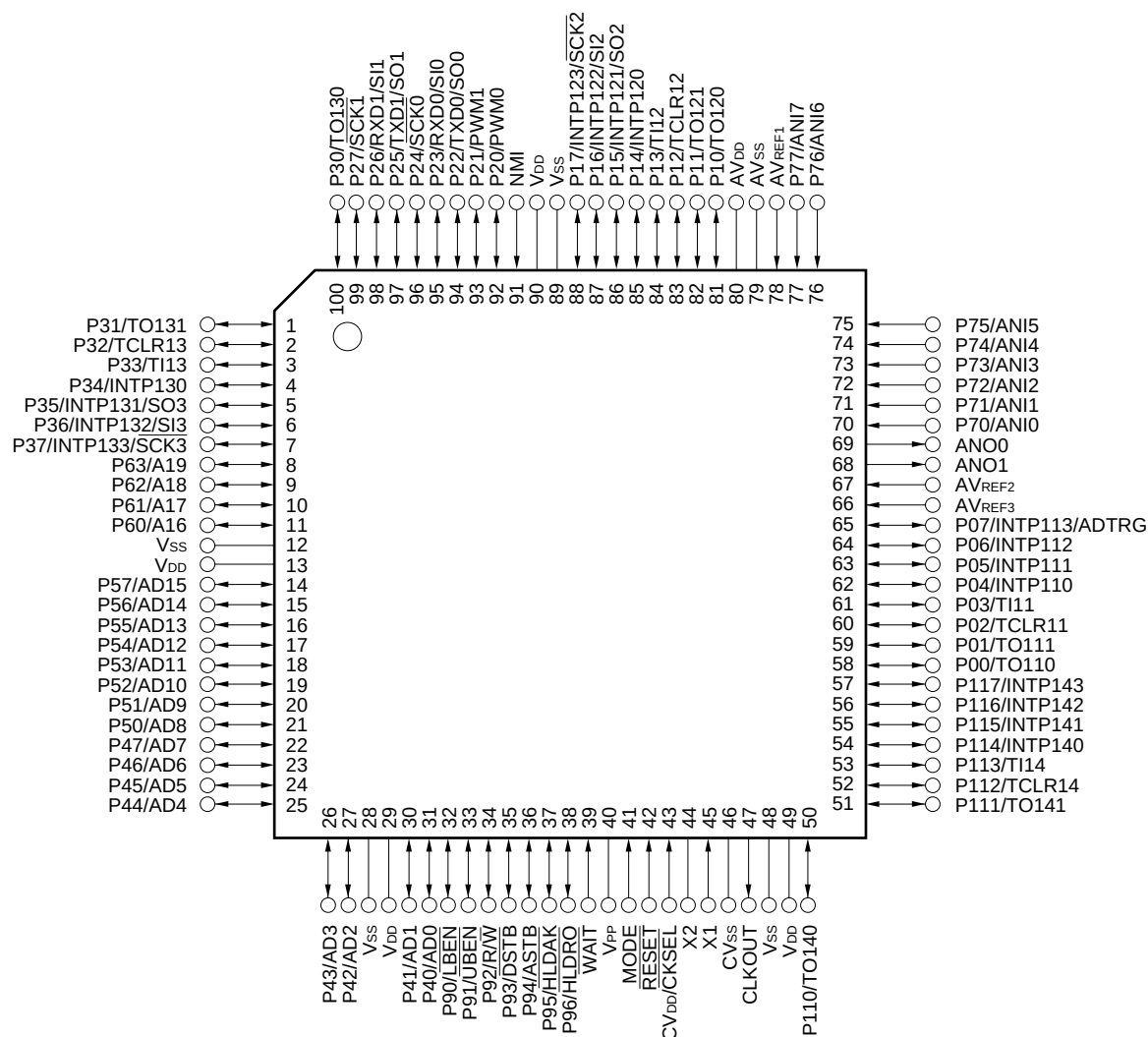
Part Number	Package
μPD70F3003GC-25-7EA	100-pin plastic QFP (fine pitch) (14 × 14 mm)

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

PIN CONFIGURATION (Top View)

- 100-pin plastic QFP (fine pitch) (14 × 14 mm)

μPD70F3003GC-25-7EA

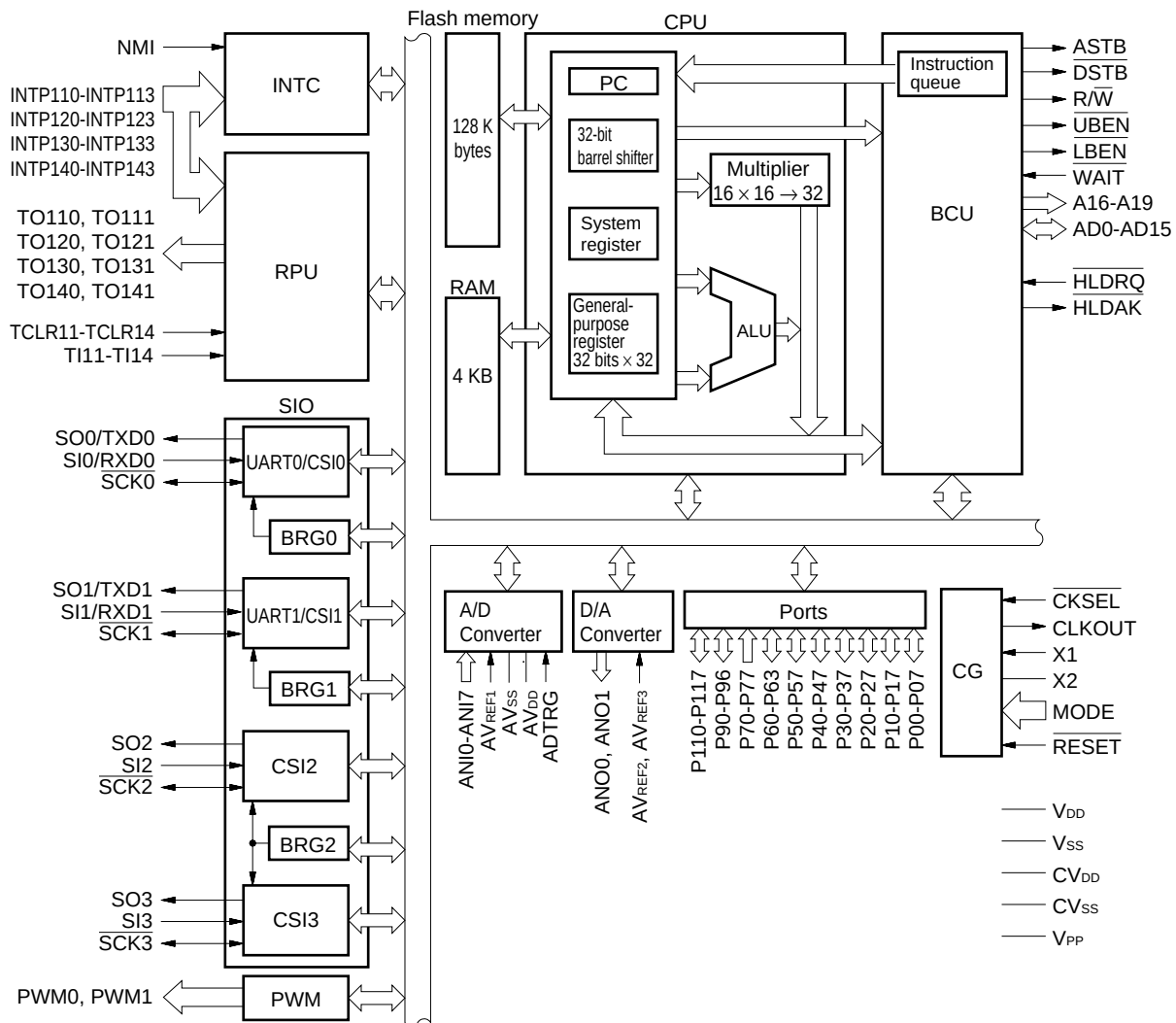


Caution Directly connect V_{PP} pin to V_{SS} pin except the case that μPD70F3003 is used in flash memory programming mode.

PIN NAMES

A16-A19	: Address Bus	P40-P47	: Port4
AD0-AD15	: Address/Data Bus	P50-P57	: Port5
ADTRG	: AD Trigger Input	P60-P63	: Port6
ANI0-ANI7	: Analog Input	P70-P77	: Port7
ANO0, ANO1	: Analog Output	P90-P96	: Port9
ASTB	: Address Strobe	P110-P117	: Port11
AV _{DD}	: Analog V _{DD}	PWM0, PWM1	: Pulse Width Modulation
AV _{REF1} -AV _{REF3}	: Analog Reference Voltage	<u>RESET</u>	: Reset
AV _{SS}	: Analog V _{SS}	R/ <u>W</u>	: Read/Write Status
CV _{DD}	: Power Supply for Clock Generator	RXD0, <u>PXD1</u>	: Receive Data
CV _{SS}	: Ground for Clock Generator	<u>SCK0-SCK3</u>	: Serial Clock
★ <u>CKSEL</u>	: Clock Select	SI0-SI3	: Serial Input
CLKOUT	: Clock Output	SO0-SO3	: Serial Output
<u>DSTB</u>	: Data Strobe	TO110, TO111,	: Timer Output
<u>HLD</u> AK	: Hold Acknowledge	TO120, TO121,	
<u>HLDRQ</u>	: Hold Request	TO130, TO131,	
INTP110-INTP113,	: Interrupt Request from Peripherals	TO140, TO141	
INTP120-INTP123,		TCLR11-TCLR14	: Timer Clear
INTP130-INTP133,		TI11-TI14	: Timer Input
INTP140-INTP143		TXD0, TXD1	: Transmit Data
<u>LBEN</u>	: Lower Byte Enable	<u>UBEN</u>	: Upper Byte Enable
MODE	: Mode	<u>WAIT</u>	: Wait
NMI	: Non-maskable Interrupt Request	X1, X2	: Crystal
P00-P07	: Port 0	V _{DD}	: Power Supply
P10-P17	: Port 1	V _{PP}	: Programming Power Supply
P20-P27	: Port 2	V _{SS}	: Ground
P30-P37	: Port 3		

INTERNAL BLOCK DIAGRAM



CONTENTS

1. DIFFERENCES AMONG PRODUCTS	6
2. PIN FUNCTIONS	7
2.1 Port Pins	7
2.2 Pins Other Than Port Pins	9
2.3 I/O Circuits of Pins and Recommended Connections of Unused Pins	11
3. PROGRAMMING FLASH MEMORY	14
3.1 Selecting Communication Mode	14
3.2 Flash Memory Programming Function	15
3.3 Connecting Dedicated Flash Programmer	15
4. ELECTRICAL SPECIFICATIONS	16
4.1 Normal Operation Mode	16
4.2 Flash Memory Programming Mode	37
5. PACKAGE DRAWING	39
6. RECOMMENDED SOLDERING CONDITIONS	40

★ 1. DIFFERENCES AMONG PRODUCTS

Parameter			μPD703003	μPD703003A	μPD703004A	μPD703025A	μPD70F3003	μPD70F3003A	μPD70F3025A
Internal ROM			Mask ROM				Flash memory		
			128K bytes		96K bytes	256K bytes	128K bytes		256K bytes
Internal RAM			4K bytes			8K bytes	4K bytes		8K bytes
Operation mode	Normal operation mode	Single chip mode	Provided						
		ROM-less mode	Provided	None			Provided	None	
	Flash memory programming mode		None				Provided		
V _{PP} pin			None				Provided		
CKC register value at reset			00H	MODE = 0: 03H MODE = 1: 00H			00H	MODE = 0: 03H MODE = 1: 00H	
Electrical specifications			Current consumption, etc. differs. (Refer to each product data sheets.)						
Others			Noise immunity and noise radiation differ because circuit scale and mask layout differ.						

2. PIN FUNCTIONS

2.1 Port Pins

(1/2)

Pin Name	I/O	Function	Shared with:
P00	I/O	Port 0 8-bit I/O port. Can be set in input or output mode in 1-bit units.	TO110
P01			TO111
P02			TCLR11
P03			TI11
P04			INTP110
P05			INTP111
P06			INTP112
P07			INTP113/ADTRG
P10	I/O	Port 1 8-bit I/O port. Can be set in input or output mode in 1-bit units.	TO120
P11			TO121
P12			TCLR12
P13			TI12
P14			INTP120
P15			INTP121/SO2
P16			INTP122/SI2
P17			INTP123/ $\overline{\text{SCK2}}$
P20	I/O	Port 2 8-bit I/O port. Can be set in input or output mode in 1-bit units.	PWM0
P21			PWM1
P22			TXD0/SO0
P23			RXD0/SI0
P24			$\overline{\text{SCK0}}$
P25			TXD1/SO1
P26			RXD1/SI1
P27			$\overline{\text{SCK1}}$
P30	I/O	Port 3 8-bit I/O port. Can be set in input or output mode in 1-bit units.	TO130
P31			TO131
P32			TCLR13
P33			TI13
P34			INTP130
P35			INTP131/SO3
P36			INTP132/SI3
P37			INTP133/ $\overline{\text{SCK3}}$
P40-P47	I/O	Port 4 8-bit I/O port. Can be set in input or output mode in 1-bit units.	AD0-AD7
P50-P57	I/O	Port 5 8-bit I/O port. Can be set in input or output mode in 1-bit units.	AD8-AD15

(2/2)

Pin Name	I/O	Function	Shared with:
P60-P63	I/O	Port 6 4-bit I/O port. Can be set in input or output mode in 1-bit units.	A16-A19
P70-P77	Input	Port 7 8-bit input port.	ANI0-ANI7
P90	I/O	Port 9 7-bit I/O port. Can be set in input or output mode in 1-bit units.	$\overline{\text{LBEN}}$
P91			$\overline{\text{UBEN}}$
P92			R/ $\overline{\text{W}}$
P93			$\overline{\text{DSTB}}$
P94			$\overline{\text{ASTB}}$
P95			$\overline{\text{HLD\!AK}}$
P96			$\overline{\text{HLD\!RQ}}$
P110	I/O	Port 11 8-bit I/O port. Can be set in input or output mode in 1-bit units.	TO140
P111			TO141
P112			TCLR14
P113			TI14
P114			INTP140
P115			INTP141
P116			INTP142
P117			INTP143

2.2 Pins Other Than Port Pins

(1/2)

Pin Name	I/O	Function	Shared with:
TO110	Output	Pulse signal output of timer 11-14	P00
TO111			P01
TO120			P10
TO121			P11
TO130			P30
TO131			P31
TO140			P110
TO141			P111
TCLR11	Input	External clear signal of timer 11-14	P02
TCLR12			P12
TCLR13			P32
TCLR14			P112
TI11	Input	External count clock of timer 11-14	P03
TI12			P13
TI13			P33
TI14			P113
INTP110	Input	External maskable interrupt reuest input and external capture trigger input of timer 11	P04
INTP111			P05
INTP112			P06
INTP113			P07/ADTRG
INTP120	Input	External maskable interrupt reuest input and external capture trigger input of timer 12	P14
INTP121			P15/SO2
INTP122			P16/S12
INTP123			P17/ $\overline{\text{SCK2}}$
INTP130	Input	External maskable interrupt reuest input and external capture trigger input of timer 13	P34
INTP131			P35/SO3
INTP132			P36/SI3
INTP133			P37/ $\overline{\text{SCK3}}$
INTP140	Input	External maskable interrupt reuest input and external capture trigger input of timer 14	P114
INTP141			P115
INTP142			P116
INTP143			P117
SO0	Output	Serial transmit data output of CSI0-CSI3 (3-wire)	P22/TXD0
SO1			P25/TXD1
SO2			P15/INTP121
SO3			P35/INTP131
SI0	Input	Serial receive data output of CSI0-CSI3 (3-wire)	P23/RXD0
SI1			P26/RXD1
SI2			P16/INTP122
SI3			P36/INTP132

(2/2)

Pin Name	I/O	Function	Shared with:
$\overline{\text{SCK0}}$	I/O	Serial clock I/O of CSI0-CSI3 (3-wire)	P24
$\overline{\text{SCK1}}$			P27
$\overline{\text{SCK2}}$			P17/INTP123
$\overline{\text{SCK3}}$			P37/INTP133
TXD0	Output	Serial transmit data output of UART0-UART1	P22/SO0
TXD1			P25/SO1
RXD0	Input	Serial receive data input of UART0-UART1	P23/SI0
RXD1			P26/SI1
PWM0	Output	Pulse signal output of PWM	P20
PWM1			P21
AD0-AD7	I/O	16-bit multiplexed address/data bus when external memory is connected	P40-P47
AD8-AD15			P50-P57
A16-A19	Output	High-order address bus when external memory is connected	P60-P63
$\overline{\text{LBEN}}$	Output	Low-order byte enable signal output of external data bus	P90
$\overline{\text{UBEN}}$		High-order byte enable signal output of external data bus	P91
$\text{R}/\overline{\text{W}}$	Output	External read/write status output	P92
$\overline{\text{DSTB}}$		External data strobe signal output	P93
ASTB		External address strobe signal output	P94
$\overline{\text{HLD\!AK}}$	Output	Bus hold acknowledge output	P95
$\overline{\text{HLDRQ}}$	Input	Bus hold request input	P96
ANI0-ANI7	Input	Analog input to A/D converter	P70-P77
ANO0, ANO1	Output	Analog output of D/A converter	—
NMI	Input	Non-maskable interrupt request input	—
CLKOUT	Output	System clock output	—
★ $\overline{\text{CKSEL}}$	Input	Input specifying operation mode of clock generator	CV _{DD}
$\overline{\text{WAIT}}$	Input	Control signal input inserting wait state in bus cycle	—
MODE	Input	Operation mode specification	—
$\overline{\text{RESET}}$	Input	System reset input	—
X1	Input	System clock resonator connection. Input external clock to X1 to supply external clock.	—
X2	—		—
ADTRG	Input	A/D converter external trigger input	P07/INTP113
AV _{REF1}	Input	Reference voltage input for A/D converter	—
AV _{REF2}	Input	Reference voltage input for D/A converter	—
AV _{REF3}			—
AV _{DD}	—	Positive power supply for A/D converter	—
AV _{SS}	—	Ground potential for A/D converter	—
CV _{DD}	—	Positive power supply for internal clock generator	$\overline{\text{CKSEL}}$
CV _{SS}	—	Ground potential for internal clock generator	—
V _{DD}	—	Positive power supply	—
V _{SS}	—	Ground potential	—
V _{PP}	—	High voltage application pin when program is written/verified	—

2.3 I/O Circuits of Pins and Recommended Connections of Unused Pins

Table 2-1 shows the I/O circuit type of each pin, and the recommended connections of the unused pins. Figure 2-1 shows a partially simplified diagram of each circuit.

When connecting a pin to V_{DD} or V_{SS} via resistor, use of a resistor of 1 to 10 k Ω is recommended.

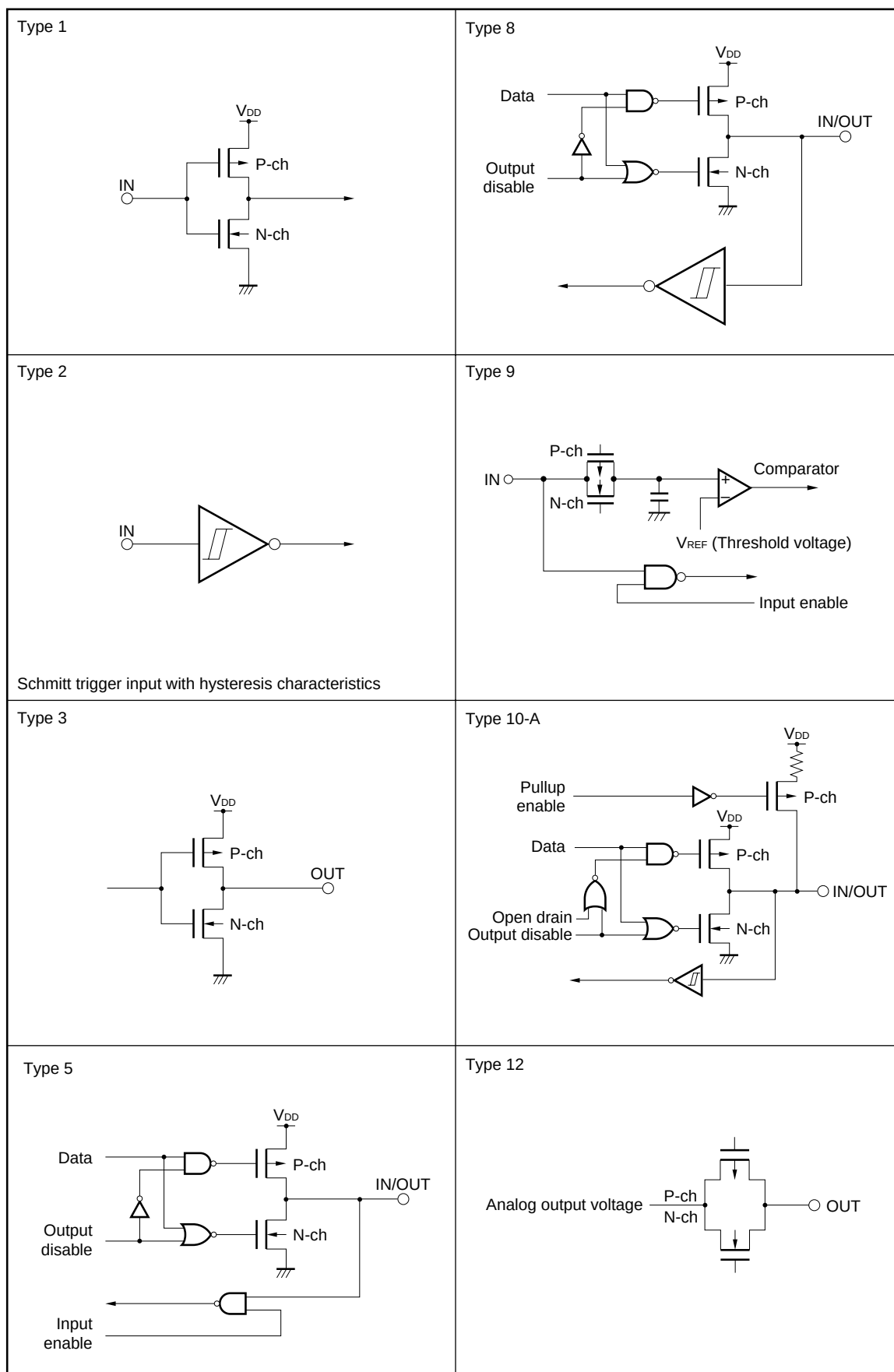
Table 2-1. I/O Circuit Types of Each Pin and Recommended Connections of Unused Pins (1/2)

Pin	I/O Circuit Type	Recommended Connections
P00/TO110, P01/TO111	5	Input : Individually connect to V_{DD} or V_{SS} via resistor. Output : Leave unconnected.
P02/TCLR11, P03/TI11, P04/INTP110-P07/INTP113/ADTRG	8	
P10-TO120, P11/TO121	5	
P12/TCLR12, P13/TI12 P14/INTP120 P15/INTP121/SO2 P16/INTP122/SI2 P17/INTP123/ $\overline{SCK2}$	8	
P20/PWM0, P21/PWM1 P22/TXD0/SO0	5	
P23/RXD0/SI0, P24/ $\overline{SCK0}$	8	
P25/TXD1/SO1	5	
P26/RXD1/SI1, P27/ $\overline{SCK1}$	8	
P30/TO130, P31/TO131	5	
P32/TCLR13, P33/TI13 P34/INTP130	8	
P35/INTP131/SO3 P36/INTP132/SI3 P37/INTP133/ $\overline{SCK3}$	10-A	
P40/AD0-P47/AD7 P50/AD8-P57/AD15 P60/A16-P63/A19	5	
P70/ANI0-P77/ANI7	9	
P90/ $\overline{LBEN}$ P91/ $\overline{UBEN}$ P92/ $\overline{R/\overline{W}}$ P93/ $\overline{DSTB}$ P94/ASTB P95/HLDAK P96/HLDRQ P110/TO140, P111/TO141	5	
P112/TCLR14, P113/TI14 P114/INTP140-P117/INTP143	8	

Table 2-1. I/O Circuit Types of Each Pin and Recommended Connections of Unused Pins (2/2)

Pin	I/O Circuit Type	Recommended Connections
ANO0, ANO1	12	Leave unconnected.
NMI	2	Directly connect to V _{SS} .
CLKOUT	3	Leave unconnected.
WAIT	1	Directly connect to V _{DD} .
MODE	2	—
RESET		—
★ CV _{DD} /CKSEL		—
AV _{REF1} -AV _{REF3} , AV _{SS}	—	Directly connect to V _{SS} .
AV _{DD}	—	Directly connect to V _{DD} .
V _{PP}	—	Directly connect to V _{SS} .

Figure 2-1. I/O Circuits of Pins



3. PROGRAMMING FLASH MEMORY

There are the following two methods for writing a program to the flash memory.

(1) On-board programming

Write a program to the flash memory using a dedicated flash programmer after the μ PD70F3003 has been mounted on the target board. Also mount a connector, etc. on the target board to communicate with the dedicated flash programmer.

(2) Off-board programming

Write a program using a dedicated adapter before the μ PD70F3003 has been mounted on the target board.

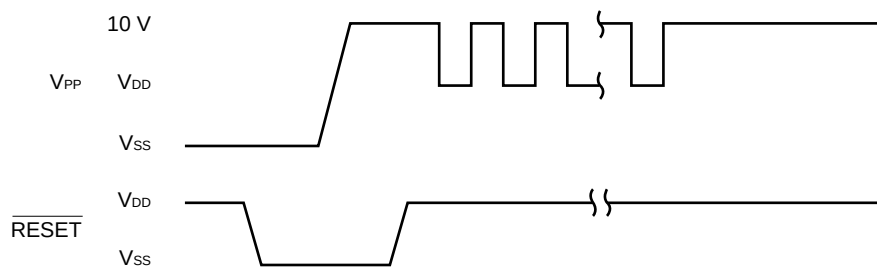
3.1 Selecting Communication Mode

To write the flash memory, use a dedicated flash programmer and serial communication. Select a serial communication mode from those listed in Table 3-1 in the format shown in Figure 3-1. Each communication mode is selected by the number of V_{PP} pulses shown in Table 3-1.

Table 3-1. Communication Modes

Communication Mode	Pins Used	Number of V_{PP} Pulses
CSI	$\overline{SCK0}$ (serial clock input) SO0 (serial data output) SI0 (serial data input)	0
UART	TXD0 (serial data output) RXD0 (serial data input)	8

Figure 3-1. Communication Mode Selecting Format



3.2 Flash Memory Programming Function

The flash memory is written by transferring or receiving commands and data in a selected communication mode. The major functions of flash memory programming are listed in Table 3-2.

★

Table 3-2. Major Functions of Flash Memory Programming

Function	Description
Batch erasure	Erases all contents of memory.
Batch blank check	Checks erased status of entire memory.
Data write	Writes flash memory based on write start address and number of data to be written (in bytes).
Batch verify	Compares all contents of memory with input data.

3.3 Connecting Dedicated Flash Programmer

The dedicated flash programmer and μPD70F3003 are connected differently depending on the selected communication mode. Figures 3-2 through 3-3 show the connections in the respective communication modes.

Figure 3-2. Connection of Dedicated Flash Programmer in UART Mode

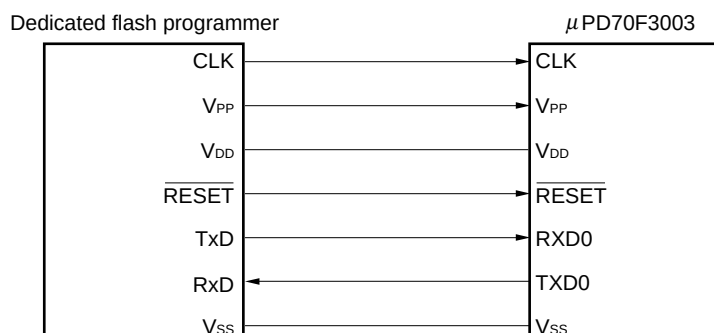
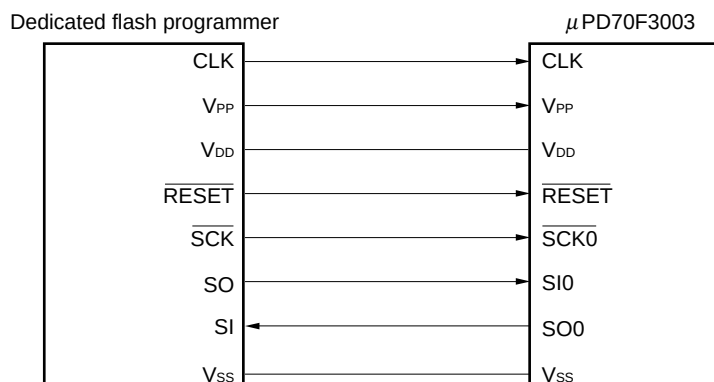


Figure 3-3. Connection of Dedicated Flash Programmer in CSI Mode



4. ELECTRICAL SPECIFICATIONS

4.1 Normal Operation Mode

Absolute Maximum Ratings ($T_A = 25\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Condition		Ratings	Unit
Supply voltage	V_{DD}	V_{DD} pin		-0.5 to +7.0	V
	CV_{DD}	CV_{DD} pin		-0.5 to $V_{DD} + 0.3$	V
	CV_{SS}	CV_{SS} pin		-0.5 to +0.5	V
	AV_{DD}	AV_{DD} pin		-0.5 to $V_{DD} + 0.3$	V
	AV_{SS}	AV_{SS} pin		-0.5 to +0.5	V
Input voltage	V_{I1}	Note , $V_{DD} = 5.0\text{ V} \pm 10\%$		-0.5 to $V_{DD} + 0.3$	V
	V_{I2}	V_{PP} pin in flash memory programming mode, $V_{DD} = 5.0\text{ V} \pm 10\%$		-0.5 to +11.0	V
Clock input voltage	V_K	X1 pin, $V_{DD} = 5.0\text{ V} \pm 10\%$		-0.5 to $V_{DD} + 1.0$	V
Output current, low	I_{CL}	1 pin		4.0	mA
		Total of all pins		100	mA
Output current, high	I_{CH}	1 pin		-4.0	mA
		Total of all pins		-100	mA
Output voltage	V_O	$V_{DD} = 5.0\text{ V} \pm 10\%$		-0.5 to $V_{DD} + 0.3$	V
Analog input voltage	V_{IAN}	P70/ANI0-P77/ANI7	$AV_{DD} > V_{DD}$	-0.5 to $V_{DD} + 0.3$	V
			$V_{DD} \geq AV_{DD}$	-0.5 to $AV_{DD} + 0.3$	V
Analog reference input voltage	AV_{REF}	$AV_{REF1}-AV_{REF3}$	$AV_{DD} > V_{DD}$	-0.5 to $V_{DD} + 0.3$	V
			$V_{DD} \geq AV_{DD}$	-0.5 to $AV_{DD} + 0.3$	V
★ Operating ambient temperature	T_A			-40 to +70	$^{\circ}\text{C}$
★ Storage temperature	T_{stg}			-40 to +100	$^{\circ}\text{C}$

Note Except X1, P70/AN0-P77/AN7, $AV_{REF1}-AV_{REF3}$

Cautions 1. Do not directly connect the output (or I/O) pins of two or more IC products, and do not directly connect them to V_{DD} , V_{CC} , or GND pin. Open-drain pins and open-collector pins may be directly connected to one another however. Moreover, an external circuit that is designed to prevent contention of output can be connected to pins that go into a high-impedance state.

2. Should the absolute maximum rating of even one of the above parameters be exceeded even momentarily, the quality of the program may be degraded. The absolute maximum ratings are, therefore, the values exceeding which the product may be physically damaged. Use the product so that these values are never exceeded.

The normal operating ranges of ratings and conditions in which the quality of the product is guaranteed are specified in the following DC Characteristics and AC Characteristics.

Capacitance ($T_A = 25\text{ }^{\circ}\text{C}$, $V_{DD} = V_{SS} = 0\text{ V}$)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_i	$f_c = 1\text{ MHz}$ Pins other than tested pin: 0 V			15	pF
I/O capacitance	C_{io}				15	pF
Output capacitance	C_o				15	pF

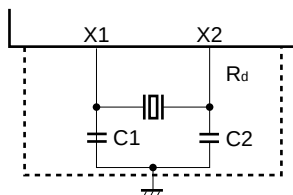
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Operating Conditions

Operation Mode	Internal Operating Clock Frequency (ϕ)	Operating Temperature (T_A)	Supply Voltage (V_{DD})
Direct mode	20 to 25 MHz	-40 to $+70\text{ }^{\circ}\text{C}$	$5.0\text{ V} \pm 5\%$
PLL mode	Self oscillation frequency to 25 MHz	-40 to $+70\text{ }^{\circ}\text{C}$	$5.0\text{ V} \pm 5\%$

Remark The internal operating clock frequency range in the PLL mode means the range in which the functional operation is guaranteed, and the frequency in the PLL lock status is specified by f_{cylx} .

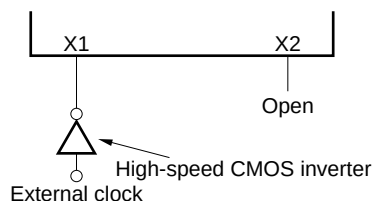
★ Recommended Oscillation Circuit

(a) Ceramic resonator connection (TDK, Murata Mfg.: $T_A = -40$ to $+85$ °C, Kyocera: $T_A = -20$ to $+80$ °C)

Manufacturer	Part Number	Oscillation Frequency f_{xx} (MHz)	Recommended Circuit Constants			Oscillation Voltage Range		Oscillation Stabilization Time (MAX.)
			C1(pF)	C2 (pF)	R_d (Ω)	MIN. (V)	MAX. (V)	T_{OST} (ms)
TDK Corp.	CCR5.0MC3	5.0	Provided	Provided	—	4.5	5.5	0.42
	FCR5.0MC5	5.0	Provided	Provided	—	4.5	5.5	0.38
Murata Mfg. Co. Ltd.	CSA5.00MG040	5.0	100	100	—	4.5	5.5	0.51
	CST5.00MGW040	5.0	Provided	Provided	—	4.5	5.5	0.51
Kyocera Corp.	KBR-5.0MKS	5.0	Provided	Provided	680	4.5	5.5	0.20

- Cautions**
1. Connect the oscillation circuit as closely to X1 and X2 pins as possible.
 2. Do not route any other signal lines in the range indicated by the broken line in the above figure.
 3. Thoroughly evaluate the matching between the μ PD70F3003 and resonator.

(b) External clock input



- Cautions**
1. Connect the high-speed CMOS inverter as closely to X1 pin as possible.
 2. Thoroughly evaluate the matching between the μ PD70F3003 and high-speed CMOS inverter.

★ DC Characteristics ($T_A = -40$ to $+70$ °C, $V_{DD} = 5.0$ V $\pm$ 5 %, $V_{SS} = 0$ V)

Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input voltage, high		V_{IH}	Except X1 and Note	2.2		$V_{DD} + 0.3$	V
			Note	$0.8 V_{DD}$		$V_{DD} + 0.3$	V
Input voltage, low		V_{IL}	Except X1 and Note	-0.5		+0.8	V
			Note	-0.5		$0.2 V_{DD}$	V
Clock input voltage, high		V_{XH}	X1	$0.8 V_{DD}$		$V_{DD} + 0.5$	V
Clock input voltage, low		V_{XL}	X1	-0.5		+0.6	V
Schmitt trigger input threshold voltage		V_{T+}	Note , rising		3.0		V
		V_{T-}	Note , falling		2.0		V
Schmitt trigger input hysteresis width		$V_{T+} - V_{T-}$	Note	0.5			V
Output voltage, high		V_{OH}	$I_{OH} = -2.5$ mA	$0.7 V_{DD}$			V
			$I_{OH} = -100$ μA	$V_{DD} - 0.5$			V
Output voltage, low		V_{OL}	$I_{OC} = 2.5$ mA			0.45	V
Input leakage current, high		I_{LIH}	$V_I = V_{DD}$			10	μA
Input leakage current, low		I_{LIL}	$V_I = 0$ V			-10	μA
Output leakage current, high		I_{LOH}	$V_O = V_{DD}$			10	μA
Output leakage current, low		I_{LOL}	$V_O = 0$ V			-10	μA
Software pull-up resistor		R	P35/INTP131/SO3, P36/INTP132/SI3, P37/INTP133/SCK3	15	40	90	kΩ
Supply current	Operating	I_{DD1}	Direct mode		$2.6 \times \phi + 7.5$	$2.9 \times \phi + 22$	mA
			PLL mode		$2.7 \times \phi + 9.5$	$3.0 \times \phi + 25$	mA
	In HALT mode	I_{DD2}	Direct mode		$1.4 \times \phi + 7.5$	$1.5 \times \phi + 18$	mA
			PLL mode		$1.5 \times \phi + 9.5$	$1.6 \times \phi + 20$	mA
	In IDLE mode	I_{DD3}	Direct mode		$18.6 \times \phi + 100$	$22 \times \phi + 200$	μA
			PLL mode		$0.05 \times \phi + 4$	$0.1 \times \phi + 8$	mA
	In STOP mode	I_{DD4}	-40 °C $\leq T_A \leq +50$ °C		2	50	μA
			50 °C $< T_A \leq 70$ °C		2	200	μA

Note P02/TCLR11, P03/TI11, P04/INTP110-P07/INTP113, P12/TCLR12, P13/TI12, P14/INTP120, P15/INTP121/SO2, P16/INTP122/SI2, P17/INTP123/SCK2, P23/RXD0/SI0, P24/SCK0, P26/RXD1/SI1, P27/SCK1, P32/TCLR32, P33/TI13, P34/INTP130, P35/INTP131/SO3, P36/INTP132/SI3, P37/INTP133/SCK3, P112/TCLR14, P113/TI14, P114/INTP140-P117/INTP143, RESET, NMI, MODE

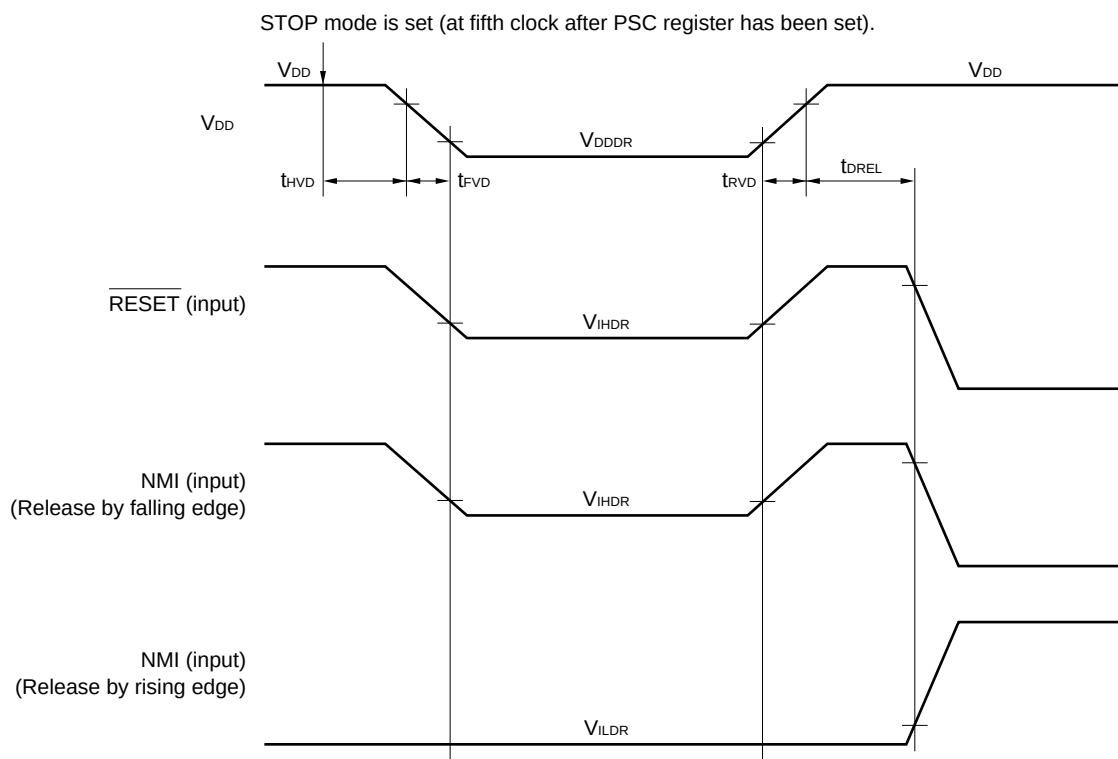
Remarks 1. TYP. value is a value for your reference at $T_A = 25$ °C and $V_{DD} = 5.0$ V. The supply current does not include AV_{REF1} - AV_{REF3} and the current running through the software pull-up resistor.
2. ϕ : Internal system clock frequency

Data Retention Characteristics ($T_A = -40$ to $+70$ °C)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Data hold voltage	V_{DDDR}	STOP mode	1.5		5.5	V
★ ★ Data hold current	I_{DDDR}	$V_{DD} = V_{DDDR}$ -40 °C $\leq T_A \leq +50$ °C		$0.2 V_{DDDR}$	50	μ A
		50 °C $< T_A \leq 70$ °C		$0.2 V_{DDDR}$	200	μ A
Supply voltage rise time	t_{RVD}		200			μ s
Supply voltage fall time	t_{FVD}		200			μ s
Supply voltage hold time (vs. STOP mode setting)	t_{HVD}		0			ms
STOP mode release signal input time	t_{DREL}		0			ns
Data hold input voltage, high	V_{IHDR}	Note	$0.9 V_{DDDR}$		V_{DDDR}	V
Data hold input voltage, low	V_{ILDR}	Note	0		$0.1 V_{DDDR}$	V

Note P02/TCLR11, P03/TI11, P04/INTP110-P07/INTP113, P12/TCLR12, P13/TI12, P14/INTP120, P15/INTP121/SO2, P16/INTP122/SI2, P17/INTP123/SCK2, P23/RXD0/SI0, P24/SCK0, P26/RXD1/SI1, P27/SCK1, P32/TCLR32, P33/TI13, P34/INTP130, P35/INTP131/SO3, P36/INTP132/SI3, P37/INTP133/SCK3, P112/TCLR14, P113/TI14, P114/INTP140-P117/INTP143, RESET, NMI, MODE, X1

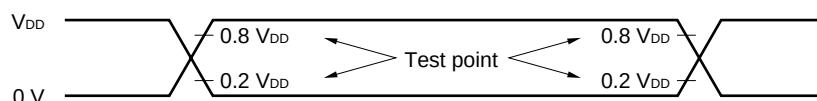
Remark TYP. value is a value for your reference at $T_A = 25$ °C and $V_{DD} = 5.0$ V.



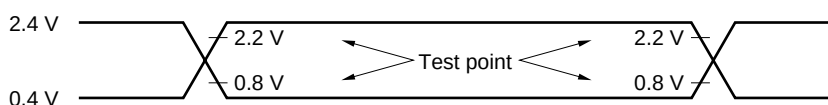
★ AC Characteristics ($T_A = -40$ to $+70$ °C, $V_{DD} = 5.0$ V $\pm$ 5 %, $V_{SS} = 0$ V)

AC test input wave

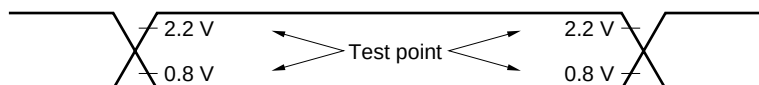
- (a) P02/TCLR11, P03/TI11, P04/INTP110-P07/INTP113, P12/TCLR12, P13/TI12, P14/INTP120, P15/INTP121/SO2, P16/INTP122/SI2, P17/INTP123/SCK2, P23/RXD0/SI0, P24/SCK0, P26/RXD1/SI1, P27/SCK1, P32/TCLR32, P33/TI13, P34/INTP130, P35/INTP131/SO3, P36/INTP132/SI3, P37/INTP133/SCK3, P112, TCLR14, P113/TI14, P114/INTP140-P117/INTP143, RESET, NMI, MODE, X1



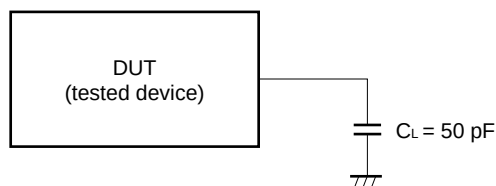
- (b) Other than (a)



AC test output test point



Load condition



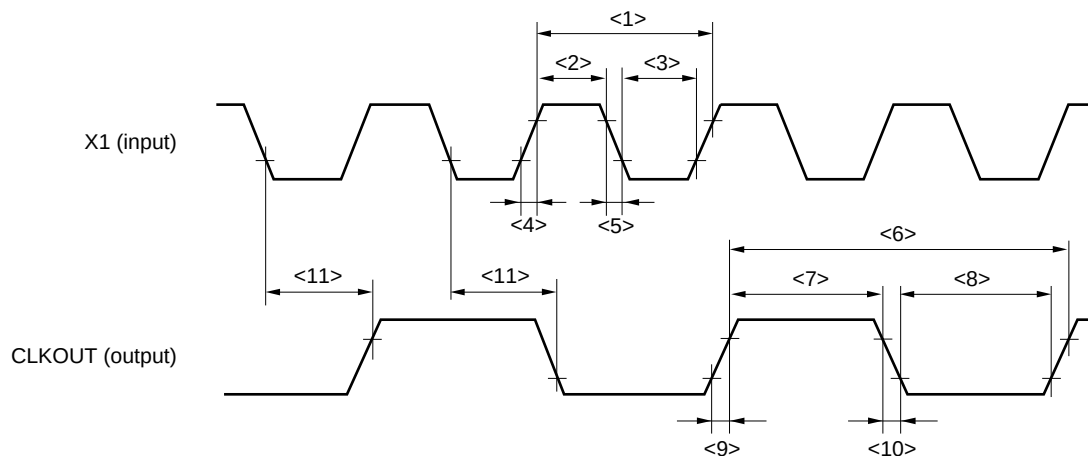
Caution If the load capacitance exceeds 50 pF due to the circuit configuration, decrease the load capacitance of this device to less than 50 pF by using a buffer.

★ (1) Clock timing

Parameter	Symbol	Condition	MIN.	MAX.	Unit
X1 input cycle	<1> t_{CYX}	Direct mode	20	25	ns
		PLL mode (PLL lock status)	200	227	ns
X1 input width, high	<2> t_{WXH}	Direct mode	7		ns
		PLL mode	80		ns
X1 input width, low	<3> t_{WXL}	Direct mode	7		ns
		PLL mode	80		ns
X1 input rise time	<4> t_{XR}	Direct mode		7	ns
		PLL mode		15	ns
X1 input fall time	<5> t_{XF}	Direct mode		7	ns
		PLL mode		15	ns
CPU operating frequency	— ϕ	Direct mode	20	25	MHz
		PLL mode	Note	25	MHz
CLKOUT output cycle	<6> t_{CYK}		40	50	ns
CLKOUT width, high	<7> t_{WKH}		0.5 T – 5		ns
CLKOUT width, low	<8> t_{WKL}		0.5 T – 5		ns
CLKOUT rise time	<9> t_{XR}			5	ns
CLKOUT fall time	<10> t_{XF}			5	ns
X1 $\downarrow \rightarrow$ CLKOUT delay time	<11> t_{DXK}	Direct mode	3	17	ns

★ **Note** Self oscillation frequency.**Remark** T = t_{CYK}

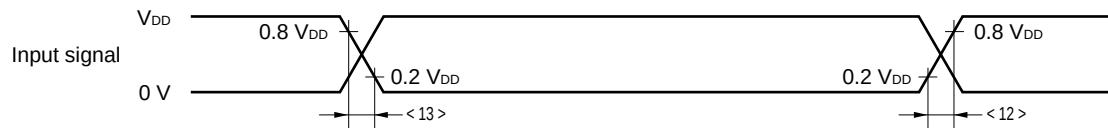
Parameter	Symbol	Condition	TYP.	Unit
Self oscillation frequency	— ϕ_P	PLL mode	5	MHz



(2) Input wave

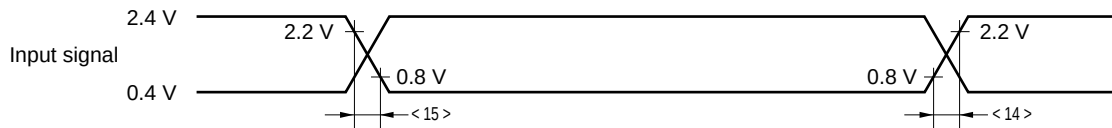
- (a) P02/TCLR11, P03/TI11, P04/INTP110-P07/INTP113, P12/TCLR12, P13/TI12, P14/INTP120, P15/INTP121/SO2, P16/INTP122/SI2, P17/INTP123/SCK2, P23/RXD0/SI0, P24/SCK0, P26/RXD1/SI1, P27/SCK1, P32/TCLR32, P33/TI13, P34/INTP130, P35/INTP131/SO3, P36/INTP132/SI3, P37/INTP133/SCK3, P112/TCLR14, P113/TI14, P114/INTP140-P117/INTP143, RESET, NMI, MODE

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input rise time	<12> t_{IR2}			20	ns
Input fall time	<13> t_{IF2}			20	ns



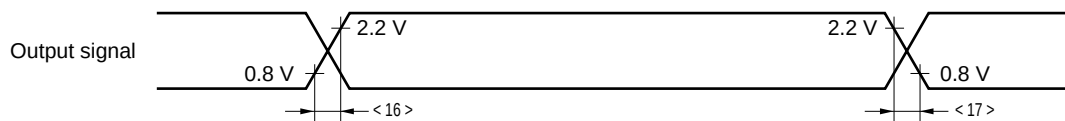
(b) Other than (a)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input rise time	<14> t_{IR1}			10	ns
Input fall time	<15> t_{IF1}			10	ns



★ (3) Output wave (other than CLKOUT)

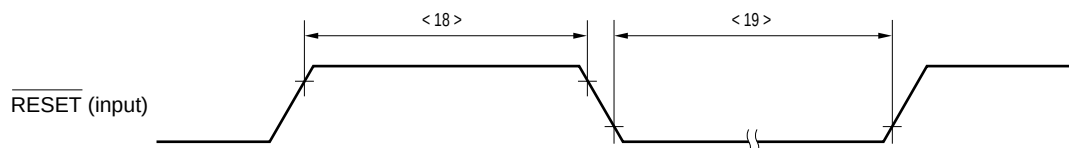
Parameter	Symbol		Condition	MIN.	MAX.	Unit
Output rise time	<16>	t_{OR}			12	ns
Output fall time	<17>	t_{OF}			12	ns



(4) Reset timing

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{\text{RESET}}$ width, high	<18>	t_{WRSH}		500		ns
$\overline{\text{RESET}}$ width, low	<19>	t_{WRSL}	On power application, or on releasing STOP mode	$500 + T_{OST}$		ns
			Except on power application, or except on releasing STOP mode	500		ns

Remark T_{OST} : oscillation stabilization time



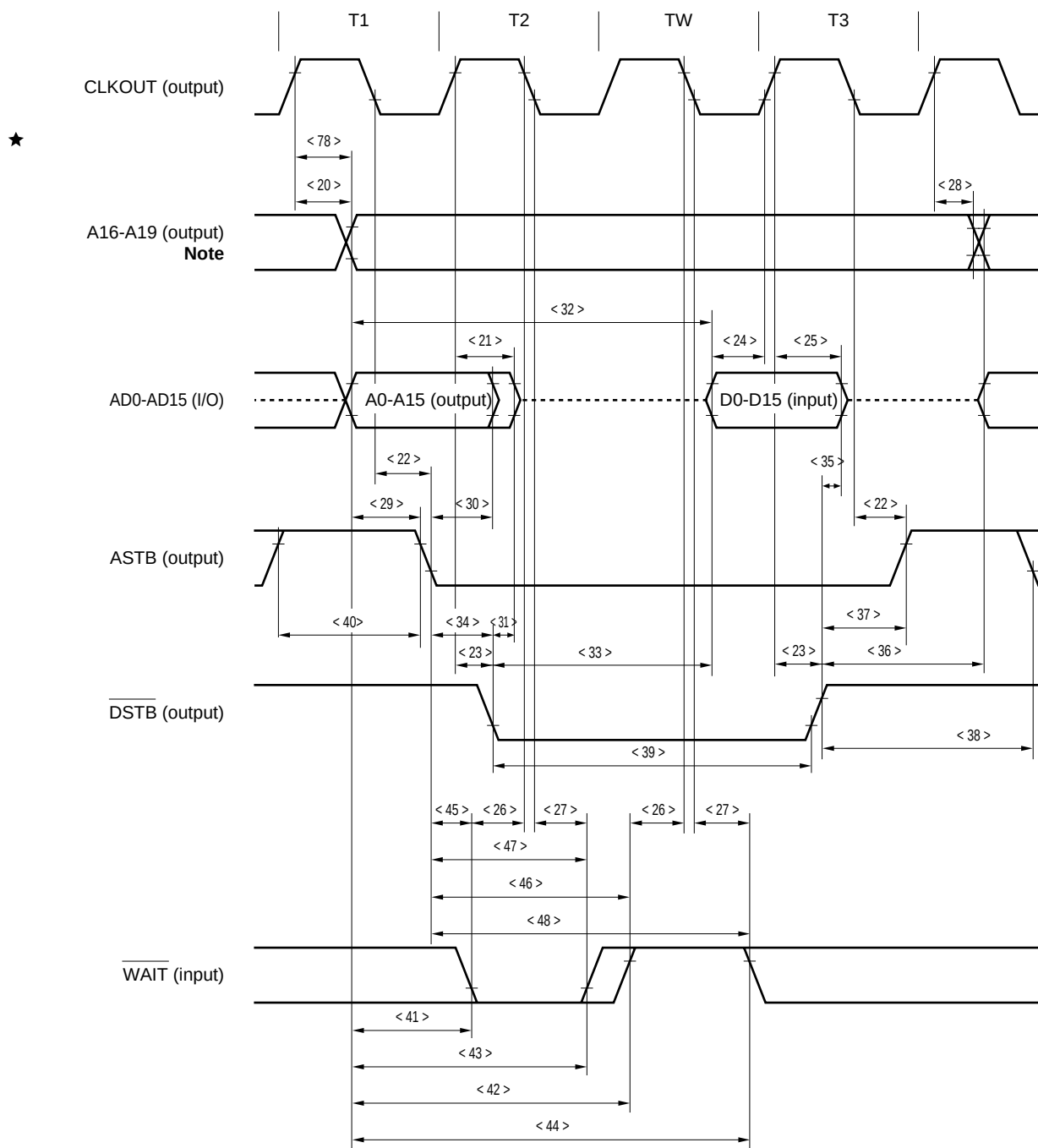
(5) Read timing (1/2)

	Parameter	Symbol	Condition	MIN.	MAX.	Unit
	CLKOUT $\uparrow \rightarrow$ address delay time	<20> t_{DKA}		3	20	ns
★	CLKOUT $\uparrow \rightarrow \overline{R\overline{W}}, \overline{UBEN}, \overline{LBEN}$, delay time	<78> t_{DKA2}		-2	+13	ns
	CLKOUT $\uparrow \rightarrow$ address float delay time	<21> t_{FKA}		3	15	ns
★	CLKOUT $\downarrow \rightarrow$ ASTB delay time	<22> t_{DKST}		-2	+13	ns
★	CLKOUT $\downarrow \rightarrow \overline{DSTB}$ delay time	<23> t_{DKD}		-2	+13	ns
★	Data input setup time (vs. CLKOUT $\uparrow$)	<24> t_{SIDK}		7		ns
	Data input hold time (vs. CLKOUT $\uparrow$)	<25> t_{HKID}		5		ns
★	$\overline{WAIT}$ setup time (vs. CLKOUT $\downarrow$)	<26> t_{SWTK}		8		ns
	$\overline{WAIT}$ hold time (vs. CLKOUT $\downarrow$)	<27> t_{HKWT}		5		ns
	Address hold time (vs. CLKOUT $\uparrow$)	<28> t_{HKA}		0		ns
	Address setup time (vs. ASTB $\downarrow$)	<29> t_{SAST}		0.5 T - 10		ns
	Address hold time (vs. ASTB $\downarrow$)	<30> t_{HSTA}		0.5 T - 10		ns
	$\overline{DSTB} \downarrow \rightarrow$ address float delay time	<31> t_{FDA}			0	ns
	Data input setup time (vs. address)	<32> t_{SAID}			(2 + n) T - 20	ns
	Data input setup time (vs. $\overline{DSTB} \downarrow$)	<33> t_{SDID}			(1 + n) T - 20	ns
	ASTB $\downarrow \rightarrow \overline{DSTB} \downarrow$ delay time	<34> t_{DSTD}		0.5 T - 10		ns
	Data input hold time (vs. $\overline{DSTB} \uparrow$)	<35> t_{HDID}		0		ns
★	$\overline{DSTB} \uparrow \rightarrow$ address output delay time	<36> t_{DDA}		(1 + i) T - 3		ns
	$\overline{DSTB} \uparrow \rightarrow$ ASTB $\uparrow$ delay time	<37> t_{DDSTH}		0.5 T - 10		ns
	$\overline{DSTB} \uparrow \rightarrow$ ASTB $\downarrow$ delay time	<38> t_{DDSTL}		(1.5 + i) T - 10		ns
	$\overline{DSTB}$ width, low	<39> t_{WDL}		(1 + n) T - 10		ns
	ASTB width, high	<40> t_{WSTH}		T - 10		ns
	$\overline{WAIT}$ setup time (vs. address)	<41> t_{SAWT1}	$n \geq 1$		1.5 T - 20	ns
		<42> t_{SAWT2}			(1.5 + n) T - 20	ns
	$\overline{WAIT}$ hold time (vs. address)	<43> t_{HAWT1}	$n \geq 1$	(0.5 + n) T		ns
		<44> t_{HAWT2}		(1.5 + n) T		ns
	$\overline{WAIT}$ setup time (vs. ASTB $\downarrow$)	<45> t_{SSTWT1}	$n \geq 1$		T - 15	ns
		<46> t_{SSTWT2}			(1 + n) T - 15	ns
	$\overline{WAIT}$ hold time (vs. ASTB $\downarrow$)	<47> t_{HSTWT1}	$n \geq 1$	nT		ns
		<48> t_{HSTWT2}		(1 + n) T		ns

Remarks 1. T = t_{CYK}

2. n indicates the number of wait clocks inserted in the bus cycle. The sampling timing differs when the programmable wait state is inserted.
3. i indicates the number of idle states (0 or 1) to be inserted in the read cycle.
4. Be sure to observe at least one of data input hold times t_{HKID} (<25>) and t_{HDID} (<35>).

(5) Read Timing (2/2): 1 wait



Note $\overline{R/W}$ (output), $\overline{UBEN}$ (output), $\overline{LBEN}$ (output)

Remark The broken line indicates the high-impedance state.

(6) Write timing (1/2)

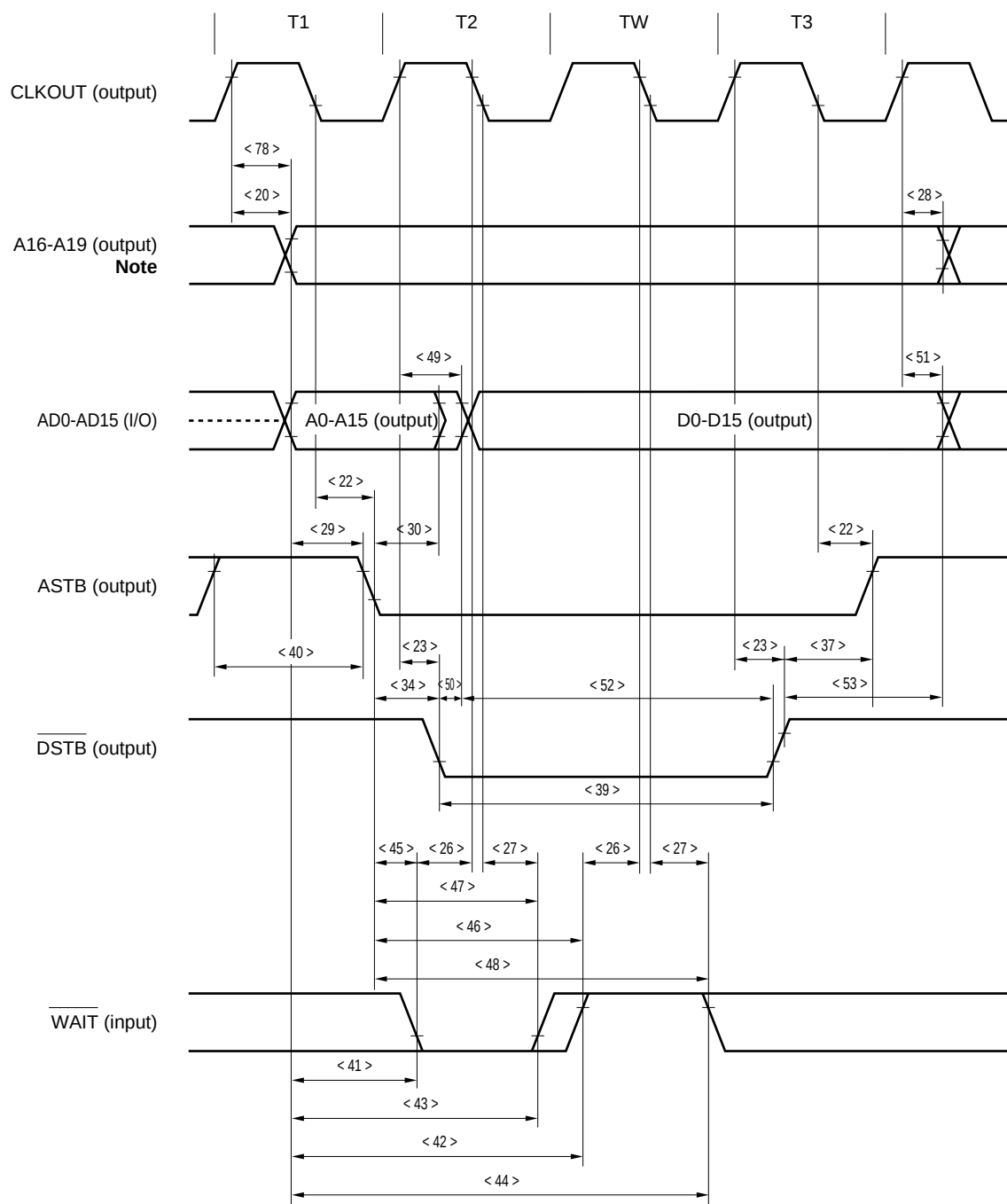
Parameter	Symbol	Condition	MIN.	MAX.	Unit
CLKOUT $\uparrow \rightarrow$ address delay time	<20> t_{DKA}		3	20	ns
CLKOUT $\uparrow \rightarrow \overline{R/\overline{W}}, \overline{UBEN}, \overline{LBEN}$ delay time	<78> t_{DKA2}		-2	+13	ns
CLKOUT $\downarrow \rightarrow$ ASTB delay time	<22> t_{DKST}		-2	+13	ns
CLKOUT $\uparrow \rightarrow \overline{DSTB}$ delay time	<23> t_{DKD}		-2	+13	ns
$\overline{WAIT}$ setup time (vs. CLKOUT $\downarrow$)	<26> t_{SWTK}		8		ns
$\overline{WAIT}$ hold time (vs. CLKOUT $\downarrow$)	<27> t_{HKWT}		5		ns
Address hold time (vs. CLKOUT $\uparrow$)	<28> t_{HKA}		0		ns
Address setup time (vs. ASTB $\downarrow$)	<29> t_{SAST}		$0.5 T - 10$		ns
Address hold time (vs. ASTB $\downarrow$)	<30> t_{HSTA}		$0.5 T - 10$		ns
ASTB $\downarrow \rightarrow \overline{DSTB} \downarrow$ delay time	<34> t_{DSTD}		$0.5 T - 10$		ns
$\overline{DSTB} \uparrow \rightarrow$ ASTB $\uparrow$ delay time	<37> t_{DDSTH}		$0.5 T - 10$		ns
$\overline{DSTB}$ width, low	<39> t_{WDL}		$(1 + n) T - 10$		ns
ASTB width, high	<40> t_{WSTH}		$T - 10$		ns
$\overline{WAIT}$ setup time (vs. address)	<41> t_{SAWT1}	$n \geq 1$		$1.5 T - 20$	ns
	<42> t_{SAWT2}			$(1.5 + n) T - 20$	ns
$\overline{WAIT}$ hold time (vs. address)	<43> t_{HAWT1}	$n \geq 1$	$(0.5 + n) T$		ns
	<44> t_{HAWT2}		$(1.5 + n) T$		ns
$\overline{WAIT}$ setup time (vs. ASTB $\downarrow$)	<45> t_{SSTWT1}	$n \geq 1$		$T - 15$	ns
	<46> t_{SSTWT2}			$(1 + n) T - 15$	ns
$\overline{WAIT}$ hold time (vs. ASTB $\downarrow$)	<47> t_{HSTWT1}	$n \geq 1$	nT		ns
	<48> t_{HSTWT2}		$(1 + n) T$		ns
CLKOUT $\uparrow \rightarrow$ data output delay time	<49> t_{DKOD}			20	ns
$\overline{DSTB} \downarrow \rightarrow$ data output delay time	<50> t_{DDOD}			10	ns
Data output hold time (vs. CLKOUT $\uparrow$)	<51> t_{HKOD}		0		ns
Data output setup time (vs. $\overline{DSTB} \uparrow$)	<52> t_{SODD}		$(1 + n) T - 15$		ns
Data output hold time (vs. $\overline{DSTB} \uparrow$)	<53> t_{HDOD}		$T - 10$		ns

Remarks 1. $T = t_{CYK}$

2. n indicates the number of wait clocks inserted in the bus cycle. The sampling timing differs when the programmable wait state is inserted.

(6) Write timing (2/2): 1 wait

★



Note $\overline{R/W}$ (output), $\overline{UBEN}$ (output), $\overline{LBEN}$ (output)

Remark The broken line indicates the high-impedance state.

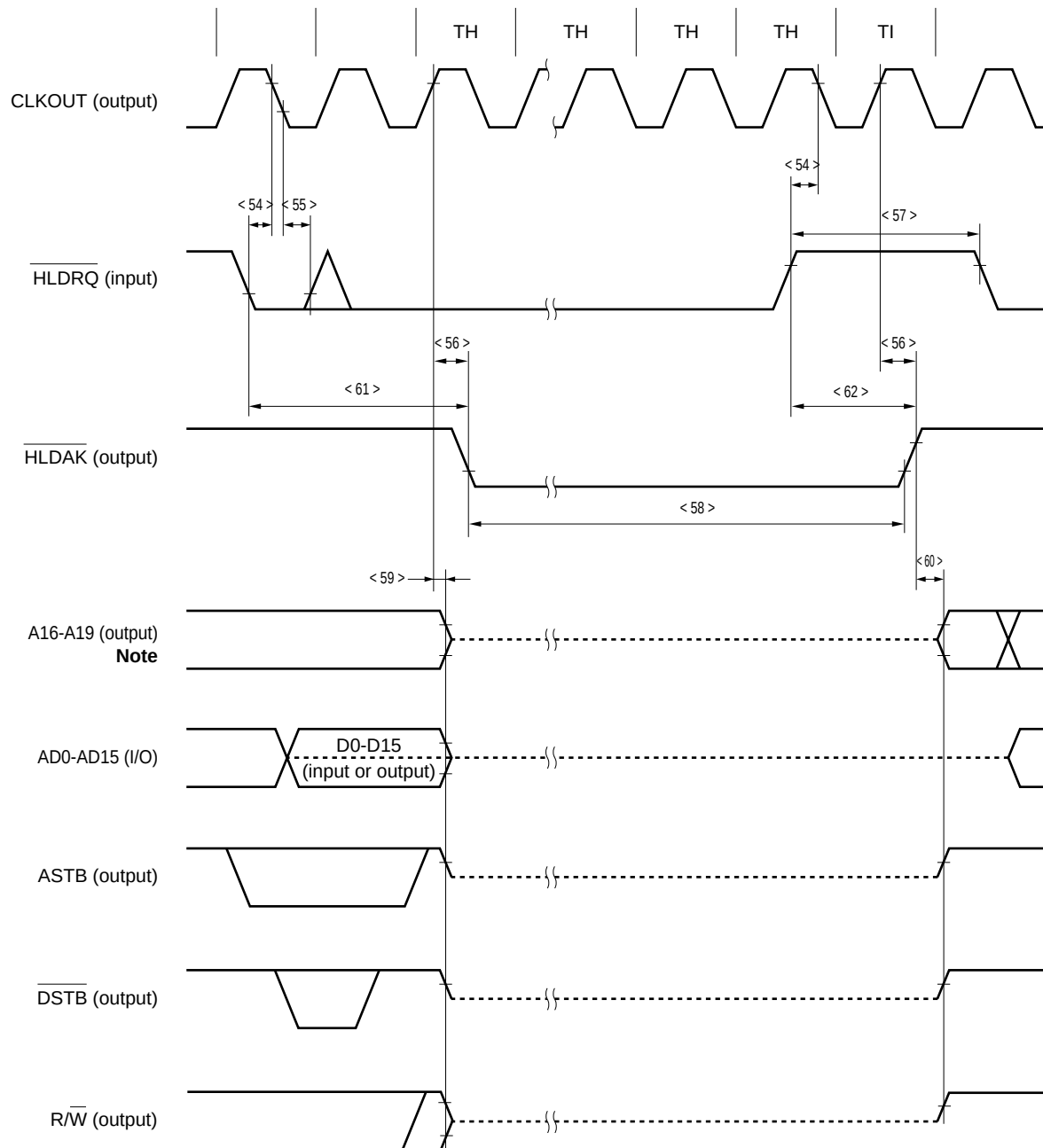
(7) Bus hold timing (1/2)

	Parameter	Symbol	Condition	MIN.	MAX.	Unit
★	$\overline{\text{HLDRQ}}$ setup time (vs. CLKOUT $\downarrow$)	<54> t_{SHOK}		8		ns
	$\overline{\text{HLDRQ}}$ hold time (vs. CLKOUT $\downarrow$)	<55> t_{HKHQ}		5		ns
	CLKOUT $\uparrow \rightarrow \overline{\text{HLDAK}}$ delay time	<56> t_{DKHA}			20	ns
	$\overline{\text{HLDRQ}}$ width, high	<57> t_{WHQH}		$T + 10$		ns
	$\overline{\text{HLDAK}}$ width, low	<58> t_{WHAL}		$T - 10$		ns
★	CLKOUT $\uparrow \rightarrow$ Bus float delay time	<59> t_{DKF}			20	ns
	$\overline{\text{HLDAK}}$ $\uparrow \rightarrow$ bus output delay time	<60> t_{DHAC}		-3		ns
	$\overline{\text{HLDRQ}}$ $\downarrow \rightarrow \overline{\text{HLDAK}}$ $\downarrow$ delay time	<61> t_{DHQHA1}			$(2n + 7.5)T + 20$	ns
	$\overline{\text{HLDRQ}}$ $\uparrow \rightarrow \overline{\text{HLDAK}}$ $\uparrow$ delay time	<62> t_{DHQHA2}		$0.5T$	$1.5T + 20$	ns

Remarks 1. $T = t_{\text{CYK}}$

2. n indicates the number of wait clocks inserted in the bus cycle. The sampling timing differs when the programmable wait state is inserted.

(7) Bus hold timing (2/2)



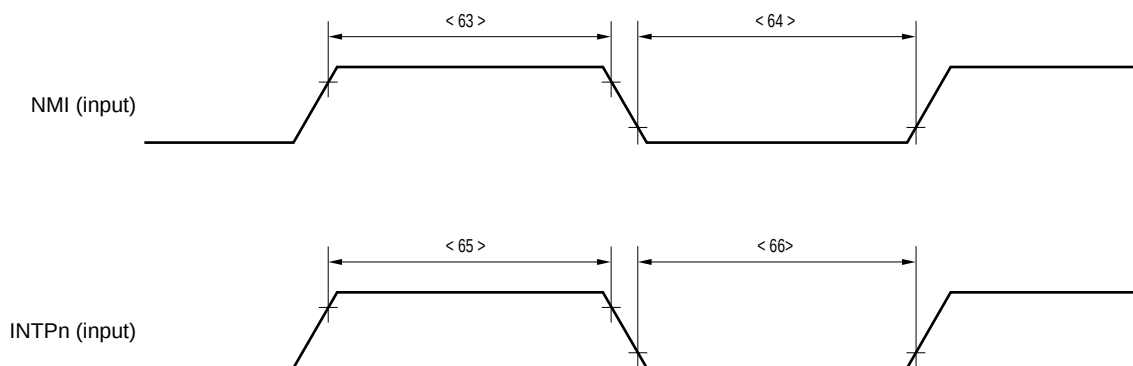
Note $\overline{\text{UBEN}}$ (output), $\overline{\text{LBEN}}$ (output)

Remark The broken line indicates the high-impedance state.

(8) Interrupt timing

Parameter	Symbol	Condition	MIN.	MAX.	Unit
NMI width, high	<63> t_{WNIH}		500		ns
NMI width, low	<64> t_{WNIL}		500		ns
INTPn width, high	<65> t_{WITH}	n = 110-113, 120-123, 130-133, 140-143	3 T + 10		ns
INTPn width, low	<66> t_{WITL}	n = 110-113, 120-123, 130-133, 140-143	3 T + 10		ns

Remark T = t_{CYK}



Remark n = 110-113, 120-123, 130-133, 140-143

(9) CSI timing (1/2)

(a) Master mode

(i) CSI0-CSI2 timing

Parameter	Symbol	Condition	MIN.	MAX.	Unit
$\overline{\text{SCKn}}$ cycle	<67> t_{CYSK1}	Output	160		ns
$\overline{\text{SCKn}}$ width, high	<68> t_{WSKH1}	Output	$0.5 t_{\text{CYSK1}} - 20$		ns
$\overline{\text{SCKn}}$ width, low	<69> t_{WSKL1}	Output	$0.5 t_{\text{CYSK1}} - 20$		ns
★ SIn setup time (vs. $\overline{\text{SCKn}}$ $\uparrow$)	<70> t_{SSISK1}		50		ns
SIn hold time (vs. $\overline{\text{SCKn}}$ $\uparrow$)	<71> t_{HSKSI1}		0		ns
SOn output delay time (vs. $\overline{\text{SCKn}}$ $\downarrow$)	<72> t_{DSKSO1}			18	ns
SOn output hold time (vs. $\overline{\text{SCKn}}$ $\uparrow$)	<73> t_{HSKSO1}		$0.5 t_{\text{CYSK1}} - 5$		ns

Remark n = 0-2

★ (ii) CSI3 timing

Parameter	Symbol	Condition	MIN.	MAX.	Unit
$\overline{\text{SCK3}}$ cycle	<67> t_{CYSK3}	Output $R_L = 1.5$ $k\Omega$	500		ns
$\overline{\text{SCK3}}$ width, high	<68> t_{WSKH3}	Output $C_L = 50$ pF	$0.5 t_{\text{CYSK3}} - 150$		ns
$\overline{\text{SCK3}}$ width, low	<69> t_{WSKL3}	Output	$0.5 t_{\text{CYSK3}} - 70$		ns
SI3 setup time (vs. $\overline{\text{SCK3}}$ $\uparrow$)	<70> t_{SSISK3}		100		ns
SI3 hold time (vs. $\overline{\text{SCK3}}$ $\uparrow$)	<71> t_{HSKSI3}		50		ns
SO3 output delay time (vs. $\overline{\text{SCK3}}$ $\downarrow$)	<72> t_{DSKSO3}	$R_L = 1.5 K\Omega$ $C_L = 50 pF$		150	ns
SO3 output hold time (vs. $\overline{\text{SCK3}}$ $\uparrow$)	<73> t_{HSKSO3}		t_{WSKH3}		ns

Remark R_L and C_L are the load resistance and load capacitance respectively of the $\overline{\text{SCK3}}$ and SO3 output lines.

(b) Slave mode

(i) CSI0-CSI2 timing

Parameter	Symbol	Condition	MIN.	MAX.	Unit
$\overline{\text{SCKn}}$ cycle	<67> t_{CYSK2}	Input	160		ns
$\overline{\text{SCKn}}$ width, high	<68> t_{WSKH2}	Input	50		ns
$\overline{\text{SCKn}}$ width, low	<69> t_{WSKL2}	Input	50		ns
SIn setup time (vs. $\overline{\text{SCKn}}$ $\uparrow$)	<70> t_{SSISK2}		10		ns
SIn hold time (vs. $\overline{\text{SCKn}}$ $\uparrow$)	<71> t_{HSKSI2}		10		ns
★ SOn output delay time (vs. $\overline{\text{SCKn}}$ $\downarrow$)	<72> t_{DSKSO2}			45	ns
SOn output hold time (vs. $\overline{\text{SCKn}}$ $\uparrow$)	<73> t_{HSKSO2}		t_{WSKH2}		ns

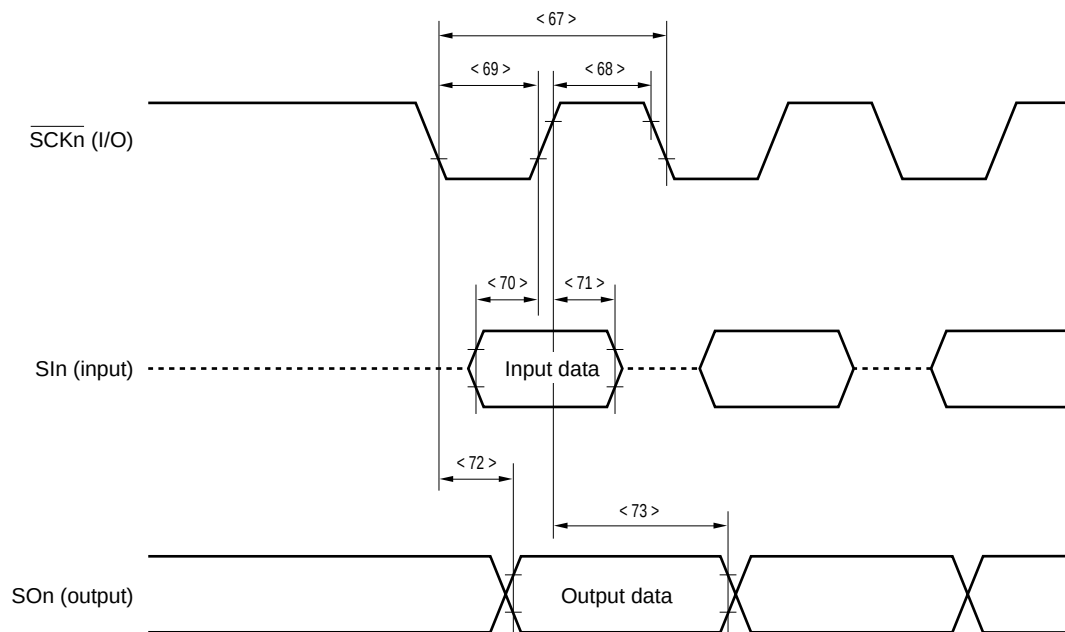
Remark n = 0-2

(9) CSI timing (2/2)

(ii) CSI3 timing

Parameter	Symbol	Condition	MIN.	MAX.	Unit
$\overline{\text{SCK3}}$ cycle	<67> t_{CYSK4}	Input	500		ns
$\overline{\text{SCK3}}$ width, high	<68> t_{WSKH4}	Input	100		ns
$\overline{\text{SCK3}}$ width, low	<69> t_{WSKL4}	Input	180		ns
SI3 setup time (vs. $\overline{\text{SCK3}}$ $\uparrow$)	<70> t_{SSISK4}		100		ns
SI3 hold time (vs. $\overline{\text{SCK3}}$ $\uparrow$)	<71> t_{HSKSI4}		50		ns
SO3 output delay time (vs. $\overline{\text{SCK3}}$ $\downarrow$)	<72> t_{DSKSO4}	$R_L = 1.5 \text{ k}\Omega$		150	ns
SO3 output hold time (vs. $\overline{\text{SCK3}}$ $\uparrow$)	<73> t_{HSKSO4}	$C_L = 50 \text{ pF}$	t_{WSKH4}		ns

Remark R_L and C_L are the load resistance and load capacitance respectively of the $\overline{\text{SCK3}}$ and SO3 output lines.

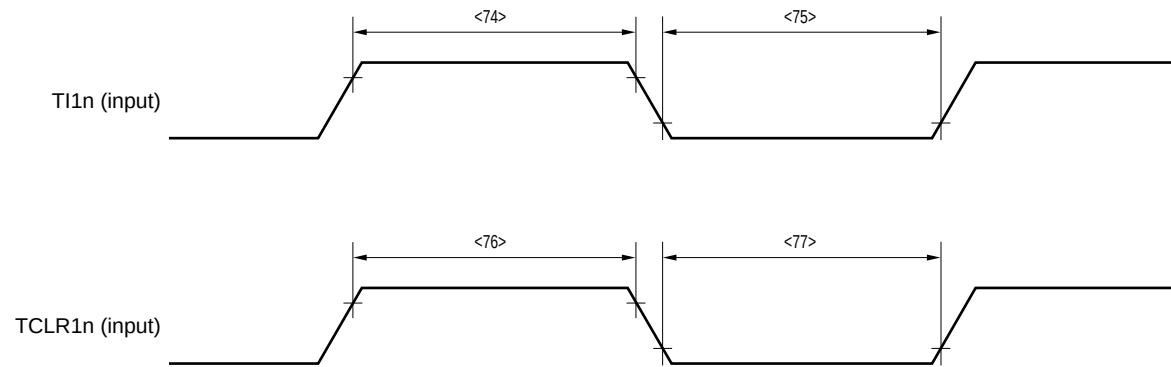


Remark 1. The broken line indicates the high-impedance state.
2. $n = 0-3$

(10) RPU timing

Parameter	Symbol		Condition	MIN.	MAX.	Unit
TI1n width, high	<74>	t _{WTIH}		3 T + 10		ns
TI1n width, low	<75>	t _{WTIL}		3 T + 10		ns
TCLR1n width, high	<76>	t _{WTCH}		3 T + 10		ns
TCLR1n width, low	<77>	t _{WTCL}		3 T + 10		ns

Remark T = t_{CYK}



Remark n = 1-4

★ A/D Converter Characteristics ($T_A = -40$ to $+70$ °C, $V_{DD} = AV_{DD} = 5\text{ V} \pm 5\%$, $V_{SS} = V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	—		10			bit
Overall error ^{Note 1}	—	$4.5\text{ V} \leq AV_{REF1} \leq AV_{DD}$			± 0.55	%FSR
	—	$3.5\text{ V} \leq AV_{REF1} \leq AV_{DD}$			± 0.7	%FSR
Quantize error	—				$\pm 1/2$	LSB
Conversion time	t_{CONV}	$4.5\text{ V} \leq AV_{REF1} \leq AV_{DD}$	48			t_{CYK}
		$3.5\text{ V} \leq AV_{REF1} \leq AV_{DD}$	48			t_{CYK}
Sampling time	t_{SAMP}	$4.5\text{ V} \leq AV_{REF1} \leq AV_{DD}$	8			t_{CYK}
	—	$3.5\text{ V} \leq AV_{REF1} \leq AV_{DD}$	8			t_{CYK}
Zero-scale error ^{Note 1}	—	$4.5\text{ V} \leq AV_{REF1} \leq AV_{DD}$		± 3.0	± 4.5	LSB
	—	$3.5\text{ V} \leq AV_{REF1} \leq AV_{DD}$		± 3.0	± 5.5	LSB
Full-scale error ^{Note 1}	—	$4.5\text{ V} \leq AV_{REF1} \leq AV_{DD}$		± 1.5	± 2.5	LSB
	—	$3.5\text{ V} \leq AV_{REF1} \leq AV_{DD}$		± 1.5	± 4.5	LSB
Non-linear error ^{Note 1}	—	$4.5\text{ V} \leq AV_{REF1} \leq AV_{DD}$		± 1.5	± 3.5	LSB
	—	$3.5\text{ V} \leq AV_{REF1} \leq AV_{DD}$		± 1.5	± 4.5	LSB
Analog input voltage ^{Note 2}	V_{IAN}		-0.3		$AV_{DD} + 0.3$	V
Reference voltage	AV_{REF1}		3.5		AV_{DD}	V
AV_{REF1} current	AI_{REF1}			1.2	3.0	mA
AV_{DD} supply current	AI_{DD}			2.3	6.0	mA

Notes 1. Except quantize error

2. The conversion result is 000H when $V_{IAN} = 0$.

Converted with 10-bit resolution when $0 < V_{IAN} < AV_{REF1}$.

The conversion result is 3FFH when $AV_{REF1} \leq V_{IAN} \leq AV_{DD}$.

★ D/A Converter Characteristics ($T_A = -40$ to $+70$ °C, $V_{DD} = AV_{DD} = 5\text{ V} \pm 5\%$, $V_{SS} = AV_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	—				8	bit
Overall error	—	Load conditions: 2 M Ω , 30 pF $AV_{REF2} = V_{DD}$ $AV_{REF3} = 0$			0.8	%
	—	Load conditions: 2 M Ω , 30 pF $AV_{REF2} = 0.75 V_{DD}$ $AV_{REF3} = 0.25 V_{DD}$			1.0	%
	—	Load conditions: 4 M Ω , 30 pF $AV_{REF2} = V_{DD}$ $AV_{REF3} = 0$			0.6	%
	—	Load conditions: 4 M Ω , 30 pF $AV_{REF2} = 0.75 V_{DD}$ $AV_{REF3} = 0.25 V_{DD}$			0.8	%
Settling time	—	Load conditions: 2 M Ω , 30 pF			10	μ s
Output resistance	RO			10		k Ω
AV_{REF2} input voltage	AV_{REF2}		0.75 V_{DD}		V_{DD}	V
AV_{REF3} input voltage	AV_{REF3}		0		0.25 V_{DD}	V
★ $AV_{REF2}-AV_{REF3}$ resistance value	R_{AIREF}	DACS0, DACS1 = 55H	2	5		k Ω

4.2 Flash Memory Programming Mode

★ **Basic Characteristics** ($T_A = 10$ to $40\text{ }^{\circ}\text{C}$ (When overwritten), $T_A = -40$ to $+70\text{ }^{\circ}\text{C}$ (When not overwritten), $V_{DD} = 5\text{ V} \pm 5\%$, $V_{SS} = 0\text{ V}$, $V_{PP} = 10\text{ V} \pm 0.3\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operating frequency	f_x		20		25	MHz
Supply voltage	V_{DD}		4.75		5.25	V
	V_{PPL}	V_{PP} low level detection	-0.5		$0.2 V_{DD}$	V
	V_{PPM}	V_{PP} , V_{DD} level detection	$0.8 V_{DD}$		$1.2 V_{DD}$	V
	V_{PPH}	V_{PP} high voltage detection	9.7		10.3	V
V_{DD} supply current	I_{DD}				$3.0 \times \phi + 25$	mA
V_{PP} supply current	I_{PP}	$V_{PP} = 10\text{ V}$			100	mA
Number of rewrite	C_{WRT}				5	times
Write time	t_{WRT}	Note 1		200	500	μs
Erasure time	t_{ERASE}	Note 2		20	40	s

Notes 1. When retried 10 times with $50\text{ }\mu\text{s}$ write time.

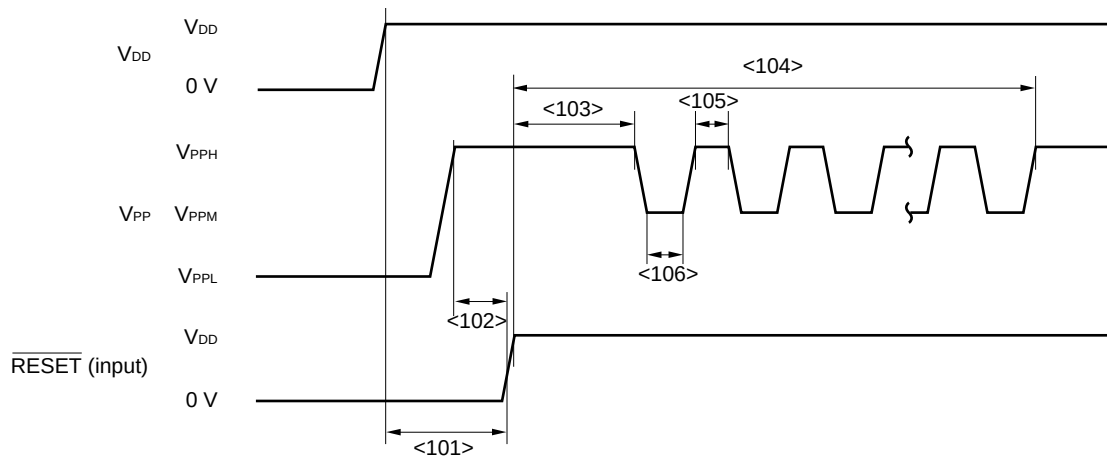
2. When retried 20 times with 2 s erasure time.

Remark ϕ : Internal system clock frequency.

Serial Write Operation Characteristics

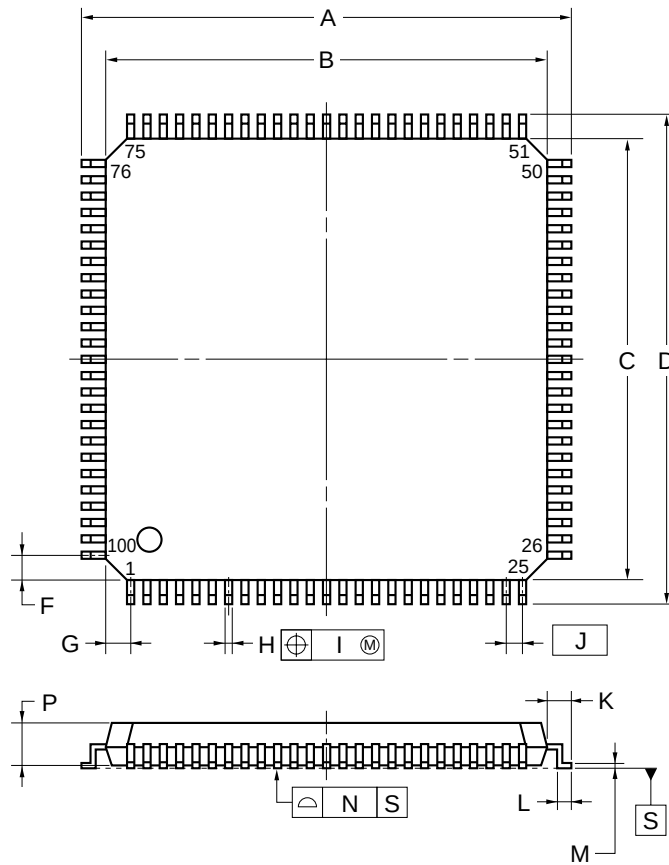
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$V_{DD} \uparrow \rightarrow \overline{\text{RESET}} \uparrow$ setup time	<101> t_{DRRR}		10			ms
$V_{PP} \uparrow \rightarrow \overline{\text{RESET}} \uparrow$ setup time	<102> t_{PSRR}		1.0			μs
$\overline{\text{RESET}} \uparrow \rightarrow V_{PP}$ count start time	<103> t_{RRCF}		$5T + 500$			ns
Count end time	<104> t_{COUNT}				10	ms
V_{PP} counter width, high	<105> t_{CH}		1.0			μs
V_{PP} counter width, low	<106> t_{CL}		1.0			μs

Remark $T = t_{\text{CYK}}$

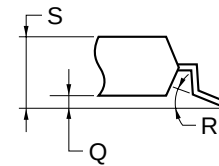


★ 5. PACKAGE DRAWING

100 PIN PLASTIC QFP (FINE PITCH) (□14)



detail of lead end



NOTE

1. Controlling dimension—— millimeter.
2. Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	16.0±0.2	0.630±0.008
B	14.0±0.2	0.551 ^{+0.009} _{-0.008}
C	14.0±0.2	0.551 ^{+0.009} _{-0.008}
D	16.0±0.2	0.630±0.008
F	1.0	0.039
G	1.0	0.039
H	0.22 ^{+0.05} _{-0.04}	0.009±0.002
I	0.10	0.004
J	0.5 (T.P.)	0.020 (T.P.)
K	1.0±0.2	0.039 ^{+0.009} _{-0.008}
L	0.5±0.2	0.020 ^{+0.008} _{-0.009}
M	0.17 ^{+0.03} _{-0.07}	0.007 ^{+0.001} _{-0.003}
N	0.10	0.004
P	1.45±0.05	0.057 ^{+0.003} _{-0.002}
Q	0.125±0.075	0.005±0.003
R	5°±5°	5°±5°
S	1.7 MAX.	0.067 MAX.

P100GC-50-7EA-3

★ 6. RECOMMENDED SOLDERING CONDITIONS

Solder this product under the following recommended conditions.

For details of the recommended soldering conditions, refer to information document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended, consult NEC.

Table 6-1. Soldering Conditions of Surface Mount Type

Soldering Method(s)	Soldering Conditions	Recommended Conditions Symbol
Infrared reflow	Package peak temperature: 235 °C, Time: 30 secs. max. (210 °C min.), Number of times: twice max., Number of days: 7 ^{Note} (after that, prebaking is necessary at 125 °C for 10 hours) <Precaution> Products other than in heat-resistance trays (such as those packaged in a magazine, taping, or non-heat-resistance tray) cannot be baked while they are in their package.	IR35-107-2
VPS	Package peak temperature: 215 °C, Time: 40 secs. max. (200 °C min.), Number of times: twice max., Number of days: 7 ^{Note} (after that, prebaking is necessary at 125 °C for 10 hours) <Precaution> Products other than in heat-resistance trays (such as those packaged in a magazine, taping, or non-heat-resistance tray) cannot be baked while they are in their package.	VP15-107-2
Partial pin heating	Pin temperature: 300 °C max., Time: 3 seconds max. (per device side)	—

Note Number of days in storage after the dry pack has been opened. The storage conditions are at 25 °C, 65% RH MAX.

Caution Do not use two or more soldering methods in combination. (except partial heating).

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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NEC Electronics Inc. (U.S.)

Santa Clara, California
Tel: 408-588-6000
800-366-9782
Fax: 408-588-6130
800-729-9288

NEC Electronics (Germany) GmbH

Duesseldorf, Germany
Tel: 0211-65 03 02
Fax: 0211-65 03 490

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Tel: 01908-691-133
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Fax: 02-66 75 42 99

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Benelux Office
Eindhoven, The Netherlands
Tel: 040-2445845
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Tel: 01-30-67 58 00
Fax: 01-30-67 58 99

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Spain Office
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Tel: 08-63 80 820
Fax: 08-63 80 388

NEC Electronics Hong Kong Ltd.

Hong Kong
Tel: 2886-9318
Fax: 2886-9022/9044

NEC Electronics Hong Kong Ltd.

Seoul Branch
Seoul, Korea
Tel: 02-528-0303
Fax: 02-528-4411

NEC Electronics Singapore Pte. Ltd.

United Square, Singapore 1130
Tel: 65-253-8311
Fax: 65-250-3583

NEC Electronics Taiwan Ltd.

Taipei, Taiwan
Tel: 02-2719-2377
Fax: 02-2719-5951

NEC do Brasil S.A.

Electron Devices Division
Rodovia Presidente Dutra, Km 214
07210-902-Guarulhos-SP Brasil
Tel: 55-11-6465-6810
Fax: 55-11-6465-6829

J99.1

Related document : μPD703003 Data Sheet (U12261E)
 μPD703003A, 703004A, 703025A Data Sheet (U13188J) (Japanese version)
 μPD70F3003A, 70F3025A Data Sheet (U13189E)
 V850 Family Instruction Table (U10229E)

Reference document: Concept of Electrical Characteristics - Microcomputers (IEI-601) (Japanese version)

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