NEC

MOS INTEGRATED CIRCUIT

μPD70P3002

V852™
32-/16-BIT SINGLE-CHIP MICROCONTROLLER

The μPD70P3002 is a one-time PROM version of the μPD703002. Because this device can be programmed by users only once, it is suited for applications involving small-scale production of many different products, and rapid development and time-to-market of new products.

The details of functions are described in the following user's manuals. Be sure to read them before designing.

V852 User's Manual Hardware : U10038E
V850 Family™ User's Manual Architecture : U10243E

FEATURES

- Compatible with μPD703002
  - Can be replaced with mask ROM version, μPD703002, for mass production of application set
- Internal PROM: 90 Kbytes
  - Can be written only once
- PROM programming characteristics: μPD27C1001A compatible
- QTOP™ microcontroller compatible

Remark QTOP microcontroller is NEC's microcontroller with one-time PROM, with total support of writing service (from program writing, to marking, screening, and verifying).

ORDERING INFORMATION

Part Number	Package
μPD70P3002GC-25-7EA	100-pin plastic QFP (fine pitch) (14 × 14 mm)
μPD70P3002GC-25-×××-7EA	100-pin plastic QFP (fine pitch) (14 × 14 mm) (QTOP microcontroller)

Remark ××× indicates the ROM code suffix.

The one-time PROM version is referred to as "PROM" in this document.

The information in this document is subject to change without notice.

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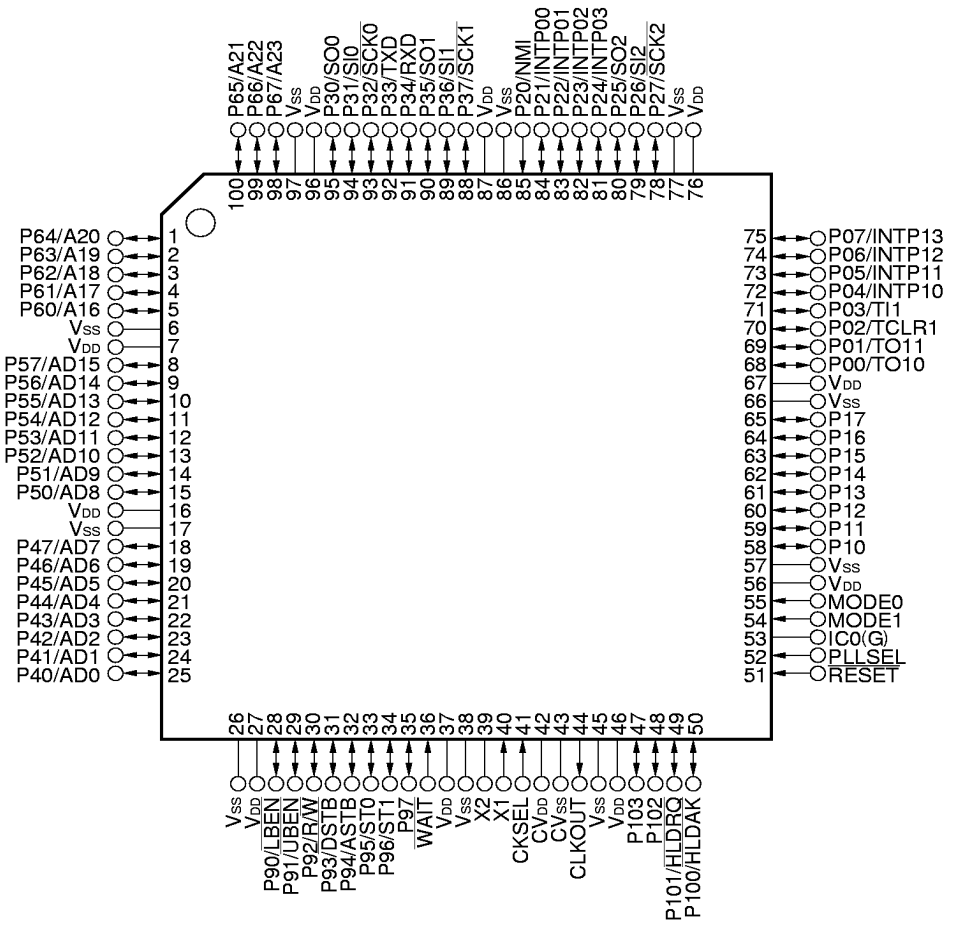
Date Published July 1997 N
Printed in Japan

The mark ★ shows major revised points.

PIN CONFIGURATION (Top View)

(1) Normal operation mode

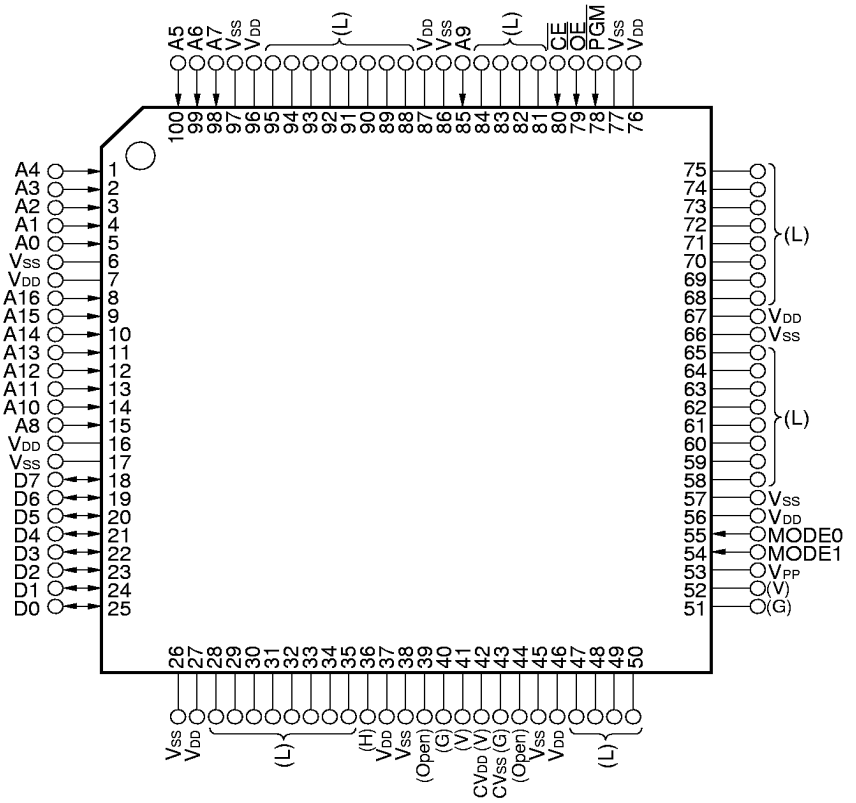


Caution The letters in parentheses indicate the processing of the pins not used in the normal operation mode.

G: Directly connect this pin to VSS.

P00 to P07	:	Port0	A16 to A23	:	Address Bus
P10 to P17	:	Port1	$\overline{\text{LBEN}}$	:	Lower Byte Enable
P20 to P27	:	Port2	$\overline{\text{UBEN}}$	:	Upper Byte Enable
P30 to P37	:	Port3	R/$\overline{\text{W}}$	:	Read/Write Status
P40 to P47	:	Port4	$\overline{\text{DSTB}}$	:	Data Strobe
P50 to P57	:	Port5	ASTB	:	Address Strobe
P60 to P67	:	Port6	ST0, ST1	:	Status
P90 to P97	:	Port9	$\overline{\text{HLDAK}}$	:	Hold Acknowledge
P100 to P103	:	Port10	$\overline{\text{HLDRQ}}$	:	Hold Request
TO10, TO11	:	Timer Output	CLKOUT	:	Clock Output
TCLR1	:	Timer Clear	CKSEL	:	Clock Select
TI1	:	Timer Input	PLLSEL	:	PLL Select
INTP00 to INTP03,			$\overline{\text{WAIT}}$	:	Wait
INTP10 to INTP13	:	Interrupt Request From Peripherals	MODE0, MODE1	:	Mode
NMI	:	Non-maskable Interrupt Request	$\overline{\text{RESET}}$	:	Reset
SO0 to SO2	:	Serial Output	X1, X2	:	Crystal
SI0 to SI2	:	Serial Input	CV_{DD}	:	Clock Generator Power Supply
$\overline{\text{SCK0}}$ to $\overline{\text{SCK2}}$	:	Serial Clock	CV_{SS}	:	Clock Generator Ground
TXD	:	Transmit Data	V_{DD}	:	Power Supply
RXD	:	Receive Data	V_{SS}	:	Ground
AD0 to AD15	:	Address/Data Bus	IC0	:	Internally Connected

(2) PROM programming mode



Caution The letters in parentheses indicate the processing of the pins not used in the normal operation mode.

L : Individually connect to V_{SS} via a resistor.

H : Connect to V_{DD} via a resistor.

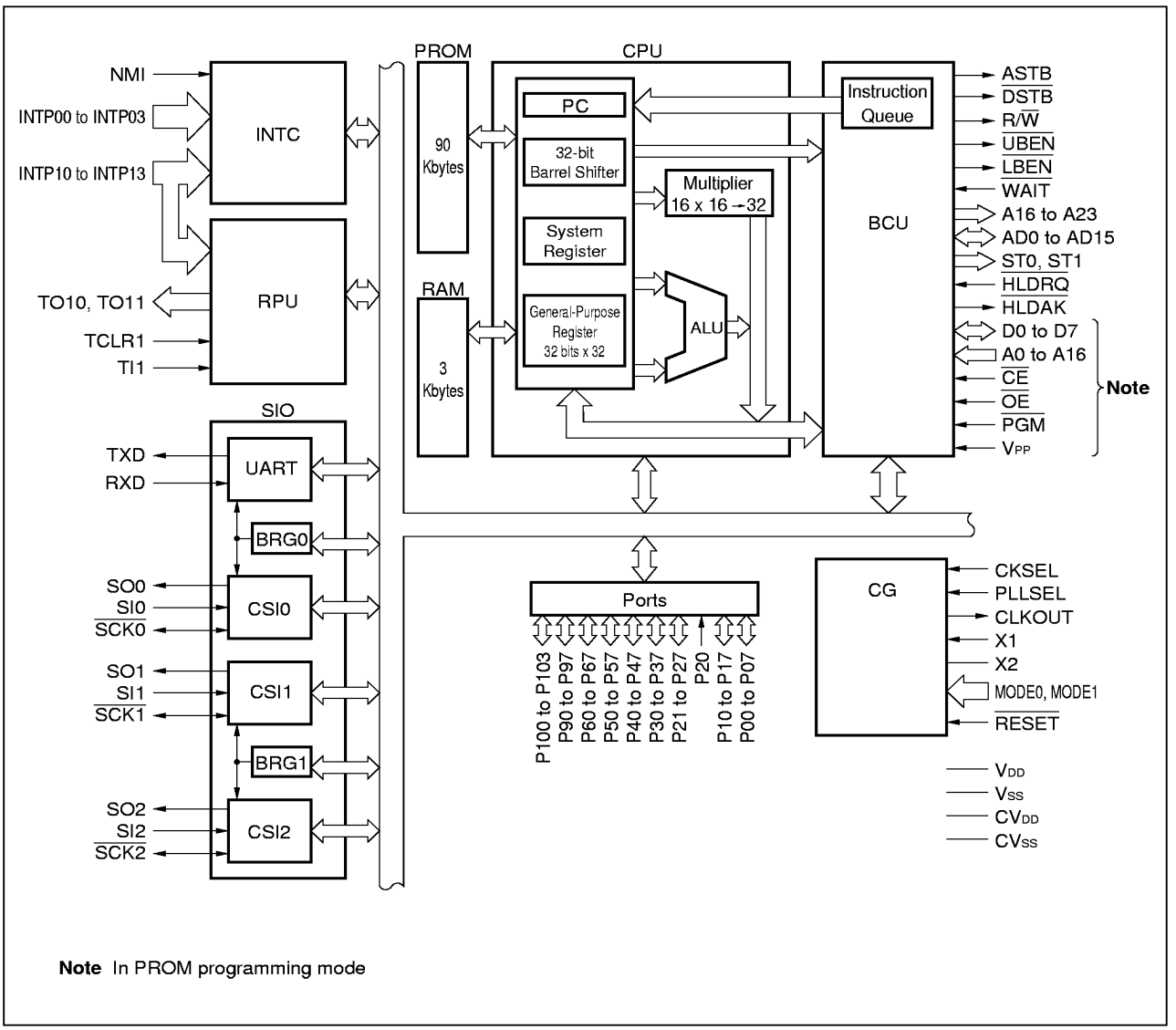
G : Directly connect this pin to V_{SS}.

V : Directly connect this pin to V_{DD}.

Open : Connect nothing.

A0 to A16	:	Address Bus	MODE0, MODE1	:	Programming Mode Set
D0 to D7	:	Data Bus	V_{DD}	:	Power Supply
$\overline{CE}$	:	Chip Enable	V_{SS}	:	Ground
$\overline{OE}$	:	Output Enable	V_{PP}	:	Programming Power Supply
$\overline{PGM}$	:	Programming Mode			

INTERNAL BLOCK DIAGRAM



Note In PROM programming mode

CONTENTS

1. DIFFERENCES BETWEEN μPD70P3002 AND μPD703002

The μPD70P3002 is a PROM version of the μPD703002. Therefore, these two versions are identical except for differences because of the ROM specifications (for example, specifications concerning writing and verifying). Table 1-1 and 1-2 show the differences between the two.

Note that this document mainly describes the PROM specifications of the μPD70P3002. For the other functions, refer to the documents on the μPD703002.

Table 1-1. Differences between μPD70P3002 and μPD703002

Item \ Part Number	μPD70P3002	μPD703002
Internal program memory (electrical writing)	One-time PROM (can be written only once)	Mask ROM
PROM programming pin	Provided	None
Setting of MODE0 and MODE1 pins	• In normal operation mode MODE0, 1 = LH • In PROM programming mode MODE0, 1 = HH	• In normal operation mode MODE0, 1 = LH • In ROM-less mode MODE0, 1 = LL
Electrical specifications	Refer to **Table 1-2 Electrical Specifications Differences between μPD70P3002 and μPD703002**	
Others	Noise immunity and noise radiation differ because circuit scale and mask layout differ.	

Cautions 1. The PROM and mask ROM versions differ from each other in terms of noise immunity and noise emission. When replacing the PROM version with the mask ROM version in the course of switching from experimental production to mass production, perform thorough evaluation with the CS model (not ES model) of the mask ROM version.

2. Directly connect the MODE0 and MODE1 pins to V_{DD} or V_{SS}.

★ **3. If the PROM version is replaced with the mask ROM version, the same code should be written in the vacant area of internal ROM.**

Remark L : low level
H : high level

Table 1-2. Electrical Specifications Differences between μPD70P3002 and μPD703002

Item			Symbol
Absolute maximum ratings	Input voltage		V_{I2}
	Operating ambient temperature		T_A
DC characteristics	Supply current	Operating	I_{DD1}
		In HALT mode	I_{DD2}
		In IDLE mode	I_{DD3}
		In STOP mode	I_{DD4}
Data retention characteristics	Data hold current		I_{DDDR}
AC characteristics	Clock timing	Freerunning oscillation frequency	ϕ_P
Recommended oscillation circuit			—

2. PIN FUNCTION LIST

2.1 Normal Operation Mode (MODE0 = L, MODE1 = H)

2.1.1 Port pins

(1/2)

Pin Name	I/O	Function	Alternate Function
P00	I/O	Port 0 8-bit I/O port Input/output can be specified bit-wise.	TO10
P01			TO11
P02			TCLR1
P03			TI1
P04			INTP10
P05			INTP11
P06			INTP12
P07			INTP13
P10 to P17	I/O	Port 1 8-bit I/O port Input/output can be specified bit-wise.	—
P20	Input	Port 2 P20 is an input-only port. Operates as an NMI input when a valid edge is input. Shows NMI input status at bit 0 of P2 register. P21 to P27 are 7-bit I/O ports. Input/output can be specified bit-wise.	NMI
P21	I/O		INTP00
P22			INTP01
P23			INTP02
P24			INTP03
P25			SO2
P26			SI2
P27			$\overline{SCK2}$
P30	I/O	Port 3 8-bit I/O port Input/output can be specified bit-wise.	SO0
P31			SI0
P32			$\overline{SCK0}$
P33			TXD
P34			RXD
P35			SO1
P36			SI1
P37			$\overline{SCK1}$
P40 to P47	I/O	Port 4 8-bit I/O port Input/output can be specified bit-wise.	AD0 to AD7
P50 to P57	I/O	Port 5 8-bit I/O port Input/output can be specified bit-wise.	AD8 to AD15
P60 to P67	I/O	Port 6 8-bit I/O port Input/output can be specified bit-wise.	A16 to A23

(2/2)

Pin Name	I/O	Function	Alternate Function
P90	I/O	Port 9 8-bit I/O port Input/output can be specified bit-wise.	$\overline{\text{LBEN}}$
P91			$\overline{\text{UBEN}}$
P92			R/$\overline{\text{W}}$
P93			$\overline{\text{DSTB}}$
P94			ASTB
P95			ST0
P96			ST1
P97			—
P100	I/O	Port 10 4-bit I/O port Input/output can be specified bit-wise.	$\overline{\text{HLDAK}}$
P101			$\overline{\text{HLDRQ}}$
P102			—
P103			—

2.1.2 Non-port pins

(1/2)

Pin Name	I/O	Function	Alternate Function
TO10	Output	Pulse signal output of timer 1	P00
TO11			P01
TCLR1	Input	External clear signal input of timer 1	P02
TI1		External count clock input of timer 1	P03
INTP10	Input	External maskable interrupt request input and external capture trigger input of timer 1	P04
INTP11			P05
INTP12			P06
INTP13			P07
NMI	Input	Non-maskable interrupt request input	P20
INTP00	Input	External maskable interrupt request input	P21
INTP01			P22
INTP02			P23
INTP03			P24
SO0	Output	Serial transmit data output of CSI0	P30
SI0	Input	Serial receive data input of CSI0	P31
$\overline{\text{SCK0}}$	I/O	Serial clock I/O of CSI0	P32
SO1	Output	Serial transmit data output of CSI1	P35
SI1	Input	Serial receive data input of CSI1	P36
$\overline{\text{SCK1}}$	I/O	Serial clock I/O of CSI1	P37
SO2	Output	Serial transmit data output of CSI2	P25
SI2	Input	Serial receive data input of CSI2	P26
$\overline{\text{SCK2}}$	I/O	Serial clock I/O of CSI2	P27
TXD	Output	Serial transmit data output of UART	P33
RXD	Input	Serial receive data input of UART	P34

(2/2)

Pin Name	I/O	Function	Alternate Function
AD0 to AD7	I/O	16-bit multiplexed address/data bus when external memory is connected	P40 to P47
AD8 to AD15			P50 to P57
A16 to A23	Output	High-order address bus when external memory is connected	P60 to P67
$\overline{LBEN}$	Output	Low-order byte enable signal output of external data bus	P90
$\overline{UBEN}$		High-order byte enable signal output of external data bus	P91
R/$\overline{W}$		External read/write status output	P92
$\overline{DSTB}$		External data strobe signal output	P93
ASTB		External address strobe signal output	P94
ST0		External bus cycle status output	P95
ST1			P96
$\overline{HLDAK}$	Output	Bus hold acknowledge output	P100
$\overline{HLDRQ}$	Input	Bus hold request input	P101
CLKOUT	Output	System clock output	—
CKSEL	Input	Input specifying operation mode of clock generator	—
PLLSEL	Input	Input specifying PLL multiplication coefficient	—
$\overline{WAIT}$	Input	Control signal input inserting wait state in bus cycle	—
MODE0, MODE1	Input	Operation mode specification	—
$\overline{RESET}$	Input	System reset input	—
X1	Input	System clock oscillator connection	—
X2	—	Input external clock to X1 to supply external clock	—
CV_{DD}	—	Positive power supply for internal clock generator	—
CV_{SS}	—	Ground potential for internal clock generator	—
V_{DD}	—	Positive power supply	—
V_{SS}	—	Ground potential	—
IC0	—	Internally connected	—

2.2 PROM Programming Mode (MODE0 = H, MODE1 = H)

Pin Name	Function	Function in Normal Mode
A0 to A7	Low-order address (A0 to A7) input	P60/A16 to P67/A23
A8, A9, A10 to A16	High-order address (A8 to A16) input	P50/AD8, P20/NMI, P51/AD9 to P57/AD15
D0 to D7	Data I/O	P40/AD0 to P47/AD7
$\overline{CE}$	$\overline{CE}$ (chip enable) input	P25/SO2
$\overline{OE}$	$\overline{OE}$ (output enable) input	P26/SI2
$\overline{PGM}$	$\overline{PGM}$ (program) input	P27/$\overline{SCK2}$
V_{PP}	Power for program writing	IC0
MODE0, MODE1	Operation mode specification	MODE0, MODE1

2.3 Pin I/O Circuits and Recommended Connections of Unused Pins

Table 2-1 shows the I/O circuit type of each pin in the normal operation mode, and the recommended connections of the unused pins. Figure 2-1 shows a partially simplified diagram of each circuit.

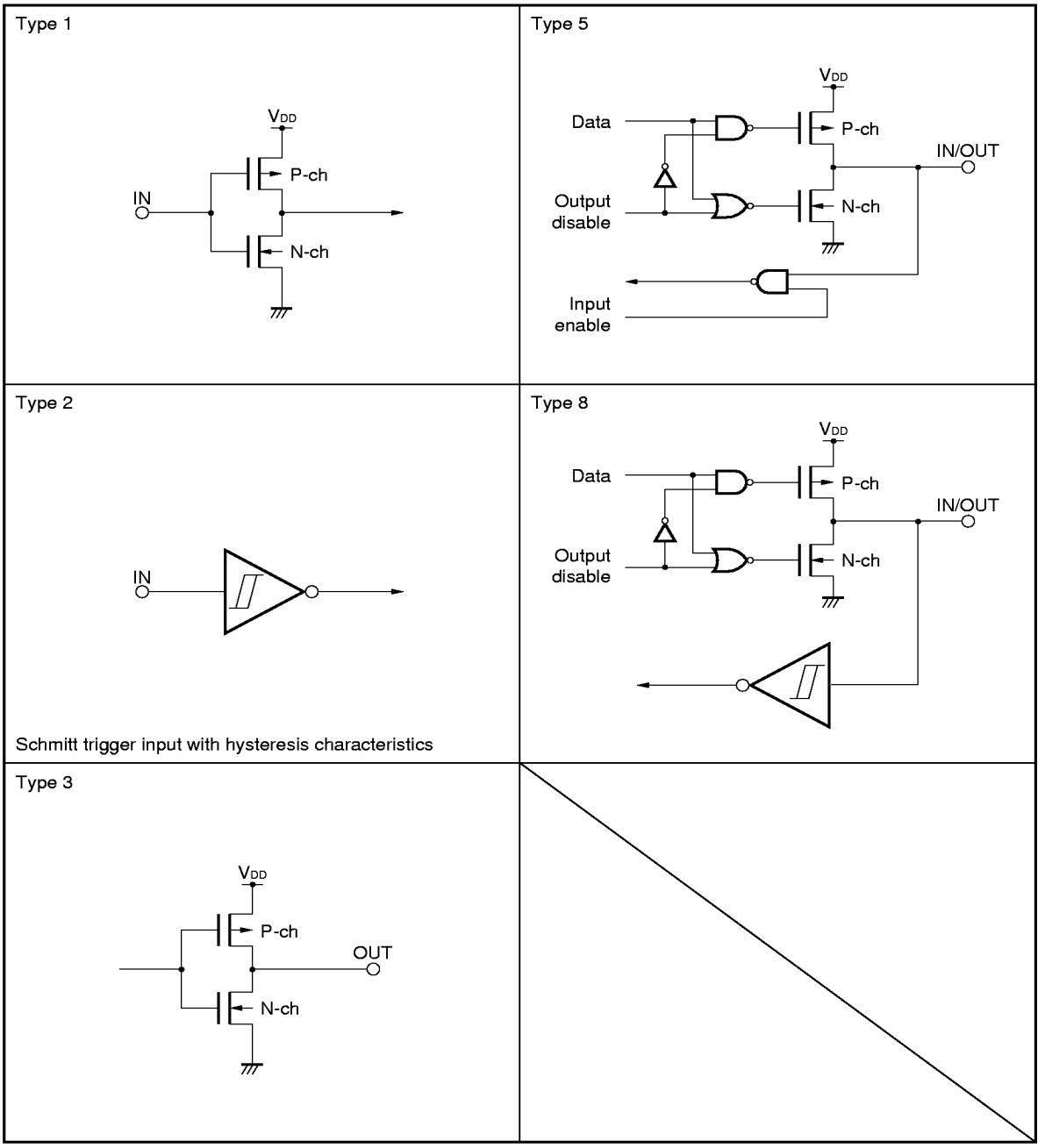
In the PROM programming mode, connect the unused pins by referring to the diagram in **PIN CONFIGURATION**.

When connecting a pin to V_{DD} or V_{SS} via a resistor, use of a resistor of 3 to 10 kΩ is recommended.

Table 2-1. Types of Pin I/O Circuits and Recommended Connections of Unused Pins

Pin	I/O Circuit Type	Recommended Connections
P00/TO10, P01/TO11	5	Input : Individually connect to V_{DD} or V_{SS} via resistor. Output : Open
P02/TCLR1, P03/TI1 P04/INTP10 to P07/INTP13	8	
P10 to P17	5	
P20/NMI	2	Directly connect to V_{SS}.
P21/INTP00 to P24/INTP03	8	Input : Individually connect to V_{DD} or V_{SS} via resistor. Output : Open
P25/SO2	5	
P26/SI2, P27/$\overline{SCK2}$	8	
P30/SO0	5	
P31/SI0, P32/$\overline{SCK0}$	8	
P33/TXD, P34/RXD, P35/SO1	5	
P36/SI1, P37/$\overline{SCK1}$	8	
P40/AD0 to P47/AD7	5	
P50/AD8 to P57/AD15		
P60/A16 to P67/A23		
P90/$\overline{LBEN}$		
P91/$\overline{UBEN}$		
P92/R/$\overline{W}$		
P93/$\overline{DSTB}$		
P94/ASTB		
P95/ST0, P96/ST1		
P97		
P100/$\overline{HLDAK}$		
P101/$\overline{HLDRQ}$		
P102, P103		
CLKOUT	3	Open
CKSEL	2	—
PLLSEL	2	—
$\overline{WAIT}$	1	Directly connect to V_{DD}.
MODE0, MODE1	2	—
$\overline{RESET}$		
IC0	—	Directly connect to V_{SS}.
★ CV_{DD}	—	Directly connect to V_{DD}.
★ CV_{SS}	—	Directly connect to V_{SS}.

Figure 2-1. Pin I/O Circuits



3. PROM PROGRAMMING

The μPD70P3002 has a 90 Kbytes × 8 bit PROM that can be electrically written. To program this PROM, set the PROM programming mode by using the V_{PP}, MODE0, and MODE1 pins.

The programming characteristics are compatible with those of the μPD27C1001A.

Table 3-1. Pin Functions in PROM Programming Mode

Function	Normal Operation Mode	PROM Programming Mode
Address input	P60/A16 to P67/A23, P50/AD8, P20/NMI, P51/AD9 to P57/AD15	A0 to A16
Data I/O	P40/AD0 to P47/AD7	D0 to D7
Program input	P27/$\overline{SCK2}$	$\overline{PGM}$
Chip enable input	P25/SO2	$\overline{CE}$
Output enable input	P26/SI2	$\overline{OE}$
Program voltage	IC0	V_{PP}
Mode specification	MODE0, MODE1	

3.1 Operation Mode

To set the programming writing/verify mode, set as follows: V_{PP} = +12.5 V, MODE0 = H, MODE1 = H

In this mode, the modes shown in Table 3-2 can be selected by using the $\overline{CE}$, $\overline{OE}$, and $\overline{PGM}$ pins.

To read the contents of the PROM, set the read mode.

Connect the unused pins by referring to the diagram in **PIN CONFIGURATION**.

Table 3-2. Operation Modes for PROM Programming

Operation Mode	MODE0	MODE1	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{DD}	D0 to D7
Page data latch mode	H	H	H	L	H	+12.5 V	+6.5V	Data input
Page write mode			H	H	L			High impedance
Byte write mode			L	H	L			Data input
Program verify mode			L	L	H			Data output
Program inhibit mode			x	L	L			High impedance[Note]
			x	H	H			
Read mode			L	L	H	+5.0 V	+5.0 V	Data output
Output disable mode			L	H	x			High impedance[Note]
Standby mode			H	x	x			High impedance[Note]

Note L or H can be input (address input is invalid).

Remark x: L or H

(1) Page data latch mode

The page data latch mode can be set by making the $\overline{CE}$ and $\overline{PGM}$ pins high and $\overline{OE}$ pin low at the beginning of the page write mode.

In the page data latch mode, 1 page or 4 bytes of data are latched to the internal address/data latch circuit.

(2) Page write mode

In this mode, page write is executed by applying a program pulse of 0.1 ms to the $\overline{PGM}$ pin when $\overline{CE}$ = H and $\overline{OE}$ = H after 1 page or 4 bytes of addresses and data have been latched in the page data latch mode. After that, the program is verified when $\overline{CE}$ = L and $\overline{OE}$ = L.

If the program cannot be written by applying the program pulse once, writing and verification are repeatedly executed X times (X ≤ 10).

(3) Byte write mode

Byte write is executed by applying a program pulse (active low) of 0.1 ms to the $\overline{PGM}$ pin when $\overline{CE}$ = L and $\overline{OE}$ = H. After that, the program is verified when $\overline{OE}$ = L.

If the program cannot be written by applying the program pulse once, writing and verification are repeatedly executed X times (X ≤ 10).

(4) Program verify mode

The program verify mode is set when $\overline{CE}$ = L, $\overline{OE}$ = L, and $\overline{PGM}$ = H.

Check to see if the program has been correctly written, in this mode.

(5) Program inhibit mode

The program inhibit mode is used to write a program to one of several μPD70P3002s whose $\overline{OE}$, V_{PP} and D0 through D7 pins are connected in parallel.

To write a program, either the page write mode or byte write mode above is used. At this time, the program is not written to any device whose $\overline{PGM}$ pin is made high.

(6) Read mode

The read mode is set when $\overline{CE}$ = L, $\overline{OE}$ = L, and $\overline{PGM}$ = H.

(7) Output disable mode

The data output goes into a high-impedance state and the output disable mode is set by making $\overline{CE}$ low and $\overline{OE}$ high.

When two or more μPD70P3002s are connected to the data bus, any one of the devices can be selected and data can be read by controlling the $\overline{OE}$ pin.

(8) Standby mode

The standby mode is set by making $\overline{CE}$ high.

In this mode, the data output goes into a high-impedance state regardless of the status of $\overline{OE}$.

3.2 PROM Writing Procedure

Figure 3-1. Flowchart in Page Program Mode

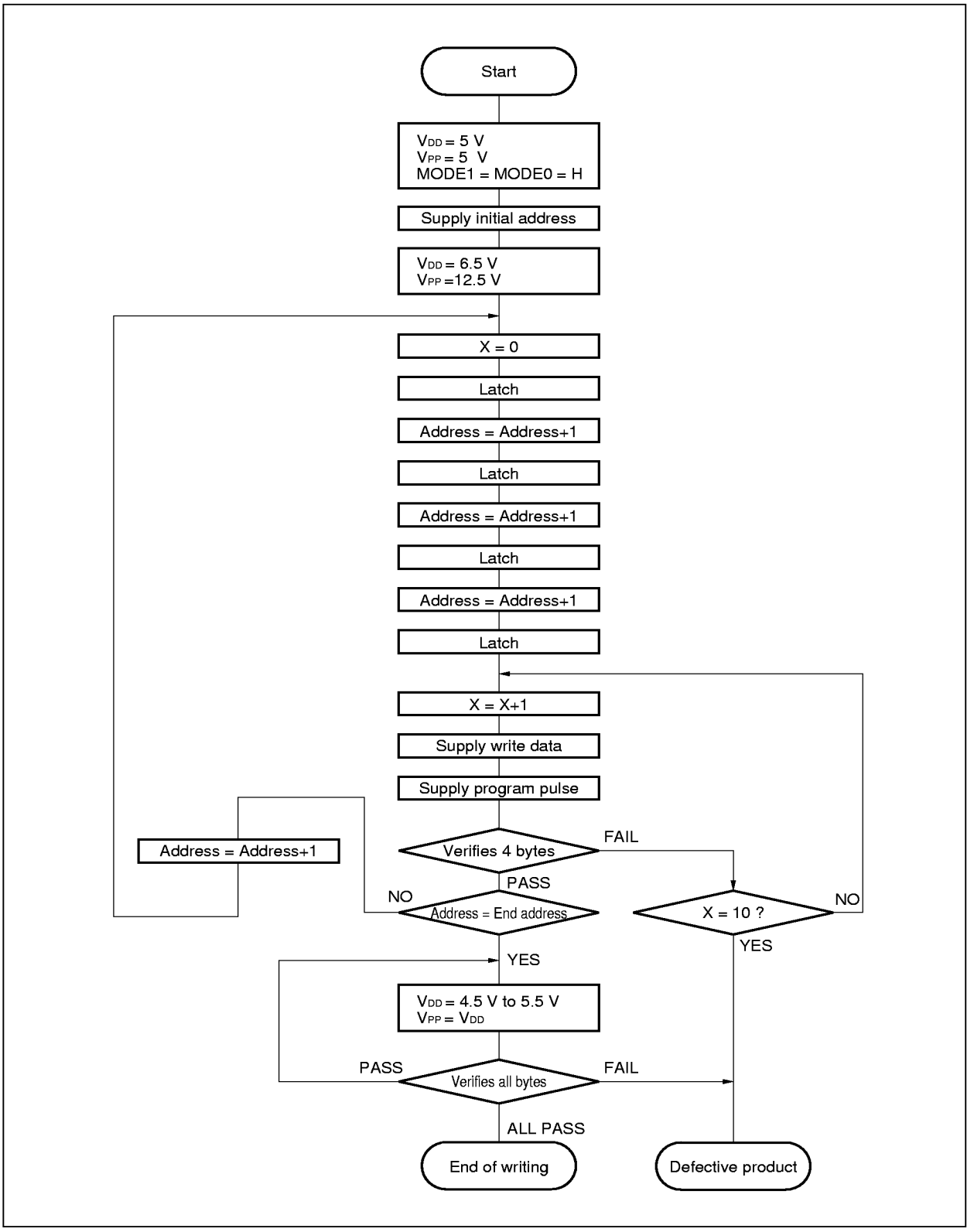
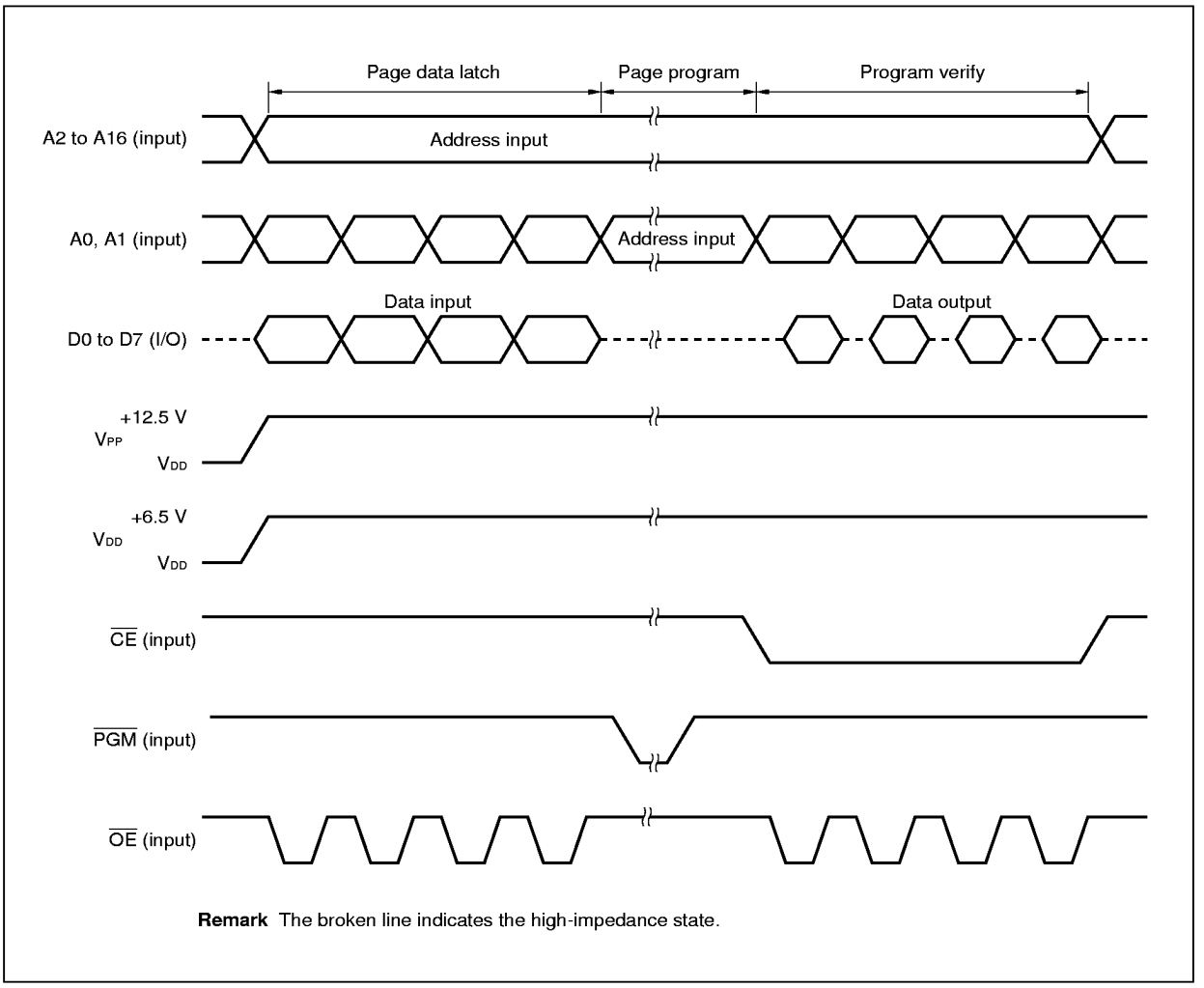


Figure 3-2. PROM Writing/Verify Timing (page program mode)



Remark The broken line indicates the high-impedance state.

Figure 3-3. Flowchart in Byte Program Mode

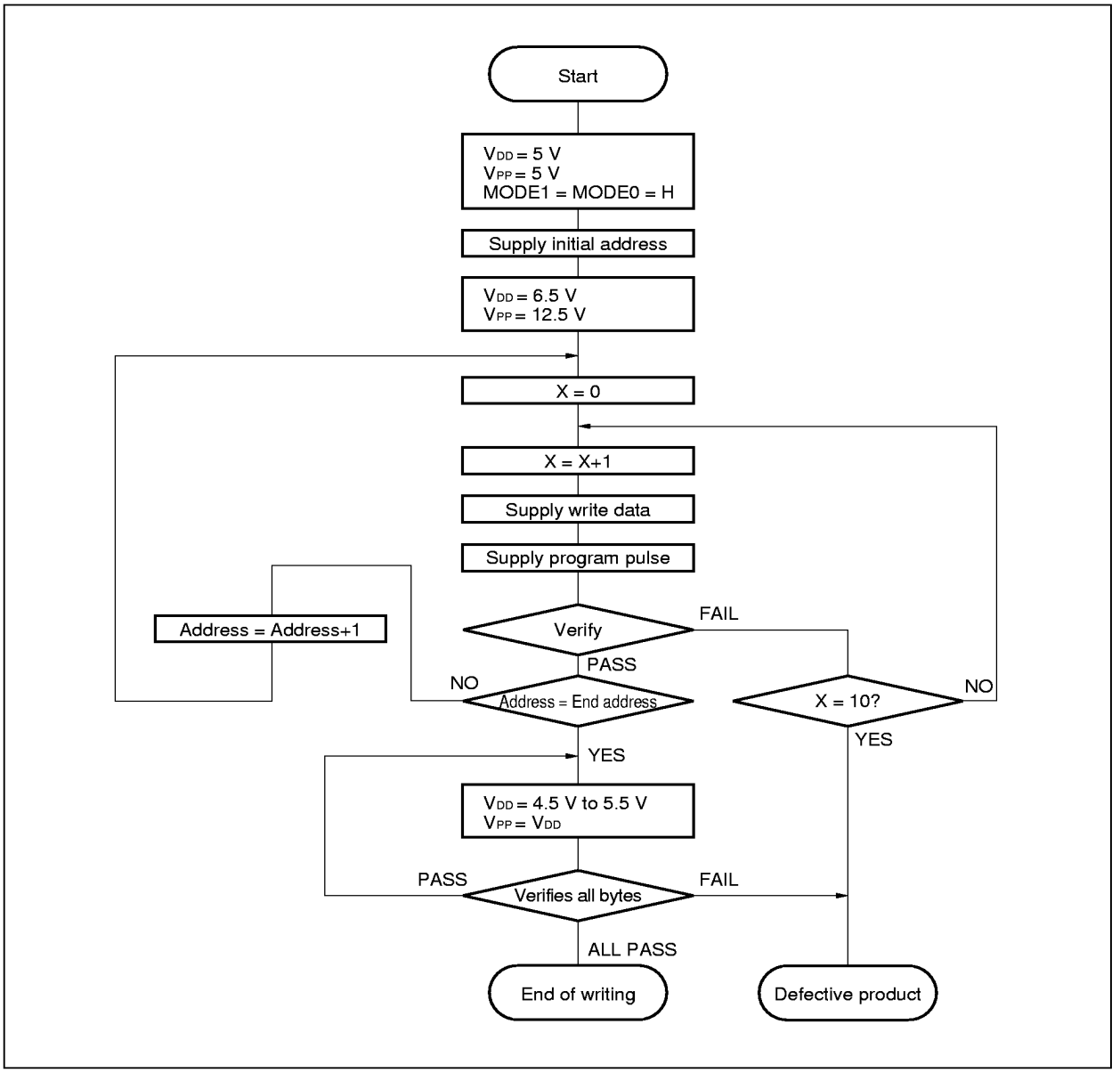
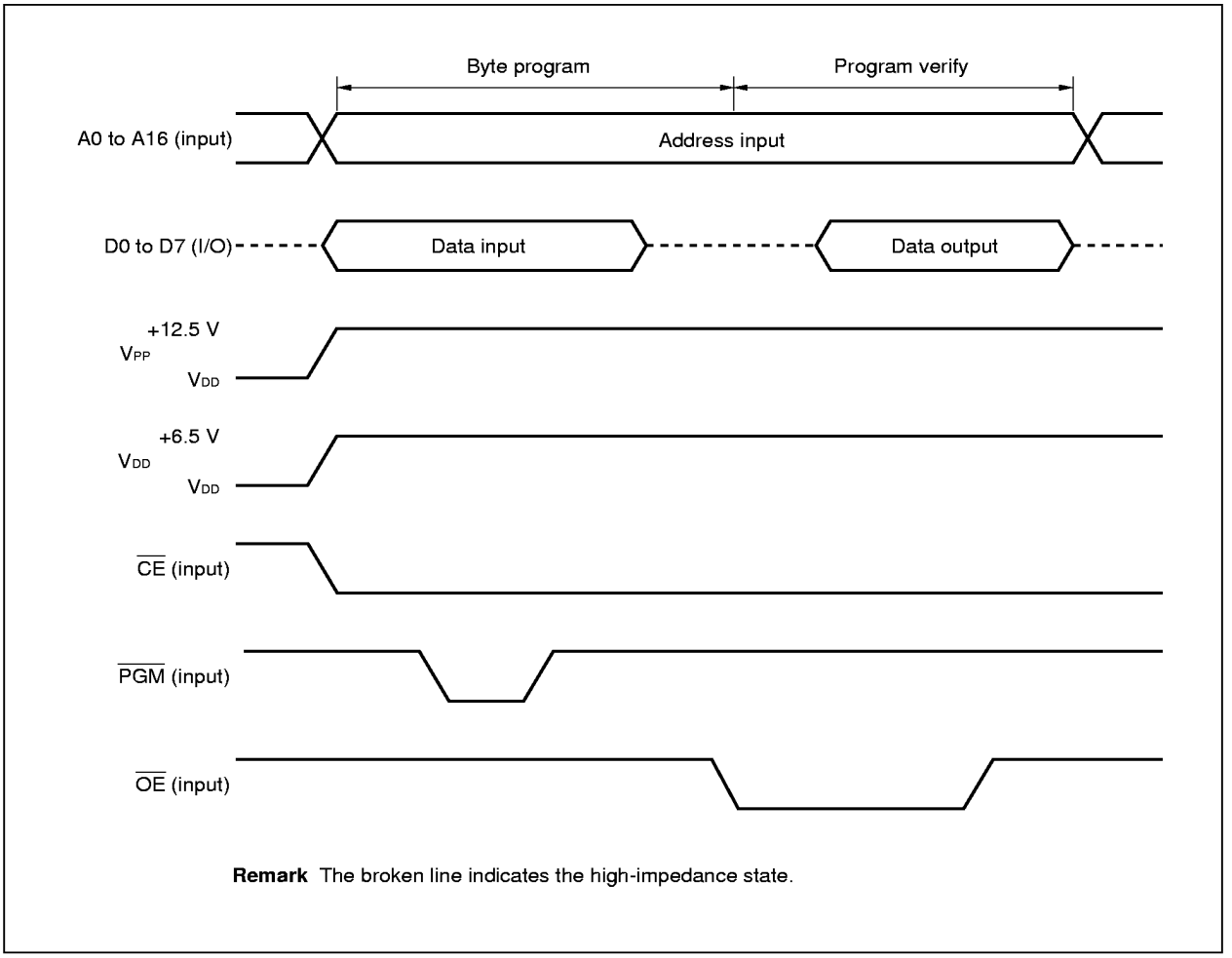


Figure 3-4. PROM Writing/Verifying Timing (byte program mode)



Remark The broken line indicates the high-impedance state.

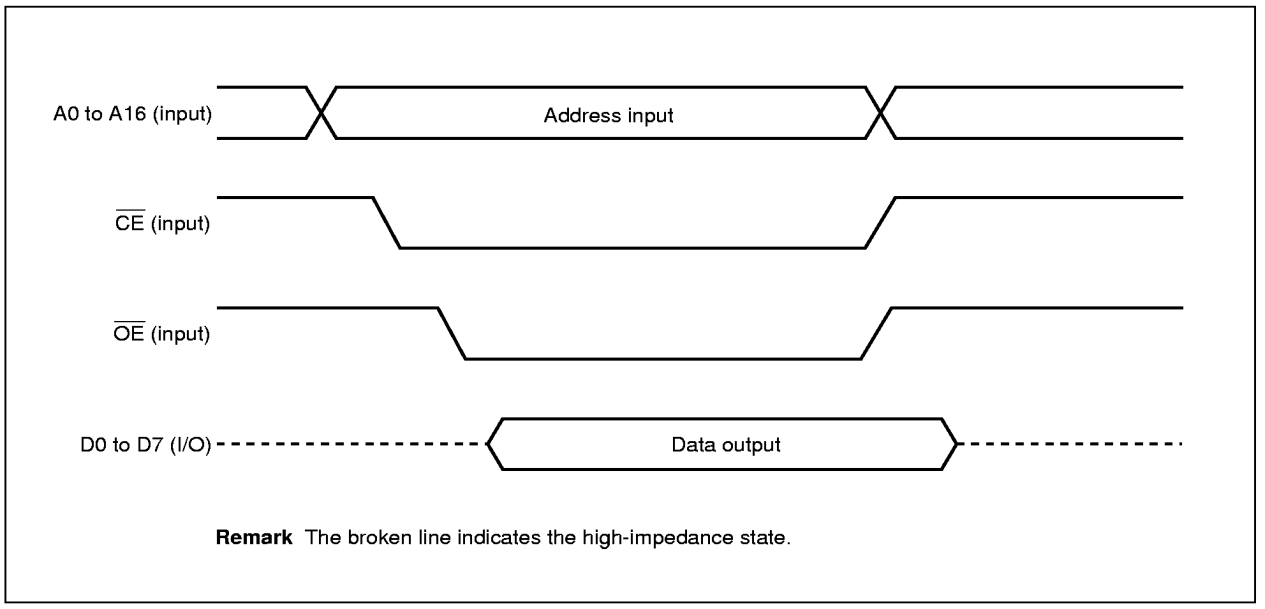
3.3 PROM Reading Procedure

The procedure to read the contents of the PROM to the external data bus (D0 to D7) is as follows:

(1) Fix the MODE0 and MODE1 pins to low level. Connect the unused pins by referring to the diagram in **PIN CONFIGURATION (2) PROM Programming mode**.
(2) Supply +5 V to the V_{DD} and V_{PP} pins.
(3) Input the address of the data to be read to the A0 to A16 pins.
(4) Set the read mode ($\overline{CE}$ = L, $\overline{OE}$ = L).
(5) Data are output to pins D0 to D7.

Figure 3-5 shows the timing of steps (2) to (5) above.

Figure 3-5. PROM Reading Timing



Remark The broken line indicates the high-impedance state.

4. SCREENING OF ONE-TIME PROM VERSION

Because of its structure, the one-time PROM version cannot be completely tested by NEC before shipment. It is recommended to perform screening to verify the PROM, after writing the necessary data to the PROM and storing the device under the following conditions:

Storage Temperature	Storage Time
125°C	24 hours

NEC offers a service, at a charge, called QTOP microcontroller, for writing, marking, screening, and verifying one-time PROMs. For details, consult an NEC representative.

5. NOTES ON RELEASING STOP MODE WHEN EXTERNAL CLOCK IS USED

When an external clock is used, the clock is supplied by an external system.

To release the STOP mode (by $\overline{\text{RESET}}$ or NMI input), therefore, resume clock supply at least 150 μs before inputting the $\overline{\text{RESET}}$ or NMI signal to make sure that a sufficiently long time elapses to allow the PROM to stabilize.

6. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Condition	Ratings	Unit
Supply voltage	V_{DD}	V_{DD} pin	–0.5 to +7.0	V
	CV_{DD}	CV_{DD} pin	–0.5 to +7.0	V
	CV_{SS}	CV_{SS} pin	–0.5 to +0.5	V
Input voltage	V_{I1}	Except X1 pin, V_{DD} = 5.0 V ±10%	–0.5 to V_{DD} + 0.3	V
	V_{I2}	V_{PP} pin in PROM programming mode, V_{DD} = 5.0 V ±10%	–0.5 to +13.5	V
Clock input voltage	V_X	X1 pin, V_{DD} = 5.0 V ±10%	–0.5 to V_{DD} + 1.0	V
Output current, low	I_{OL}	1 pin	4.0	mA
		Total of all pins	100	mA
Output current, high	I_{OH}	1 pin	–4.0	mA
		Total of all pins	–100	mA
Output voltage	V_O	V_{DD} = 5.0 V ±10%	–0.5 to V_{DD} + 0.3	V
Operating ambient temperature	T_A		–10 to +70	°C
Storage temperature	T_{stg}		–65 to +150	°C

Cautions 1. Do not directly connect the output (or I/O) pins of IC products, and do not directly connect them to V_{DD}, V_{CC}, or GND pin. Open-drain pins and open-collector pins may be directly connected to one another however. Moreover, an external circuit that is designed to prevent contention of output can be connected to pins that go into a high-impedance state.

2. Should the absolute maximum rating of even one of the above parameters be exceeded even momentarily, the quality of the product may be degraded. The absolute maximum ratings are, therefore, the values exceeding which the product may be physically damaged. Use the product so that these values are never exceeded.

The normal operating ranges of ratings and conditions in which the quality of the product is guaranteed are specified in the following DC Characteristics and AC Characteristics.

Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	fc = 1 MHz			15	pF
I/O capacitance	C_{IO}	Unmeasured pins returned to 0 V.			15	pF
Output capacitance	C_O				15	pF

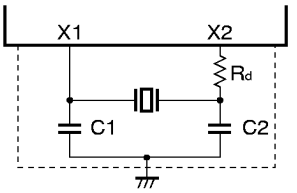
Operating Conditions

Operation Mode	Internal Operating Clock Frequency (ϕ)	Operating Temperature (T_A)	Supply Voltage (V_{DD})
Direct mode	0 to 25 MHz	–10 to +70°C	5.0 V ±10%
PLL mode	Freerunning oscillation frequency to 25 MHz	–10 to +70°C	5.0 V ±10%

Recommended Oscillation Circuit

(a) Ceramic resonator connection (T_A = –10 to +70°C)

(i) Manufacturer: Kyocera



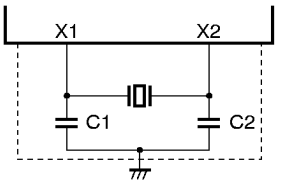
Part Number	Oscillation Frequency f_{XX} (MHz)	Recommended Circuit Constants			Oscillation Voltage Range		Oscillation Stabilization Time (MAX.) T_{OST} (ms)
		C1 (pF)	C2 (pF)	R_d (Ω)	MIN. (V)	MAX. (V)	
KBR-2.0MS	2.0	100	100	820	4.5	5.5	0.80
KBR-2.7MS	2.7	100	100	820	4.5	5.5	0.60
KBR-3.2MS	3.2	82	82	0	4.5	5.5	0.32
KBR-5.0MSB	5.0	33	33	680	4.5	5.5	0.24
KBR-5.0MKC	5.0	Provided	Provided	680	4.5	5.5	0.24
KBR-10.0M	10.0	33	33	0	4.5	5.5	0.20
KBR-13.5MY	13.5	15	15	0	4.5	5.5	0.40
KBR-16.0MY	16.0	10	10	0	4.5	5.5	0.40
KBR-24.0MY	24.0	10	10	0	4.5	5.5	0.26
PBRC5.0A	5.0	33	33	680	4.5	5.5	0.24
PBRC5.0B	5.0	Provided	Provided	680	4.5	5.5	0.24

Cautions 1. Connect the oscillation circuit as closely to X1 and X2 pins as possible.

2. Do not route any other signal lines in the range indicated by the broken line in the above figure.

3. Thoroughly evaluate the compatibility of the μPD70P3002 and resonator.

(ii) Manufacturer: TDK Corp., Murata Mfg.



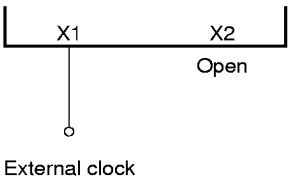
Manufacturer	Part Number	Oscillation Frequency f_{XX} (MHz)	Recommended Circuit Constants		Oscillation Voltage Range		Oscillation Stabilization Time (MAX.) T_{OST} (ms)
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)	
TDK	CCR2.0MC33	2.0	Provided	Provided	4.5	5.5	0.52
	CCR3.2MC3	3.2	Provided	Provided	4.5	5.5	0.34
	CCR5.0MC3	5.0	Provided	Provided	4.5	5.5	0.80
	FCR5.0MC5	5.0	Provided	Provided	4.5	5.5	0.48
	CCR10.0MC5	10.0	Provided	Provided	4.5	5.5	0.22
	CCR16.0MC6	16.0	Provided	Provided	4.5	5.5	0.66
	FCR25.0MCG	25.0	Provided	Provided	4.5	5.5	0.48
Murata Mfg.	CST2.00MG040	2.0	Provided	Provided	4.5	5.5	0.61
	CSA2.00MG040	2.0	100	100	4.5	5.5	0.61
	CST2.70MGW040	2.7	Provided	Provided	4.5	5.5	0.47
	CSA2.70MG040	2.7	100	100	4.5	5.5	0.47
	CST3.20MGW040	3.2	Provided	Provided	4.5	5.5	0.5
	CSA3.20MG040	3.2	100	100	4.5	5.5	0.5
	CST5.00MGW040	5.0	Provided	Provided	4.5	5.5	0.5
	CSA5.00MG040	5.0	100	100	4.5	5.5	0.5
	CST10.0MTW	10.0	Provided	Provided	4.5	5.5	0.1
	CSA10.0MTZ	10.0	30	30	4.5	5.5	0.1
	CST13.50MXW040	13.5	Provided	Provided	4.5	5.5	0.41
	CST13.50MXZ040	13.5	30	30	4.5	5.5	0.41
	CST16.00MXW040	16.0	Provided	Provided	4.5	5.5	0.35
	CST16.00MXZ0403	16.0	30	30	4.5	5.5	0.35
	CST25.00MXW040	25.0	Provided	Provided	4.5	5.5	0.24
	CSA25.00MXZ040	25.0	15	15	4.5	5.5	0.24

Cautions 1. Connect the oscillation circuit as closely to X1 and X2 pins as possible.

2. Do not route any other signal lines in the range indicated by the broken line in the above figure.

3. Thoroughly evaluate the compatibility of the μPD70P3002 and resonator.

(b) External clock input



Caution Input CMOS level voltage to the X1 pin.

DC Characteristics (T_A = –10 to +70°C, V_{DD} = 5.0 V ±10%, V_{SS} = 0 V)

Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input voltage, high		V_{IH}	Except X1 and **Note**	2.2		V_{DD}	V
			Note	0.8V_{DD}		V_{DD}	V
Input voltage, low		V_{IL}	Except X1 and **Note**	0		0.8	V
			Note	0		0.2V_{DD}	V
X1 clock input voltage, high		V_{XH}	Direct mode	0.8V_{DD}		V_{DD}	V
			PLL mode	0.8V_{DD}		V_{DD}	V
X1 clock input voltage, low		V_{XL}	Direct mode	0		0.6	V
			PLL mode	0		0.6	V
Schmitt trigger input threshold voltage		V_{T^+}	**Note**, rising		3.0		V
		V_{T^-}	**Note**, falling		2.0		V
Schmitt trigger input hysteresis width		$V_{T^+} - V_{T^-}$	**Note**	0.5			V
Output voltage, high		V_{OH}	I_{OH} = –2.5 mA	0.7V_{DD}			V
			I_{OH} = –100 μA	V_{DD} – 0.4			V
Output voltage, low		V_{OL}	I_{OC} = 2.5 mA			0.45	V
Input leakage current, high		I_{LIH}	V_I = V_{DD}			10	μA
Input leakage current, low		I_{LIL}	V_I = 0 V			–10	μA
Output leakage current, high		I_{LOH}	V_O = V_{DD}			10	μA
Output leakage current, low		I_{LOL}	V_O = 0 V			–10	μA
Supply current	Operating	I_{DD1}	Direct mode		2.0 × ϕ + 14	3.0 × ϕ + 15	mA
			PLL mode		2.1 × ϕ + 16	3.2 × ϕ + 18	mA
	In HALT mode	I_{DD2}	Direct mode		0.7 × ϕ + 3	0.9 × ϕ + 10	mA
			PLL mode		0.8 × ϕ + 5	1.1 × ϕ + 13	mA
	In IDLE mode	I_{DD3}	Direct mode		20 × ϕ + 300	28 × ϕ + 500	μA
			PLL mode		0.2 × ϕ + 2	0.4 × ϕ + 2	mA
	In STOP mode	I_{DD4}			1	50	μA

Note $\overline{\text{RESET}}$, P02/TCLR1, P03/TI1, P04/INTP10 to P07/INTP13, P20/NMI, P21/INTP00 to P24/INTP03, P26/SI2, P27/$\overline{\text{SCK2}}$, P31/SI0, P32/$\overline{\text{SCK0}}$, P36/SI1, P37/$\overline{\text{SCK1}}$, MODE0, MODE1, CKSEL

Remarks 1. TYP. value is a value for your reference at T_A = 25°C and V_{DD} = 5.0 V.

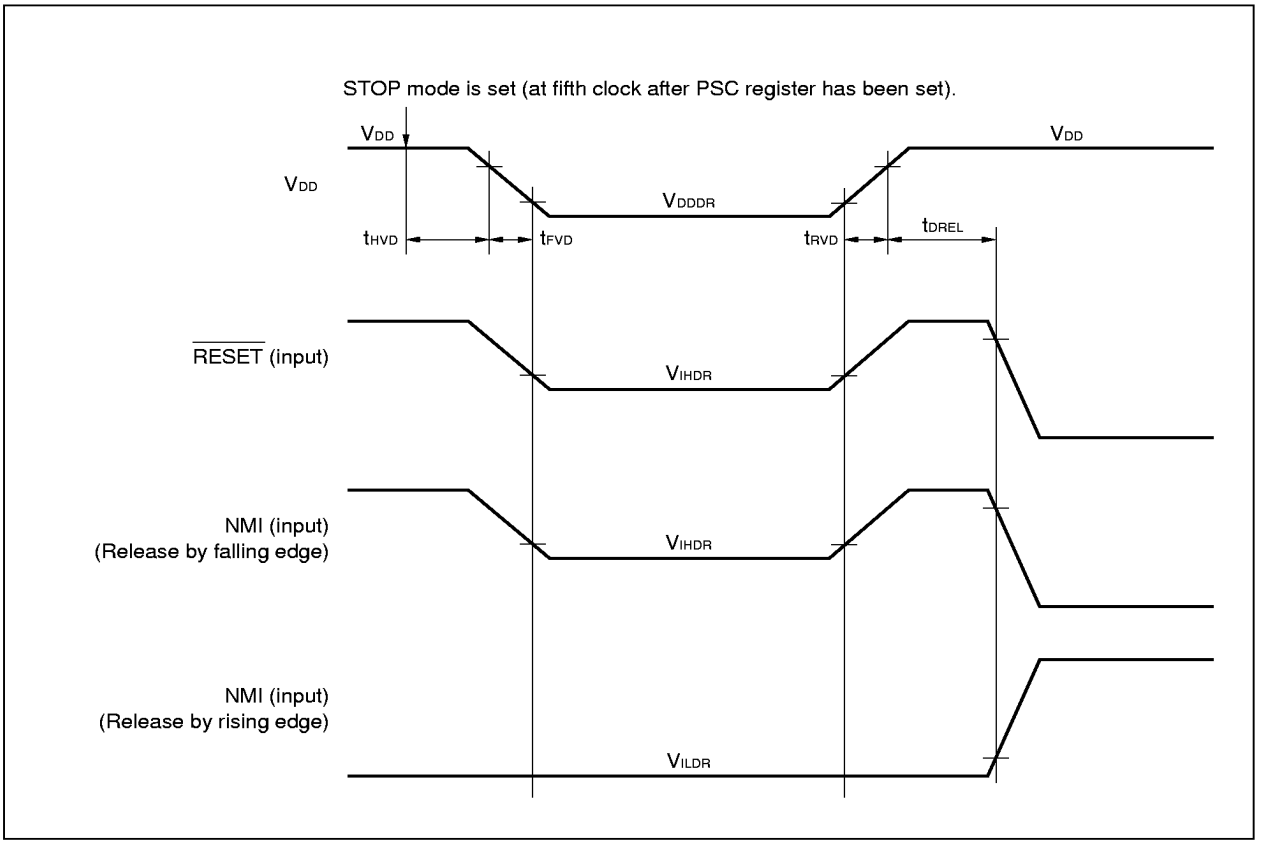
2. ϕ : Internal operating clock frequency

Data Retention Characteristics (T_A = –10 to +70°C)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Data hold voltage	V_{DDDR}	STOP mode	1.5		5.5	V
Data hold current	I_{DDDR}	$V_{DD} = V_{DDDR}$		0.2V_{DDDR}	50	μA
Supply voltage rise time	t_{RVD}		200			μs
Supply voltage fall time	t_{FVD}		200			μs
Supply voltage hold time (from STOP mode setting)	t_{HVD}		0			ms
STOP mode release signal input time	t_{DREL}		0			ns
Data hold input voltage, high	V_{IHDR}	**Note**	0.9V_{DDDR}		V_{DDDR}	V
Data hold input voltage, low	V_{ILDR}	**Note**	0		0.1V_{DDDR}	V

Note $\overline{\text{RESET}}$, P02/TCLR1, P03/TI1, P04/INTP10 to P07/INTP13, P20/NMI, P21/INTP00 to P24/INT03, P26/SI2, P27/$\overline{\text{SCK2}}$, P31/SI0, P32/$\overline{\text{SCK0}}$, P36/SI1, P37/$\overline{\text{SCK1}}$, MODE0, MODE1, CKSEL, X1

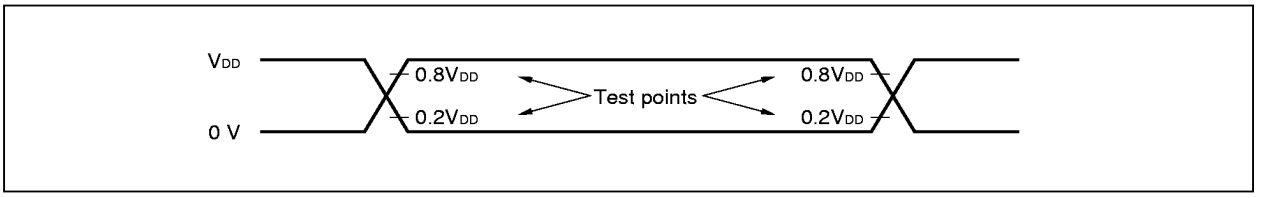
Remark TYP. value is a value for your reference at T_A = 25°C and V_{DD} = 5.0 V.



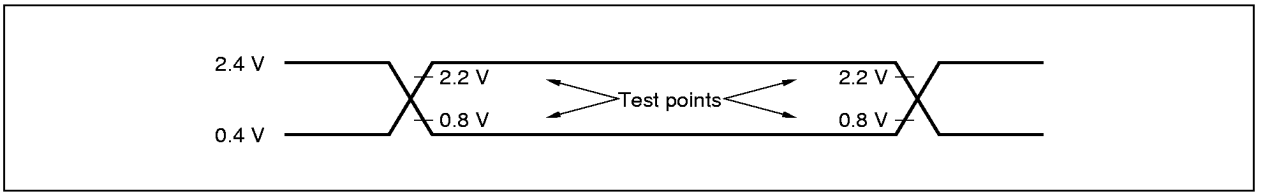
AC Characteristics (T_A = –10 to +70°C, V_{DD} = 5.0 V ±10%, V_{SS} = 0 V, C_L (output pin load capacitance) = 50 pF)

AC test input wave

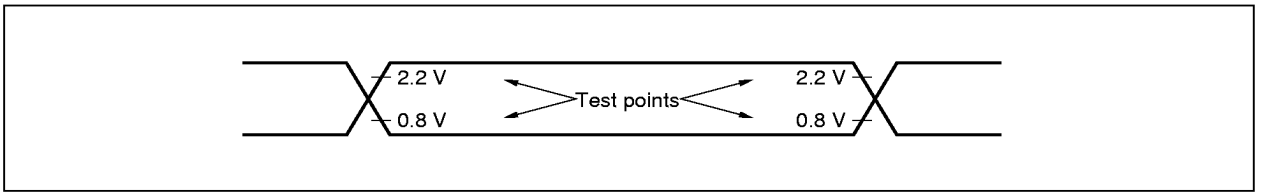
(a) $\overline{\text{RESET}}$, P02/TCLR1, P03/TI1, P04/INTP10 to P07/INTP13, P20/NMI, P21/INTP00 to P24/INTP03, P26/SI2, P27/$\overline{\text{SCK2}}$, P31/SI0, P32/$\overline{\text{SCK0}}$, P36/SI1, P37/$\overline{\text{SCK1}}$, MODE0, MODE1, CKSEL, X1



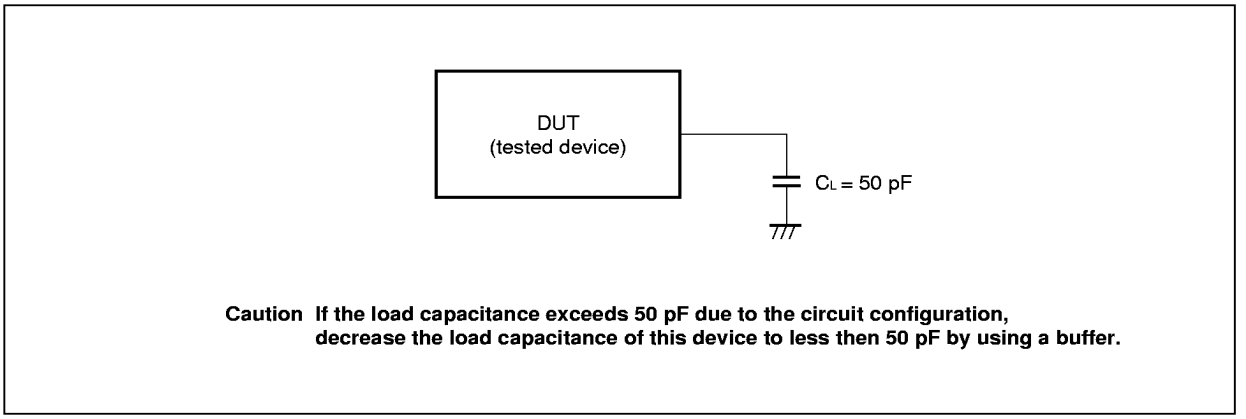
(b) Other than (a)



AC test output test point



Load condition



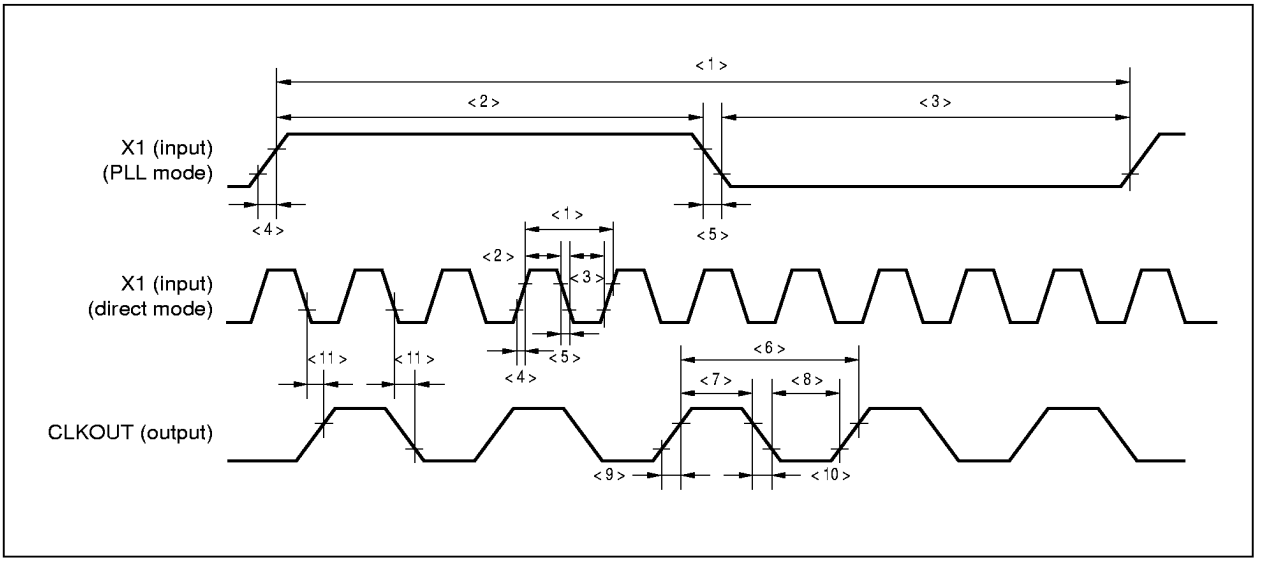
Caution If the load capacitance exceeds 50 pF due to the circuit configuration, decrease the load capacitance of this device to less then 50 pF by using a buffer.

(1) Clock timing

Parameter	Symbol		Condition	MIN.	MAX.	Unit
X1 input cycle	<1>	t_{CYX}	Direct mode	20	DC	ns
			PLL mode ($f_{XX} = \phi/5$)	200	285	ns
			PLL mode ($f_{XX} = \phi$)	40	100	ns
X1 input width, high	<2>	t_{WXH}	Direct mode	7		ns
			PLL mode ($f_{XX} = \phi/5$)	80		ns
			PLL mode ($f_{XX} = \phi$)	10		ns
X1 input width, low	<3>	t_{WXL}	Direct mode	7		ns
			PLL mode ($f_{XX} = \phi/5$)	80		ns
			PLL mode ($f_{XX} = \phi$)	10		ns
X1 input rise time	<4>	t_{XR}	Direct mode		7	ns
			PLL mode ($f_{XX} = \phi/5$)		15	ns
			PLL mode ($f_{XX} = \phi$)		7	ns
X1 input fall time	<5>	t_{XF}	Direct mode		7	ns
			PLL mode ($f_{XX} = \phi/5$)		15	ns
			PLL mode ($f_{XX} = \phi$)		7	ns
CPU operating frequency	—	ϕ		0	25	MHz
CLKOUT output cycle	<6>	t_{CYK}		40	DC	ns
CLKOUT width, high	<7>	t_{WKH}		0.5T – 10		ns
CLKOUT width, low	<8>	t_{WKL}		0.5T – 10		ns
CLKOUT rise time	<9>	t_{KR}			5	ns
CLKOUT fall time	<10>	t_{KF}			5	ns
CLKOUT delay time from X1 ↓	<11>	t_{DXK}	Direct mode	3	17	ns

Remark T = t_{CYK}

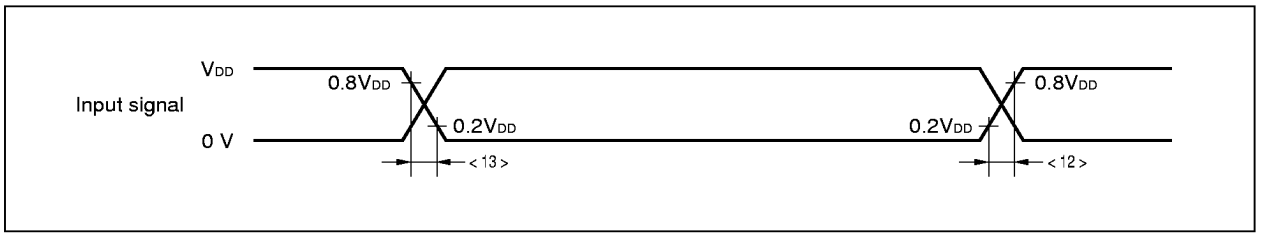
Parameter	Symbol		Condition	TYP.	Unit
Freerunning oscillation frequency	—	ϕ_P	PLL mode	3.2	MHz



(2) Input wave

(a) $\overline{\text{RESET}}$, P02/TCLR1, P03/TI1, P04/INTP10 to P07/INTP13, P20/NMI, P21/INTP00 to P24/INTP03, P26/SI2, P27/$\overline{\text{SCK2}}$, P31/SI0, P32/$\overline{\text{SCK0}}$, P36/SI1, P37/$\overline{\text{SCK1}}$, MODE0, MODE1, CKSEL, X1

Parameter	Symbol		Condition	MIN.	MAX.	Unit
Input rise time	<12>	t_{IR2}			20	ns
Input fall time	<13>	t_{IF2}			20	ns

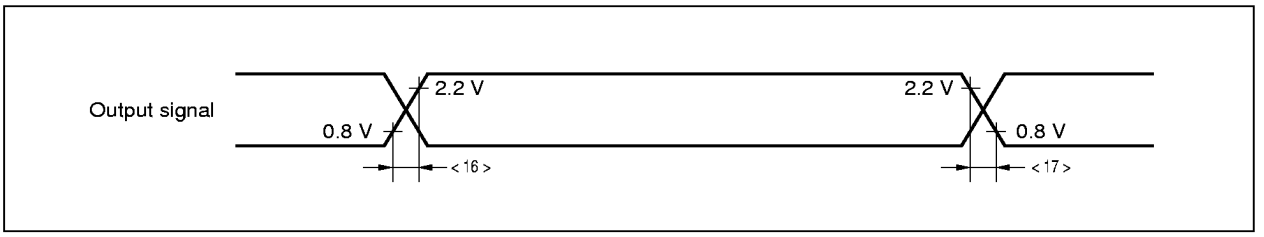


(b) Other than (a)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
Input rise time	<14>	t_{IR1}			10	ns
Input fall time	<15>	t_{IF1}			10	ns

(3) Output wave (other than CLKOUT)

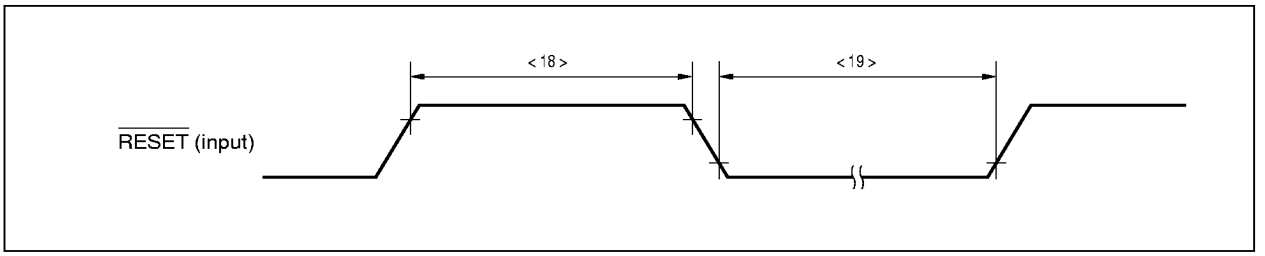
Parameter	Symbol		Condition	MIN.	MAX.	Unit
Output rise time	<16>	t_{OR}			10	ns
Output fall time	<17>	t_{OF}			10	ns



(4) Reset timing

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{\text{RESET}}$ width, high	<18>	t_{WRSH}		500		ns
$\overline{\text{RESET}}$ width, low	<19>	t_{WRSL}	On power application, or on releasing STOP mode	500 + T_{OST}		ns
			Except on power application, or except on releasing STOP mode	500		ns

Remark T_{OST}: Oscillation stabilization time



(5) Read timing (1/2)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
CLKOUT ↑→ address delay time	<20>	t_{DKA}		3	20	ns
CLKOUT ↑→ address float delay time	<21>	t_{FKA}		3	15	ns
CLKOUT ↓→ ASTB delay time	<22>	t_{DKST}		3	15	ns
CLKOUT ↑→ $\overline{DSTB}$ delay time	<23>	t_{DKD}		3	15	ns
CLKOUT ↑→ status delay time	<24>	t_{DKS}		3	15	ns
Data input setting time (to CLKOUT ↑)	<25>	t_{SIDK}		5		ns
Data input hold time (from CLKOUT ↑)	<26>	t_{HKID}		5		ns
$\overline{WAIT}$ setting time (to CLKOUT ↓)	<27>	t_{SWTK}		5		ns
$\overline{WAIT}$ hold time (from CLKOUT ↓)	<28>	t_{HKWT}		5		ns
Address hold time (from CLKOUT ↑)	<29>	t_{HKA}		0		ns
Address setting time (to ASTB ↓)	<30>	t_{SAST}		0.5T – 10		ns
Address hold time (from ASTB ↓)	<31>	t_{HSTA}		0.5T – 10		ns
$\overline{DSTB}$ ↓→ address float delay time	<32>	t_{FDA}			0	ns
Data input setting time (to address)	<33>	t_{SAID}			(2 + n)T – 20	ns
Data input setting time (to $\overline{DSTB}$ ↓)	<34>	t_{SDID}			(1 + n)T – 20	ns
ASTB ↓→ $\overline{DSTB}$ ↓ delay time	<35>	t_{DSTD}		0.5T – 10		ns
Data input hold time (from $\overline{DSTB}$ ↑)	<36>	t_{HDID}		0		ns
$\overline{DSTB}$ ↑→ address output delay time	<37>	t_{DDA}		(1 + i)T		ns
$\overline{DSTB}$ ↑→ ASTB ↑ delay time	<38>	t_{DDSTH}		0.5T – 10		ns
$\overline{DSTB}$ ↑→ ASTB ↓ delay time	<39>	t_{DDSTL}		(1.5 + i)T – 10		ns
Status setting time (to ASTB ↓)	<40>	t_{SSST}		0.5T – 10		ns
Status hold time (from ASTB ↑)	<41>	t_{HSTS}		0.5T – 10		ns
$\overline{DSTB}$ width, low	<42>	t_{WDL}		(1 + n)T – 10		ns
ASTB width, high	<43>	t_{WSTH}		T – 10		ns
$\overline{WAIT}$ setting time (to address)	<44>	t_{SAWT1}	n ≥ 1		1.5T – 20	ns
	<45>	t_{SAWT2}			(1.5 + n)T – 20	ns
$\overline{WAIT}$ hold time (from address)	<46>	t_{HAWT1}	n ≥ 1	(0.5 + n)T		ns
	<47>	t_{HAWT2}		(1.5 + n)T		ns
$\overline{WAIT}$ setting time (to ASTB ↓)	<48>	t_{SSTWT1}	n ≥ 1		T – 15	ns
	<49>	t_{SSTWT2}			(1 + n)T – 15	ns
$\overline{WAIT}$ hold time (from ASTB ↓)	<50>	t_{HSTWT1}	n ≥ 1	nT		ns
	<51>	t_{HSTWT2}		(1 + n)T		ns

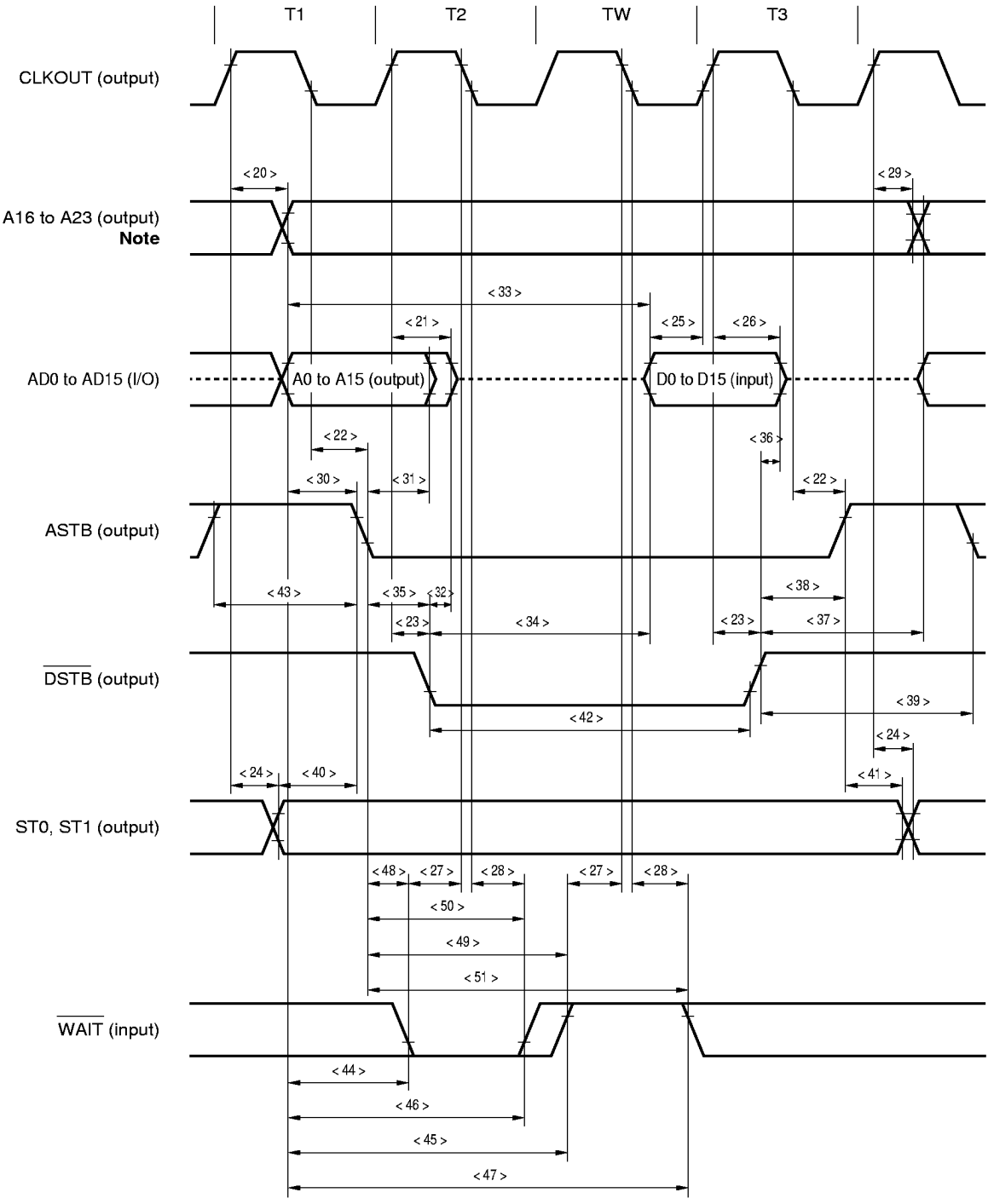
Remarks 1. T = t_{CYK}

2. n indicates the number of wait clocks inserted in the bus cycle. The sampling timing differs when the programmable wait state is inserted.

3. i indicates the number of idle states (0 or 1) to be inserted in the read cycle.

4. Be sure to observe at least one of data input hold times t_{HKID} (<26>) and t_{HDID} (<36>).

(5) Read Timing (2/2): 1 wait



Note R/$\overline{W}$ (output), $\overline{UBEN}$ (output), $\overline{LBEN}$ (output)

Remark The broken line indicates the high-impedance state.

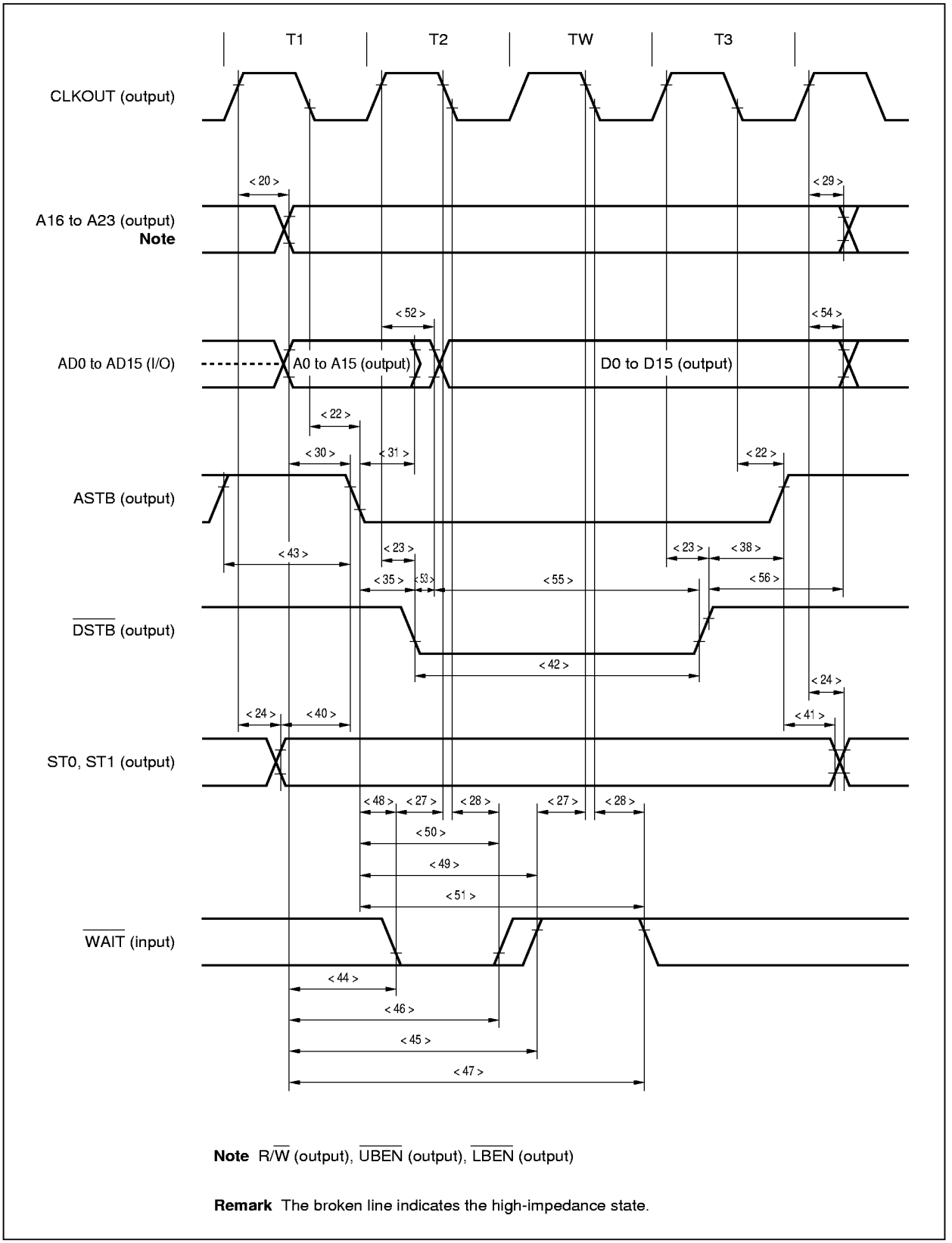
(6) Write timing (1/2)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
CLKOUT ↑→ address delay time	<20>	t_{DKA}		3	20	ns
CLKOUT ↓→ ASTB delay time	<22>	t_{DKST}		3	15	ns
CLKOUT ↑→ $\overline{DSTB}$ delay time	<23>	t_{DKD}		3	15	ns
CLKOUT ↑→ status delay time	<24>	t_{DKS}		3	15	ns
$\overline{WAIT}$ setting time (to CLKOUT ↓)	<27>	t_{SWTK}		5		ns
$\overline{WAIT}$ hold time (from CLKOUT ↓)	<28>	t_{HKWT}		5		ns
Address hold time (from CLKOUT ↑)	<29>	t_{HKA}		0		ns
Address setting time (to ASTB ↓)	<30>	t_{SAST}		0.5T – 10		ns
Address hold time (from ASTB ↓)	<31>	t_{HSTA}		0.5T – 10		ns
ASTB ↓→ $\overline{DSTB}$ ↓ delay time	<35>	t_{DSTD}		0.5T – 10		ns
$\overline{DSTB}$ ↑→ ASTB ↑ delay time	<38>	t_{DDSTH}		0.5T – 10		ns
Status setting time (to ASTB ↓)	<40>	t_{SSST}		0.5T – 10		ns
Status hold time (from ASTB ↑)	<41>	t_{HSTS}		0.5T – 10		ns
$\overline{DSTB}$ width, low	<42>	t_{WDL}		(1 + n)T – 10		ns
ASTB width, high	<43>	t_{WSTH}		T – 10		ns
$\overline{WAIT}$ setting time (to address)	<44>	t_{SAWT1}	n ≥ 1		1.5T – 20	ns
	<45>	t_{SAWT2}			(1.5 + n)T – 20	ns
$\overline{WAIT}$ hold time (from address)	<46>	t_{HAWT1}	n ≥ 1	(0.5 + n)T		ns
	<47>	t_{HAWT2}		(1.5 + n)T		ns
$\overline{WAIT}$ setting time (to ASTB ↓)	<48>	t_{SSTWT1}	n ≥ 1		T – 15	ns
	<49>	t_{SSTWT2}			(1 + n)T – 15	ns
$\overline{WAIT}$ hold time (from ASTB ↓)	<50>	t_{HSTWT1}	n ≥ 1	nT		ns
	<51>	t_{HSTWT2}		(1 + n)T		ns
CLKOUT ↑→ data output delay time	<52>	t_{DKOD}			20	ns
$\overline{DSTB}$ ↓→ data output delay time	<53>	t_{DDOD}			10	ns
Data output hold time (from CLKOUT ↑)	<54>	t_{HKOD}		0		ns
Data output setting time (to $\overline{DSTB}$ ↑)	<55>	t_{SODD}		(1 + n)T – 15		ns
Data output hold time (from $\overline{DSTB}$ ↑)	<56>	t_{HDOD}		T – 10		ns

Remarks 1. T = t_{CYK}

2. n indicates the number of wait clocks inserted in the bus cycle. The sampling timing differs when the programmable wait state is inserted.

(6) Write timing (2/2): 1 wait



Note R/$\overline{W}$ (output), $\overline{UBEN}$ (output), $\overline{LBEN}$ (output)

Remark The broken line indicates the high-impedance state.

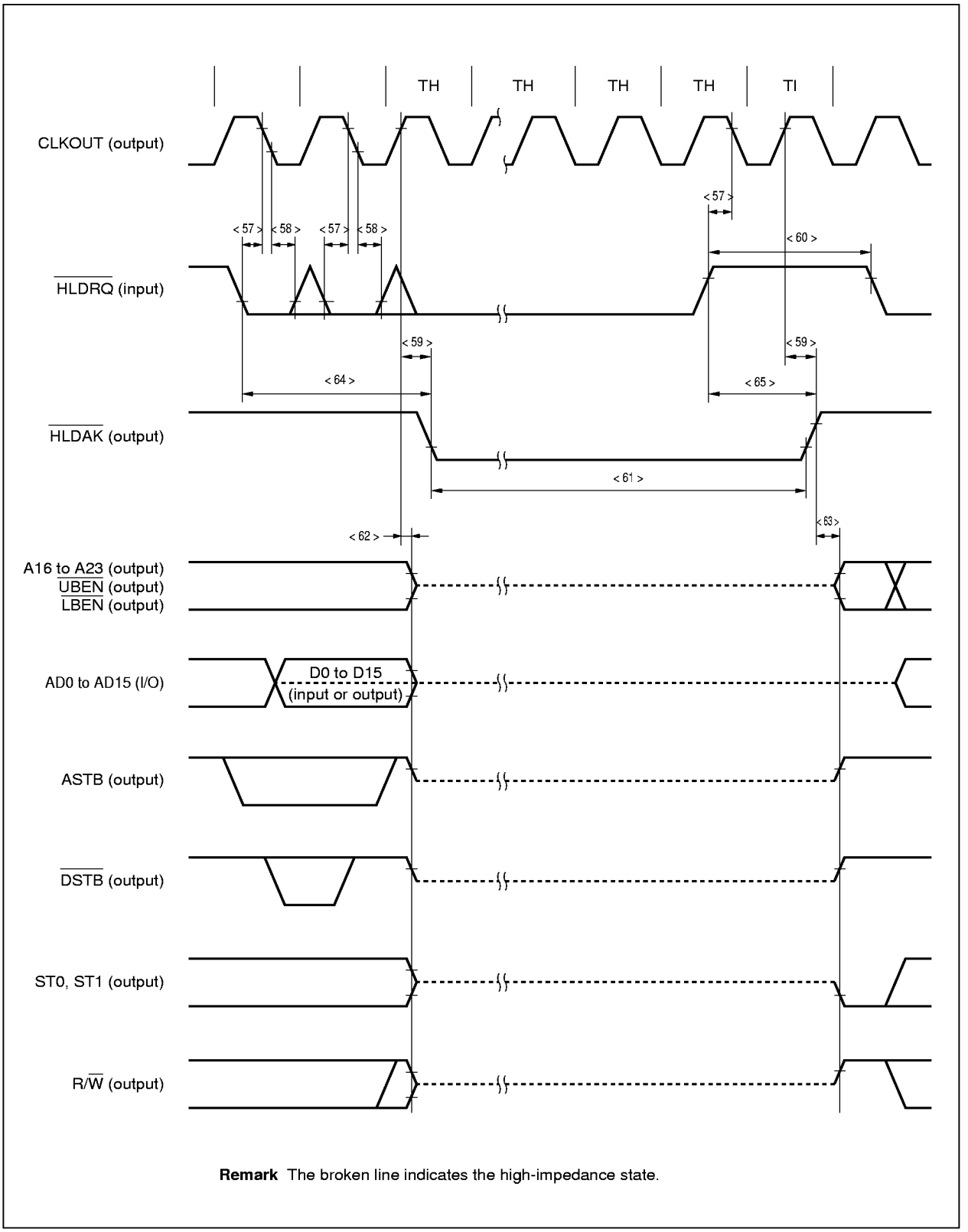
(7) Bus hold timing (1/2)

	Parameter	Symbol		Condition	MIN.	MAX.	Unit
	$\overline{HLDRQ}$ setting time (to CLKOUT ↓)	<57>	t_{SHOK}		5		ns
	$\overline{HLDRQ}$ hold time (from CLKOUT ↓)	<58>	t_{HKHQ}		5		ns
	CLKOUT ↑→ $\overline{HLDAK}$ delay time	<59>	t_{DKHA}			20	ns
	$\overline{HLDRQ}$ width, high	<60>	t_{WHQH}		T + 10		ns
	$\overline{HLDAK}$ width, low	<61>	t_{WHAL}		T – 10		ns
★	CLKOUT ↑→ bus float delay time	<62>	t_{DKF}			20	ns
	$\overline{HLDAK}$ ↑→ bus output delay time	<63>	t_{DHAC}		–3		ns
	$\overline{HLDRQ}$ ↓→ $\overline{HLDAK}$ ↓ delay time	<64>	t_{DHQHA1}			(2n + 7.5)T + 20	ns
	$\overline{HLDRQ}$ ↑→ $\overline{HLDAK}$ ↑ delay time	<65>	t_{DHQHA2}		0.5T	1.5T + 20	ns

Remarks 1. T = t_{CYK}

2. n indicates the number of wait clocks inserted in the bus cycle. The sampling timing differs when the programmable wait state is inserted.

(7) Bus hold timing (2/2)

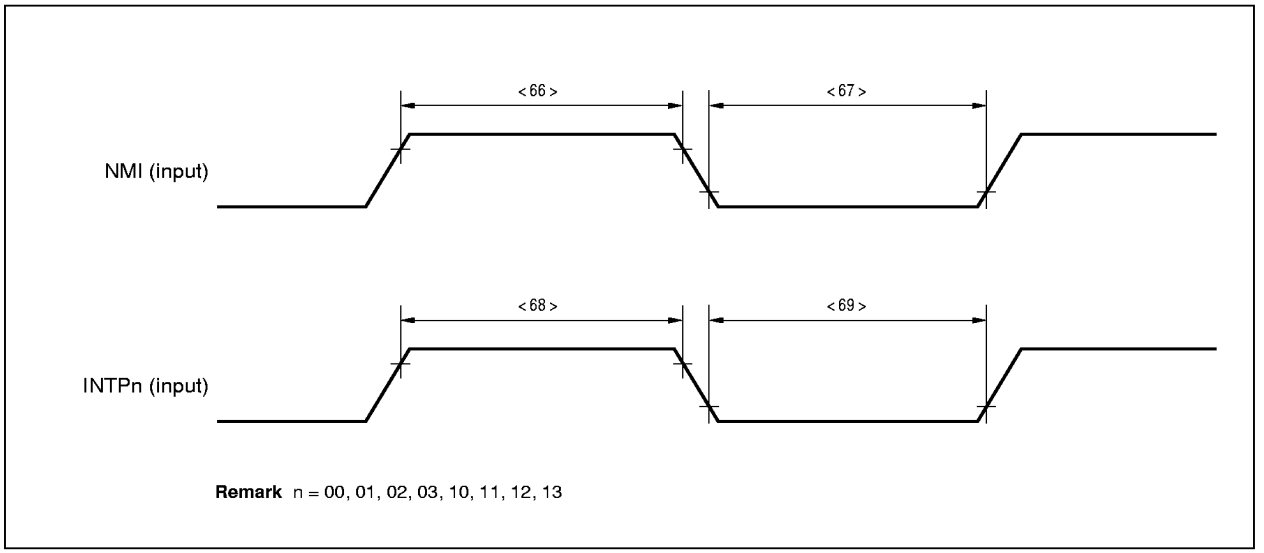


Remark The broken line indicates the high-impedance state.

(8) Interrupt timing

Parameter	Symbol		Condition	MIN.	MAX.	Unit
NMI width, high	<66>	t_{WNIH}		500		ns
NMI width, low	<67>	t_{WNIL}		500		ns
INTPn width, high	<68>	t_{WITH}	n = 00, 01, 02, 03, 10, 11, 12, 13	3T + 10		ns
INTPn width, low	<69>	t_{WITL}	n = 00, 01, 02, 03, 10, 11, 12, 13	3T + 10		ns

Remark T = t_{CYK}



Remark n = 00, 01, 02, 03, 10, 11, 12, 13

(9) CSI timing

(a) Master mode

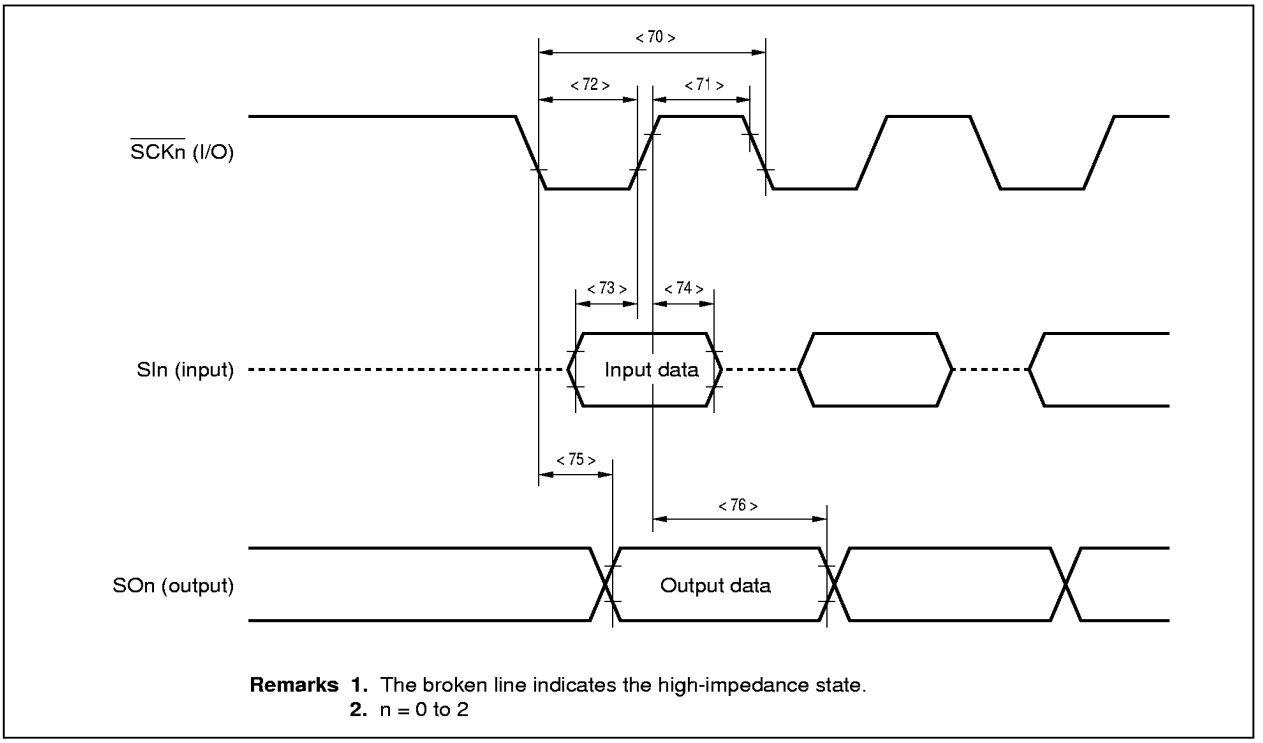
Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{SCKn}$ cycle	<70>	t_{CYSK}	Output	250		ns
$\overline{SCKn}$ width, high	<71>	t_{WSKH}	Output	$0.5t_{CYSK}$ – 20		ns
$\overline{SCKn}$ width, low	<72>	t_{WSKL}	Output	$0.5t_{CYSK}$ – 25		ns
SIn setting time (to $\overline{SCKn}$ ↑)	<73>	t_{SSISK}		45		ns
SIn hold time (from $\overline{SCKn}$ ↑)	<74>	t_{HSKSI}		0		ns
SOn output delay time (from $\overline{SCKn}$ ↓)	<75>	t_{DSKSO}			25	ns
SOn output hold time (from $\overline{SCKn}$ ↑)	<76>	t_{HSKSO}		$0.5t_{CYSK}$ – 5		ns

Caution When the internal clock is selected as the serial clock, set ϕ to 8 MHz or lower if specifying ϕ/2, and set ϕ to 16 MHz or lower if specifying ϕ/4 (ϕ = internal operation clock frequency). To select a higher operating frequency than those indicated above, select the baud rate generator (BRG) output instead of the internal clock.

(b) Slave mode

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{SCKn}$ cycle	<70>	t_{CYSK}	Input	250		ns
$\overline{SCKn}$ width, high	<71>	t_{WSKH}	Input	70		ns
$\overline{SCKn}$ width, low	<72>	t_{WSKL}	Input	70		ns
SIn setting time (to $\overline{SCKn}$ ↑)	<73>	t_{SSISK}		10		ns
SIn hold time (from $\overline{SCKn}$ ↑)	<74>	t_{HSKSI}		15		ns
SOn output delay time (from $\overline{SCKn}$ ↓)	<75>	t_{DSKSO}			55	ns
SOn output hold time (from $\overline{SCKn}$ ↑)	<76>	t_{HSKSO}		t_{WSKH}		ns

Caution When the internal clock is selected as the serial clock, set ϕ to 8 MHz or lower if specifying ϕ/2, and set ϕ to 16 MHz or lower if specifying ϕ/4 (ϕ = internal operation clock frequency). To select a higher operating frequency than those indicated above, select the baud rate generator (BRG) output instead of the internal clock.

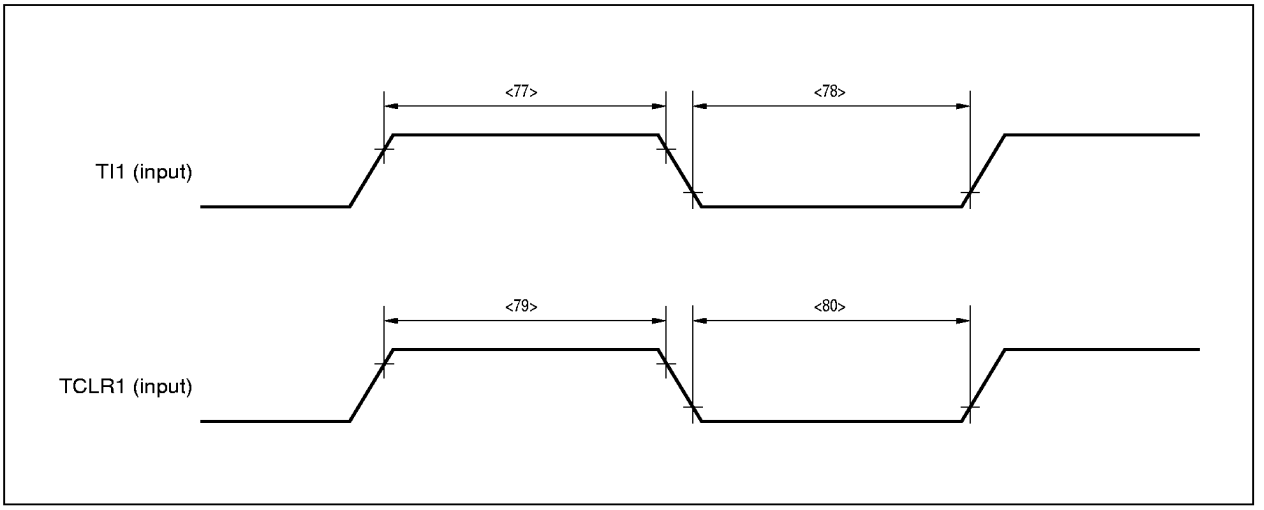


Remarks 1. The broken line indicates the high-impedance state.
2. n = 0 to 2

(10) RPU timing

Parameter	Symbol		Condition	MIN.	MAX.	Unit
TI1 width, high	<77>	t_{WTIH}		3T + 10		ns
TI1 width, low	<78>	t_{WTIL}		3T + 10		ns
TCLR1 width, high	<79>	t_{WTCH}		3T + 10		ns
TCLR1 width, low	<80>	t_{WTCL}		3T + 10		ns

Remark T = t_{CYK}



DC Programming Characteristics

PROM write mode (T_A = 25 ±5°C, V_{DD} = 6.5 ±0.25 V, V_{PP} = 12.5 ±0.3 V)

Parameter	Symbol	Symbol[Note]	Condition	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH}	V_{IH}		0.7V_{DD}		V_{DD}	V
Input voltage, low	V_{IL}	V_{IL}		0		0.3V_{DD}	V
Output voltage, high	V_{OH}	V_{OH}	I_{OH} = –1 mA	V_{DD} – 1.0			V
Output voltage, low	V_{OL}	V_{OL}	I_{OL} = 1.6 mA			0.4	V
Input leakage current	I_{LI}	I_{LI}	0 ≤ V_{IN} ≤ V_{DD}	–10		+10	μA
V_{PP} supply voltage	V_{PP}	V_{PP}		12.2	12.5	12.8	V
V_{DD} supply voltage	V_{DD}	V_{CC}		6.25	6.5	6.75	V
V_{PP} supply current	I_{PP}	I_{PP}	$\overline{PGM}$ = V_{IL}			50	mA
V_{DD} supply current	I_{DD}	I_{CC}				50	mA

Note Symbol of the corresponding μPD27C1001A

PROM read mode (T_A = 25 ±5°C, V_{DD} = 5.0 ±0.5 V, V_{PP} = V_{DD} ±0.6 V)

Parameter	Symbol	Symbol[Note]	Condition	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH}	V_{IH}		0.7V_{DD}		V_{DD}	V
Input voltage, low	V_{IL}	V_{IL}		0		0.3V_{DD}	V
Output voltage, high	V_{OH1}	V_{OH1}	I_{OH} = –1 mA	V_{DD} – 1.0			V
	V_{OH2}	V_{OH2}	I_{OH} = –100 μA	V_{DD} – 0.5			V
Output voltage, low	V_{OL}	V_{OL}	I_{OL} = 1.6 mA			0.4	V
Input leakage current	I_{LI}	I_{LI}	0 ≤ V_{IN} ≤ V_{DD}	–10		+10	μA
Output leakage current	I_{LO}	I_{LO}	0 ≤ V_{OUT} ≤ V_{DD}, $\overline{OE}$ = V_{IH}	–10		+10	μA
V_{PP} supply voltage	V_{PP}	V_{PP}		V_{DD} – 0.6	V_{DD}	V_{DD} + 0.6	V
V_{DD} supply voltage	V_{DD}	V_{CC}		4.5	5.0	5.5	V
V_{PP} supply current	I_{PP}	I_{PP}	V_{PP} = V_{DD}			100	μA
V_{DD} supply current	I_{DD}	I_{CCA1}	$\overline{CE}$ = V_{IL}, V_{IN} = V_{IH}			50	mA

Note Symbol of the corresponding μPD27C1001A

AC Programming Characteristics

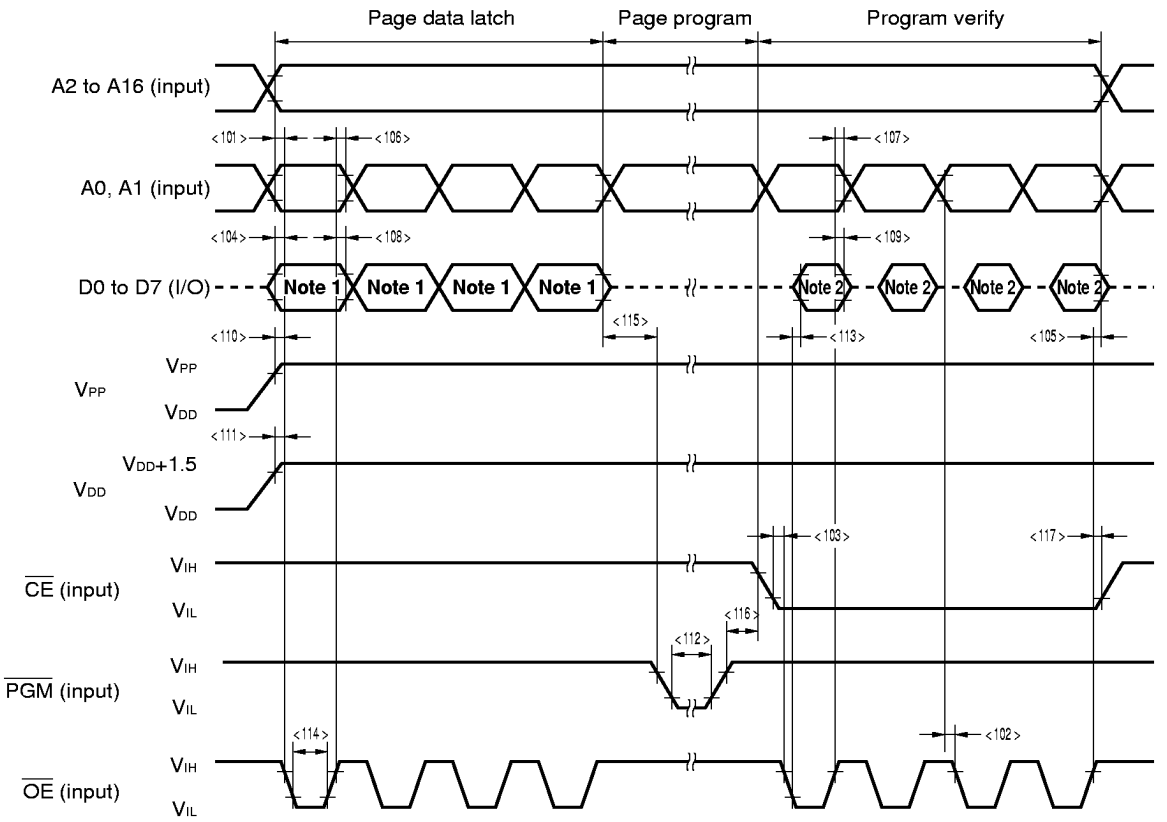
(1) PROM write mode timing (page program mode)

(T_A = 25 ±5°C, V_{DD} = 6.5 ±0.25 V, V_{PP} = 12.5 ±0.3 V) (1/2)

Parameter	Symbol		Symbol[Note]	Condition	MIN.	TYP.	MAX.	Unit
Address setup time (to $\overline{OE}$ ↓)	<101>	t_{AS}	t_{AS}		2			μs
$\overline{OE}$ set time	<102>	t_{OES}	t_{OES}		2			μs
$\overline{CE}$ setup time (to $\overline{OE}$ ↓)	<103>	t_{CES}	t_{CES}		2			μs
Input data setup time (to $\overline{OE}$ ↓)	<104>	t_{DS}	t_{DS}		2			μs
Address hold time (from $\overline{OE}$ ↑)	<105>	t_{AH}	t_{AH}		2			μs
	<106>	t_{AHL}	t_{AHL}		2			μs
	<107>	t_{AHV}	t_{AHV}		0			μs
Input data hold time (from $\overline{OE}$ ↑)	<108>	t_{DH}	t_{DH}		2			μs
$\overline{OE}$ ↑→ data output float delay time	<109>	t_{DF}	t_{DF}		0		250	ns
V_{PP} setup time (to $\overline{OE}$ ↓)	<110>	t_{VPS}	t_{VPS}		1.0			ms
V_{DD} setup time (to $\overline{OE}$ ↓)	<111>	t_{VDS}	t_{VCS}		1.0			ms
Program pulse width	<112>	t_{PW}	t_{PW}		0.095	0.1	0.105	ms
$\overline{OE}$ ↓→ valid data delay time	<113>	t_{OE}	t_{OE}				1	μs
$\overline{OE}$ pulse width in data latch	<114>	t_{LW}	t_{LW}		1			μs
$\overline{PGM}$ set time	<115>	t_{PGMS}	t_{PGMS}		2			μs
$\overline{CE}$ hold time	<116>	t_{CEH}	t_{CEH}		2			μs
$\overline{OE}$ hold time	<117>	t_{OEH}	t_{OEH}		2			μs

Note Symbol of the corresponding μPD27C1001A

(1) PROM write mode timing (page program mode) (2/2)



Notes 1. D0 to D7 (input)

2. D0 to D7 (output)

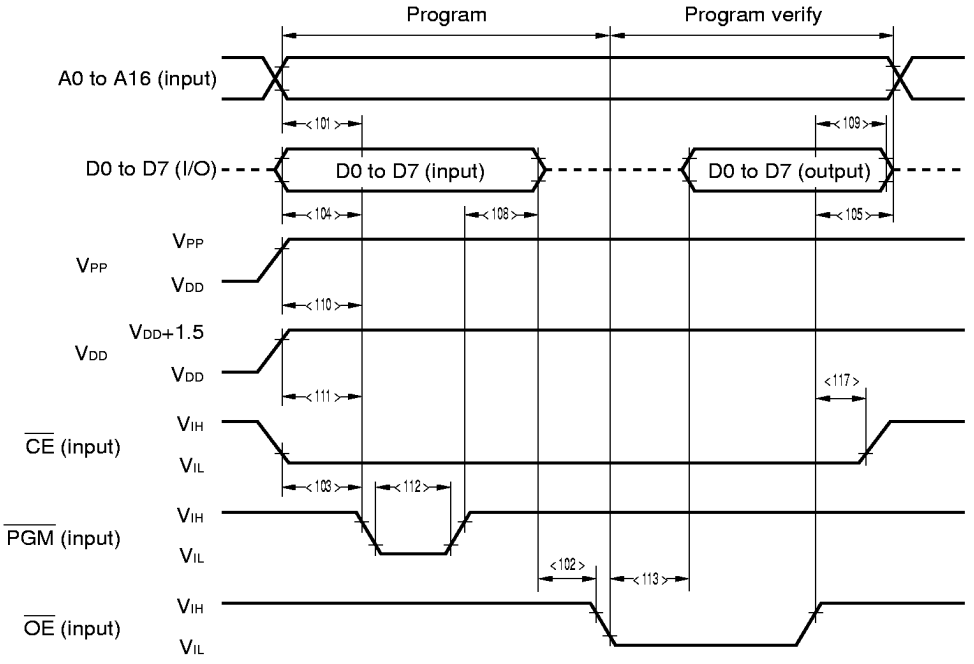
Remark The broken line indicates the high-impedance state.

(2) PROM write mode timing (byte program mode)

(T_A = 25 ±5°C, V_{DD} = 6.5 ±0.25 V, V_{PP} = 12.5 ±0.3 V)

Parameter	Symbol		Symbol[Note]	Condition	MIN.	TYP.	MAX.	Unit
Address setup time (to $\overline{PGM}$ ↓)	<101>	t_{AS}	t_{AS}		2			μs
$\overline{OE}$ set time	<102>	t_{OES}	t_{OES}		2			μs
$\overline{CE}$ setup time (to $\overline{PGM}$ ↓)	<103>	t_{CES}	t_{CES}		2			μs
Input data setup time (to $\overline{PGM}$ ↓)	<104>	t_{DS}	t_{DS}		2			μs
Address hold time (from $\overline{OE}$ ↑)	<105>	t_{AH}	t_{AH}		2			μs
Input data hold time (from $\overline{PGM}$ ↑)	<108>	t_{DH}	t_{DH}		2			μs
$\overline{OE}$ ↑→ data output float delay time	<109>	t_{DF}	t_{DF}		0		250	ns
V_{PP} setup time (to $\overline{PGM}$ ↓)	<110>	t_{VPS}	t_{VPS}		1.0			ms
V_{DD} setup time (to $\overline{PGM}$ ↓)	<111>	t_{VDS}	t_{VDS}		1.0			ms
Program pulse width	<112>	t_{PW}	t_{PW}		0.095	0.1	0.105	ms
$\overline{OE}$ ↓→ valid data delay time	<113>	t_{OE}	t_{OE}				1	μs
$\overline{OE}$ hold time	<117>	t_{OEH}	—		2			μs

Note Symbol of the corresponding μPD27C1001A



Cautions 1. Apply V_{DD} before V_{PP}, and turn off V_{DD} after V_{PP}.

2. Keep V_{PP} to less than +13.5 V including overshoot.

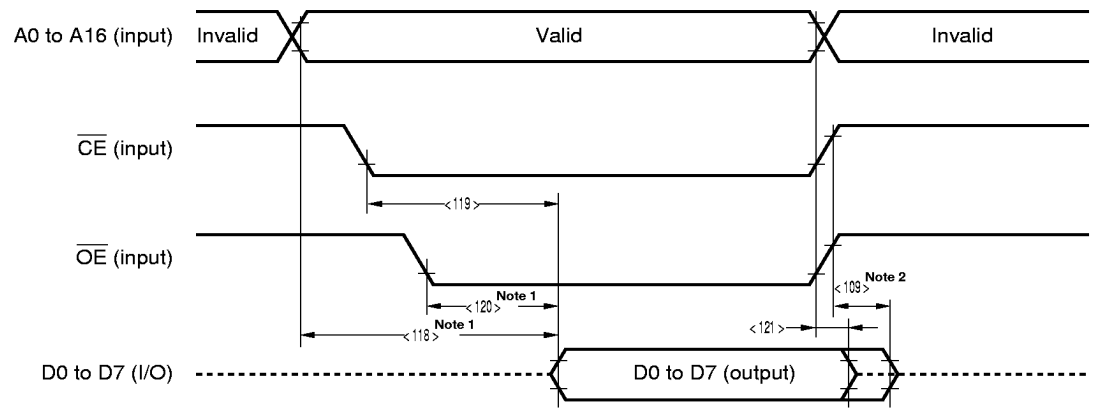
3. If the device is pulled out of the socket while +12.5 V is applied to V_{PP}, the reliability may be degraded.

Remark The broken line indicates the high-impedance state.

(3) PROM read mode timing (T_A = 25 ±5°C, V_{DD} = 5.0 ±0.5 V, V_{PP} = V_{DD} ±0.6 V)

Parameter	Symbol		Symbol[Note]	Condition	MIN.	TYP.	MAX.	Unit
Address → data output delay time	<118>	t_{ACC}	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}			1	μs
$\overline{CE}$ ↓→ data output delay time	<119>	t_{CE}	t_{CE}	$\overline{OE}$ = V_{IL}			1	μs
$\overline{OE}$ ↓→ data output delay time	<120>	t_{OE}	t_{OE}	$\overline{CE}$ = V_{IL}			1	μs
$\overline{OE}$ ↑→ data output float delay time	<109>	t_{DF}	t_{DF}	$\overline{CE}$ = V_{IL}	0		60	ns
Address → data hold time	<121>	t_{OH}	t_{OH}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0			ns

Note Symbol of the corresponding μPD27C1001A



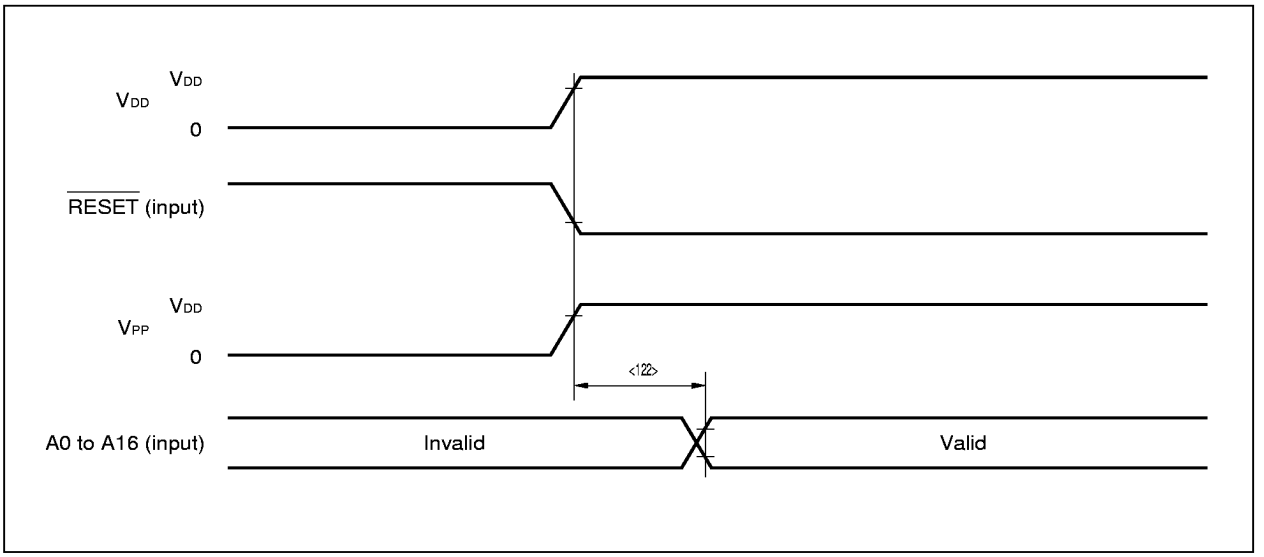
Notes 1. To read within the range of t_{ACC} (< 118 >), the delay time of $\overline{OE}$ input from the falling of $\overline{CE}$ must be $t_{ACC} - t_{OE}$ (< 118 > − < 120 >) max.

2. t_{DF} (< 109 >) is the time after either $\overline{OE}$ or $\overline{CE}$ first reaches V_{IH}.

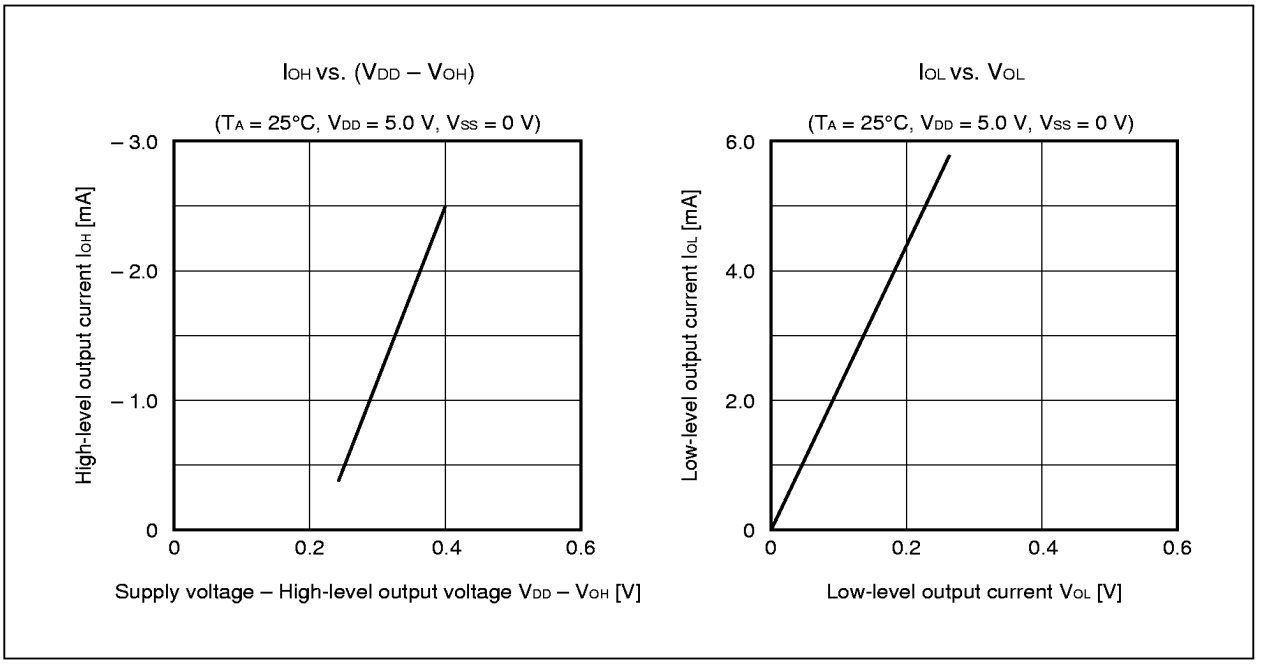
Remark The broken line indicates the high-impedance state.

(4) PROM programming mode setting timing (T_A = 25°C, V_{SS} = 0 V)

Parameter	Symbol		Condition	MIN.	TYP.	MAX.	Unit
PROM programming mode setup time	<122>	t_{SMA}		10			μs

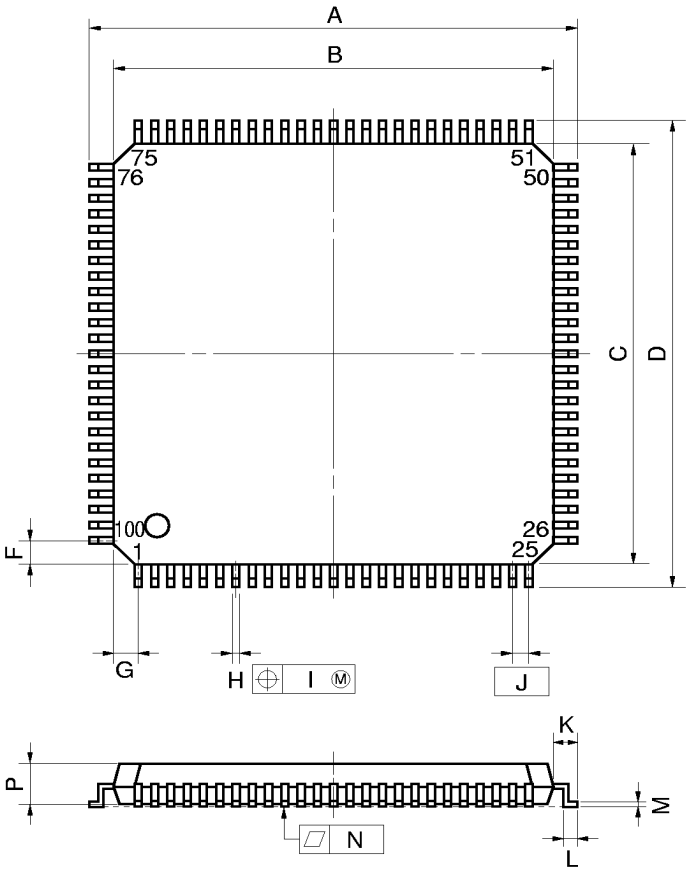


7. CHARACTERISTICS CURVES (REFERENCE)



8. PACKAGE DRAWING

100 PIN PLASTIC QFP (FINE PITCH) (□14)



NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	16.0±0.2	0.630±0.008
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	16.0±0.2	0.630±0.008
F	1.0	0.039
G	1.0	0.039
H	$0.22^{+0.05}_{-0.04}$	0.009±0.002
I	0.10	0.004
J	0.5 (T.P.)	0.020 (T.P.)
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
L	0.5±0.2	$0.020^{+0.008}_{-0.009}$
M	$0.17^{+0.03}_{-0.07}$	$0.007^{+0.001}_{-0.003}$
N	0.10	0.004
P	1.45	0.057
Q	0.125±0.075	0.005±0.003
R	5°±5°	5°±5°
S	1.7 MAX.	0.067 MAX.

P100GC-50-7EA-2

9. RECOMMENDED SOLDERING CONDITIONS

The μPD70P3002 should be soldered and mounted under the following recommended conditions.

For the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Table 9-1. Soldering Conditions

Soldering Method	Soldering Conditions	Symbol
Infrared reflow	Package peak temperature: 235°C, Reflow time: 30 seconds or below (210°C or higher), Number of reflow processes: 2 max., Exposure limit: 7 days[Note] (after that, prebaking is necessary at 125°C for 10 hours)	IR35-107-2
VPS	Package peak temperature: 215°C, Reflow time: 40 seconds or below (200°C or higher), Number of reflow processes: 2 max., Exposure limit: 7 days[Note] (after that, prebaking is necessary at 125°C for 10 hours)	VP15-107-2
Partial heating	Pin temperature: 300°C or below, Time: 3 seconds or below (per side of device)	—

Note Exposure limit after dry-pack is opened. Storage conditions: temperature of 25°C and relative humidity of 65% or less.

Caution Do not use different soldering methods together (except for partial heating).

APPENDIX PROM WRITING TOOLS

(1) Hardware tools

	Product	Product Name	Description
	PROM programmer	PG-1500	NEC PROM programmer. The NEC PROM programmer can program PROM-contained single-chip microcontrollers in stand-alone mode or under control of a host machine when connected with an optional PROM programmer adapter. This programmer can also program representative PROMs from 256-Kbit to 4-Mbit models.
		UNISITE	Data I/O Japan Co., Ltd. PROM programmers
		2900	
		3900	
		MODEL1890A	Minato Electronics Inc. PROM programmers
★		AF-9704 Rev.22.50 or later	Ando Electric Co., Ltd. PROM programmers
★		AF-9705 Rev.01.37 or later (Algorithm: Rev.02.40 or later)	
★		AF-9706 Rev.01.60 or later	
	PROM programmer adapter	PA-70P3000GC	PROM programmer adapter to write program to μPD70P3002 on general-purpose PROM programmer such as PG-1500

(2) Software tools

Product	Host Machine	OS	Supply Medium	Part Number	Description
PG-1500 controller	PC-9800 Series	MS-DOS	3.5" FD	μS5A13PG1500	Controls PG-1500 on host machine by connecting PG-1500 and host machine with serial or parallel interface.
	IBM PC/AT™ and compatible machines	PC DOS	3.5" FD	μS7B13PG1500	

Remark The operations of the PG-1500 controller are guaranteed only on the above host machine and OS.