

CD4051BM/CD4051BC Single 8-Channel Analog Multiplexer/Demultiplexer **CD4052BM/CD4052BC Dual 4-Channel Analog Multiplexer/Demultiplexer** **CD4053BM/CD4053BC Triple 2-Channel Analog Multiplexer/Demultiplexer**

General Description

These analog multiplexers/demultiplexers are digitally controlled analog switches having low "ON" impedance and very low "OFF" leakage currents. Control of analog signals up to 15V_{p-p} can be achieved by digital signal amplitudes of 3–15V. For example, if V_{DD} = 5V, V_{SS} = 0V and V_{EE} = –5V, analog signals from –5V to +5V can be controlled by digital inputs of 0–5V. The multiplexer circuits dissipate extremely low quiescent power over the full V_{DD}–V_{SS} and V_{DD}–V_{EE} supply voltage ranges, independent of the logic state of the control signals. When a logical "1" is present at the inhibit input terminal all channels are "OFF".

CD4051BM/CD4051BC is a single 8-channel multiplexer having three binary control inputs, A, B, and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned "ON" and connect the input to the output.

CD4052BM/CD4052BC is a differential 4-channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select 1 or 4 pairs of channels to be turned on and connect the differential analog inputs to the differential outputs.

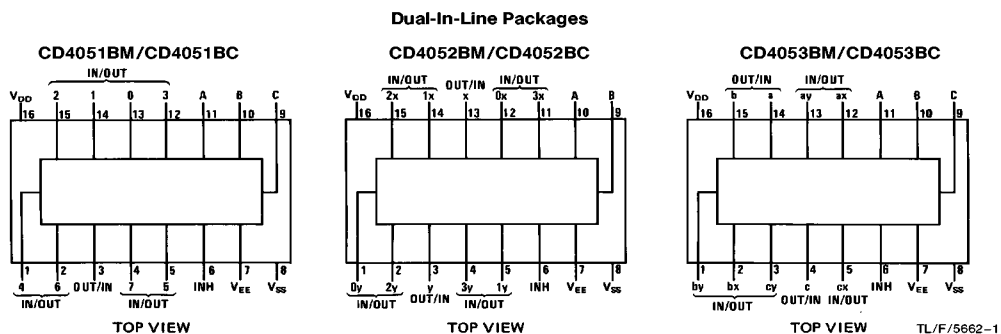
CD4053BM/CD4053BC is a triple 2-channel multiplexer having three separate digital control inputs, A, B, and C, and

an inhibit input. Each control input selects one of a pair of channels which are connected in a single-pole double-throw configuration.

Features

- Wide range of digital and analog signal levels: digital 3–15V, analog to 15V_{p-p}
- Low "ON" resistance: 80Ω (typ.) over entire 15V_{p-p} signal-input range for V_{DD}–V_{EE} = 15V
- High "OFF" resistance: channel leakage of ±10 pA (typ.) at V_{DD}–V_{EE} = 10V
- Logic level conversion for digital addressing signals of 3–15V (V_{DD}–V_{SS} = 3–15V) to switch analog signals to 15 V_{p-p} (V_{DD}–V_{EE} = 15V)
- Matched switch characteristics: ΔR_{ON} = 5Ω (typ.) for V_{DD}–V_{EE} = 15V
- Very low quiescent power dissipation under all digital-control input and supply conditions: 1 μW (typ.) at V_{DD}–V_{SS} = V_{DD}–V_{EE} = 10V
- Binary address decoding on chip

Connection Diagrams



Order Number CD4051B, CD4052B, or CD4053B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

DC Supply Voltage (V_{DD})	− 0.5 V_{DC} to + 18 V_{DC}
Input Voltage (V_{IN})	− 0.5 V_{DC} to V_{DD} + 0.5 V_{DC}
Storage Temperature Range (T_S)	− 65°C to + 150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temp. (T_L) (soldering, 10 sec.)	260°C

Recommended Operating Conditions

DC Supply Voltage (V_{DD})	+ 5 V_{DC} to + 15 V_{DC}
Input Voltage (V_{IN})	0V to V_{DD} V_{DC}
Operating Temperature Range (T_A)	
4051BM/4052BM/4053BM	− 55°C to + 125°C
4051BC/4052BC/4053BC	− 40°C to + 85°C

DC Electrical Characteristics (Note 2)

Symbol	Parameter	Conditions	− 55°C		+ 25°			+ 125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I _{DD}	Quiescent Device Current	V _{DD} = 5V V _{DD} = 10V V _{DD} = 15V		5 10 20			5 10 20		150 300 600	μA μA μA
Signal Inputs (V _{IS}) and Outputs (V _{OS})										
R _{ON}	“ON” Resistance (Peak for V _{EE} ≤ V _{IS} ≤ V _{DD})	R _L = 10 kΩ (any channel selected)	V _{DD} = 2.5V, V _{EE} = − 2.5V or V _{DD} = 5V, V _{EE} = 0V	800		270	1050		1300	Ω
			V _{DD} = 5V V _{EE} = − 5V or V _{DD} = 10V, V _{EE} = 0V	310		120	400		550	Ω
			V _{DD} = 7.5V, V _{EE} = − 7.5V or V _{DD} = 15V, V _{EE} = 0V	200		80	240		320	Ω
ΔR _{ON}	Δ“ON” Resistance Between Any Two Channels	R _L = 10 kΩ (any channel selected)	V _{DD} = 2.5V, V _{EE} = − 2.5V or V _{DD} = 5V, V _{EE} = 0V			10				Ω
			V _{DD} = 5V, V _{EE} = − 5V or V _{DD} = 10V, V _{EE} = 0V			10				Ω
			V _{DD} = 7.5V, V _{EE} = − 7.5V or V _{DD} = 15V, V _{EE} = 0V			5				Ω
	“OFF” Channel Leakage Current, any channel “OFF”	V _{DD} = 7.5V, O/I = ± 7.5V, I/O = 0V	± 50		± 0.01	± 50		± 500	nA	
	“OFF” Channel Leakage Current, all channels “OFF” (Common OUT/IN)	Inhibit = 7.5V V _{DD} = 7.5V, V _{EE} = − 7.5V, O/I = 0V, I/O = ± 7.5V	± 200		± 0.08	± 200		± 2000	nA	
		CD4051	± 200		± 0.04	± 200		± 2000	nA	
CD4052		± 200		± 0.02	± 200		± 2000	nA		
Control Inputs A, B, C and Inhibit										
V _{IL}	Low Level Input Voltage	V _{EE} = V _{SS} R _L = 1 kΩ to V _{SS} I _{IS} < 2 μA on all OFF channels V _{IS} = V _{DD} thru 1 kΩ V _{DD} = 5V V _{DD} = 10V V _{DD} = 15V		1.5 3.0 4.0			1.5 3.0 4.0		1.5 3.0 4.0	V V V
V _{IH}	High Level Input Voltage	V _{DD} = 5 V _{DD} = 10 V _{DD} = 15	3.5 7 11		3.5 7 11			3.5 7 11		V V V

Note 1: “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. Except for “Operating Temperature Range” they are not meant to imply that the devices should be operated at these limits. The table of “Electrical Characteristics” provides conditions for actual device operation.

Note 2: All voltages measured with respect to V_{SS} unless otherwise specified.

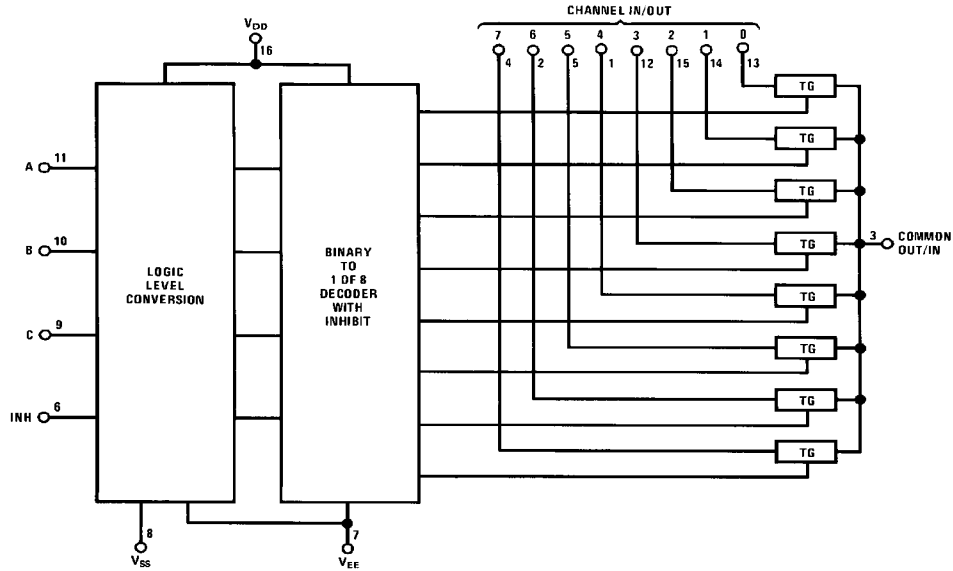
DC Electrical Characteristics (Note 2) (Continued)										
Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I _{IN}	Input Current	V _{DD} = 15V, V _{IN} = 0V V _{DD} = 15V, V _{IN} = 15V V _{EE} = 0V V _{EE} = 0V		−0.1 0.1		−10 ^{−5} 10 ^{−5}	−0.1 0.1		−1.0 1.0	μA μA
I _{DD}	Quiescent Device Current	V _{DD} = 5V V _{DD} = 10V V _{DD} = 15V V _{EE} = 0V		20 40 80			20 40 80		150 300 600	μA μA μA
Signal Inputs (V _{IS}) and Outputs (V _{OS})										
R _{ON}	“ON” Resistance (Peak for V _{EE} ≤ V _{IS} ≤ V _{DD})	R _L = 10 kΩ (any channel selected)	V _{DD} = 2.5V, V _{EE} = −2.5V or V _{DD} = 5V, V _{EE} = 0V V _{DD} = 5V, V _{EE} = −5V or V _{DD} = 10V, V _{EE} = 0V V _{DD} = 7.5V, V _{EE} = −7.5V or V _{DD} = 15V, V _{EE} = 0V	850 330 210		270 120 80	1050 400 240		1200 520 300	Ω Ω Ω
ΔR _{ON}	Δ“ON” Resistance Between Any Two Channels	R _L = 10 kΩ (any channel selected)	V _{DD} = 2.5V, V _{EE} = −2.5V or V _{DD} = 5V, V _{EE} = 0V			10				Ω
			V _{DD} = 5V, V _{EE} = −5V or V _{DD} = 10V, V _{EE} = 0V			10				Ω
			V _{DD} = 7.5V, V _{EE} = −7.5V or V _{DD} = 15V, V _{EE} = 0V			5				Ω
	“OFF” Channel Leakage Current, any channel “OFF”	V _{DD} = 7.5V, V _{EE} = −7.5V O/I = ±7.5V, I/O = 0V		±50		±0.01	±50		±500	nA
	“OFF” Channel Leakage Current, all channels “OFF” (Common OUT/IN)	Inhibit = 7.5V V _{DD} = 7.5V, V _{EE} = −7.5V, O/I = 0V	CD4051 CD4052	±200 ±200		±0.08 ±0.04	±200 ±200		±2000 ±2000	nA nA
		I/O = ±7.5V	CD4053	±200		±0.02	±200		±2000	nA
Control Inputs A, B, C and Inhibit										
V _{IL}	Low Level Input Voltage	V _{EE} = V _{SS} R _L = 1 kΩ to V _{SS} I _{IS} < 2 μA on all OFF Channels V _{IS} = V _{DD} thru 1 kΩ V _{DD} = 5V V _{DD} = 10V V _{DD} = 15V		1.5 3.0 4.0			1.5 3.0 4.0		1.5 3.0 4.0	V V V
V _{IH}	High Level Input Voltage	V _{DD} = 5 V _{DD} = 10 V _{DD} = 15	3.5 7 11		3.5 7 11			3.5 7 11		V V V
I _{IN}	Input Current	V _{DD} = 15V, V _{IN} = 0V V _{DD} = 15V, V _{IN} = 15V V _{EE} = 0V V _{EE} = 0V		−0.1 0.1		−10 ^{−5} 10 ^{−5}	−0.1 0.1		−1.0 1.0	μA μA
Note 1: “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. Except for “Operating Temperature Range” they are not meant to imply that the devices should be operated at these limits. The table of “Electrical Characteristics” provides conditions for actual device operation. Note 2: All voltages measured with respect to V _{SS} unless otherwise specified.										

AC Electrical Characteristics* $T_A = 25^\circ\text{C}$, $t_r = t_f = 20\text{ ns}$, unless otherwise specified.

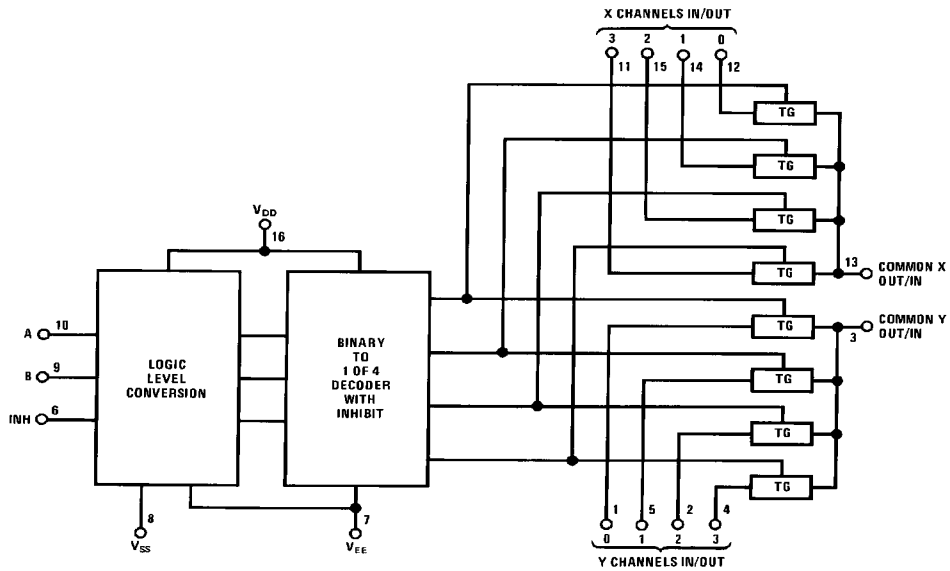
Symbol	Parameter	Conditions	V _{DD}	Min	Typ	Max	Units
t _{PZH} , t _{PZL}	Propagation Delay Time from Inhibit to Signal Output (channel turning on)	V _{EE} = V _{SS} = 0V R _L = 1 k Ω C _L = 50 pF	5V 10V 15V		600 225 160	1200 450 320	ns
t _{PHZ} , t _{PLZ}	Propagation Delay Time from Inhibit to Signal Output (channel turning off)	V _{EE} = V _{SS} = 0V R _L = 1 k Ω C _L = 50 pF	5V 10V 15V		210 100 75	420 200 150	ns
C _{IN}	Input Capacitance Control input Signal Input (IN/OUT)				5 10	7.5 15	pF pF
C _{OUT}	Output Capacitance (common OUT/IN)						
	CD4051 CD4052 CD4053	V _{EE} = V _{SS} = 0V	10V 10V 10V		30 15 8		pF pF pF
C _{IOS}	Feedthrough Capacitance				0.2		pF
C _{PD}	Power Dissipation Capacitance						
	CD4051 CD4052 CD4053				110 140 70		pF pF pF
Signal Inputs (V_{IS}) and Outputs (V_{OS})							
	Sine Wave Response (Distortion)	R _L = 10 k Ω f _{IS} = 1 kHz V _{IS} = 5 V _{p-p} V _{EE} = V _{SI} = 0V	10V		0.04		%
	Frequency Response, Channel "ON" (Sine Wave Input)	R _L = 1 k Ω , V _{EE} = 0V, V _{IS} = 5V _{p-p} , 20 log ₁₀ V _{OS} /V _{IS} = -3 dB	10V		40		MHz
	Feedthrough, Channel "OFF"	R _L = 1 k Ω , V _{EE} = V _{SS} = 0V, V _{IS} = 5V _{p-p} , 20 log ₁₀ V _{OS} /V _{IS} = -40 dB	10V		10		MHz
	Crosstalk Between Any Two Channels (frequency at 40 dB)	R _L = 1 k Ω , V _{EE} = V _{SS} = 0V, V _{IS} (A) = 5V _{p-p} , 20 log ₁₀ V _{OS} (B)/V _{IS} (A) = -40 dB (Note 3)	10V		3		MHz
t _{PHL} , t _{PLH}	Propagation Delay Signal Input to Signal Output	V _{EE} = V _{SS} = 0V C _L = 50 pF	5V 10V 15V		25 15 10	55 35 25	ns ns ns
Control Inputs, A, B, C and Inhibit							
	Control Input to Signal Crosstalk	V _{EE} = V _{SS} = 0V, R _L = 10 k Ω at both ends of channel. Input Square Wave Amplitude = 10V	10V		65		mV (peak)
t _{PHL} , t _{PLH}	Propagation Delay Time from Address to Signal Output (channels "ON" or "OFF")	V _{EE} = V _{SS} = 0V C _L = 50 pF	5V 10V 15V		500 180 120	1000 360 240	ns ns ns
*AC Parameters are guaranteed by DC correlated testing. Note 3: A, B are two arbitrary channels with A turned "ON" and B "OFF".							

Block Diagrams

CD4051BM/CD4051BC



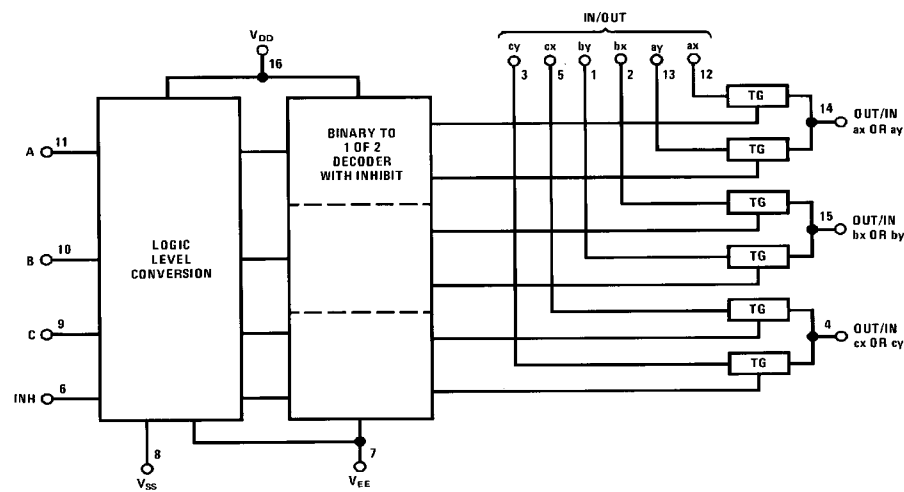
CD4052BM/CD4052BC



TL/F/5662-2

Block Diagrams (Continued)

CD4053BM/CD4053BC



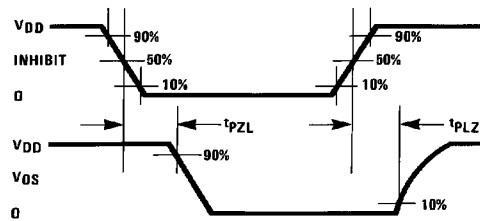
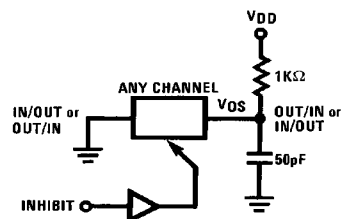
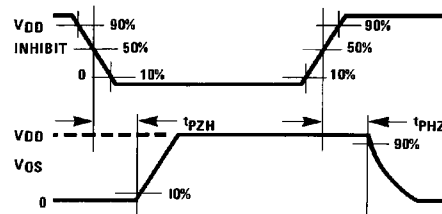
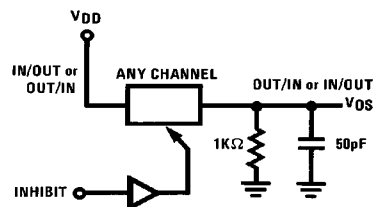
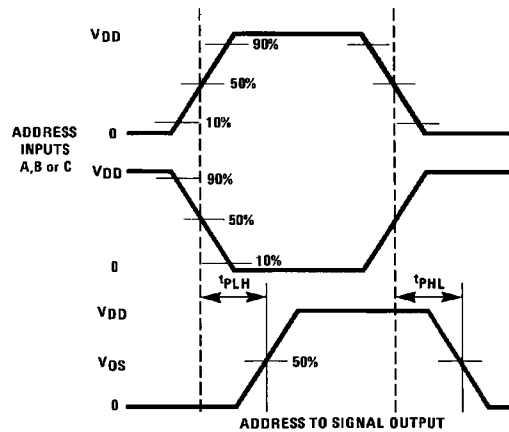
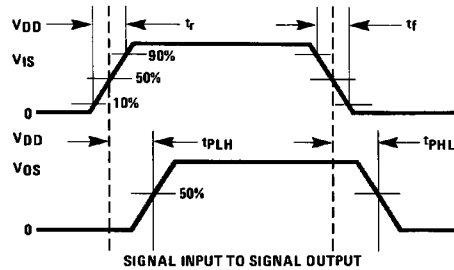
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Truth Table

INPUT STATES				"ON" CHANNELS		
INHIBIT	C	B	A	CD4051B	CD4052B	CD4053B
0	0	0	0	0	0X, 0Y	cx, bx, ax
0	0	0	1	1	1X, 1Y	cx, bx, ay
0	0	1	0	2	2X, 2Y	cx, by, ax
0	0	1	1	3	3X, 3Y	cx, by, ay
0	1	0	0	4		cy, bx, ax
0	1	0	1	5		cy, bx, ay
0	1	1	0	6		cy, by, ax
0	1	1	1	7		cy, by, ay
1	*	*	*	NONE	NONE	NONE

*Don't Care condition.

Switching Time Waveforms



TL/F/5662-4

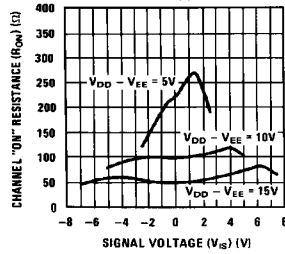
Special Considerations

In certain applications the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into IN/OUT pin, the voltage drop across the bidirectional switch must

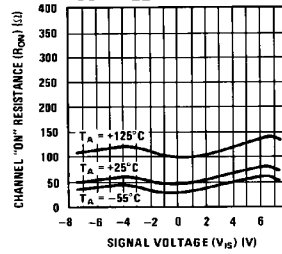
not exceed 0.6V at $T_A \leq 25^\circ\text{C}$, or 0.4V at $T_A > 25^\circ\text{C}$ (calculated from R_{ON} values shown). No V_{DD} current will flow through R_L if the switch current flows into OUT/IN pin.

Typical Performance Characteristics

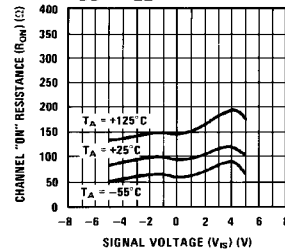
“ON” Resistance vs Signal Voltage for $T_A = 25^\circ\text{C}$



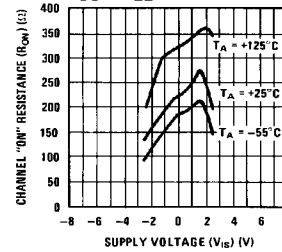
“ON” Resistance as a Function of Temperature for $V_{DD} - V_{EE} = 15\text{V}$



“ON” Resistance as a Function of Temperature for $V_{DD} - V_{EE} = 10\text{V}$



“ON” Resistance as a Function of Temperature for $V_{DD} - V_{EE} = 5\text{V}$



TL/F/5662-5

Physical Dimensions inches (millimeters)

Diagram illustrating the physical dimensions of the J16A (REV L) Cavity Dual-In-Line Package (J). The package is shown in three views: top, side, and end view.

Top View Dimensions:

- Overall length: 0.785 [19.94] MAX
- Lead pitch: 0.037 ± 0.005 [0.94 ± 0.13] TYP
- Lead width: 0.005 [0.13] MIN TYP
- Lead height: 0.020 [0.51] MIN TYP
- Lead angle: 90° ± 4° TYP
- Lead thickness: 0.018 ± 0.003 [0.46 ± 0.08] TYP
- Lead spacing: 0.055 ± 0.005 [1.40 ± 0.13] TYP
- Lead width at base: 0.020 - 0.060 [0.51 - 1.52] TYP
- Lead width at tip: 0.150 [3.81] MIN TYP
- Lead width at base (both ends): 0.125 - 0.200 [3.18 - 5.08] TYP
- Lead width at base (both ends): 0.080 [2.03] MAX
- Lead width at base (both ends): 0.100 ± 0.010 [2.54 ± 0.25] TYP
- Lead width at base (both ends): 0.005 [0.13] MIN TYP
- Lead width at base (both ends): 0.0025 [0.64] R
- Lead width at base (both ends): 0.0005 - 0.020 [0.13 - 0.51] R TYP

Side View Dimensions:

- Overall height: 0.290 - 0.320 [7.37 - 8.13]
- Lead height: 0.180 [4.57] MAX
- Lead angle: 95° ± 5° TYP
- Lead width at base: 0.310 - 0.410 [7.87 - 10.41]
- Lead width at base: 0.010 ± 0.002 [0.25 ± 0.05] TYP
- Lead width at base: 0.010 ± 0.002 [0.25 ± 0.05] TYP

End View Dimensions:

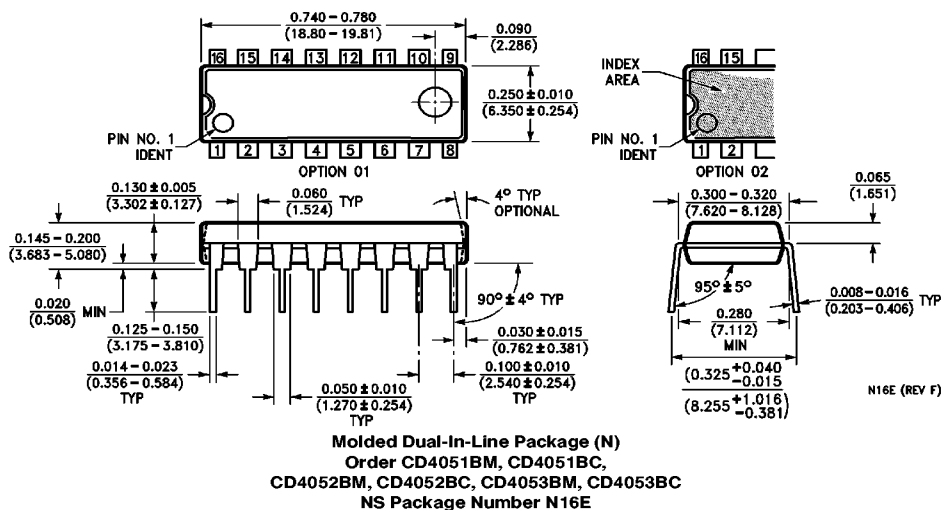
- Overall width: 0.385 - 0.394 [9.804 - 10.00]
- Lead width: 0.028 - 0.244 [0.711 - 6.198]
- Lead angle: 30° TYP
- Lead width at base: 0.010 MAX [0.254]

Ordering Information:

Order Number CD4051BMJ, CD4051BCJ, CD4052BMJ, CD4052BCJ, CD4053BMJ or CD4053BCJ
NS Package Number J16A

J16A (REV L)

Physical Dimensions inches (millimeters) (Continued)



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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



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