NEC

MOS INTEGRATED CIRCUIT

μPD780021, 780022, 780023, 780024

8-BIT SINGLE-CHIP MICROCONTROLLERS

DESCRIPTION

The μPD780021, 780022, 780023, and 780024 are members of the μPD780024 Subseries of the 78K/0 Series. Only selected functions of the existing μPD78054 Subseries are provided, and the serial interface is enhanced.

A flash memory version, the μPD78F0034, that can operate in the same power supply voltage range as the mask ROM version, and various development tools, are available.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μPD780024, 780034, 780024Y, 780034Y Subseries User's Manual: U12022E
78K/0 Series User's Manual – Instructions : U12326E

FEATURES

- Internal ROM and RAM

Item / Part Number	Program Memory (Internal ROM)	Data Memory (Internal High-Speed RAM)	Package
μPD780021	8 Kbytes	512 bytes	• 64-pin plastic shrink DIP (750 mil)
μPD780022	16 Kbytes		• 64-pin plastic QFP (14 × 14 mm)
μPD780023	24 Kbytes	1024 bytes	• 64-pin plastic LQFP (12 × 12 mm)
μPD780024	32 Kbytes		

- External memory expansion space: 64 Kbytes
- Minimum instruction execution time: 0.24 μs (at f_X = 8.38-MHz operation)
- I/O ports: 51 (N-ch open-drain 5-V withstand voltage: 4)
- ★ • 8-bit resolution A/D converter: 8 channels (AV_{DD} = 2.7 to 5.5 V)
- Serial interface: 3 channels
- Timer: 5 channels
- Power supply voltage: V_{DD} = 1.8 to 5.5 V

APPLICATIONS

Telephones, home electric appliances, pagers, AV equipment, car audios, office automation equipments, etc.

The information in this document is subject to change without notice.

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The mark ★ shows major revised points.

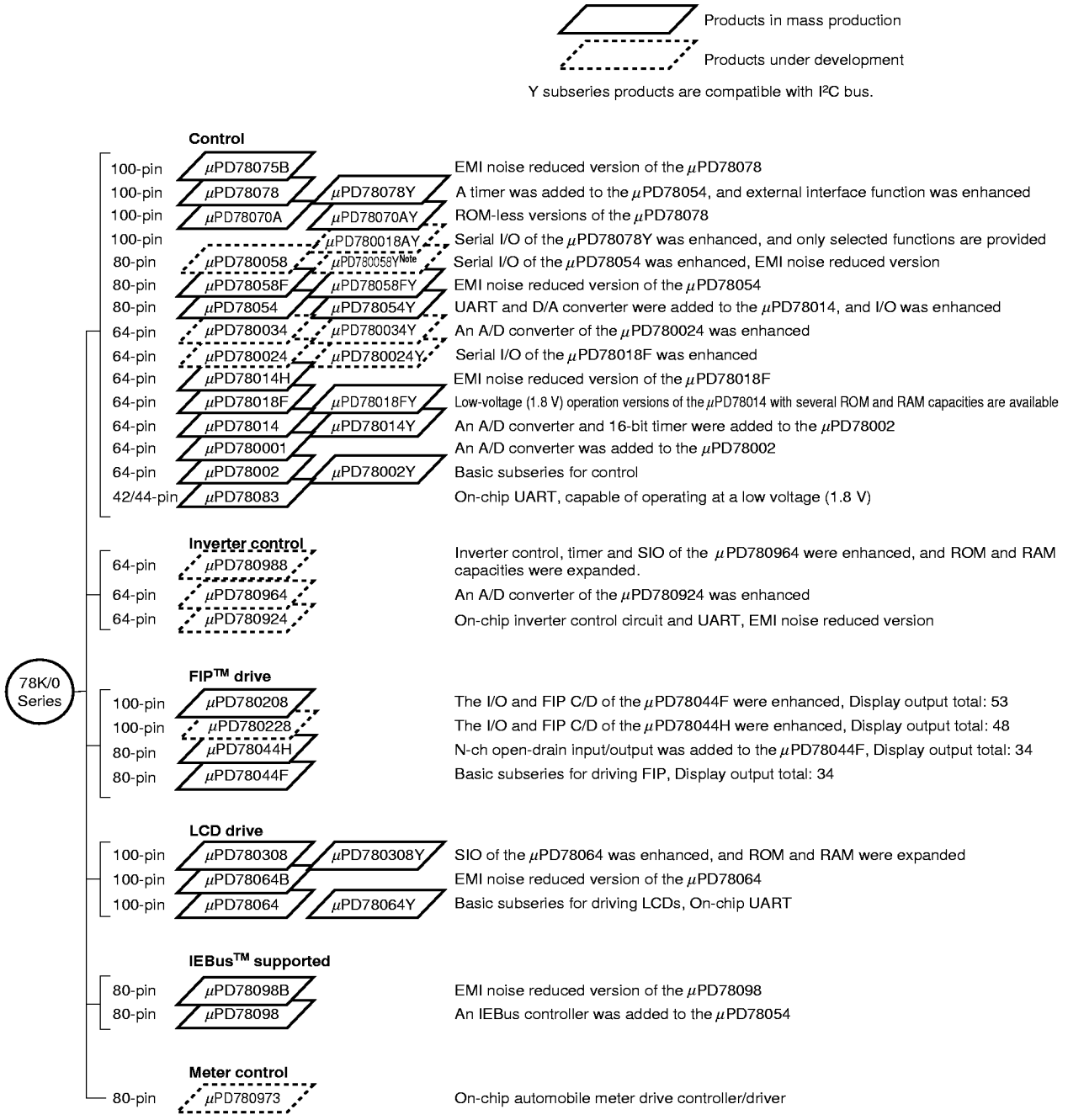
ORDERING INFORMATION

Part Number	Package
μPD780021CW-×××	64-pin plastic shrink DIP (750 mils)
μPD780021GC-×××-AB8	64-pin plastic QFP (14 × 14 mm)
μPD780021GK-×××-8A8	64-pin plastic LQFP (12 × 12 mm)
μPD780022CW-×××	64-pin plastic shrink DIP (750 mils)
μPD780022GC-×××-AB8	64-pin plastic QFP (14 × 14 mm)
μPD780022GK-×××-8A8	64-pin plastic LQFP (12 × 12 mm)
μPD780023CW-×××	64-pin plastic shrink DIP (750 mils)
μPD780023GC-×××-AB8	64-pin plastic QFP (14 × 14 mm)
μPD780023GK-×××-8A8	64-pin plastic LQFP (12 × 12 mm)
μPD780024CW-×××	64-pin plastic shrink DIP (750 mils)
μPD780024GC-×××-AB8	64-pin plastic QFP (14 × 14 mm)
μPD780024GK-×××-8A8	64-pin plastic LQFP (12 × 12 mm)

Remark ××× indicates the ROM code suffix.

★ 78K/0 SERIES PRODUCT DEVELOPMENT

These products are a further development in the 78K/0 Series. The designations appearing inside the boxes are subseries names.



Note Under planning

The major functional differences among the subseries are shown below.

Subseries Name \ Function		ROM Capacity	Timer				8-bit A/D	10-bit A/D	8-bit D/A	Serial Interface	I/O	V_{DD} MIN. Value	External Expansion
			8-bit	16-bit	Watch	WDT							
Control	μPD78075B	32 K-40 K	4 ch	1 ch	1 ch	1 ch	8 ch	–	2 ch	3 ch (UART: 1 ch)	88	1.8 V	Available
	μPD78078	48 K-60 K											
	μPD78070A	–									61	2.7 V	
	μPD780058	24 K-60 K	2 ch							3 ch (time-division UART: 1ch)	68	1.8 V	
	μPD78058F	48 K-60 K								3 ch (UART: 1 ch)	69	2.7 V	
	μPD78054	16 K-60 K										2.0 V	
	μPD780034	8 K-32 K					–	8 ch	–	3 ch (UART: 1 ch,	51	1.8 V	
	μPD780024						8 ch	–		time-division 3-wire: 1 ch)			
	μPD78014H									2 ch	53		
	μPD78018F	8 K-60 K											
	μPD78014	8 K-32 K										2.7 V	
	μPD780001	8 K		–	–					1 ch	39		–
	μPD78002	8 K-16 K			1 ch		–				53		Available
	μPD78083				–		8 ch			1 ch (UART: 1 ch)	33	1.8 V	–
Inverter control	μPD780988	32 K-60 K	3 ch	**Note 1**	–	1 ch	–	8 ch	–	3 ch (UART: 2 ch)	47	4.0 V	Available
	μPD780964	8 K-32 K		**Note 2**						2 ch (UART: 2 ch)		2.7 V	
	μPD780924						8 ch	–					
FIP drive	μPD780208	32 K-60 K	2 ch	1 ch	1 ch	1 ch	8 ch	–	–	2 ch	74	2.7 V	–
	μPD780228	48 K-60 K	3 ch	–	–					1 ch	72	4.5 V	
	μPD78044H	32 K-48 K	2 ch	1 ch	1 ch						68	2.7 V	
	μPD78044F	16 K-40 K								2 ch			
LCD drive	μPD780308	48 K-60 K	2 ch	1 ch	1 ch	1 ch	8 ch	–	–	3 ch (time-division UART: 1 ch)	57	2.0 V	–
	μPD78064B	32 K								2 ch (UART: 1 ch)			
	μPD78064	16 K-32 K											
IEBus supported	μPD78098B	40 K-60 K	2 ch	1 ch	1 ch	1 ch	8 ch	–	2 ch	3 ch (UART: 1 ch)	69	2.7 V	Available
	μPD78098	32 K-60 K											
Meter control	μPD780973	24 K-32 K	3 ch	1 ch	1 ch	1 ch	5 ch	–	–	2 ch (UART: 1 ch)	56	4.5 V	–

Notes 1. 16-bit timer: 2 channels
10-bit timer: 1 channel
2. 10-bit timer: 1 channel

FUNCTION OVERVIEW

Item \ Part Number		μPD780021	μPD780022	μPD780023	μPD780024
Internal memory	ROM	8 Kbytes	16 Kbytes	24 Kbytes	32 Kbytes
	High-speed RAM	512 bytes		1024 bytes	
Memory space		64 Kbytes			
General-purpose registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)			
Minimum instruction execution time		On-chip minimum instruction execution time cycle change function			
	When main system clock selected	0.24 μs/0.48 μs/0.95 μs/1.91 μs/3.81 μs (at 8.38-MHz operation)			
	When subsystem clock selected	122 μs (at 32.768-kHz operation)			
Instruction set		• 16-bit operation • Multiply/divide (8 bits × 8 bits,16 bits ÷ 8 bits) • Bit manipulate (set, reset, test, Boolean operation) • BCD adjust, etc.			
I/O ports		Total : 51 • CMOS input : 8 • CMOS I/O : 39 • N-ch open-drain I/O (5-V withstand voltage) : 4			
★ A/D converter		• 8-bit resolution x 8 channels • Low-voltage operation available: AV_{DD} = 2.7 to 5.5 V			
Serial interface		• 3-wire serial I/O mode : 2 channels • UART mode : 1 channel			
Timer		• 16-bit timer/event counter : 1 channel • 8-bit timer/event counter : 2 channels • Watch timer : 1 channel • Watchdog timer : 1 channel			
Timer output		3 (8-bit PWM output capable: 2)			
Clock output		• 65.5 kHz, 131 kHz, 262 kHz, 524 kHz, 1.05 MHz, 2.10 MHz, 4.19 MHz, 8.38 MHz (main system clock: at 8.38-MHz operation) • 32.768 kHz (subsystem clock: at 32.768-kHz operation)			
Buzzer output		1.02 kHz, 2.05 kHz, 4.10 kHz, 8.19 kHz (main system clock: at 8.38-MHz operation)			
Vectored interrupt sources	Maskable	Internal : 13, external : 5			
	Non-maskable	Internal : 1			
	Software	1			
Power supply voltage		V_{DD} = 1.8 to 5.5 V			
Operating ambient temperature		T_A = –40 to +85°C			
Package		• 64-pin plastic shrink DIP (750 mils) • 64-pin plastic QFP (14 × 14 mm) • 64-pin plastic LQFP (12 × 12 mm)			

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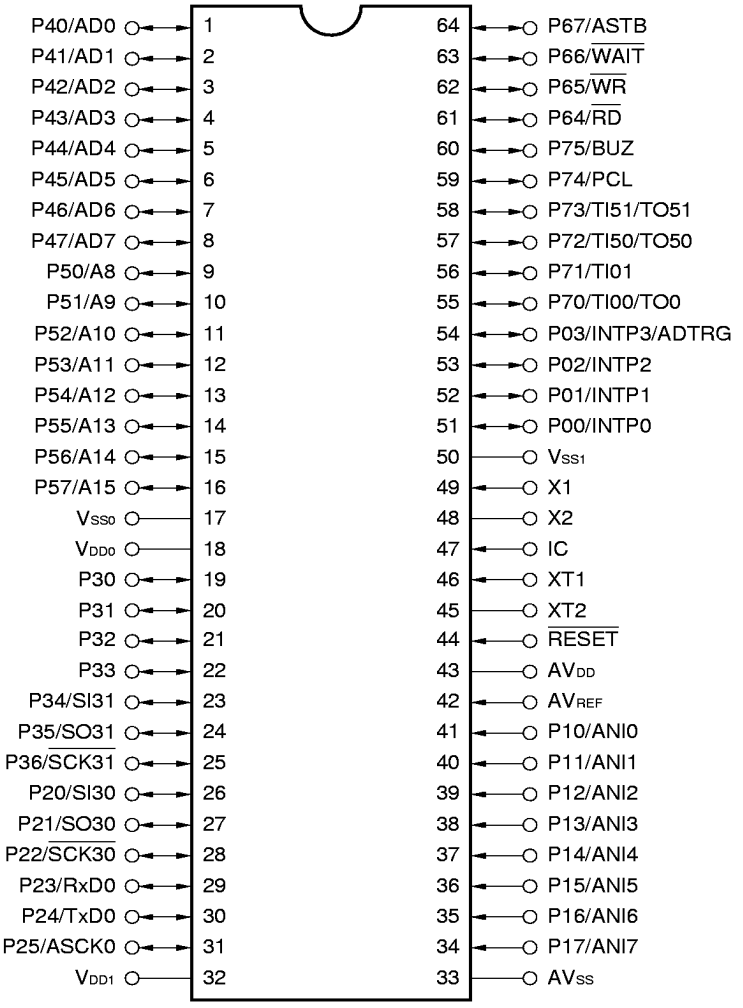
1. PIN CONFIGURATION (Top View)

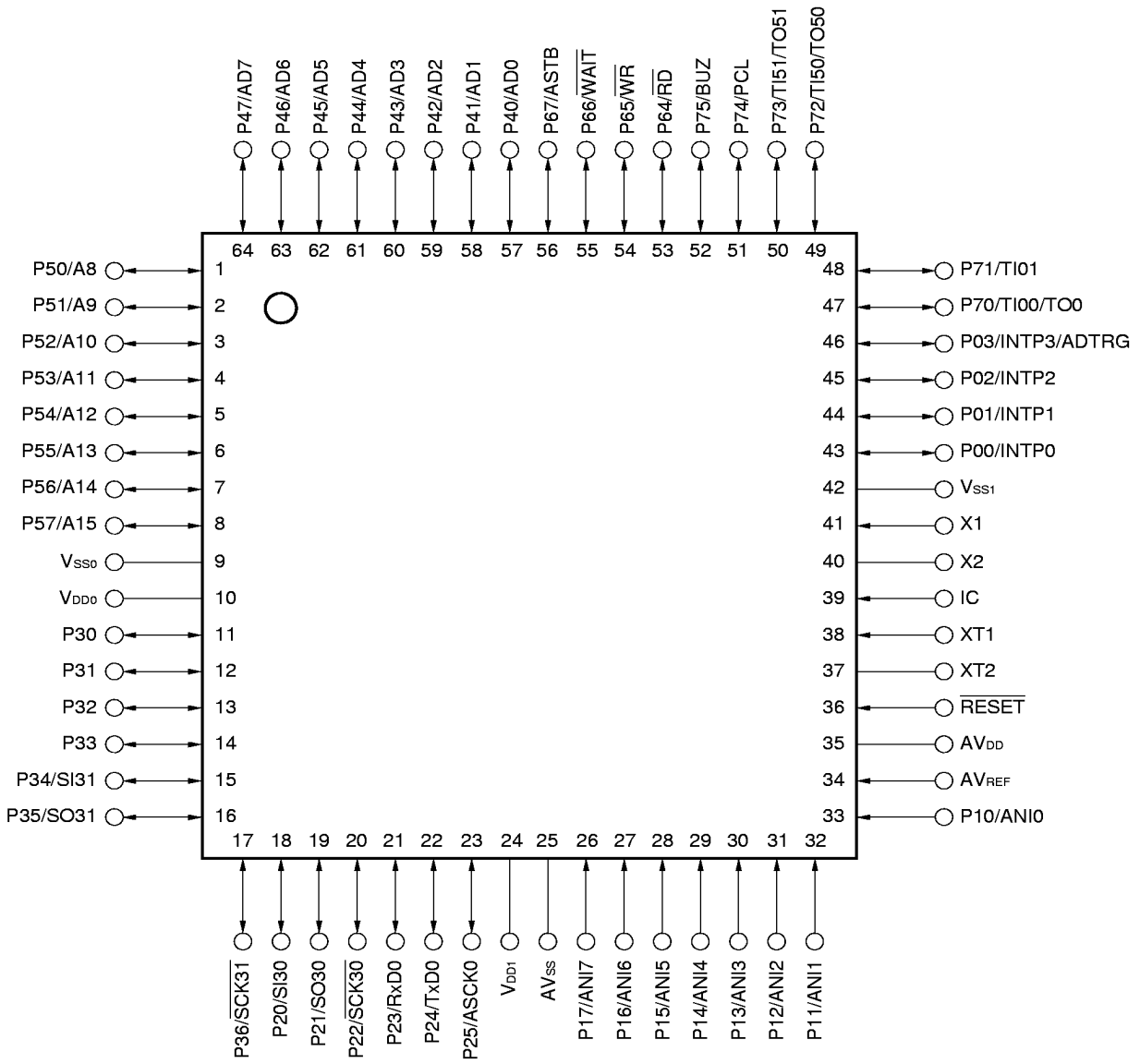
- **64-pin plastic shrink DIP (750 mil)**
  μPD780021CW-×××, 780022CW-×××, 780023CW-×××, 780024CW-×××



★ **Cautions 1. Connect the IC (Internally Connected) pin directly to V_{SS0} or V_{SS1}.**
2. Connect the AV_{SS} pin to V_{SS0}.

Remark When the μPD780021, 780022, 780023, and 780024 are used in applications where the noise generated inside the microcontroller needs to be reduced, the implementation of noise reduction measures, such as supplying voltage to V_{DD0} and V_{DD1} individually and connecting V_{SS0} and V_{SS1} to different ground lines, is recommended.

- **64-pin plastic QFP (14 × 14 mm)**
  μPD780021GC-×××-AB8, 780022GC-×××-AB8, 780023GC-×××-AB8, 780024GC-×××-AB8
- **64-pin plastic LQFP (12 × 12 mm)**
  μPD780021GK-×××-8A8, 780022GK-×××-8A8, 780023GK-×××-8A8, 780024GK-×××-8A8

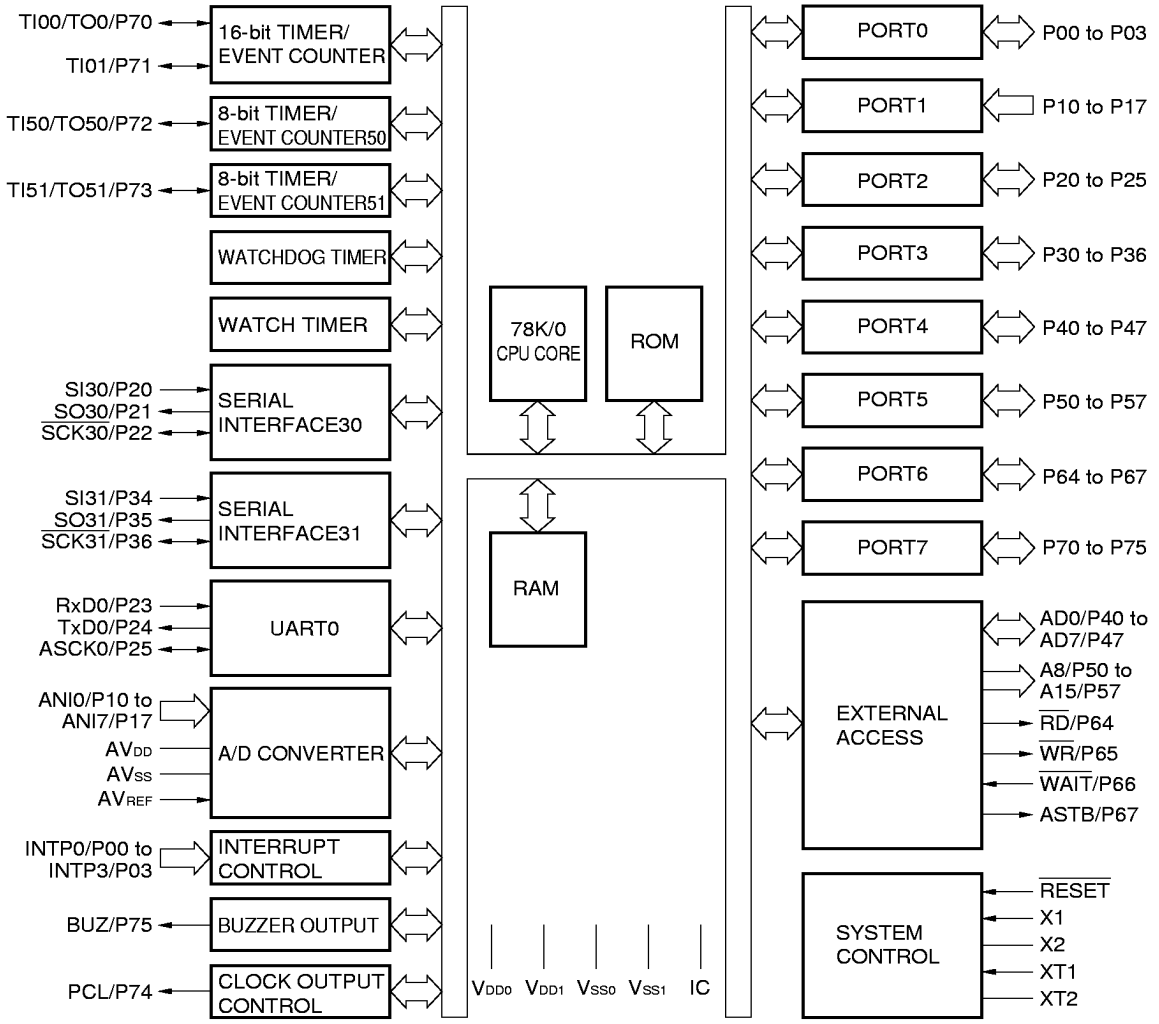


★ **Cautions 1. Connect the IC (Internally Connected) pin directly to V_{SS0} or V_{SS1}.**
2. Connect the AV_{SS} pin to V_{SS0}.

Remark When the μPD780021, 780022, 780023, and 780024 are used in applications where the noise generated inside the microcontroller needs to be reduced, the implementation of noise reduction measures, such as supplying voltage to V_{DD0} and V_{DD1} individually and connecting V_{SS0} and V_{SS1} to different ground lines, is recommended.

A8 to A15	: Address Bus	P64 to P67	: Port 6
AD0 to AD7	: Address/Data Bus	P70 to P75	: Port 7
ADTRG	: AD Trigger Input	PCL	: Programmable Clock
ANI0 to ANI7	: Analog Input	$\overline{RD}$	: Read Strobe
ASCK0	: Asynchronous Serial Clock	$\overline{RESET}$	: Reset
ASTB	: Address Strobe	RxD0	: Receive Data
AV_{DD}	: Analog Power Supply	$\overline{SCK30}$, $\overline{SCK31}$	: Serial Clock
AV_{REF}	: Analog Reference Voltage	SI30, SI31	: Serial Input
AV_{SS}	: Analog Ground	SO30, SO31	: Serial Output
BUZ	: Buzzer Clock	TI00, TI01, TI50, TI51	: Timer Input
IC	: Internally Connected	TO0, TO50, TO51	: Timer Output
INTP0 to INTP3	: Interrupt from Peripherals	TxD0	: Transmit Data
P00 to P03	: Port 0	V_{DD0}, V_{DD1}	: Power Supply
P10 to P17	: Port 1	V_{SS0}, V_{SS1}	: Ground
P20 to P25	: Port 2	$\overline{WAIT}$	: Wait
P30 to P36	: Port 3	$\overline{WR}$	: Write Strobe
P40 to P47	: Port 4	X1, X2	: Crystal (Main System Clock)
P50 to P57	: Port 5	XT1, XT2	: Crystal (Subsystem Clock)

2. BLOCK DIAGRAM



Remark The internal ROM and RAM capacities depend on the product.

3. PIN FUNCTIONS

3.1 Port Pins (1/2)

Pin Name	I/O	Function	After Reset	Alternate Function
P00	I/O	Port 0 4-bit input/output port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be connected by software.	Input	INTP0
P01				INTP1
P02				INTP2
P03				INTP3/ADTRG
P10 to P17	Input	Port 1 8-bit input only port.	Input	ANI0 to ANI7
P20	I/O	Port 2 6-bit input/output port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be connected by software.	Input	SI30
P21				SO30
P22				$\overline{\text{SCK30}}$
P23				RxD0
P24				TxD0
P25				ASCK0
P30	I/O	Port 3 7-bit input/output port. Input/output can be specified bit-wise.	N-ch open-drain input/output port. An on-chip pull-up resistor can be specified by mask option. LEDs can be driven directly.	Input	—
P31					
P32					
P33					
P34			When used as an input port, an on-chip pull-up resistor can be connected by software.		SI31
P35					SO31
P36					$\overline{\text{SCK31}}$
P40 to P47	I/O	Port 4 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be connected by software. Interrupt request flag (KRIF) is set to 1 by the falling edge detection.		Input	AD0 to AD7
P50 to P57	I/O	Port 5 8-bit input/output port. LEDs can be driven directly. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be connected by software.		Input	A8 to A15
P64	I/O	Port 6 4-bit input/output port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be connected by software.		Input	$\overline{\text{RD}}$
P65					$\overline{\text{WR}}$
P66					$\overline{\text{WAIT}}$
P67					ASTB

3.1 Port Pins (2/2)

Pin Name	I/O	Function	After Reset	Alternate Function
P70	I/O	Port 7 6-bit input/output port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be connected by software.	Input	TI00/TO0
P71				TI01
P72				TI50/TO50
P73				TI51/TO51
P74				PCL
P75				BUZ

3.2 Non-port Pins (1/2)

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0	Input	External interrupt request input for which the effective edge (rising edge, falling edge, or both rising edge and falling edge) can be specified.	Input	P00
INTP1				P01
INTP2				P02
INTP3				P03/ADTRG
SI30	Input	Serial interface serial data input.	Input	P20
SI31				P34
SO30	Output	Serial interface serial data output.	Input	P21
SO31				P35
$\overline{SCK30}$	I/O	Serial interface serial clock input/output.	Input	P22
$\overline{SCK31}$				P36
RxD0	Input	Serial data input for asynchronous serial interface.	Input	P23
TxD0	Output	Serial data output for asynchronous serial interface.	Input	P24
ASCK0	Input	Serial clock input for asynchronous serial interface.	Input	P25
TI00	Input	External count clock input to 16-bit timer (TM0). Capture trigger input to capture register (CR01) of 16-bit timer (TM0).	Input	P70/TO0
TI01		Capture trigger input to capture register (CR00) of 16-bit timer (TM0).		P71
TI50		External count clock input to 8-bit timer (TM50).		P72/TO50
TI51		External count clock input to 8-bit timer (TM51).		P73/TO51
TO0	Output	16-bit timer (TM0) output.	Input	P70/TI00
TO50		8-bit timer (TM50) output (shared with 8-bit PWM output).	Input	P72/TI50
TO51		8-bit timer (TM51) output (shared with 8-bit PWM output).		P73/TI51
PCL	Output	Clock output (for trimming of main system clock and subsystem clock).	Input	P74
BUZ	Output	Buzzer output.	Input	P75
AD0 to AD7	I/O	Lower address/data bus for extending memory externally.	Input	P40 to P47
A8 to A15	Output	Higher address bus for extending memory externally.	Input	P50 to P57
$\overline{RD}$	Output	Strobe signal output for read operation of external memory.	Input	P64
$\overline{WR}$		Strobe signal output for write operation of external memory.		P65
$\overline{WAIT}$	Input	Inserting wait for accessing external memory.	Input	P66
ASTB	Output	Strobe output which externally latches address information output to port 4 and port 5 to access external memory.	Input	P67

3.2 Non-port Pins (2/2)

Pin Name	I/O	Function	After Reset	Alternate Function
ANI0 to ANI7	Input	A/D converter analog input.	Input	P10 to P17
ADTRG	Input	A/D converter trigger signal input.	Input	P03/INTP3
AV_{REF}	Input	A/D converter reference voltage input.	—	—
AV_{DD}	—	A/D converter analog power supply. Set potential to that of V_{DD0} or V_{DD1}.	—	—
AV_{SS}	—	A/D converter ground potential. Set potential to that of V_{SS0} or V_{SS1}.	—	—
$\overline{RESET}$	Input	System reset input.	—	—
X1	Input	Connecting crystal resonator for main system clock oscillation.	—	—
X2	—		—	—
XT1	Input	Connecting crystal resonator for subsystem clock oscillation.	—	—
XT2	—		—	—
V_{DD0}	—	Positive power supply for ports.	—	—
V_{SS0}	—	Ground potential of ports.	—	—
V_{DD1}	—	Positive power supply (except ports).	—	—
V_{SS1}	—	Ground potential (except ports).	—	—
★ IC	—	Internally connected. Connect directly to V_{SS0} or V_{SS1}.	—	—

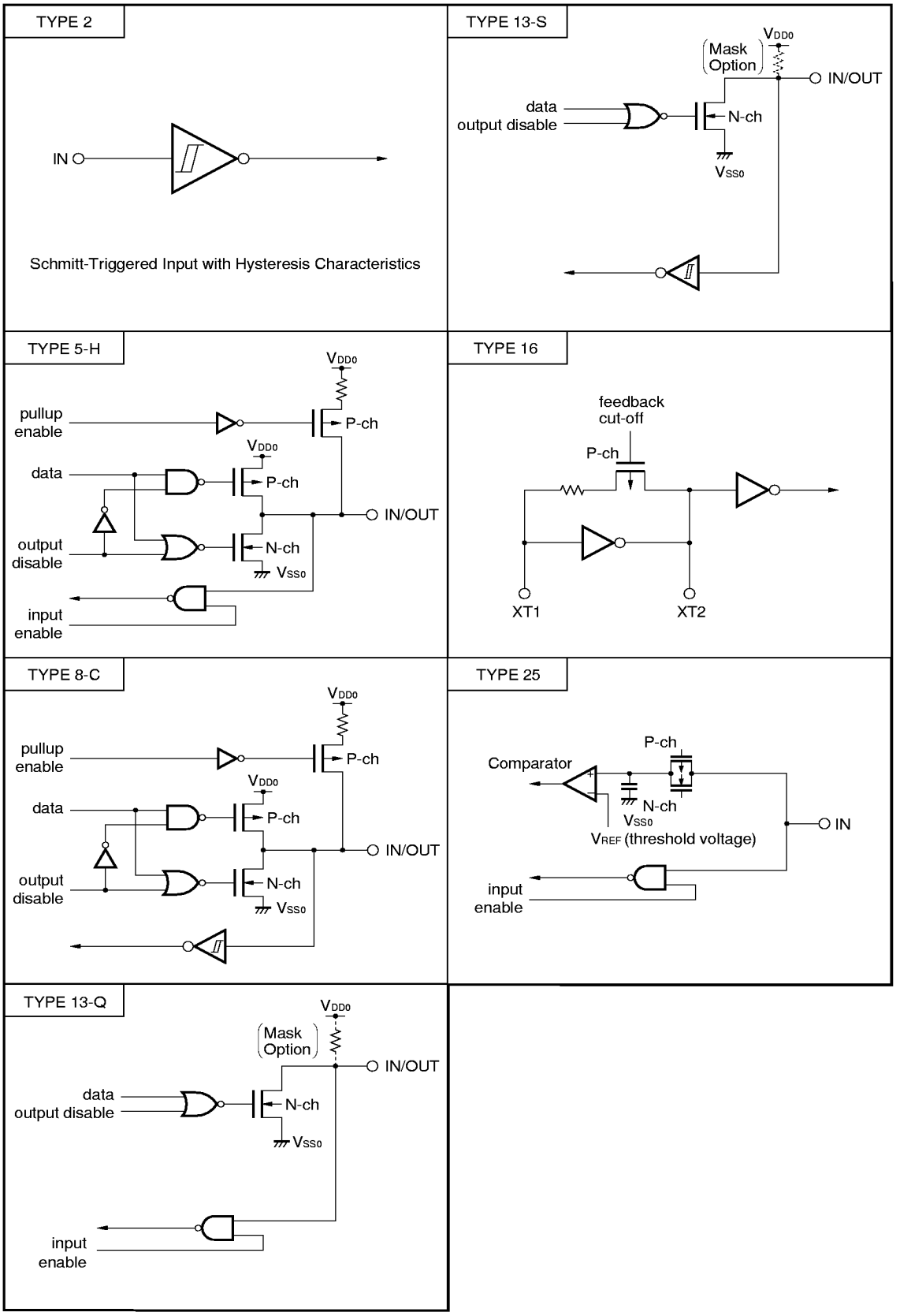
3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 3-1. For the input/output circuit configuration of each type, see Figure 3-1.

Table 3-1. Input/Output Circuit Type of Each Pin

	Pin Name	Input/output Circuit Type	I/O	Recommended Connection when not Used
	P00/INTP0	8-C	Input	Independently connect to V_{SS0} via a resistor .
	P01/INTP1			
	P02/INTP2			
	P03/INTP3			
	P10/ANI0 to P17/ANI7	25	Input	Independently connect to V_{DD0} or V_{SS0} via a resistor.
	P20/SI30	8-C	Input/output	
	P21/SO30	5-H		
	P22/$\overline{SCK30}$	8-C		
	P23/RxD0			
	P24/TxD0	5-H		
	P25/ASCK0	8-C		
	P30, P31	13-Q	Input/output	Independently connect to V_{DD0} via a resistor .
	P32, P33	13-S		
	P34/SI31	8-C		Independently connect to V_{DD0} or V_{SS0} via a resistor .
	P35/SO31	5-H		
	P36/$\overline{SCK31}$	8-C		
	P40/AD0 to P47/AD7	5-H	Input/output	Independently connect to V_{DD0} via a resistor.
	P50/A8 to P57/A15			Independently connect to V_{DD0} or V_{SS0} via a resistor.
	P64/$\overline{RD}$			
	P65/$\overline{WR}$			
	P66/$\overline{WAIT}$			
	P67/ASTB			
	P70/TI00/TO0	8-C		
	P71/TI01			
	P72/TI50/TO50			
	P73/TI51/TO51			
	P74/PCL	5-H		
	P75/BUZ			
	$\overline{RESET}$	2	Input	—
	XT1	16		Connect to V_{DD0}.
	XT2		—	Leave open
	AV_{DD}	—		Connect to V_{DD0}.
★	AV_{REF}			Connect directly to V_{SS0}.
★	AV_{SS}			
★	IC			Internally connected. Connect directly to V_{SS0} or V_{SS1}.

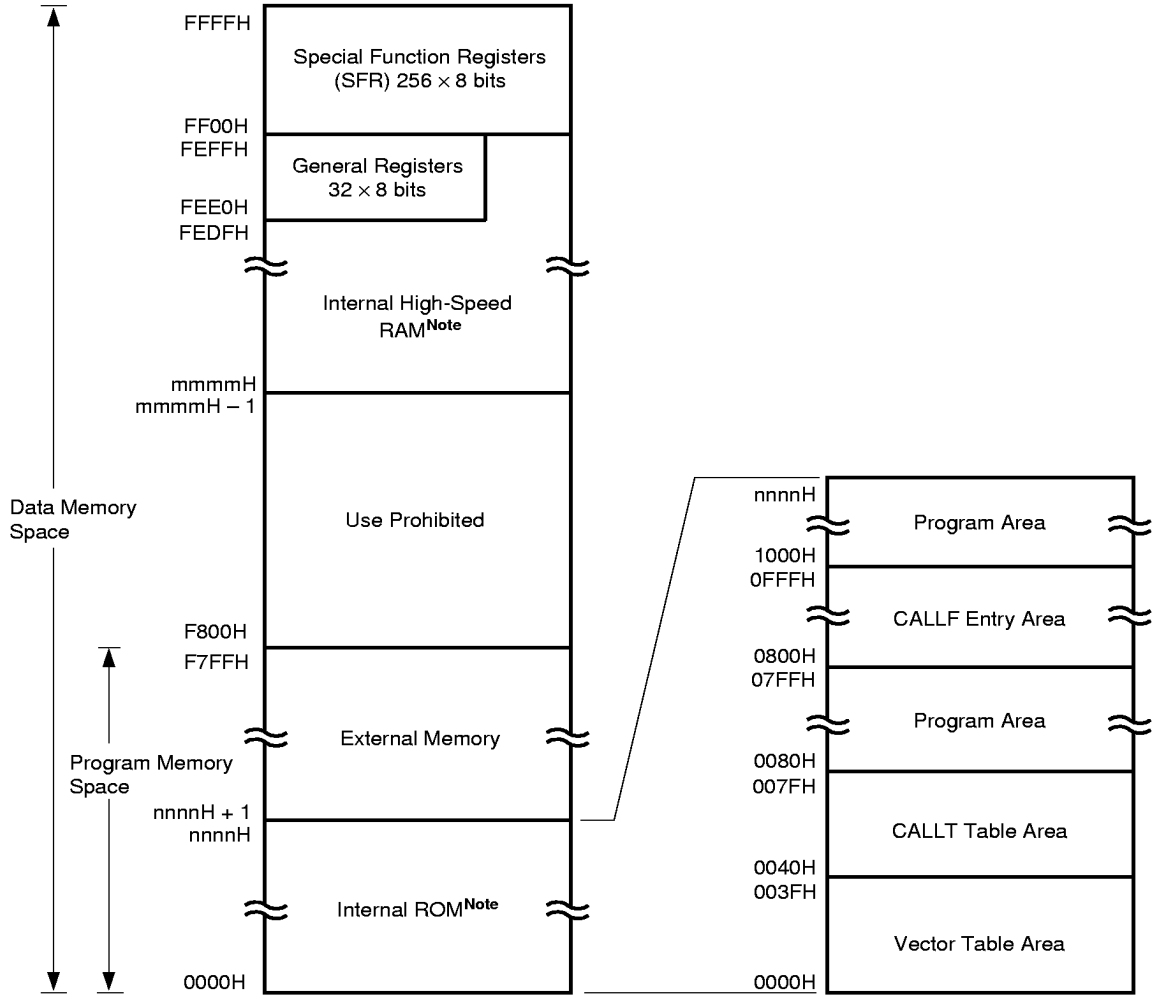
Figure 3-1. Pin Input/Output Circuits



4. MEMORY SPACE

Figure 4-1 shows the memory map of the μPD780021, 780022, 780023, and 780024.

Figure 4-1. Memory Map



Note The internal ROM capacity and internal high-speed RAM capacity depend on the products (see the following table).

Part Number	Internal ROM Last Address nnnnH	Internal High-Speed RAM Start Address mmmmH
μPD780021	1FFFH	FD00H
μPD780022	3FFFH	
μPD780023	5FFFH	FB00H
μPD780024	7FFFH	

5. PERIPHERAL HARDWARE FUNCTION FEATURES

5.1 Ports

The following 3 types of I/O ports are available.

- CMOS input (Port 1) : 8
- CMOS input/output (Port 0, Port 2 to Port 7) : 39
- N-channel open-drain input/output (P30 to P33) : 4

Total : 51

Table 5-1. Port Functions

Name	Pin Name	Function
Port 0	P00 to P03	Input/output port pins. Input/output specifiable bit-wise. When used as input port pins, on-chip pull-up resistor can be used by software.
Port 1	P10 to P17	Dedicated input port pins.
Port 2	P20 to P25	Input/output port pins. Input/output specifiable bit-wise. When used as input port pins, on-chip pull-up resistor can be used by software.
Port 3	P30 to P33	N-channel open-drain input/output port pins. Input/output specifiable bit-wise. On-chip pull-up resistor can be used by mask option. LED can be driven directly.
	P34 to P36	Input/output port pins. Input/output specifiable bit-wise. When used as input port pins, on-chip pull-up resistor can be used by software.
Port 4	P40 to P47	Input/output port pins. Input/output specifiable bit-wise. When used as input port pins, on-chip pull-up resistor can be used by software. Test input flag (KRIF) is set to 1 by falling edge detection.
Port 5	P50 to P57	Input/output port pins. Input/output specifiable bit-wise. When used as input port pins, on-chip pull-up resistor can be used by software. LED can be driven directly.
Port 6	P64 to P67	Input/output port pins. Input/output specifiable bit-wise. When used as input port pins, on-chip pull-up resistor can be used by software.
Port 7	P70 to P75	Input/output port pins. Input/output specifiable bit-wise. When used as input port pins, on-chip pull-up resistor can be used by software.

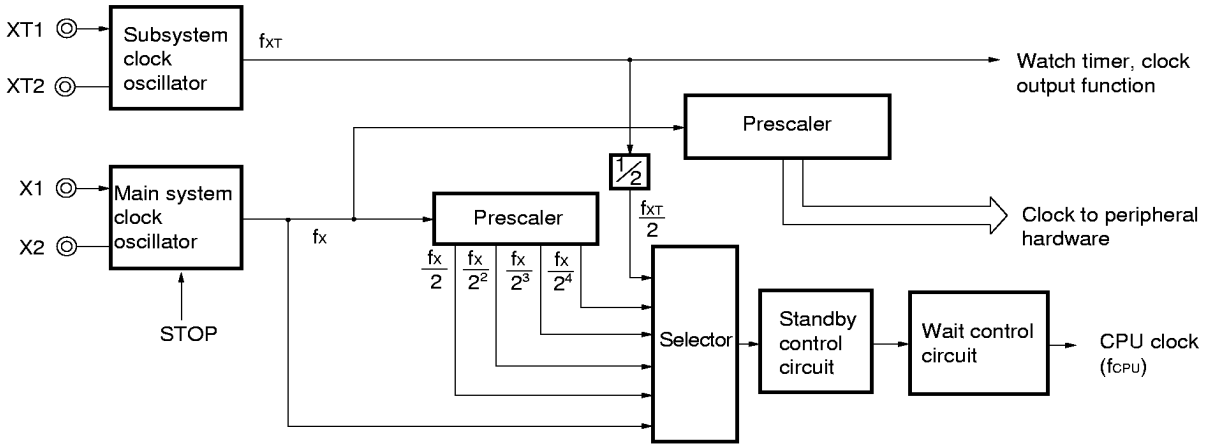
5.2 Clock Generator

A system clock generator is incorporated.

The minimum instruction execution time can also be changed.

- 0.24 μs/0.48 μs/0.95 μs/1.91 μs/3.81 μs (main system clock: at 8.38-MHz operation)
- 122 μs (subsystem clock: at 32.768-kHz operation)

Figure 5-1. Block Diagram of Clock Generator



5.3 Timer/Counter

Five timer/counter channels are incorporated.

- 16-bit timer/event counter : 1 channel
- 8-bit timer/event counter : 2 channels
- Watch timer : 1 channel
- Watchdog timer : 1 channel

Table 5-2. Operations of Timer/Event Counter

	16-Bit Timer/ Event Counter TM0	8-Bit Timer/ Event Counter TM50, TM51	Watch Timer	Watchdog Timer
Operation mode				
Interval timer	2 channels[Note 1]	2 channels	1 channel[Note 2]	1 channel[Note 3]
External event counter	1 channel	2 channels	—	—
Function				
Timer output	1 output	2 outputs	—	—
PWM output	—	2 outputs	—	—
Pulse width measurement	2 inputs	—	—	—
Square wave output	1 output	2 outputs	—	—
One-shot pulse output	1 output	—	—	—
Interrupt source	2	2	2	1

Notes 1. When capture/compare registers 00, 01 (CR00, CR01) are both specified as compare registers

2. The watch timer can perform both watch timer and interval timer functions at the same time.

3. The watchdog timer has the watchdog timer and interval timer functions. However, use the watchdog timer by selecting either the watchdog timer function or the interval timer function.

Figure 5-2. Block Diagram of 16-bit Timer/Event Counter TM0

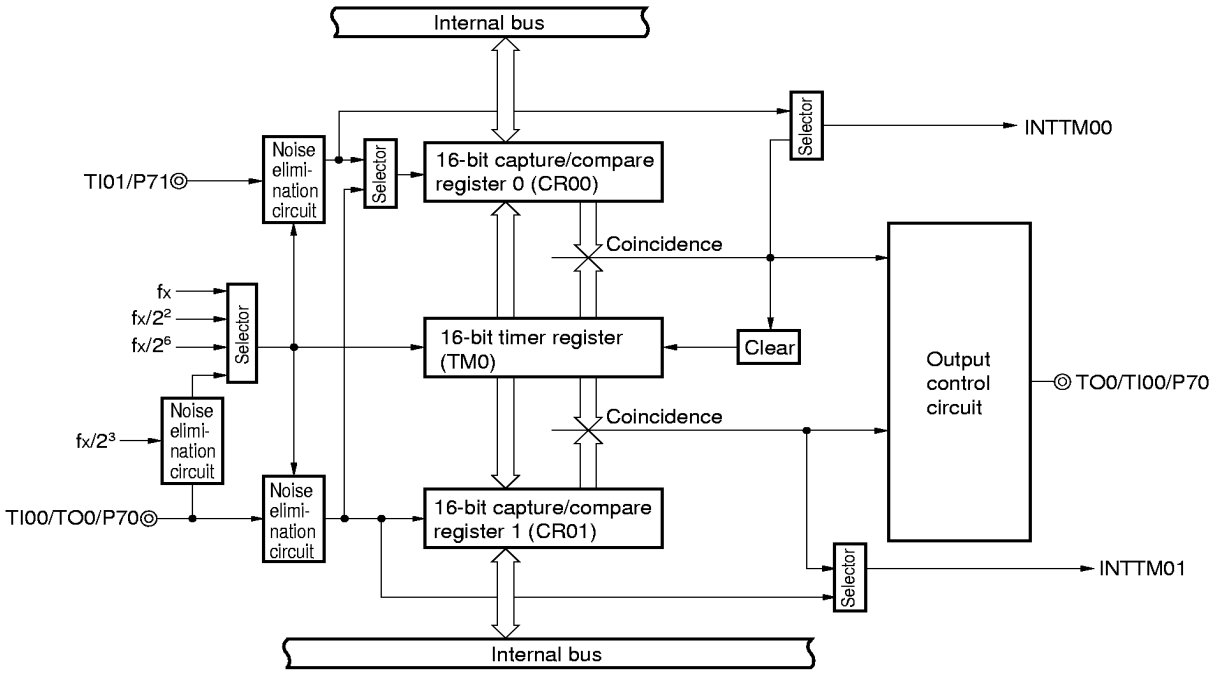


Figure 5-3. Block Diagram of 8-bit Timer/Event Counter TM50

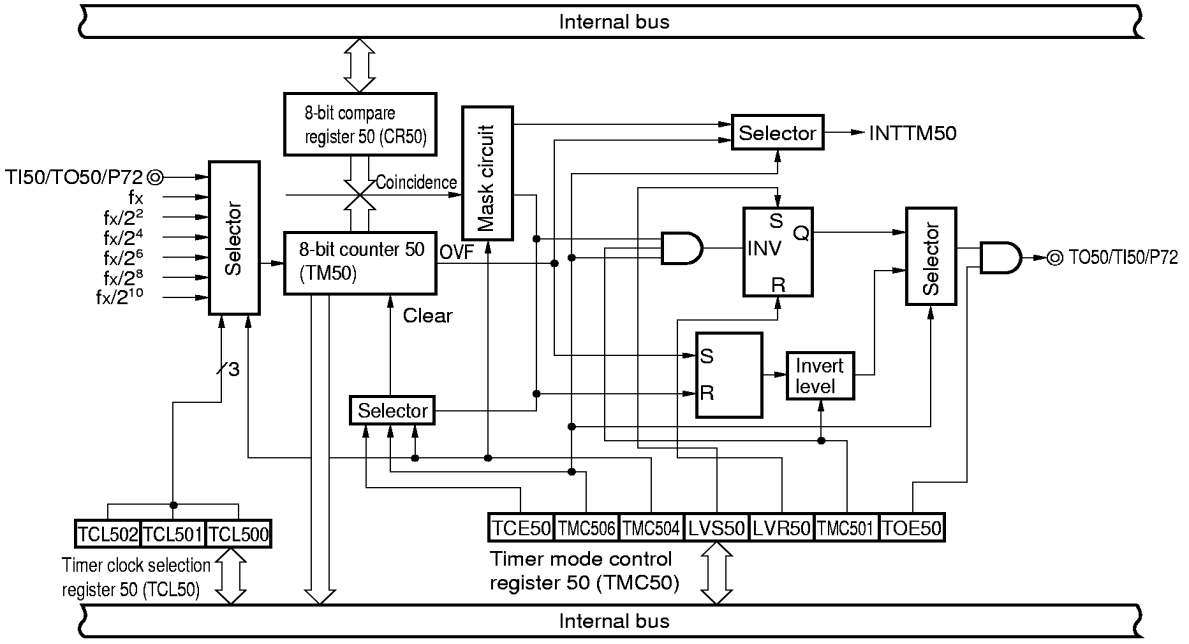


Figure 5-4. Block Diagram of 8-bit Timer/Event Counter TM51

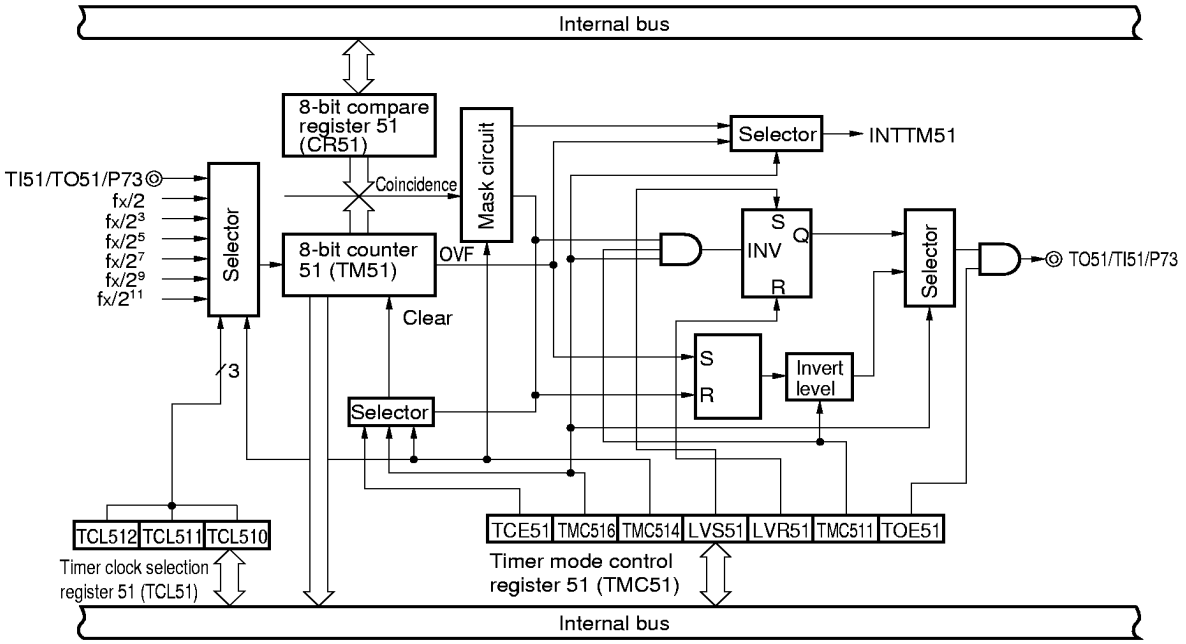
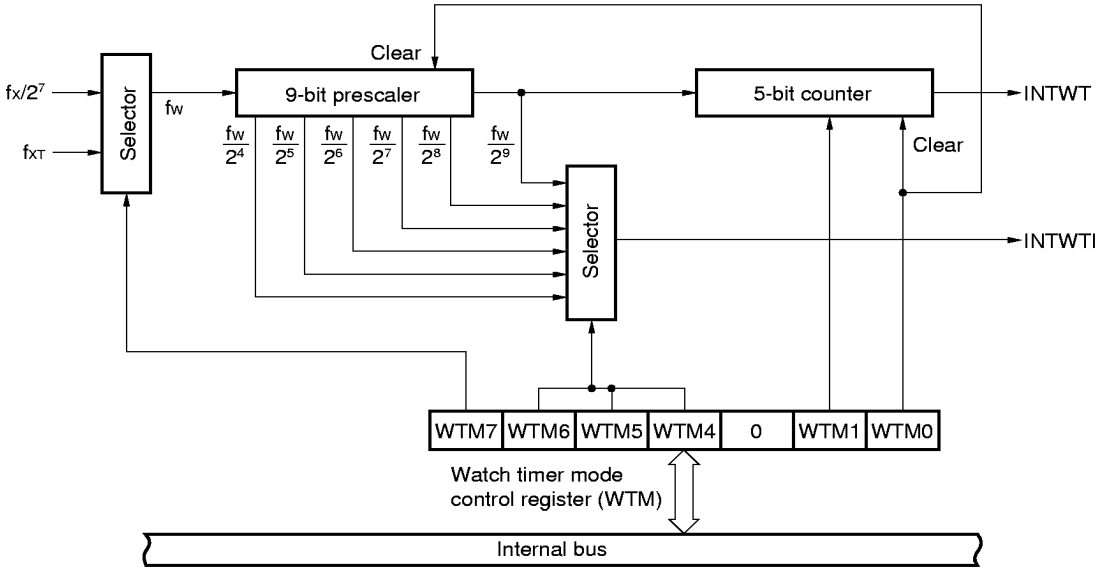
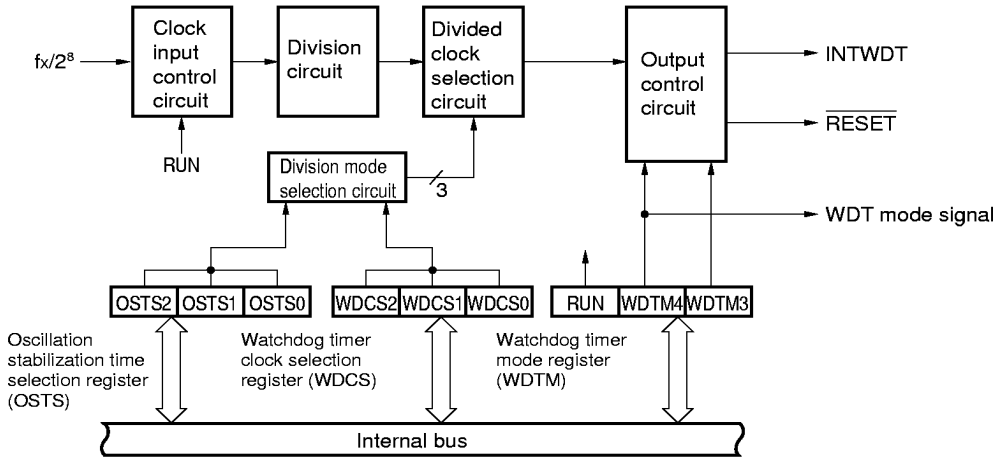


Figure 5-5. Block Diagram of Watch Timer



★ **Figure 5-6. Block Diagram of Watchdog Timer**



5.4 Clock Output/Buzzer Output Control Circuit

A clock output/buzzer output control circuit (CKU) is incorporated.

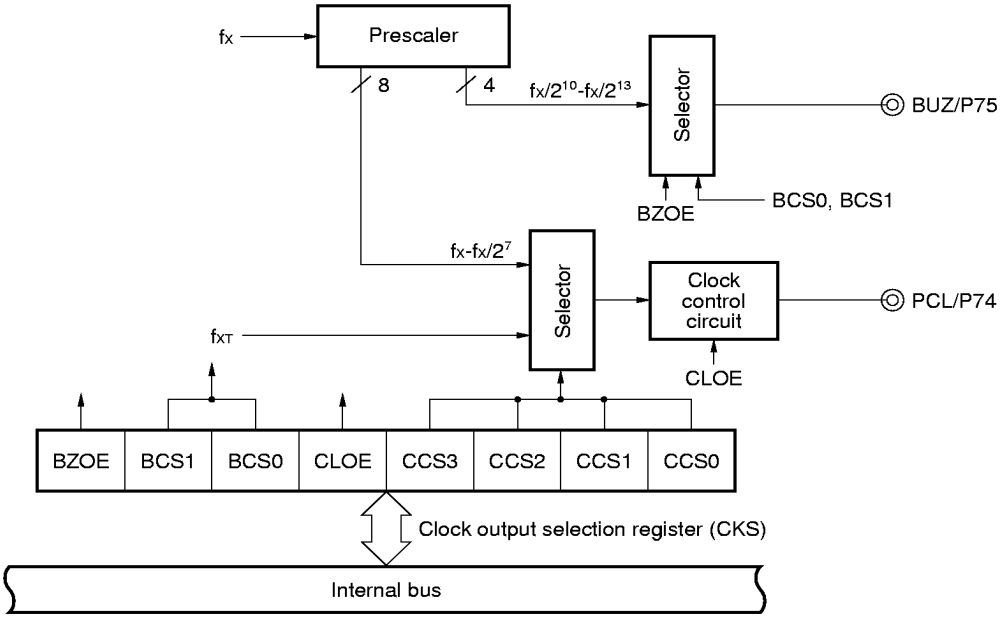
Clocks with the following frequencies can be output as a clock output.

- 65.5 kHz/131 kHz/262 kHz/524 kHz/1.05 MHz/2.10 MHz/4.19 MHz/8.38 MHz (main system clock: at 8.38-MHz operation)
- 32.768 kHz (subsystem clock: at 32.768-kHz operation)

Clocks with the following frequencies can be output as a buzzer output.

- 1.02 kHz/2.05 kHz/4.10 kHz/8.19 kHz (main system clock: at 8.38-MHz operation)

★ **Figure 5-7. Block Diagram of Clock Output/Buzzer Output Control Circuit CKU**



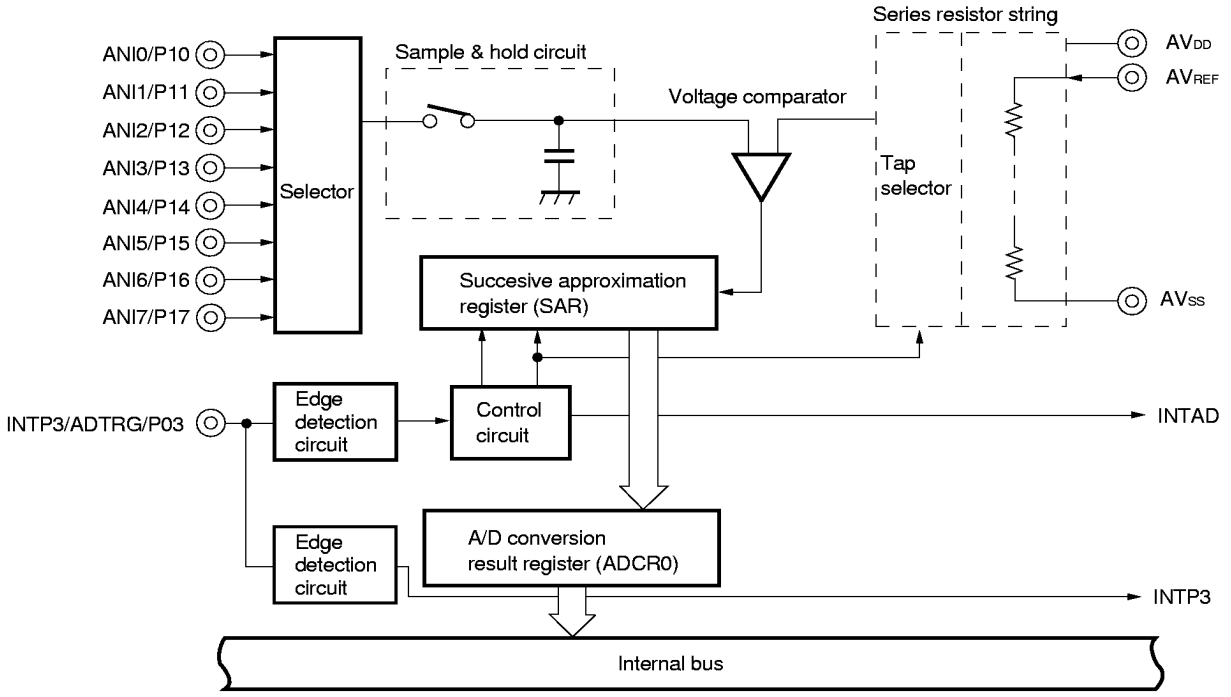
5.5 A/D Converter

An A/D converter of 8-bit resolution × 8 channels is incorporated.

The following two types of the A/D conversion operation start-up methods are available.

- Hardware start
- Software start

Figure 5-8. Block Diagram of A/D Converter



5.6 Serial Interface

Three channels of the serial interface are incorporated.

- Serial interface UART0 : 1 channel
- Serial interface SIO3n (n = 0, 1): 2 channels

(1) Serial interface UART0

The serial interface UART0 has two modes, asynchronous serial interface (UART) mode and infrared data transfer mode.

- **Asynchronous serial interface (UART) mode**

  This mode enables full-duplex operation wherein one byte of data is transmitted and received after the start bit.

  The on-chip dedicated UART baud rate generator enables communication using a wide range of selectable baud rates. In addition, a baud rate can be also defined by dividing the clock input to the ASCK0 pin.

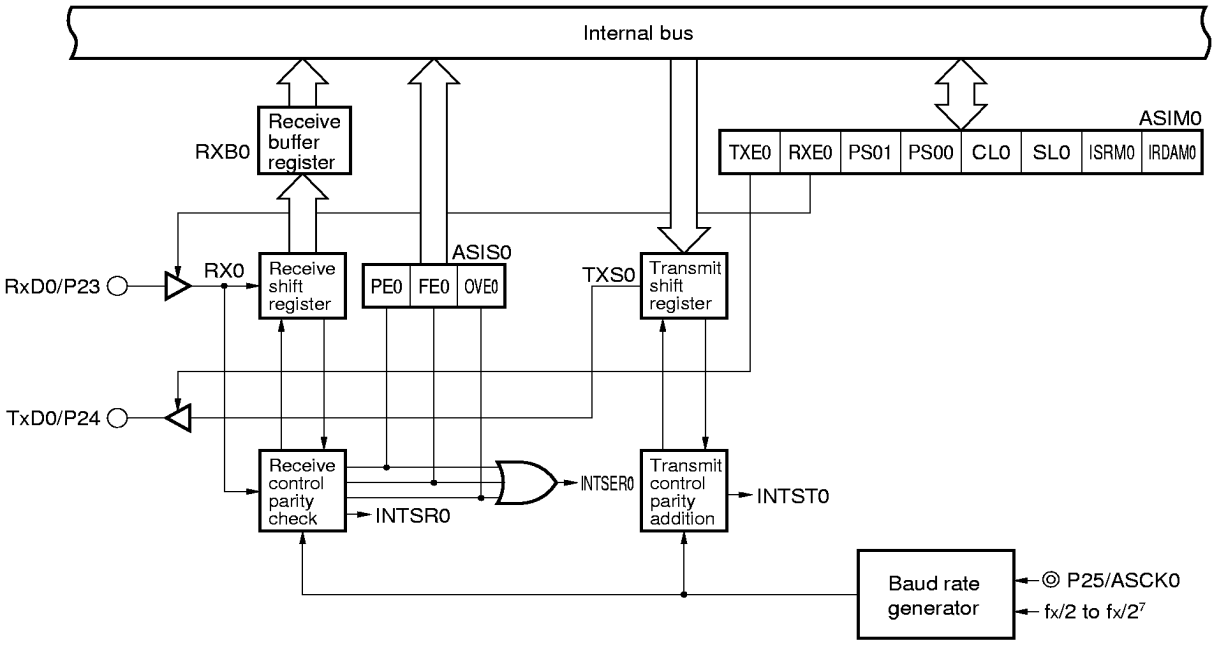
  The dedicated UART baud rate generator can also be used to generate a MIDI-standard baud rate (31.25 kbps).

★ • **Infrared data transfer mode**

  This mode enables pulse output and pulse reception in data format.

  This mode can be used for office equipment applications such as personal computers.

Figure 5-9. Block Diagram of Serial Interface UART0



(2) Serial interface SIO3n (n = 0, 1)

The serial interface SIO3n has the 3-wire serial I/O mode.

- **3-wire serial I/O mode (fixed as MSB first)**

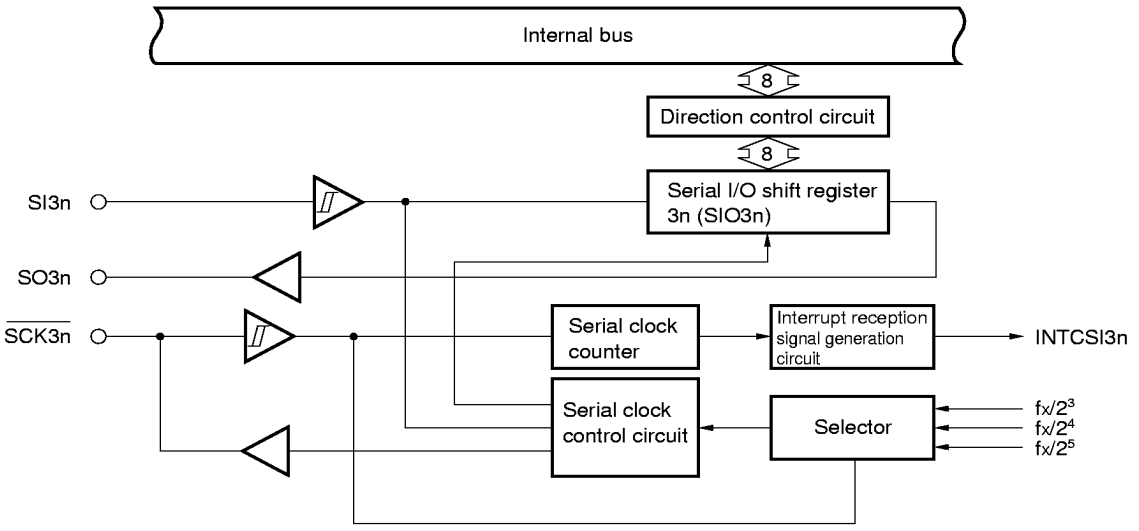
  This is an 8-bit data transfer mode using three lines: a serial clock line ($\overline{\text{SCK3n}}$), serial output line (SO3n), and serial input line (SI3n).

  Since simultaneous transmit and receive operations are enabled in the 3-wire serial I/O mode, the processing time for data transfer is reduced.

  The first bit in 8-bit data in the serial transfer is fixed as MSB.

  The 3-wire serial I/O mode is useful for connection to a peripheral I/O device that includes a clocked serial interface, a display controller, etc.

Figure 5-10. Block Diagram of Serial Interface SIO3n



Remark n = 0, 1

6. INTERRUPT FUNCTIONS

There are 20 interrupt functions of three different types, as shown below.

- Non-maskable: 1
- Maskable : 18
- Software : 1

Table 6-1. Interrupt Source List

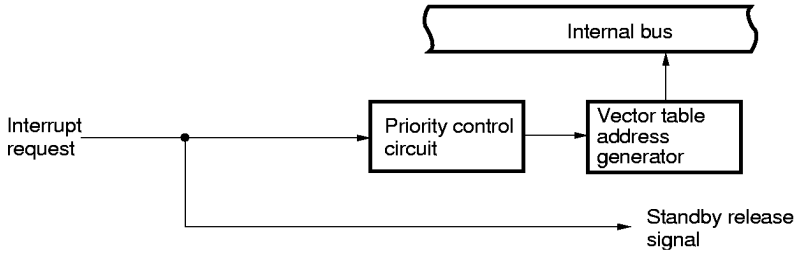
Type of Interrupt	Default Priority[Note 1]	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type[Note 2]
		Name	Trigger			
Non-maskable	—	INTWDT	Watchdog timer overflow (watchdog timer mode 1 selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Watchdog timer overflow (interval timer mode selected)			(B)
	1	INTP0	Pin input edge detection	External	0006H	(C)
	2	INTP1			0008H	
	3	INTP2			000AH	
	4	INTP3			000CH	
	5	INTSER0	Generation of serial interface UART0 reception error	Internal	000EH	(B)
	6	INTSR0	End of serial interface UART0 reception		0010H	
	7	INTST0	End of serial interface UART0 transmission		0012H	
	8	INTCSI30	End of serial interface SIO3 (SIO30) transfer		0014H	
	9	INTCSI31	End of serial interface SIO3 (SIO31) transfer		0016H	
	10	INTWTI	Reference time interval signal from watch timer		001AH	
	11	INTTM00	Generation of coincidence signal of 16-bit timer register and capture/compare register 00 (CR00) (when CR00 specified as compare register)		001CH	
	12	INTTM01	Generation of coincidence signal of 16-bit timer register and capture/compare register 01 (CR01) (when CR01 specified as compare register)		001EH	
	13	INTTM50	Generation of coincidence signal of 8-bit timer/event counter 50		0020H	
	14	INTTM51	Generation of coincidence signal of 8-bit timer/event counter 51		0022H	
	15	INTAD0	End of conversion by A/D converter		0024H	
	16	INTWT	Watch timer overflow		0026H	
	17	INTKR	Falling edge detection of port 4	External	0028H	(D)
Software	—	BRK	BRK instruction execution	—	003EH	(E)

Notes 1. The default priority is a priority order when two or more maskable interrupt requests are generated simultaneously. 0 is the highest order and 17, the lowest.

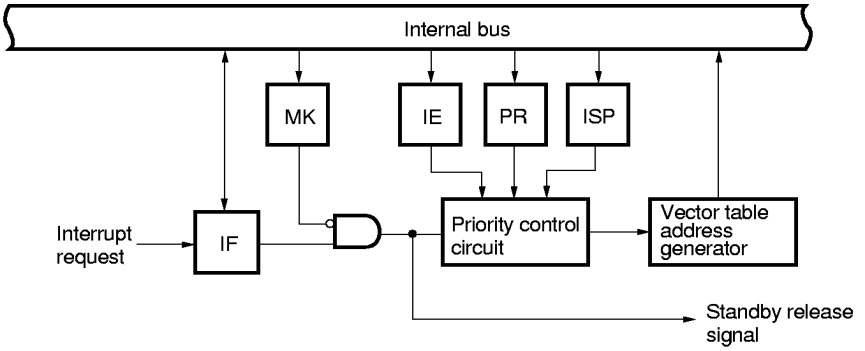
2. Basic configuration types (A) to (E) correspond to (A) to (E) in Figure 6-1, respectively.

Figure 6-1. Basic Configuration of Interrupt Function (1/2)

(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt (INTP0 to INTP3)

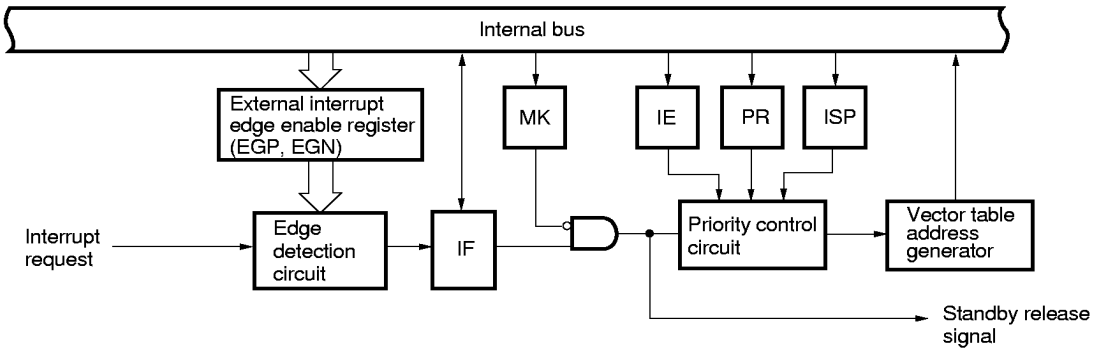
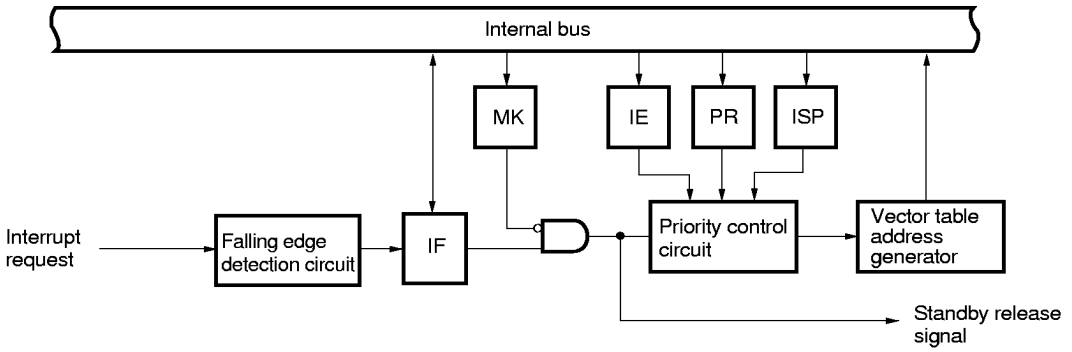
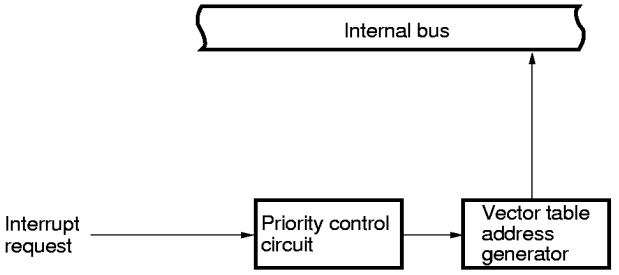


Figure 6-1. Basic Configuration of Interrupt Function (2/2)

(D) External maskable interrupt (INTKR)



(E) Software interrupt



IF : Interrupt request flag
IE : Interrupt enable flag
ISP : In-service priority flag
MK : Interrupt mask flag
PR : Priority specification flag

7. EXTERNAL DEVICE EXPANSION FUNCTIONS

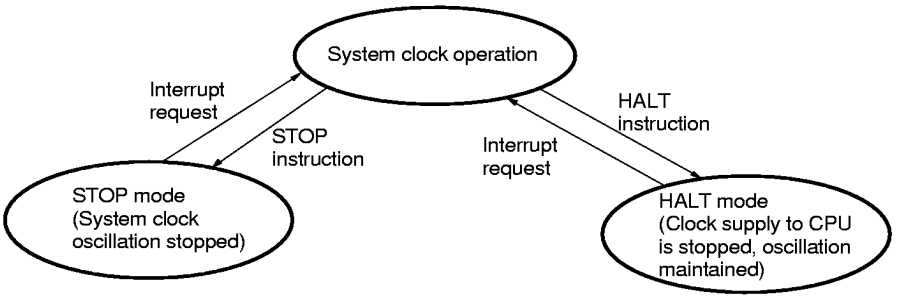
The external device expansion functions connect external devices to areas other than the internal ROM, RAM and SFR. Ports 4 to 6 are used for external device connection.

8. STANDBY FUNCTIONS

There are the following two standby functions to reduce the consumption current.

- HALT mode: The CPU operating clock is stopped. The average consumption current can be reduced by intermittent operation in combination with the normal operating mode.
- STOP mode: The system clock oscillation is stopped. The whole operation by the system clock is stopped, so that the system operates with ultra-low power consumption.

Figure 8-1. Standby Function



9. RESET FUNCTION

There are the following two reset methods.

- External reset by $\overline{\text{RESET}}$ pin
- Internal reset by watchdog timer runaway time detection

10. INSTRUCTION SET

(1) 8-bit instructions

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

First operand \ Second operand	#byte	A	r[Note]	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL + byte] [HL + B] [HL + C]	$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP											INC DEC
B, C											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV									DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]		MOV											
[HL]		MOV											ROR4 ROL4
[HL + byte] [HL + B] [HL + C]		MOV											
X													MULU
C													DIVUW

Note Except r = A

(2) 16-bit instructions

MOVW, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

First operand \ Second operand	#word	AX	rp[Note]	sfrp	saddrp	!addr16	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW[Note]						INCW, DECW PUSH, POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
!addr16		MOVW						
SP	MOVW	MOVW						

Note Only when rp = BC, DE or HL

(3) Bit manipulation instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

First operand \ Second operand	A.bit	sfr.bit	saddr.bit	PSW.bit	[HL].bit	CY	$addr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1

(4) Call instruction/branch instructions

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

First operand \ Second operand	AX	!addr16	!addr11	[addr5]	$addr16
Basic instruction	BR	CALL BR	CALLF	CALLT	BR, BC, BNC BZ, BNZ
Compound instruction					BT, BF BTCLR DBNZ

(5) Other instructions

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

★ 11. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Test Conditions		Ratings	Unit
Supply voltage	V_{DD}			–0.3 to +6.5	V
	AV_{DD}			–0.3 to V_{DD} + 0.3	V
	AV_{REF}			–0.3 to V_{DD} + 0.3	V
	AV_{SS}			–0.3 to +0.3	V
Input voltage	V_{I1}	P00 to P03, P10 to P17, P20 to P25, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75, X1, X2, XT1, XT2, $\overline{\text{RESET}}$		–0.3 to V_{DD} + 0.3	V
	V_{I2}	P30 to P33	N-ch open-drain	–0.3 to V_{DD} + 0.3	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
Analog input voltage	V_{AN}	P10 to P17	Analog input pin	AV_{SS} – 0.3 to AV_{REF0} + 0.3 and –0.3 to V_{DD} + 0.3	V
High-level output current	I_{OH}	Per pin		–10	mA
		Total for P00 to P03, P40 to P47, P50 to P57, P64 to P67, P70 to P75		–15	mA
		Total for P20 to P25, P30 to P36		–15	mA
Low-level output current	I_{OL} Note	Per pin for P00 to P03, P20 to P25, P34 to P36, P40 to P47, P64 to P67, P70 to P75	Peak value	20	mA
			Effective value	10	mA
		Per pin for P30 to P33, P50 to P57	Peak value	30	mA
			Effective value	15	mA
		Total for P00 to P03, P40 to P47, P64 to P67, P70 to P75	Peak value	50	mA
			Effective value	20	mA
		Total for P20 to P25	Peak value	20	mA
			Effective value	10	mA
		Total for P30 to P36	Peak value	100	mA
			Effective value	70	mA
		Total for P50 to P57	Peak value	100	mA
			Effective value	70	mA
Operating ambient tempature	T_A		Peak value	–40 to +85	°C
Storage temperature	T_{stg}		Effective value	–65 to +150	°C

Note The effective value should be calculated as follows: [Effective value] = [Peak value] × $\sqrt{\text{duty}}$

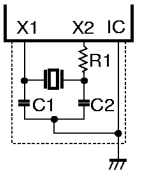
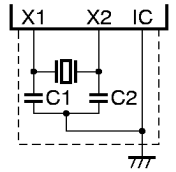
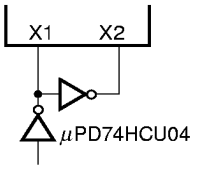
Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz Unmeasured pins returned to 0 V.				15	pF
I/O capacitance	C_{IO}	f = 1 MHz Unmeasured pins returned to 0 V.	P00 to P03, P20 to P25, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75			15	pF
			P30 to P33			20	pF

Remark Unless specified otherwise, alternate-function pin characteristics are the same as port pin characteristics.

Main System Clock Oscillation Circuit Characteristics (T_A = –40 to 85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (fx)Note 1	V_{DD} = 4.5 to 5.5 V	1.0		8.38	MHz
				1.0		5.0	
		Oscillation stabilization timeNote 2	After V_{DD} reaches oscillation voltage range MIN.			4	ms
Crystal resonator		Oscillator frequency (fx)Note 1	V_{DD} = 4.5 to 5.5 V	1.0		8.38	MHz
				1.0		5.0	
		Oscillation stabilization timeNote 2	V_{DD} = 4.5 to 5.5 V			10	ms
						30	
External clock		X1 input frequency (fx)Note 1	V_{DD} = 4.5 to 5.5 V	1.0		8.38	MHz
						5.0	
		X1 input high-/low-level width (t_{XH}, t_{XL})	V_{DD} = 4.5 to 5.5 V	50		500	ns
				85		500	

Notes 1. Indicates only oscillation circuit characteristics. Refer to AC Characteristics for instruction execution time.

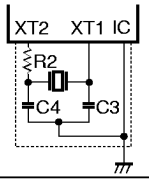
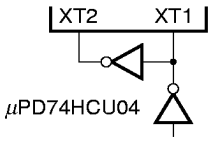
2. Time required to stabilize oscillation after reset or STOP mode release.

Cautions 1. When using the main system clock oscillator, wiring in the area enclosed with the broken line in the above figures should be carried out as follows to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always keep the ground point of the oscillator to the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern in which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. When the main system clock is stopped and the system is operated by the subsystem clock, the subsystem clock should be switched again to the main system clock after the oscillation stabilization time is secured by the program.

Subsystem Clock Oscillation Circuit Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT})Note 1		32	32.768	35	kHz
		Oscillation stabilization timeNote 2	V_{DD} = 4.5 to 5.5 V		1.2	2	s
						10	
External clock		XT1 input frequency (f_{XT})Note 1		32		100	kHz
		XT1 input high-/low-level width (t_{XTH}, t_{XTL})		5		15	μs

Notes 1. Indicates only oscillation circuit characteristics. Refer to AC Characteristics for instruction execution time.

2. Time required to stabilize oscillation after V_{DD} reaches oscillation voltage MIN.

Cautions 1. When using the subsystem clock oscillator, wiring in the area enclosed with the broken line in the above figures should be carried out as follows to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always keep the ground point of the oscillator to the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern in which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The subsystem clock oscillator is a low-amplitude circuit in order to achieve a low consumption current, and is more prone to malfunction due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P10 to P17, P21, P24, P35, P40 to P47, P50 to P57, P64 to P67, P74, P75	V_{DD} = 2.7 to 5.5 V	0.7 V_{DD}		V_{DD}	V
				0.8 V_{DD}		V_{DD}	V
	V_{IH2}	P00 to P03, P20, P22, P23, P25, P34, P36, P70 to P73, $\overline{\text{RESET}}$	V_{DD} = 2.7 to 5.5 V	0.8 V_{DD}		V_{DD}	V
				0.85 V_{DD}		V_{DD}	V
	V_{IH3}	P30-P33 (N-ch open-drain)	V_{DD} = 2.7 to 5.5 V	0.7 V_{DD}		5.5	V
				0.8 V_{DD}		5.5	V
	V_{IH4}	X1, X2	V_{DD} = 2.7 to 5.5 V	V_{DD}–0.5		V_{DD}	V
				V_{DD}–0.2		V_{DD}	V
	V_{IH5}	XT1, XT2	V_{DD} = 4.5 to 5.5 V	0.8 V_{DD}		V_{DD}	V
				0.9 V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P10 to P17, P21, P24, P35, P40 to P47, P50 to P57, P64 to P67, P74, P75	V_{DD} = 2.7 to 5.5 V	0		0.3 V_{DD}	V
				0		0.2 V_{DD}	V
	V_{IL2}	P00 to P03, P20, P22, P23, P25, P34, P36, P70 to P73, $\overline{\text{RESET}}$	V_{DD} = 2.7 to 5.5 V	0		0.2 V_{DD}	V
				0		0.15 V_{DD}	V
	V_{IL3}	P30 to P33	4.5 V ≤ V_{DD} ≤ 5.5 V	0		0.3 V_{DD}	V
			2.7 V ≤ V_{DD} < 4.5 V	0		0.2 V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V	0		0.1 V_{DD}	V
	V_{IL4}	X1, X2	V_{DD} = 2.7 to 5.5 V	0		0.4	V
				0		0.2	V
	V_{IL5}	XT1, XT2	V_{DD} = 4.5 to 5.5 V	0		0.2 V_{DD}	V
				0		0.1 V_{DD}	V
Output voltage, high	V_{OH}	V_{DD} = 4.5 to 5.5 V, I_{OH} = –1mA		V_{DD}–1.0		V_{DD}	V
		I_{OH} = –100 μA		V_{DD}–0.5		V_{DD}	V
Output voltage, low	V_{OL1}	P30 to P33, P50 to P57	V_{DD} = 4.5 to 5.5 V, I_{OL} = 15 mA		0.4	2.0	V
		P00 to P03, P20 to P25, P34 to P36, P40 to P47, P64 to P67, P70 to P75	V_{DD} = 4.5 to 5.5 V, I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	I_{OL} = 400 μA				0.5	V

Remark Unless specified otherwise, alternate-function pin characteristics are the same as port pin characteristics.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	$V_{IN} = V_{DD}$	P00 to P03, P10 to P17, P20 to P25, P34 to P36, P40 to P47, P50 to P57, P60 to P67, P70 to P75, $\overline{\text{RESET}}$			3	μA
	I_{LIH2}		X1, X2, XT1, XT2			20	μA
	I_{LIH3}	V_{IN} = 5.5 V	P30 to P33			80	μA
Input leakage current, low	I_{LIL1}	V_{IN} = 0 V	P00 to P03, P10 to P17, P20 to P25, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75, $\overline{\text{RESET}}$			–3	μA
	I_{LIL2}		X1, X2, XT1, XT2			–20	μA
	I_{LIL3}		P30 to P33			–3[Note]	μA
Output leakage current, high	I_{LOH}	$V_{OUT} = V_{DD}$				3	μA
Output leakage current, low	I_{LOL}	V_{OUT} = 0 V				–3	μA
Mask option pull-up resistor	R_1	V_{IN} = 0 V, P30, P31		15	30	90	kΩ
Software pull-up resistor	R_2	V_{IN} = 0 V, P00 to P03, P20 to P25, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75		15	30	90	kΩ

Note When the pull-up resistor is not included in P30 to P33 (specified by a mask option), a –200 μA (MAX.) low-level input leakage current flows only at the 3-clock interval (no wait) when the read instruction to port 3 (PM3) and port mode register 3 (PM3) is executed. At times other than this 3-clock interval, a –3 μA (MAX.) current flows.

Remark Unless specified otherwise, alternate-function pin characteristics are the same as port pin characteristics.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Power supply current[Note 1]	I_{DD1}	8.38-MHz crystal oscillation operating mode	V_{DD} = 5.0 V ±10%		8	16	mA
	I_{DD2}	8.38-MHz crystal oscillation HALT mode	V_{DD} = 5.0 V ±10%		1.6	3.2	mA
	I_{DD3}	32.768-kHz crystal oscillation operating mode[Note 2]	V_{DD} = 5.0 V ±10%		60	120	μA
			V_{DD} = 3.0 V ±10%		32	64	μA
			V_{DD} = 2.0 V ±10%		24	48	μA
	I_{DD4}	32.768-kHz crystal oscillation HALT mode[Note 2]	V_{DD} = 5.0 V ±10%		25	55	μA
			V_{DD} = 3.0 V ±10%		5	15	μA
			V_{DD} = 2.0 V ±10%		2.5	12.5	μA
	I_{DD5}	XT1 = V_{DD} STOP mode When feedback resistor is used	V_{DD} = 5.0 V ±10%		1	30	μA
			V_{DD} = 3.0 V ±10%		0.5	10	μA
			V_{DD} = 2.0 V ±10%		0.3	10	μA
	I_{DD6}	XT1 = V_{DD} STOP mode When feedback resistor is not used	V_{DD} = 5.0 V ±10%		0.1	30	μA
			V_{DD} = 3.0 V ±10%		0.05	10	μA
			V_{DD} = 2.0 V ±10%		0.05	10	μA

Notes 1. Does not include the on-chip pull-up resistor, AV_{REF} current, and port current.

2. When the main system clock is stopped.

AC CHARACTERISTICS

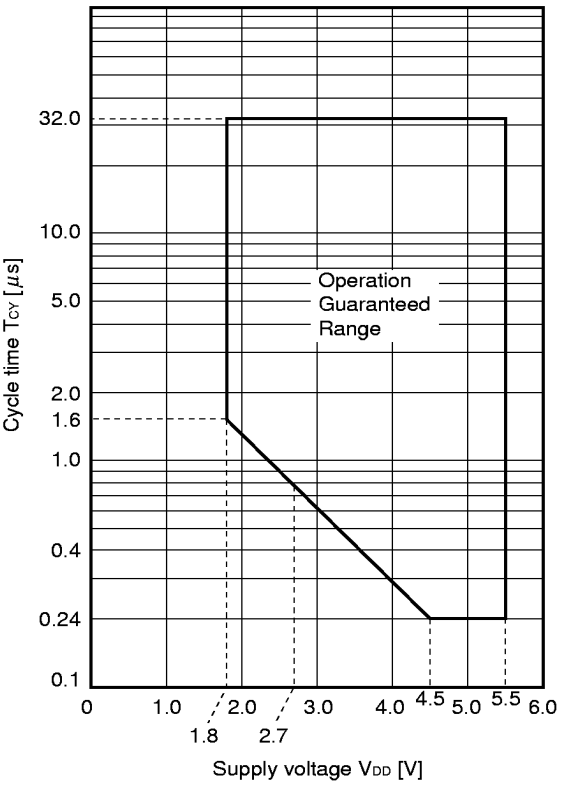
(1) Basic Operation (T_A = −40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Cycle time (Min. instruction execution time)	T_{CY}	Operating with main system clock	4.5 V ≤ V_{DD} ≤ 5.5 V	0.24		32	μs
			2.7 V ≤ V_{DD} < 4.5 V	0.8		32	μs
				1.6		32	μs
		Operating with subsystem clock		40 Note 1	122	125	μs
TI00, TI01 input high-/low-level width	t_{TIH0}, t_{TIL0}	3.5 V ≤ V_{DD} ≤ 5.5 V		$2/f_{sam}$+0.1 Note2			μs
		2.7 V ≤ V_{DD} < 3.5 V		$2/f_{sam}$+0.2 Note2			μs
		1.8 V ≤ V_{DD} < 2.7 V		$2/f_{sam}$+0.5 Note2			μs
TI50, TI51 input frequency	f_{TI5}	V_{DD} = 2.7 to 5.5 V		0		4	MHz
				0		275	kHz
TI50, TI51 input high-/low-level width	t_{TIH5}, t_{TIL5}	V_{DD} = 2.7 to 5.5 V		100			ns
				1.8			ns
Interrupt request input high-/low -level width	t_{INTH}, t_{INTL}	INTP0 to INTP3, P40 to P47	V_{DD} = 2.7 to 5.5 V	1			μs
				2			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}	V_{DD} = 2.7 to 5.5 V		10			μs
				20			μs

Notes 1. Value when using the external clock. When using a crystal resonator, the value becomes 114 μs (MIN:).

2. Selection of f_{sam} = fx, fx/4, fx/64 is possible with bits 0 and 1 (PRM00, PRM01) of prescaler mode register 0 (PRM0). However, if the TI00 valid edge is selected as the count clock, the value becomes f_{sam} = fx/8.

T_{CY} vs V_{DD} (at main system clock operation)



(2) Read/Write Operation (T_A = –40 to + 85°C, V_{DD} = 4.5 to 5.5 V) (1/3)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		$0.5t_{CY}$		ns
Address setup time	t_{ADS}		t_{CY}–40		ns
Address hold time	t_{ADH}		6		ns
Data input time from address	t_{ADD1}			$(2+2n)t_{CY}$–54	ns
	t_{ADD2}			$(3+2n)t_{CY}$–60	ns
Address output time from $\overline{RD}\downarrow$	t_{RDAD}		0	100	ns
Data input time from $\overline{RD}\downarrow$	t_{RDD1}			$(2+2n)t_{CY}$–87	ns
	t_{RDD2}			$(3+2n)t_{CY}$–93	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		$(1.5+2n)t_{CY}$–33		ns
	t_{RDL2}		$(2.5+2n)t_{CY}$–33		ns
$\overline{WAIT}\downarrow$ input time from $\overline{RD}\downarrow$	t_{RDWT1}			$0.5t_{CY}$–43	ns
	t_{RDWT2}			t_{CY}–43	ns
$\overline{WAIT}\downarrow$ input time from $\overline{WR}\downarrow$	t_{WRWT}			$0.5t_{CY}$–25	ns
$\overline{WAIT}$ low-level width	t_{WTL}		$(0.5+2n)t_{CY}$+10	$(2+2n)t_{CY}$	ns
Write data setup time	t_{WDS}		60		ns
Write data hold time	t_{WDH}		6		ns
$\overline{WR}$ low-level width	t_{WRL1}		$(1.5+2n)t_{CY}$–15		ns
$\overline{RD}\downarrow$ delay time from ASTB↓	t_{ASTRD}		6		ns
$\overline{WR}\downarrow$ delay time from ASTB↓	t_{ASTWR}		$2t_{CY}$–15		ns
ASTB↑ delay time from $\overline{RD}\uparrow$ in external fetch	t_{RDAST}		$0.8t_{CY}$–10	$1.2t_{CY}$	ns
Address hold time from $\overline{RD}\uparrow$ in external fetch	t_{RDADH}		$0.8t_{CY}$–15	$1.2t_{CY}$+30	ns
Write data output time from $\overline{RD}\uparrow$	t_{RDWD}		40		ns
Write data output time from $\overline{WR}\downarrow$	t_{WRWD}		10	60	ns
Address hold time from $\overline{WR}\uparrow$	t_{WRADH}		$0.8t_{CY}$–15	$1.2t_{CY}$+30	ns
$\overline{RD}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t_{WTRD}		$0.8t_{CY}$	$2.5t_{CY}$+25	ns
$\overline{WR}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t_{WTWR}		$0.8t_{CY}$	$2.5t_{CY}$+25	ns

Remarks **1.** $t_{CY} = T_{CY}/4$

2. n indicates the number of waits.

(2) Read/Write Operation (T_A = –40 to + 85°C, V_{DD} = 2.7 to 4.5 V) (2/3)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		$0.5t_{CY}$		ns
Address setup time	t_{ADS}		$0.5t_{CY}$–54		ns
Address hold time	t_{ADH}		10		ns
Data input time from address	t_{ADD1}			$(2+2n)t_{CY}$–108	ns
	t_{ADD2}			$(3+2n)t_{CY}$–120	ns
Address output time from $\overline{RD}\downarrow$	t_{RDAD}		0	200	ns
Data input time from $\overline{RD}\downarrow$	t_{RDD1}			$(2+2n)t_{CY}$–148	ns
	t_{RDD2}			$(3+2n)t_{CY}$–162	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		$(1.5+2n)t_{CY}$–40		ns
	t_{RDL2}		$(2.5+2n)t_{CY}$–40		ns
$\overline{WAIT}\downarrow$ input time from $\overline{RD}\downarrow$	t_{RDWT1}			$0.5t_{CY}$–60	ns
	t_{RDWT2}			t_{CY}–60	ns
$\overline{WAIT}\downarrow$ input time from $\overline{WR}\downarrow$	t_{WRWT}			$0.5t_{CY}$–50	ns
$\overline{WAIT}$ low-level width	t_{WTL}		$(0.5+2n)t_{CY}$+10	$(2+2n)t_{CY}$	ns
Write data setup time	t_{WDS}		60		ns
Write data hold time	t_{WDH}		10		ns
$\overline{WR}$ low-level width	t_{WRL1}		$(1.5+2n)t_{CY}$–30		ns
$\overline{RD}\downarrow$ delay time from ASTB↓	t_{ASTRD}		10		ns
$\overline{WR}\downarrow$ delay time from ASTB↓	t_{ASTWR}		$2t_{CY}$–30		ns
ASTB↑ delay time from $\overline{RD}\uparrow$ in external fetch	t_{RDAST}		$0.8t_{CY}$–30	$1.2t_{CY}$	ns
Address hold time from $\overline{RD}\uparrow$ in external fetch	t_{RDADH}		$0.8t_{CY}$–30	$1.2t_{CY}$+60	ns
Write data output time from $\overline{RD}\uparrow$	t_{RDWD}		40		ns
Write data output time from $\overline{WR}\downarrow$	t_{WRWD}		20	120	ns
Address hold time from $\overline{WR}\uparrow$	t_{WRADH}		$0.8t_{CY}$–30	$1.2t_{CY}$+60	ns
$\overline{RD}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t_{WTRD}		$0.5t_{CY}$	$2.5t_{CY}$+50	ns
$\overline{WR}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t_{WTWR}		$0.5t_{CY}$	$2.5t_{CY}$+50	ns

Remarks **1.** $t_{CY} = T_{CY}/4$

2. n indicates the number of waits.

(2) Read/Write Operation (T_A = –40 to + 85°C, V_{DD} = 1.8 to 2.7 V) (3/3)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		$0.5t_{CY}$		ns
Address setup time	t_{ADS}		$0.5t_{CY}$–60		ns
Address hold time	t_{ADH}		20		ns
Data input time from address	t_{ADD1}			$(2+2n)t_{CY}$–233	ns
	t_{ADD2}			$(3+2n)t_{CY}$–240	ns
Address output time from $\overline{RD}\downarrow$	t_{RDAD}		0	400	ns
Data input time from $\overline{RD}\downarrow$	t_{RDD1}			$(2+2n)t_{CY}$–325	ns
	t_{RDD2}			$(3+2n)t_{CY}$–332	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		$(1.5+2n)t_{CY}$–92		ns
	t_{RDL2}		$(2.5+2n)t_{CY}$–92		ns
$\overline{WAIT}\downarrow$ input time from $\overline{RD}\downarrow$	t_{RDWT1}			$0.5t_{CY}$–132	ns
	t_{RDWT2}			t_{CY}–132	ns
$\overline{WAIT}\downarrow$ input time from $\overline{WR}\downarrow$	t_{WRWT}			$0.5t_{CY}$–100	ns
$\overline{WAIT}$ low-level width	t_{WTL}		$(0.5+2n)t_{CY}$+10	$(2+2n)t_{CY}$	ns
Write data setup time	t_{WDS}		60		ns
Write data hold time	t_{WDH}		20		ns
$\overline{WR}$ low-level width	t_{WRL1}		$(1.5+2n)t_{CY}$–60		ns
$\overline{RD}\downarrow$ delay time from ASTB$\downarrow$	t_{ASTRD}		20		ns
$\overline{WR}\downarrow$ delay time from ASTB$\downarrow$	t_{ASTWR}		$2t_{CY}$–60		ns
ASTB$\uparrow$ delay time from $\overline{RD}\uparrow$ in external fetch	t_{RDAST}		$0.8t_{CY}$–60	$1.2t_{CY}$	ns
Address hold time from $\overline{RD}\uparrow$ in external fetch	t_{RDADH}		$0.8t_{CY}$–60	$1.2t_{CY}$+120	ns
Write data output time from $\overline{RD}\uparrow$	t_{RDWD}		40		ns
Write data output time from $\overline{WR}\downarrow$	t_{WRWD}		40	240	ns
Address hold time from $\overline{WR}\uparrow$	t_{WRADH}		$0.8t_{CY}$–60	$1.2t_{CY}$+120	ns
$\overline{RD}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t_{WTRD}		$0.5t_{CY}$	$2.5t_{CY}$+100	ns
$\overline{WR}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t_{WTWR}		$0.5t_{CY}$	$2.5t_{CY}$+100	ns

Remarks 1. $t_{CY} = T_{CY}/4$

2. n indicates the number of waits.

(3) Serial Interface (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

(a) 3-wire serial I/O mode ($\overline{SCK30}$, $\overline{SCK31}$... Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK30}$, $\overline{SCK31}$ cycle time	t_{KCY1}	4.5 V ≤ V_{DD} ≤ 5.5 V	954			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
$\overline{SCK30}$, $\overline{SCK31}$ high-/low-level width	t_{KH1}, t_{KL1}	V_{DD} = 4.5 to 5.5 V	t_{KCY1}/2–50			ns
			t_{KCY1}/2–100			ns
SI30, SI31 setup time (to $\overline{SCK30}$, $\overline{SCK31}$↑)	t_{SIK1}	4.5 V ≤ V_{DD} ≤ 5.5V	100			ns
		2.7 V ≤ V_{DD} < 4.5V	150			ns
			300			ns
SI30, SI31 hold time (from $\overline{SCK30}$, $\overline{SCK31}$↑)	t_{KSI1}		400			ns
SO30, SO31 output dealy time from $\overline{SCK30}$, $\overline{SCK31}$↓	t_{KSO1}	C = 100 pF[Note]			300	ns

Note C is the load capacitance of the $\overline{SCK30}$, $\overline{SCK31}$, SO30, and SO31 output lines.

(b) 3-wire serial I/O mode ($\overline{SCK30}$, $\overline{SCK31}$... External clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK30}$, $\overline{SCK31}$ cycle time	t_{KCY2}	4.5 V ≤ V_{DD} ≤ 5.5 V		800			ns
		2.7 V ≤ V_{DD} < 4.5 V		1600			ns
				3200			ns
$\overline{SCK30}$, $\overline{SCK31}$ high-/low-level width	t_{KH2}, t_{KL2}	4.5 V ≤ V_{DD} ≤ 5.5 V		400			ns
		2.7 V ≤ V_{DD} < 4.5 V		800			ns
				1600			ns
SI30, SI31 setup time (to $\overline{SCK30}$, $\overline{SCK31}$↑)	t_{SIK2}			100			ns
SI30, SI31 hold time (from $\overline{SCK30}$, $\overline{SCK31}$↑)	t_{KSI2}			400			ns
SO30, SO31 output dealy time from $\overline{SCK30}$, $\overline{SCK31}$↓	t_{KSO2}	C = 100 pF[Note]				300	ns
$\overline{SCK30}$, $\overline{SCK31}$ rise, fall time	t_{R2}, t_{F2}	When using external device expansion function				160	ns
		When not using external device expansion function	When using 16-bit timer expansion function			700	ns
			When not using 16-bit timer expansion function			1000	ns

Note C is the load capacitance of the SO30 and SO31 output lines.

(c) UART mode (Dedicated baud rate generator output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		4.5 V ≤ V_{DD} ≤ 5.5 V			125000	bps
		2.7 V ≤ V_{DD} < 4.5 V			78125	bps
					39063	bps

(d) UART mode (External clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
ASCK0 cycle time	t_{KCY3}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
ASCK0 high-/low-level width	t_{KH3}, t_{KL3}	4.5 V ≤ V_{DD} ≤ 5.5 V	400			ns
		2.7 V ≤ V_{DD} < 4.5 V	800			ns
			1600			ns
Transfer rate		4.5 V ≤ V_{DD} ≤ 5.5 V			39063	bps
		2.7 V ≤ V_{DD} < 4.5 V			19531	bps
					9766	bps
ASCK0 rise, fall time	t_{R3}, t_{F3}	V_{DD} = 4.5 to 5.5 V, when not using external device expansion function			1000	ns
					160	ns

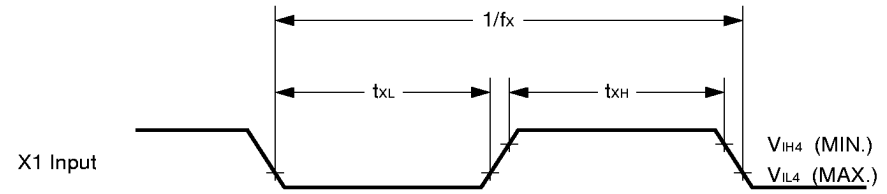
(e) UART mode (Infrared ray data transfer mode)

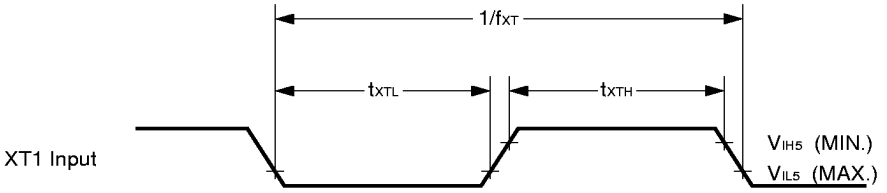
Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
Transfer rate		V_{DD} = 4.5 to 5.5 V		115200	bps
Bit rate allowable error		V_{DD} = 4.5 to 5.5 V		±0.87	%
Output pulse width		V_{DD} = 4.5 to 5.5 V	1.2	0.24/fbr[Note]	μs
Input pulse width		V_{DD} = 4.5 to 5.5 V	4/f_X		μs

Note fbr: Specified baud rate

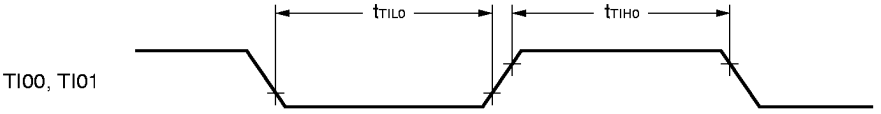
AC Timing Test Point (Excluding X1, XT1 Input)

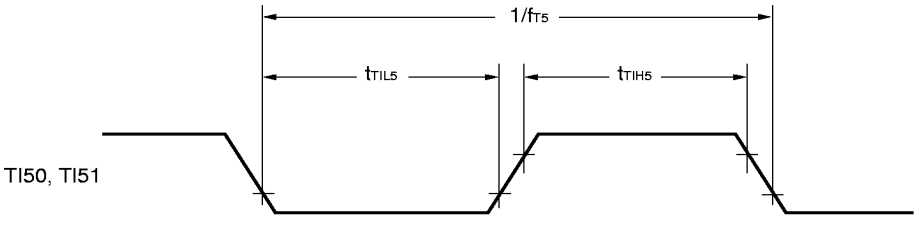
Clock Timing





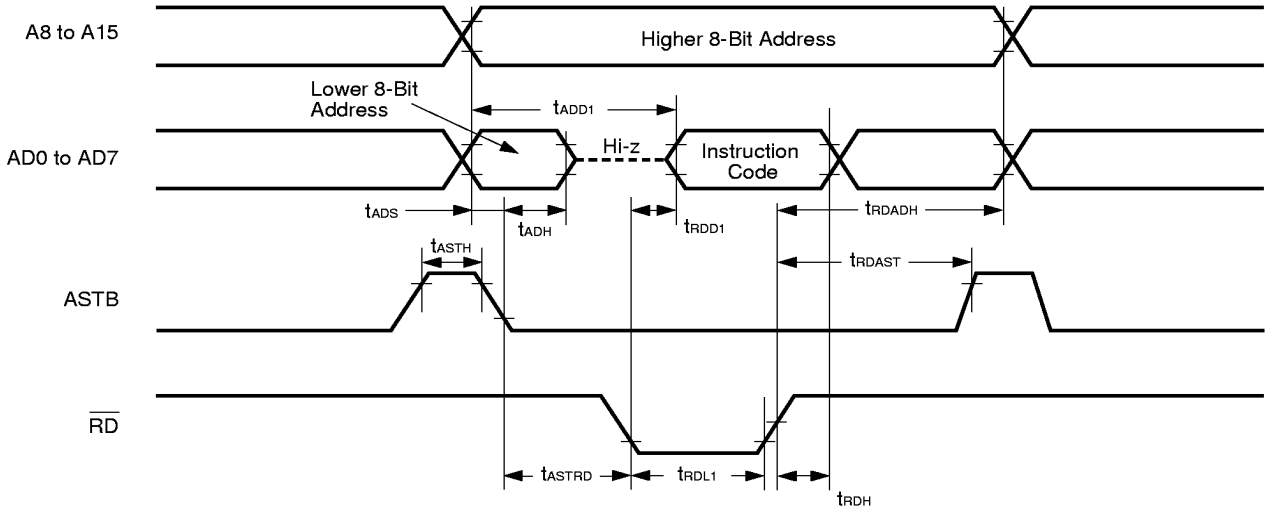
TI Timing



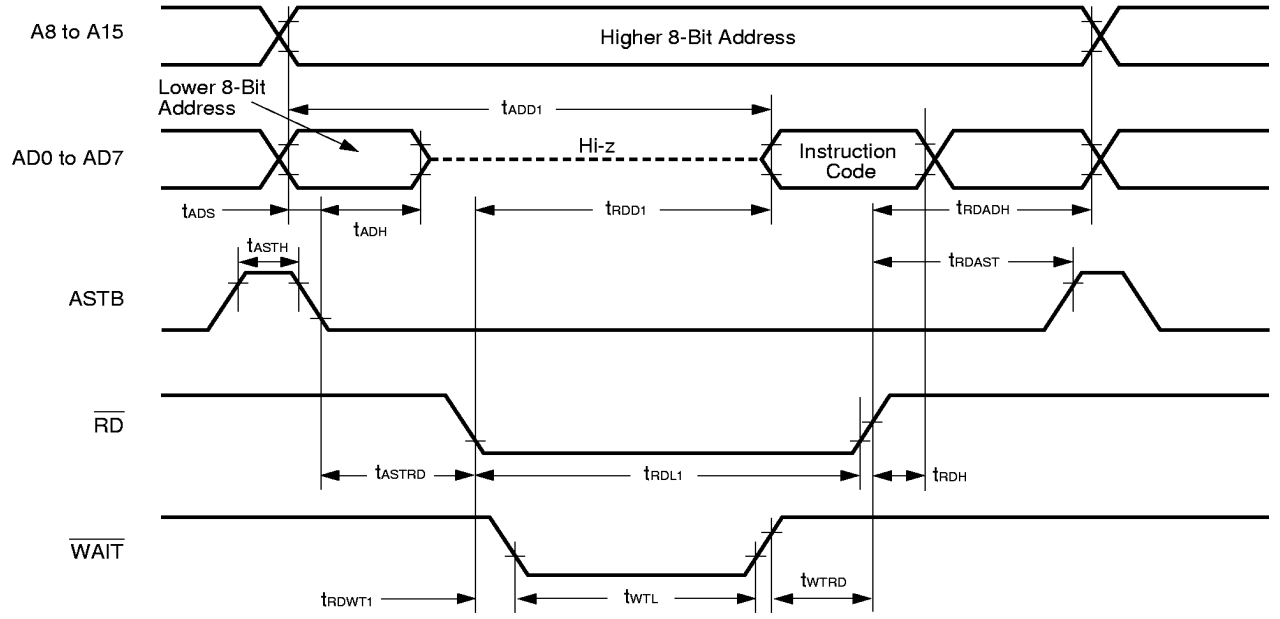


Read/Write Operation

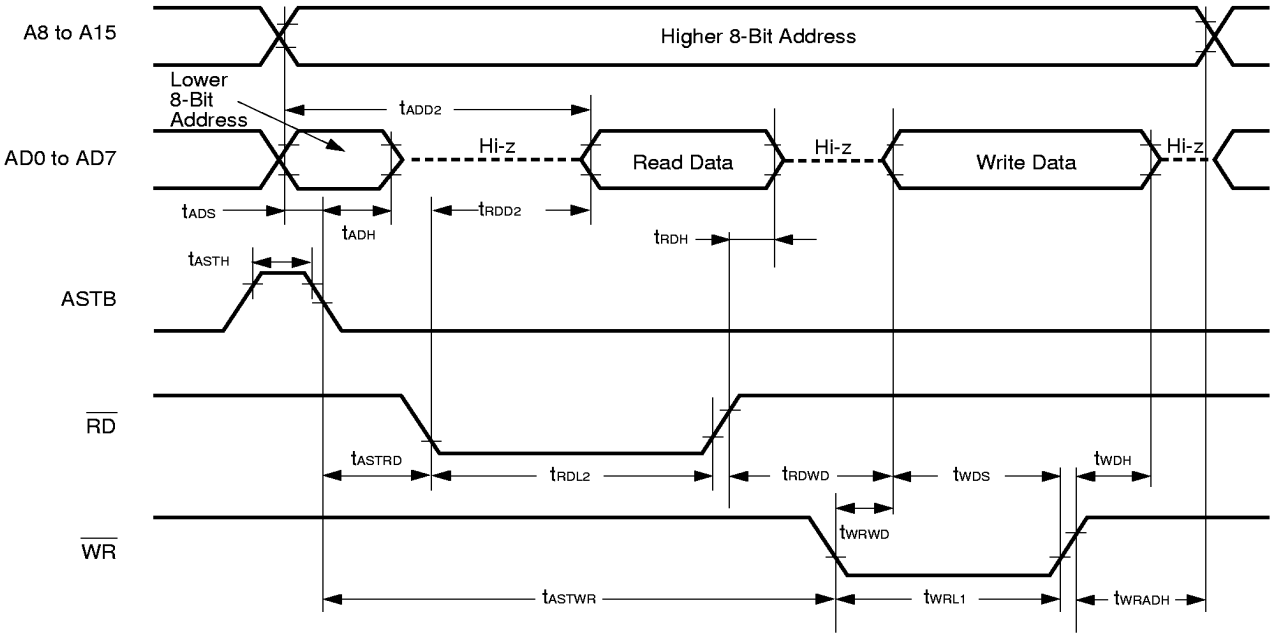
External Fetch (No Wait) :



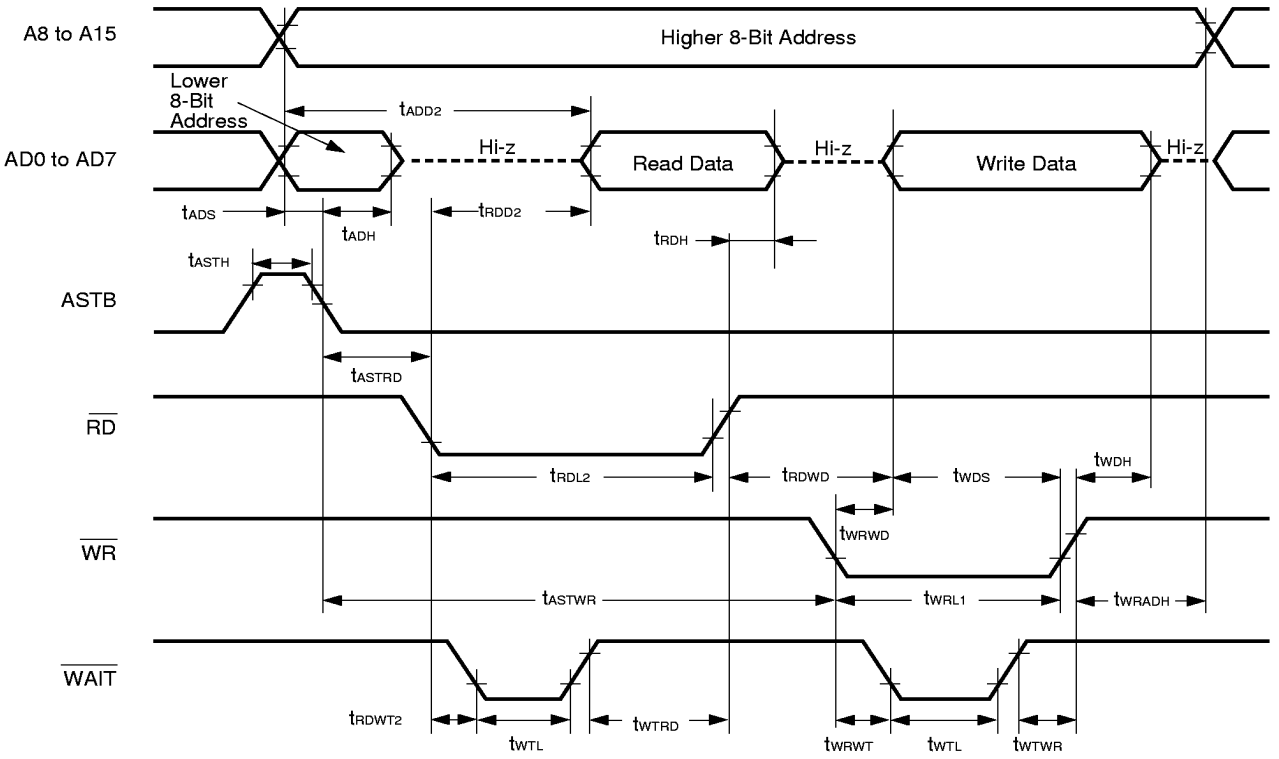
External Fetch (Wait Insertion) :



External Data Access (No Wait) :

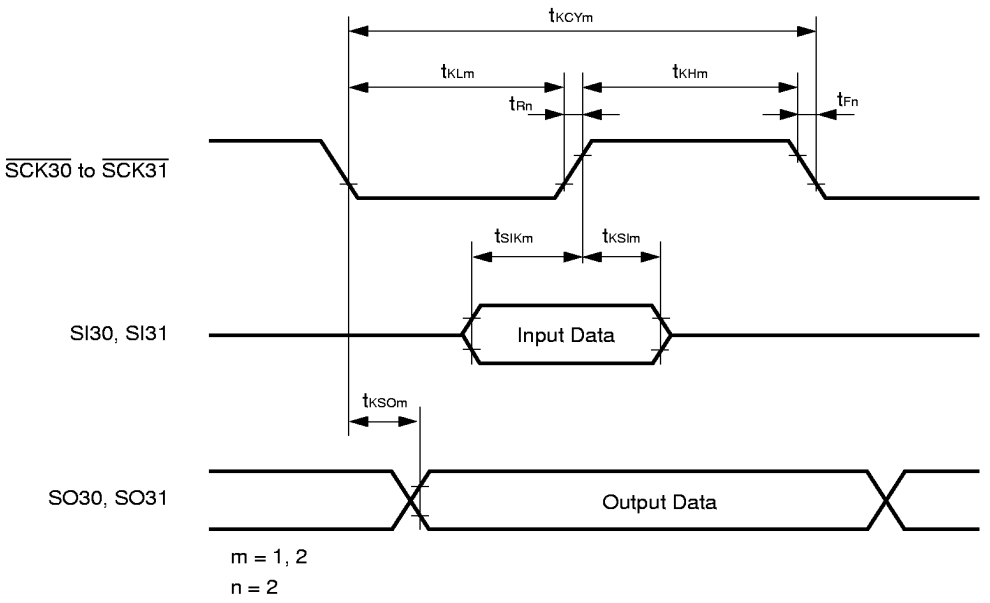


External Data Access (Wait Insertion) :

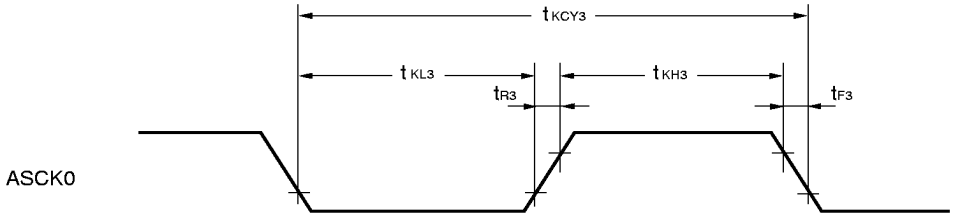


Serial Transfer Timing

3-wire Serial I/O Mode :



UART Mode (External Clock Input) :



A/D Converter Characteristics (T_A = –40 to +85°C, V_{DD} = AV_{DD} = AV_{REF} = 2.7 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Overall error[Note]					±0.6	%
Conversion time	t_{CONV}		14		200	μs
Analog input voltage	V_{IAN}		0		AV_{REF} + 0.3	V
Reference voltage	AV_{REF}		2.7		AV_{DD}	V
AV_{REF} resistance	R_{AIREF}		10	20		kΩ

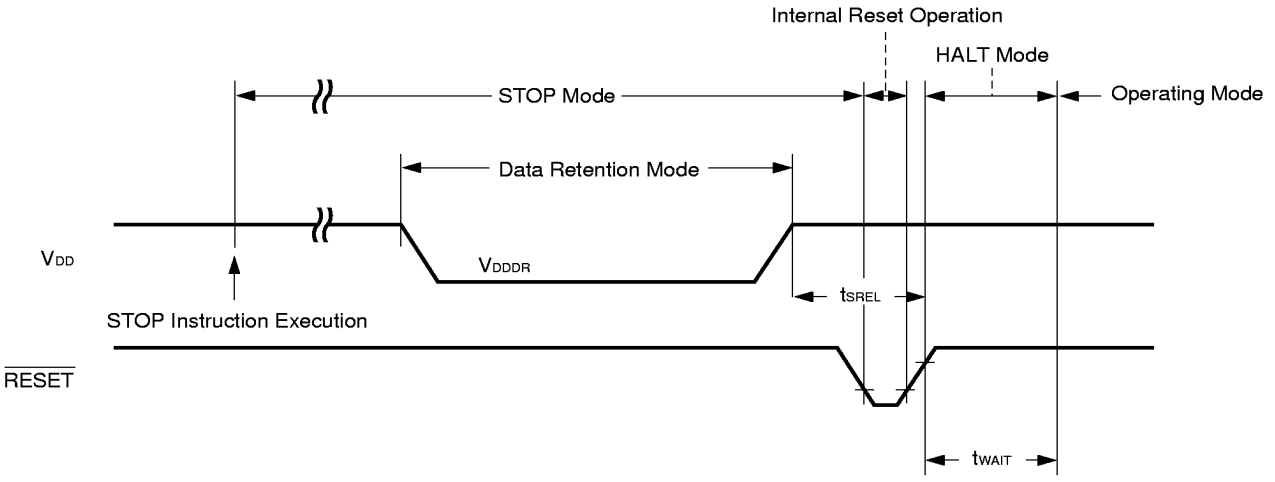
Note Overall error excluding quantization error (±1/2 LSB). It is indicated as a ratio to the full-scale value.

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

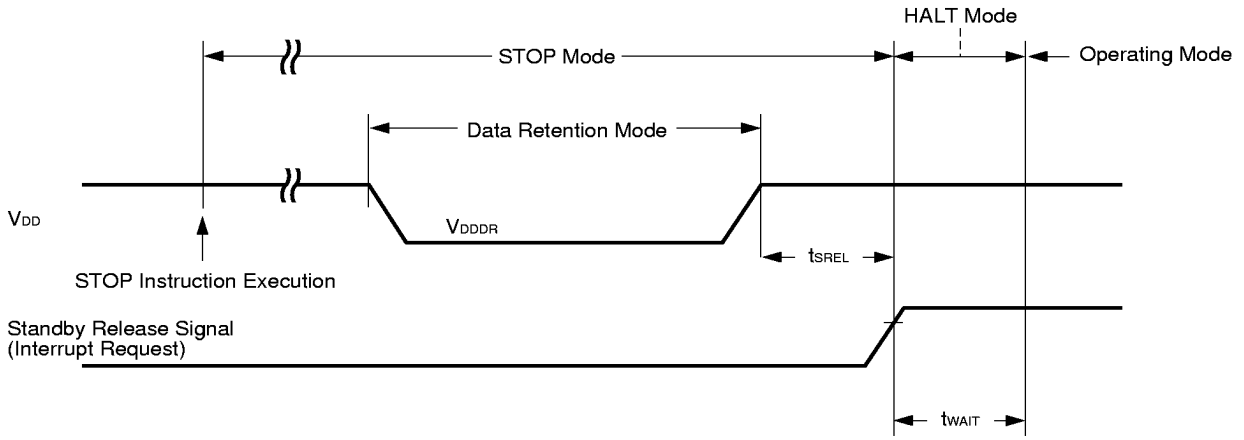
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V_{DDDR}		1.6		5.5	V
Data retention power supply current	I_{DDDR}	V_{DDDR} = 1.6 V Subsystem clock stop and feed-back resistor disconnected		0.1	10	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{RESET}$		2^{17}/fx		ms
		Release by interrupt request		**Note**		ms

Note Selection of 2^{12}/fx and 2^{14}/fx to 2^{17}/fx is possible with bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time select register (OSTS).

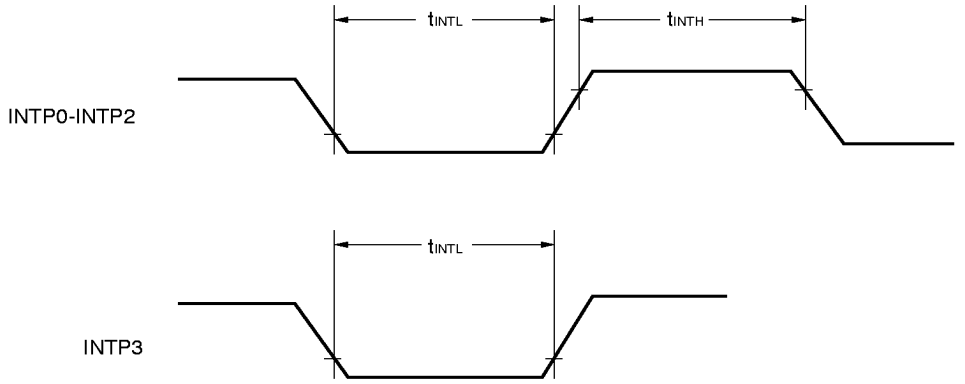
Data Retention Timing (STOP Mode Release by $\overline{RESET}$)



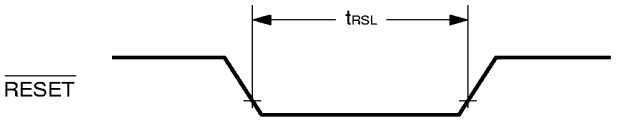
Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Request Signal)



Interrupt Request Input Timing

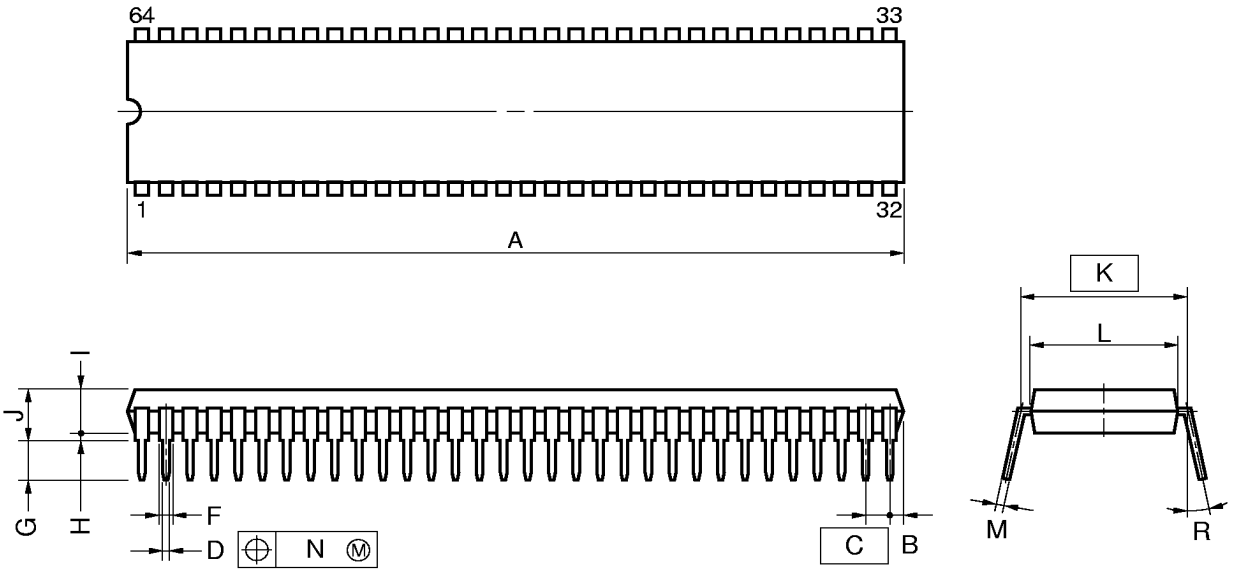


$\overline{\text{RESET}}$ Input Timing



12. PACKAGE DRAWINGS

64-PIN PLASTIC SHRINK DIP (750 mils)



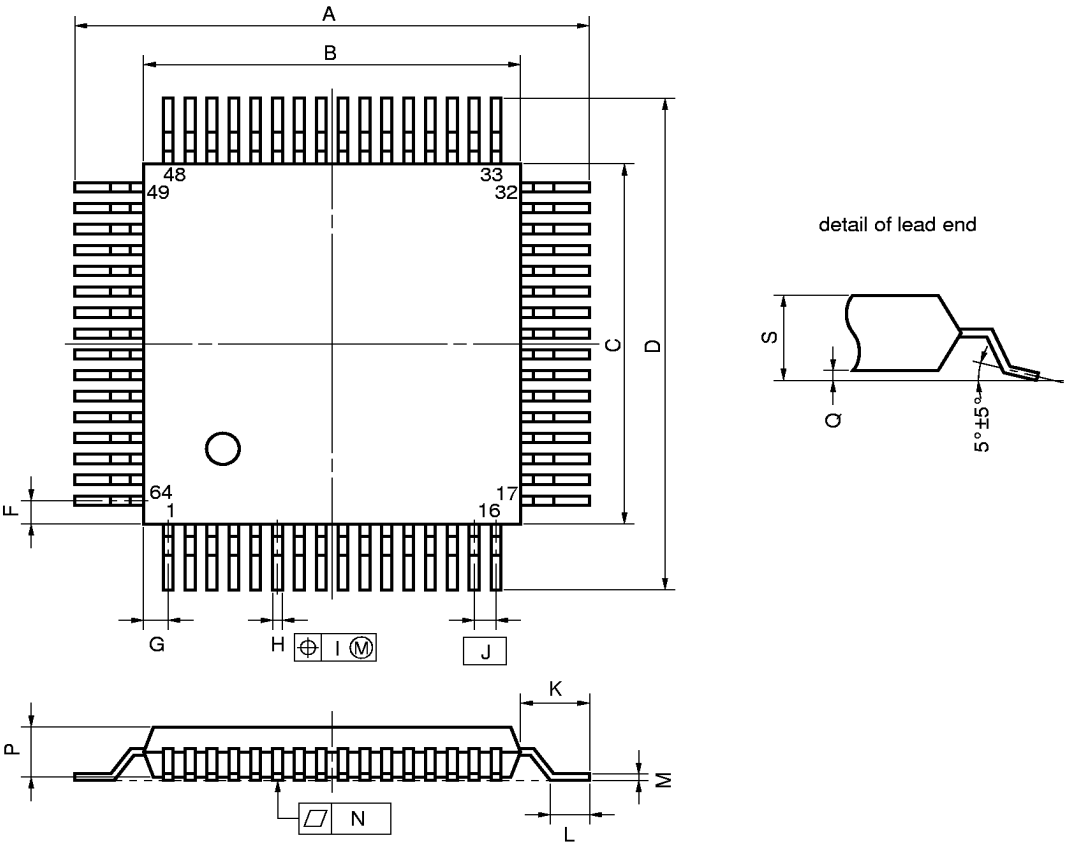
NOTE

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.
2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	58.68 MAX.	2.311 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50 ± 0.10	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	3.2±0.3	0.126±0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	17.0	0.669
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007
R	0~15°	0~15°

P64C-70-750A,C-1

64-PIN PLASTIC QFP (□14)



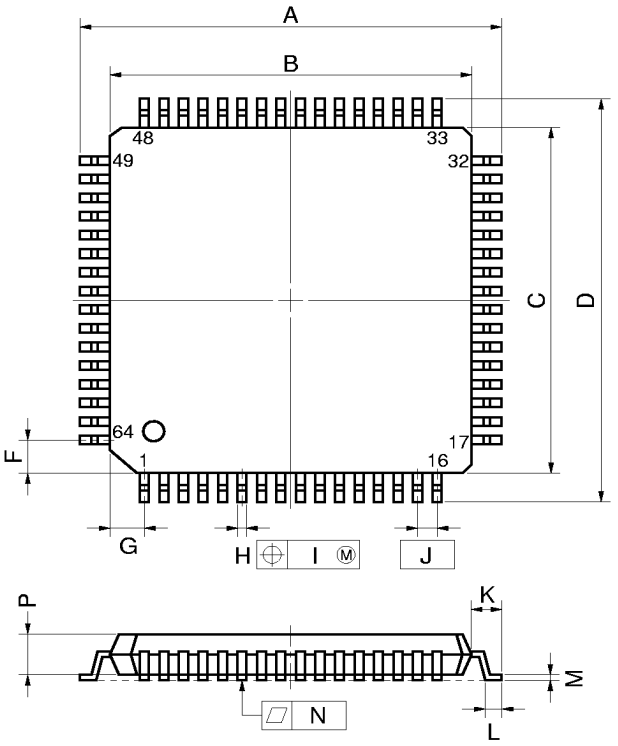
P64GC-80-AB8-3

NOTE

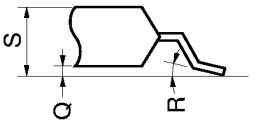
Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.6±0.4	0.693±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	0.35±0.10	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	0.071±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.55	0.100
Q	0.1±0.1	0.004±0.004
S	2.85 MAX.	0.112 MAX.

64-PIN PLASTIC LQFP (□12)



detail of lead end



NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	14.8±0.4	0.583±0.016
B	12.0±0.2	$0.472^{+0.009}_{-0.008}$
C	12.0±0.2	$0.472^{+0.009}_{-0.008}$
D	14.8±0.4	0.583±0.016
F	1.125	0.044
G	1.125	0.044
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.4±0.2	0.055±0.008
L	0.6±0.2	$0.024^{+0.008}_{-0.009}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	1.4	0.055
Q	0.125±0.075	0.005±0.003
R	5°±5°	5°±5°
S	1.7 MAX.	0.067 MAX.

P64GK-65-8A8-1

★ APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD780024 Subseries.
Also refer to **(5) Cautions on using development tools.**

(1) Language Processing Software

RA78K/0	Assembler package common to 78K/0 Series
CC78K/0	C compiler package common to 78K/0 Series
DF780024	Device file for μPD780024 Subseries
CC78K/0-L	C compiler library source file common to 78K/0 Series

(2) Flash Memory Writing Tools

Flashpro II (FL-PR2)	Flash programmer dedicated on-chip flash memory microcontroller. A product of Naitou Densei Machidaseisakusho Co., Ltd.
FA-64CW FA-64GC FA-64GK[Note]	Adapter for flash memory writing A product of Naitou Densei Machidaseisakusho Co., Ltd.

Note Under development

(3) Debugging Tool

- **When using in-circuit emulator IE-78K0-NS**

IE-78K0-NS[Note]	In-circuit emulator common to 78K/0 Series
IE-70000-MS-PS-B	Power supply unit for IE-78K0-NS
IE-70000-98-IF-C[Note]	Interface adapter when using PC-9800 series as host machine (excluding notebook PCs)
IE-70000-CD-IF[Note]	PC card and interface cable when using notebook PC of PC-9800 series as host machine
IE-70000-PC-IF-C[Note]	Interface adapter when using IBM PC/AT™ or compatible as host machine
IE-780034-NS-EM1[Note]	Emulation board to emulate μPD780024 Subseries
NP-64CW	Emulation probe for 64-pin plastic shrink DIP (CW type)
NP-64GC	Emulation probe for 64-pin plastic QFP (GC-AB8 type)
NP-64GK[Note]	Emulation probe for 64-pin plastic LQFP (GC-8A8 type)
TGK-064SBW	Conversion adapter for connecting target system board designed to mount a 64-pin plastic LQFP (GK-8A8 type) and NP-64GK.
EV-9200GC-64	Socket to be mounted on target system board manufactured for 64-pin plastic QFP (GC-AB8 type)
ID78K0-NS[Note]	Integrated debugger for IE-78K0-NS
SM78K0	System simulator common to 78K/0 Series
DF780024	Device file for μPD780024 Subseries

Note Under development

• **When using in-circuit emulator IE-78001-R-A**

IE-78001-R-A[Note]	In-circuit emulator common to 78K/0 Series
IE-70000-98-IF-B IE-70000-98-IF-C[Note]	Interface adapter when using PC-9800 series as host machine (excluding notebook PCs)
IE-70000-PC-IF-B IE-70000-PC-IF-C[Note]	Interface adapter when using IBM PC/AT or compatible as host machine
IE-78000-R-SV3	Interface adapter and cable when using EWS as host machine
IE-780034-NS-EM1[Note]	Emulation board to emulate μPD780024 Subseries
IE-78K0-R-EX1[Note]	Emulation probe conversion board to use IE-780034-NS-EM1 on IE-78001-R-A
EP-78240CW-R	Emulation probe for 64-pin plastic shrink DIP (CW type)
EP-78240GC-R	Emulation probe for 64-pin plastic QFP (GC-AB8 type)
EP-78012GK-R	Emulation probe for 64-pin plastic LQFP (GK-8A8 type)
TGK-064SBW	Conversion adapter for connecting target system board designed to mount a 64-pin plastic LQFP (GK-8A8) and NP-64GK.
EV-9200GC-64	Socket to be mounted on target system board manufactured for 64-pin plastic QFP (GC-AB8 type)
ID78K0	Integrated debugger for IE-78001-R-A
SM78K0	System simulator common to 78K/0 Series
DF780024	Device file for μPD780024 Subseries

Note Under development

(4) Real-time OS

RX78K/0	Real-time OS for 78K/0 Series
MX78K0	OS for 78K/0 Series

(5) Cautions on using development tools

- The ID-78K0-NS, ID78K0, and SM78K0 are used in combinaiton with the DF780024.
- The CC78K/0 and RX78K/0 are used in combination with the RA78K/0 and the DF780024.
- The Flashpro II, FA-64CW, FA-64GC, FA64GK, NP-64CW, NP64GC, and NP-64GK are products made by Naitou Densei Machidaseisakusho (044-822-3813).
  Contact an NEC dealer regarding the purchase of these products.
- The TGK-064SBW is a product made by TOKYO ELETECH CORPORATION.
  Refer to: Daimaru Kogyo, Ltd.
  Tokyo Electronic Components Division (03-3820-7112)
  Osaka Electronic Components Division (06-244-6672)
- For third party development tools, see the **78K/0 Series Selection Guide (U11126E)**.
- The host machines and OSs supporting each software are as follows.

Host Machine / [OS] / Software	PC PC-9800 series [Windows™] IBM PC/AT or compatible [Japanese/English Windows]	EWS HP9000 series 700™ [HP-UX™] SPARCstation™ [SunOS™] NEWS™ (RISC) [NEWS-OS™]
RA78K/0	√ **Note**	√
CC78K/0	√ **Note**	√
ID78K0-NS	√	–
ID78K0	√	√
SM78K0	√	–
RX78K/0	√ **Note**	√
MX78K0	√ **Note**	√

Note DOS-based software

★ APPENDIX B. RELATED DOCUMENTS

Device Related Documents

Document Name	Document No. (English)	Document No. (Japanese)
μPD780024, 780024Y, 780034, 780034Y Subseries User's Manual	U12022E	U12022J
μPD780021, 780022, 780023, 780024 Data Sheet	This document	U12299J
μPD78F0034 Preliminary Product Information	U11993E	U11993J
78K/0 Series User's Manual-Instructions	U12326E	U12326J
78K/0 Series Instruction Table	—	U10903J
78K/0 Series Instruction Set	—	U10904J
μPD780034 Subseries Special Function Register Table	—	To be prepared

Development Tool Documents (User's Manual)

Document Name		Document No. (English)	Document No. (Japanese)
RA78K Series Assembler Package	Operation	EEU-1399	EEU-809
	Language	EEU-1404	EEU-815
RA78K Series Structured Assembler Preprocessor		EEU-1402	U12323J
RA78K0 Assembler Package	Operation	U11802E	U11802J
	Assembly Language	U11801E	U11801J
	Structured Assembly Language	U11789E	U11789J
CC78K Series C Compiler	Operation	EEU-1280	EEU-656
	Language	EEU-1284	EEU-655
CC78K/0 C Compiler	Operation	U11517E	U11517J
	Language	U11518E	U11518J
CC78K/0 C Compiler Application Note	Programming Know-how	EEA-1208	EEU-618
CC78K Series Library Source File		—	U12322J
IE-78K0-NS		To be prepared	To be prepared
IE-78001-R-A		To be prepared	To be prepared
IE-780034-NS-EM1		To be prepared	To be prepared
EP-78240		U10332E	EEU-986
EP-78012GK-R		EEU-1538	EEU-5012
SM78K0 System Simulator-Windows based	Reference	U10181E	U10181J
SM78K Series System Simulator	External Part User Open Interface Specifications	U10092E	U10092J
ID78K0-NS Integrated Debugger	Reference	To be prepared	Under preparation
ID78K0 Integrated Debugger, EWS based	Reference	—	U11151J
ID78K0 Integrated Debugger, PC based	Reference	U11539E	U11539J
ID78K0 Integrated Debugger, Windows based	Guide	U11649E	U11649J

Caution The above related documents are subject to change without notice. Be sure to read the latest documents before designing.

Embedded Software Documents (User's Manual)

Document Name		Document No. (English)	Document No. (Japanese)
78K/0 Series Real-time OS	Basics	U11537E	U11537J
	Installation	U11536E	U11536J
78K/0 Series OS MX78K0	Basics	U12257E	U12257J

Other Documents

Document Name	Document No. (English)	Document No. (Japanese)
IC Package Manual	C10943X	
Semiconductor Device Mounting Technology Manual	C10535E	C10535J
Quality Grades on NEC Semiconductor Devices	C11531E	C11531J
NEC Semiconductor Device Reliability/Quality Control System	C10983E	C10983J
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E	C11892J
Guide to Quality Assurance for Semiconductor Devices	MEI-1202	—
Microcomputer Product Series Guide	—	U11416J

Caution The above related documents are subject to change without notice. Be sure to read the latest documents before designing.