

CD4527B Types

CMOS BCD Rate Multiplier

High-Voltage Types (20-Volt Rating)

■ CD4527B is a low-power 4-bit digital rate multiplier that provides an output-pulse rate which is the clock-input-pulse rate multiplied by 1/10 times the BCD input. For example, when the BCD input is 8, there will be 8 output pulses for every 10 input pulses. This device may be used to perform arithmetic operations (add, subtract, divide, raise to a power), solve algebraic and differential equations, generate natural logarithms and trigonometric functions, A/D and D/A conversion, and frequency division.

For fractional multipliers with more than one digit, CD4527B devices may be cascaded in two different modes: the Add mode and the Multiply mode. (See Figs.12 and 15). In the Add mode,

$$\text{Output Rate} = \left[\frac{0.1 \text{ BCD}_1 + 0.01 \text{ BCD}_2 + 0.001 \text{ BCD}_3 + \dots}{\text{Clock Rate}} \right]$$

In the Multiply mode, the fraction programmed into the first rate multiplier is multiplied by the fraction programmed into the second one,

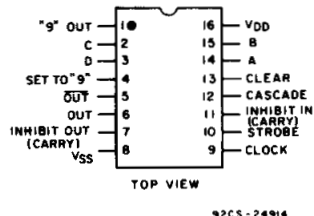
$$\text{e.g. } \frac{9}{10} \times \frac{4}{10} = \frac{36}{100} \text{ or 36 output}$$

pulses for every 100 clock input pulses.

The CD4527B types are supplied in 16-lead ceramic dual-in-line packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline package (NSR suffix), and in chip form (H suffix).

Applications:

- Numerical control
- Instrumentation
- Digital filtering
- Frequency synthesis



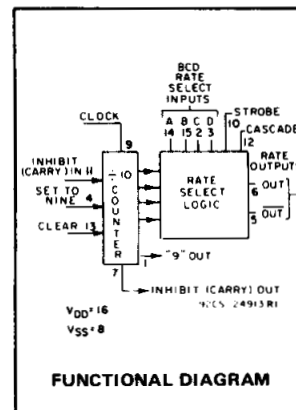
TERMINAL ASSIGNMENT

Features:

- Cascadable in multiples of 4-bits
- Set to "9" input and "9" detect output
- 100% test for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Standardized, symmetrical output characteristics
- Maximum input current of 1 μ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) =

$$\begin{aligned} 1 \text{ V at } V_{DD} &= 5 \text{ V} \\ 2 \text{ V at } V_{DD} &= 10 \text{ V} \\ 2.5 \text{ V at } V_{DD} &= 15 \text{ V} \end{aligned}$$

- Meets all requirements of JEDEC Tentative Standard No. 13B, 'Standard Specifications for Description of 'B' Series CMOS Devices'



MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

Voltages referenced to V_{SS} Terminal) -0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS -0.5V to V_{DD} +0.5V

DC INPUT CURRENT, ANY ONE INPUT ± 10 mA

POWER DISSIPATION PER PACKAGE (P_D):

For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$ 500mW

For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$ Derate Linearly at 12mW/ $^\circ\text{C}$ to 200mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$ 100mW

OPERATING-TEMPERATURE RANGE (T_A) -55°C to $+125^\circ\text{C}$

STORAGE TEMPERATURE RANGE (T_{stg}) -65°C to $+150^\circ\text{C}$

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 $\pm$ 1/32 inch (1.59 $\pm$ 0.79mm) from case for 10s max $+265^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS AT $T_A = 25^\circ\text{C}$, Except as Noted.

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS		UNITS
		Min.	Max.	
Supply Voltage Range (For $T_A = \text{Full Package-Temperature Range}$)		3	18	V
Set or Clear Pulse Width, t_W	5	160	—	ns
	10	90	—	
	15	60	—	
Clock Pulse Width, t_W	5	330	—	ns
	10	170	—	
	15	100	—	
Clock Frequency, f_{CL}	5	—	1.2	MHz
	10	dc	2.5	
	15	—	3.5	
Clock Rise or Fall Time, t_{rCL} or t_{fCL}	5, 10, 15	—	15	μ s
Inhibit In Setup Time, t_{SU}	5	100	—	ns
	10	40	—	
	15	20	—	
Inhibit In Removal Time, t_{REM}	5	240	—	ns
	10	130	—	
	15	110	—	
Set Removal Time, t_{REM}	5	150	—	ns
	10	80	—	
	15	50	—	
Clear Removal Time, t_{REM}	5	60	—	ns
	10	40	—	
	15	30	—	

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STATIC ELECTRICAL CHARACTERISTICS

CHARACTER- ISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)					+25			
				-55	-40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I _{DD} Max.	—	0,5	5	5	5	150	150	—	0.04	5	μA
	—	0,10	10	10	10	300	300	—	0.04	10	
	—	0,15	15	20	20	600	600	—	0.04	20	
	—	0,20	20	100	100	3000	3000	—	0.08	100	
Output Low (Sink) Current I _{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current, I _{OH} Min.	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	—	mA
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	—	
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—	
	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	—	
Output Voltage: Low-Level, V _{OL} Max.	—	0,5	5	0.05				—	0	0.05	V
	—	0,10	10	0.05				—	0	0.05	
	—	0,15	15	0.05				—	0	0.05	
Output Voltage: High-Level, V _{OH} Min.	—	0,5	5	4.95				4.95	5	—	V
	—	0,10	10	9.95				9.95	10	—	
	—	0,15	15	14.95				14.95	15	—	
Input Low Voltage, V _{IL} Max.	0.5, 4.5	—	5	1.5				—	—	1.5	V
	1, 9	—	10	3				—	—	3	
	1.5, 13.5	—	15	4				—	—	4	
Input High Voltage, V _{IH} Min.	0.5, 4.5	—	5	3.5				3.5	—	—	V
	1, 9	—	10	7				7	—	—	
	1.5, 13.5	—	15	11				11	—	—	
Input Current I _{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	—	±10 ⁻⁵	±0.1	μA

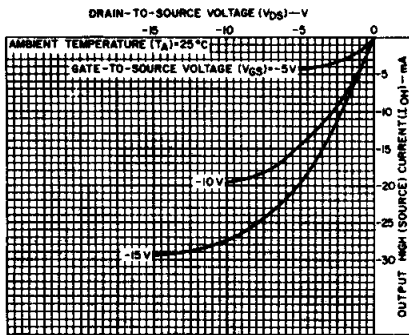


Fig.3 - Typical output high (source) current characteristics.

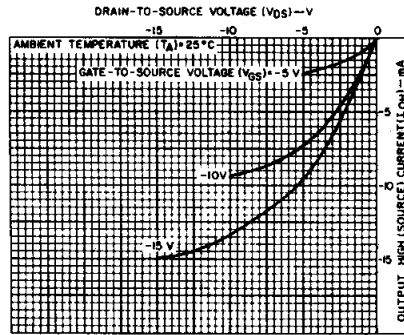


Fig.4 - Minimum output high (source) current characteristics.

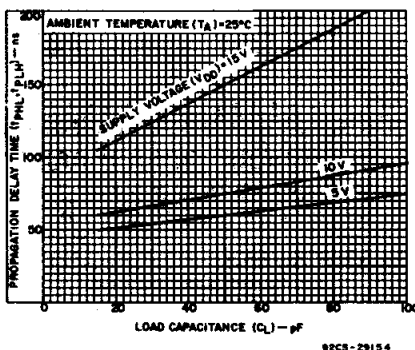


Fig.6 - Typical propagation delay time as a function of load capacitance (Clock or Strobe to Out).

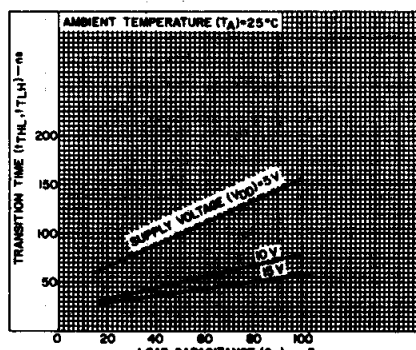


Fig.7 - Typical transition time as a function of load capacitance.

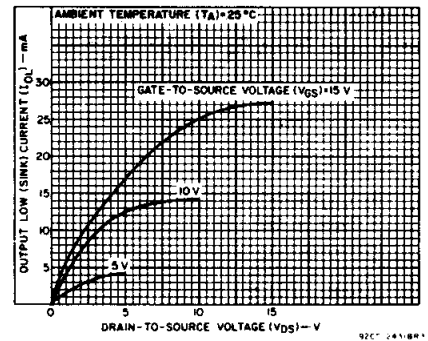


Fig.1 - Typical output low (sink) current characteristics.

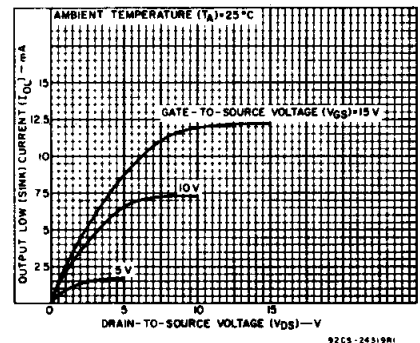


Fig.2 - Minimum output low (sink) current characteristics.

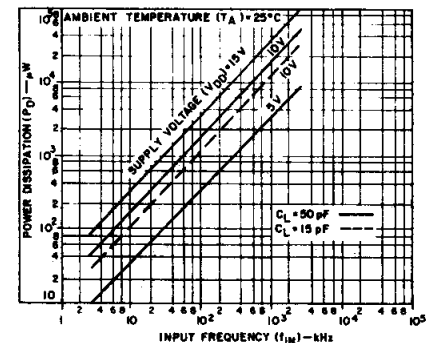


Fig.5 - Typical dynamic power dissipation as a function of input frequency.

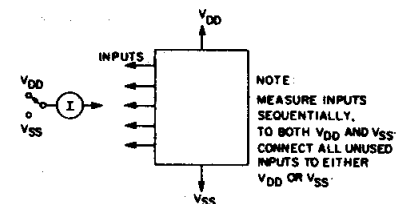


Fig.8 - Input current test circuit.

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DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$:

Input $t_r, t_f = 20 \text{ ns}$, $C_L = 50 \text{ pF}$, $R_L = 200 \text{ k}\Omega$

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		V _{DD} (V)	Min.	Typ.	Max.
Propagation Delay Time, t_{PHL} , t_{PLH} Clock to Out		5	—	110	220
		10	—	55	110
		15	—	45	90
Clock or Strobe to Out		5	—	150	300
		10	—	75	150
		15	—	60	120
Clock to Inhibit Out High Level to Low Level		5	—	320	640
		10	—	145	290
		15	—	100	200
Low Level to High Level		5	—	250	500
		10	—	100	200
		15	—	75	150
Clear to Out		5	—	380	760
		10	—	175	350
		15	—	130	260
Clock to "9" or "15" Out		5	—	300	600
		10	—	125	250
		15	—	90	180
Cascade to Out		5	—	90	180
		10	—	45	90
		15	—	35	70
Inhibit In to Inhibit Out		5	—	130	260
		10	—	60	120
		15	—	45	90
Set to Out		5	—	330	660
		10	—	150	300
		15	—	110	220
Transition Time, t_{THL} , t_{TLH}		5	—	100	200
		10	—	50	100
		15	—	40	80
Maximum Clock Frequency, f_{CL}		5	1.2	2.4	—
		10	2.5	5	—
		15	3.5	7	—
Minimum Clock Pulse Width, t_W		5	—	165	330
		10	—	85	170
		15	—	50	100
Clock Rise or Fall Time, t_{rCL} , t_{fCL}		5	—	—	15
		10	—	—	15
		15	—	—	15
Minimum Set or Clear Pulse Width, t_W		5	—	80	160
		10	—	45	90
		15	—	30	60
Minimum Inhibit In Setup Time, t_{SU}		5	—	50	100
		10	—	20	40
		15	—	10	20
Minimum Inhibit In Removal Time, t_{REM}		5	—	120	240
		10	—	65	130
		15	—	55	110
Minimum Set Removal Time, t_{REM}		5	—	75	150
		10	—	40	80
		15	—	25	50
Minimum Clear Removal Time, T_{REM}		5	—	30	60
		10	—	20	40
		15	—	15	30
Input Capacitance, C_{IN}	Any Input		—	5	7.5
					pF

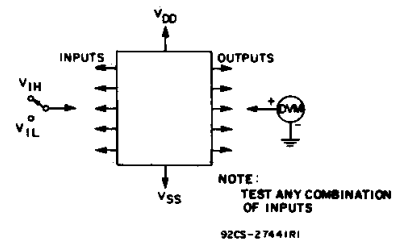


Fig. 9 - Input voltage test circuit.

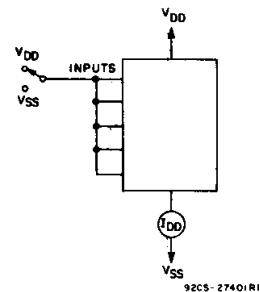


Fig. 10 - Quiescent device current test circuit.

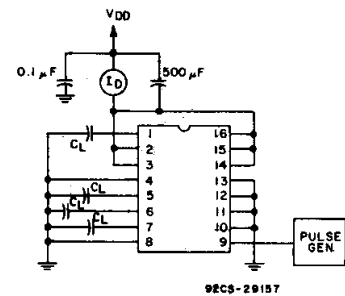


Fig. 11 - Dynamic power dissipation test circuit.

APPLICATIONS

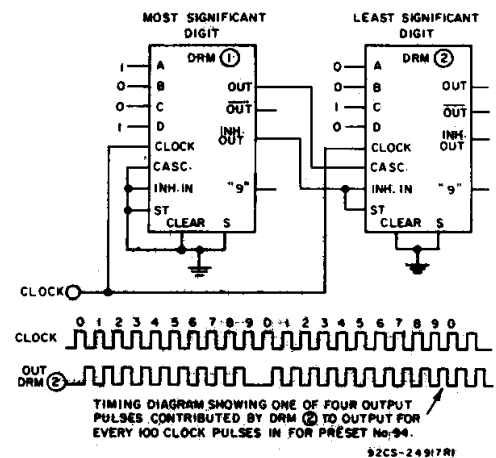


Fig. 12 - Two CD4527B's cascaded in the "Add" mode with a preset number

$$\text{of } 94 \left(\frac{9}{10} + \frac{4}{100} = \frac{94}{100} \right)$$

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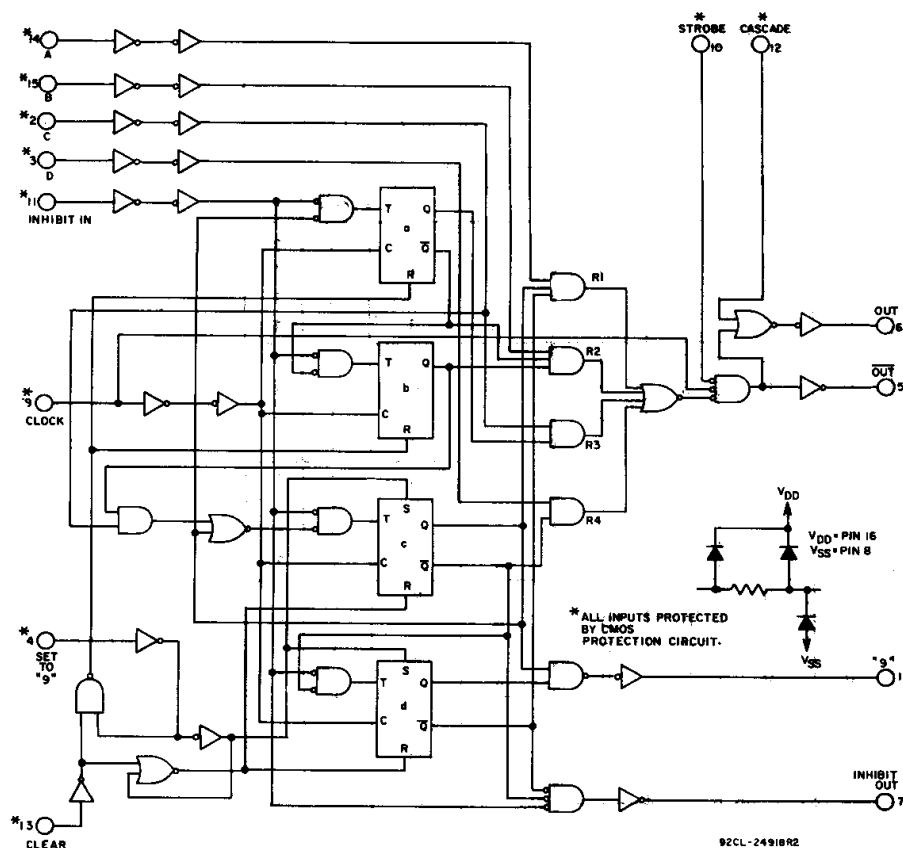


Fig. 13 - Logic diagram.

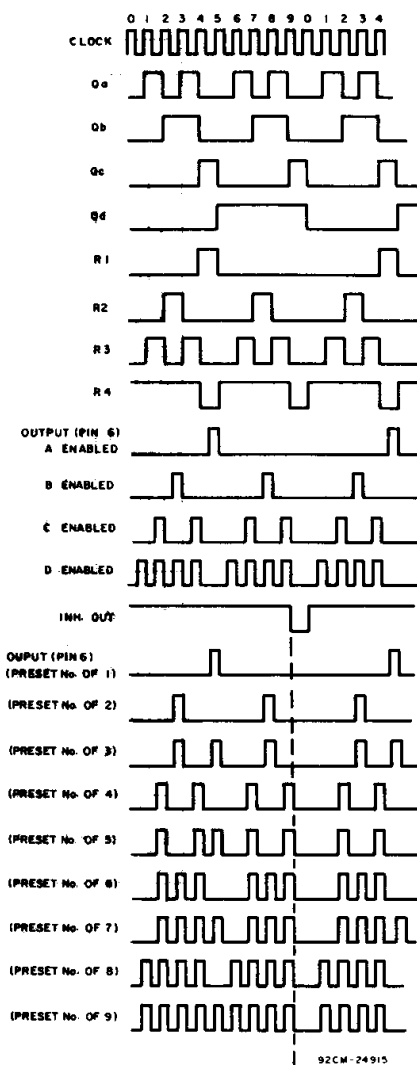
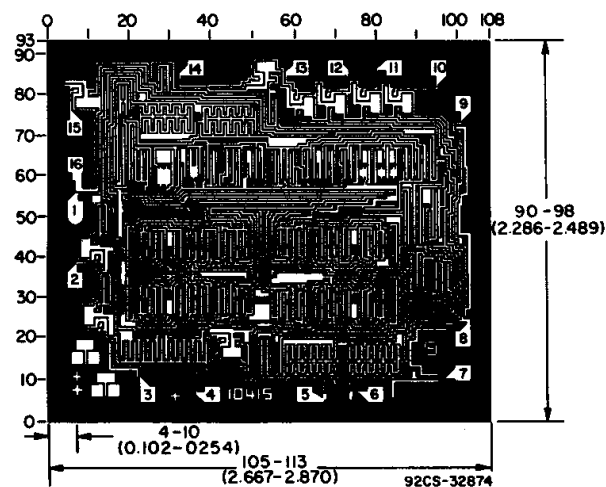


Fig. 14 - Timing diagram (See Logic Diagram).



Dimensions and Pad Layout for CD4527BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10⁻³ inch).

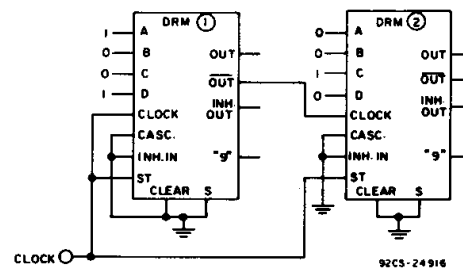


Fig. 15 - Two CD4527B's cascaded in the "Multiply" mode with a preset number

$$\text{of } 36 \left(\frac{9}{10} \times \frac{4}{10} = \frac{36}{100} \right).$$

CD4527B Types

TRUTH TABLE

INPUTS										OUTPUTS			
Number of Pulses or Input Logic Level (0 = Low; 1 = High; X = Don't Care)										Number of Pulses or Output Logic Level (L = Low; H = High)			
D	C	B	A	CLK	INH IN	STR	CAS	CLR #	SET #	OUT	$\overline{\text{OUT}}$	INH OUT	"9" OUT
0	0	0	0	10	0	0	0	0	0	L	H	1	1
0	0	0	1	10	0	0	0	0	0	1	1	1	1
0	0	1	0	10	0	0	0	0	0	2	2	1	1
0	0	1	1	10	0	0	0	0	0	3	3	1	1
0	1	0	0	10	0	0	0	0	0	4	4	1	1
0	1	0	1	10	0	0	0	0	0	5	5	1	1
0	1	1	0	10	0	0	0	0	0	6	6	1	1
0	1	1	1	10	0	0	0	0	0	7	7	1	1
1	0	0	0	10	0	0	0	0	0	8	8	1	1
1	0	0	1	10	0	0	0	0	0	9	9	1	1
1	0	1	0	10	0	0	0	0	0	8	8	1	1
1	0	1	1	10	0	0	0	0	0	9	9	1	1
1	1	0	0	10	0	0	0	0	0	8	8	1	1
1	1	0	1	10	0	0	0	0	0	9	9	1	1
1	1	1	0	10	0	0	0	0	0	8	8	1	1
1	1	1	1	10	0	0	0	0	0	9	9	1	1
X	X	X	X	10	1	0	0	0	0	†	†	H	†
X	X	X	X	10	0	1	0	0	0	L	H	1	1
X	X	X	X	10	0	0	1	0	0	H	*	1	1
1	X	X	X	10	0	0	0	1	0	10	10	H	L
0	X	X	X	10	0	0	0	1	0	L	H	H	L
X	X	X	X	10	0	0	0	0	1	L	H	L	H

* Output same as the first 16 lines of this truth table (depending on values of A, B, C, D).

† Depends on internal state of counter.

#Clear and Set Inputs should not be high at the same time; device draws increased quiescent current when in this non-valid state.

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