T-45-23-05

Recent Additions CD54AC163/3A CD54ACT163/3A

Synchronous Presettable Binary Counters

Synchronous Reset

The RCA CD54AC163 and CD54ACT163 are synchronous presettable binary counters that utilize the new RCA ADVANCED CMOS LOGIC technology. The CD54AC/ACT163 devices are reset synchronously with the clock. Counting and parallel presetting are both accomplished synchronously with the negative-to-positive transition of the clock.

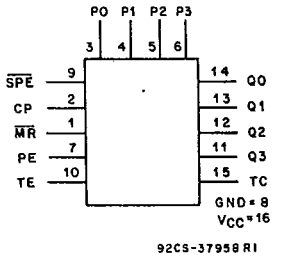
A LOW level on the Synchronous Parallel Enable input, $\overline{SPE}$, disables the counting operation and allows data at the P0 to P3 inputs to be loaded into the counter (provided that the setup and hold requirements for $\overline{SPE}$ are met).

The counters are reset with a LOW level on the Master Reset input, $\overline{MR}$. The requirements for setup and hold time with respect to the clock must be met.

Two count enables, PE and TE, in each counter are provided for n-bit cascading. Reset action occurs regardless of the level of the $\overline{SPE}$, PE, and TE inputs.

The look-ahead carry feature simplifies serial cascading of the counters. Both count enable inputs (PE and TE) must be HIGH to count. The TE input is gated with the Q outputs of all four stages so that at the maximum count, the terminal count (TC) output goes HIGH for one clock period. This TC pulse is used to enable the next cascaded stage.

The CD54AC163 and CD54ACT163 are supplied in 16-lead dual-in-line ceramic packages (F suffix).



FUNCTIONAL DIAGRAM

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Package Specifications

(See Section 11, Fig. 11)

Static Electrical Characteristics (Limits with black dots (•) are tested 100%.)

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
				+25		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	
Quiescent Supply Current (MSI) I_{CC}	V_{CC} or GND	0	5.5	—	8•	—	160•	μA

The complete static electrical test specification consists of the above by-type static tests combined with the standard static tests in the beginning of this section.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
Pn	0.13
CP	1
$\overline{MR}$, TE	0.83
$\overline{SPE}$	0.67
PE	0.5

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

Burn-In Test-Circuit Connections

Identical to CD54HC/HCT163/3A, page 5-70.

Recent Additions
CD54AC163/3A
CD54ACT163/3A

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF (Worst Case)

CHARACTERISTICS	SYMBOL	V_{CC} (V)	-55 to +125°C		UNITS
			MIN.	MAX.	
Propagation Delays: CP to Qn ($\overline{SPE}$ HIGH)	t_{PLH} t_{PHL}	1.5 3.3* 5†	— 4.3 2.8	207 23.1 16.5	ns
CP to Qn ($\overline{SPE}$ LOW)	t_{PLH} t_{PHL}	1.5 3.3 5	— 4.3 2.8	207 23.1 16.5•	ns
CP to TC	t_{PLH} t_{PHL}	1.5 3.3 5	— 4.4 2.9	209 23.4 16.7•	ns
TE to TC	t_{PLH} t_{PHL}	1.5 3.3 5	— 2.6 1.8	129 14.4 10.3•	ns
Power Dissipation Capacitance	C_{PD}§	—			pF
Input Capacitance	C_I	—	—	10	pF

SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF (Worst Case)

CHARACTERISTICS	SYMBOL	V_{CC} (V)	-55 to +125°C		UNITS
			MIN.	MAX.	
Propagation Delays: CP to Qn ($\overline{SPE}$ HIGH)	t_{PLH} t_{PHL}	5†	2.8	16.5	ns
CP to Qn ($\overline{SPE}$ LOW)		5	2.8	16.5•	ns
CP to TC		5	2.9	16.7•	ns
TE to TC		5	1.8	10.8•	ns
Power Dissipation Capacitance	C_{PD}§	—			pF
Input Capacitance	C_I	—	—	10	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption per device.
For AC, $P_D = C_{PD}V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$
For ACT, $P_D = C_{PD}V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o) + V_{CC} \Delta I_{CC}$ where f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage

(Limits with black dots (•) are tested 100%.)