

8-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μ PD78081, 78082 are members of the μ PD78083 subseries of the 78K/0 series microcontrollers.

Besides a high-speed, high-performance CPU, these microcontrollers have on-chip ROM, RAM, I/O ports, 8-bit resolution A/D converter, timer, serial interface interrupt control, and other peripheral hardware.

The μ PD78P083 devices including a one-time PROM version and an EPROM version, both of which can operate in the same power supply voltage range as a mask ROM version, and various development tools are available.

The details of the functions are described in the following user's manuals. Be sure to read it before starting design.

μ PD78083 Subseries User's Manual : IEU-1407

78K/0 Series User's Manual – Instructions : IEU-1417

FEATURES

- Internal ROM and RAM

Item Part Number	Program Memory (ROM)	Data Memory (Internal High-speed RAM)	Package
μ PD78081	8K bytes	256 bytes	42-pin plastic shrink DIP (600 mil)
μ PD78082	16K bytes	384 bytes	44-pin plastic QFP (10 × 10 mm)

- Instruction execution time can be changed from high-speed (0.4 μ s) to low-speed (12.8 μ s)
- I/O ports: 33
- 8-bit resolution A/D converter : 8 channels
- Serial interface : 1 channel
3-wire serial I/O / UART mode : 1 channel
- Timer : 3 channels
- Supply voltage : $V_{DD} = 1.8$ to 5.5 V



APPLICATION FIELDS

Air bags, CRT displays, keyboards, air conditioners, water heaters, boilers, fan heater, dash boards, etc.

The information in this document is subject to change without notice.

ORDERING INFORMATION

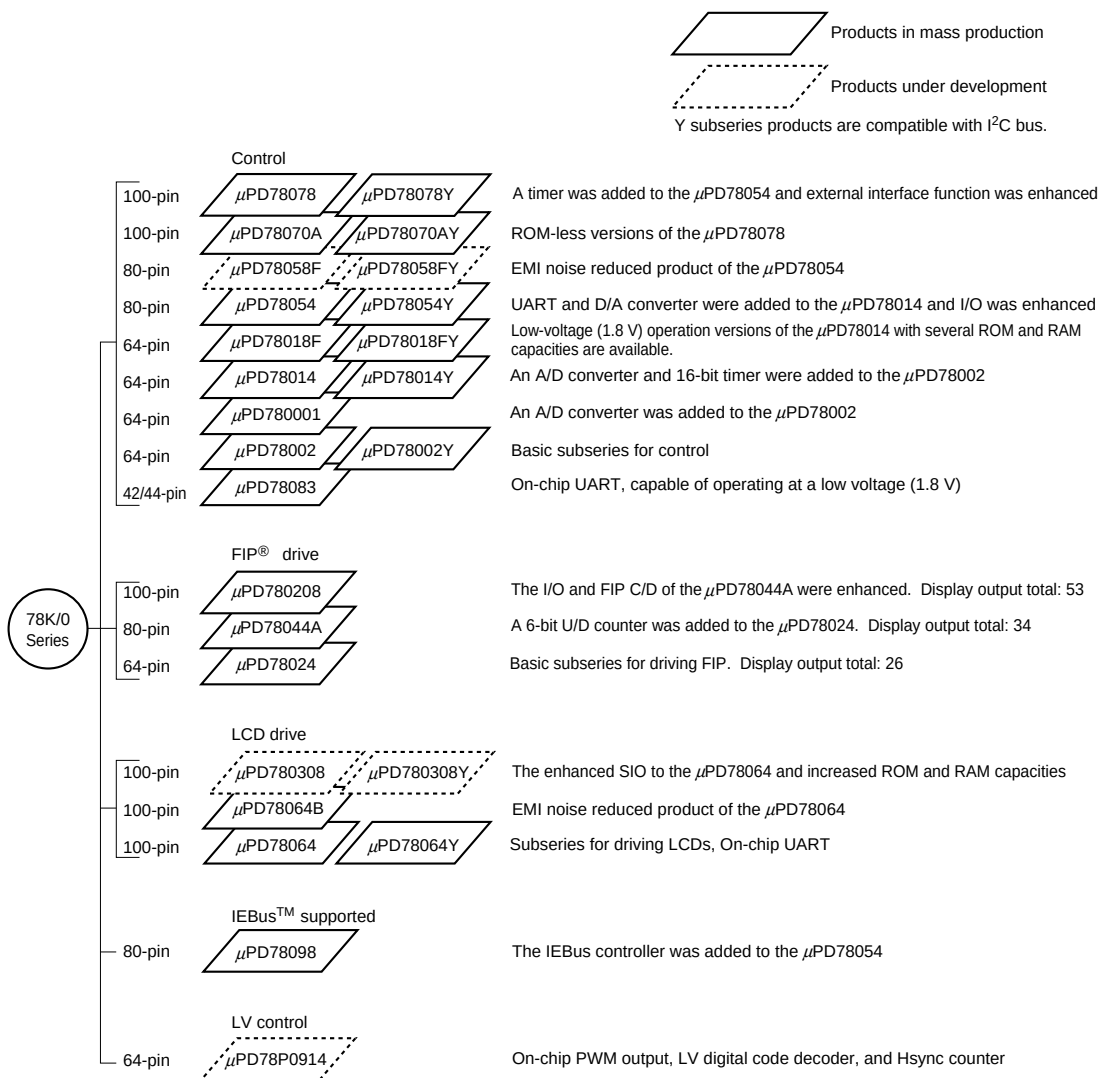
	Part Number	Package
	μPD78081CU-XXX	42-pin plastic shrink DIP (600 mil)
	μPD78081GB-XXX-3B4	44-pin plastic QFP (10 × 10 mm)
★	μPD78081GB-XXX-3BS-MTX	44-pin plastic QFP (10 × 10 mm)
	μPD78082CU-XXX	42-pin plastic shrink DIP (600 mil)
	μPD78082GB-XXX-3B4	44-pin plastic QFP (10 × 10 mm)
★	μPD78082GB-XXX-3BS-MTX	44-pin plastic QFP (10 × 10 mm)

Caution μPD78081GB, 78082GB have two kinds of package. (Refer to 11. PACKAGE DRAWINGS). Please refer an NEC's sales representative for the available package.

Remark XXX indicates ROM code suffix.

78K/0 SERIES DEVELOPMENT

The following shows the 78K/0 series products development. Subseries names are shown inside frames.



The major functional differences among the subseries are shown below.

Function Subseries Name		ROM Capacity	Timer				8-bit A/D	8-bit D/A	Serial Interface	I/O	V _{DD} MIN. Value	External Expansion
			8-bit	16-bit	Watch	WDT						
For Control	μPD78078	32 K-60 K	4ch	1ch	1ch	1ch	8ch	2ch	3ch (UART: 1ch)	88	1.8 V	○
	μPD78070A	—								61	2.7 V	
	μPD78058F	48 K-60 K	2ch						69	2.0 V		
	μPD78054	16 K-60 K							53	1.8 V		
	μPD78018F	8 K-60 K	—	2ch	53	2.7 V						
	μPD78014	8 K-32 K			1ch	39	—					
	μPD780001	8 K				53						
	μPD78002	8 K-16 K	—	33		1.8 V		○				
	μPD78083		—	—	8ch	1ch (UART: 1ch)	33	1.8 V	—			
For FIP drive	μPD780208	32 K-60 K	2ch	1ch	1ch	1ch	8ch	—	2ch	74	2.7 V	—
	μPD78044A	16 K-40 K								68		
	μPD78024	24 K-32 K								54		
LCD drive	μPD780308	48 K-60 K	2ch	1ch	1ch	1ch	8ch	—	3ch (UART: 1ch)	57	1.8 V	—
	μPD78064B	32 K							2ch (UART: 1ch)		2.0 V	
	μPD78064	16 K-32 K										
For IEBus	μPD78098	32 K-60 K	2ch	1ch	1ch	1ch	8ch	2ch	3ch (UART: 1ch)	69	2.7 V	○
LV control	μPD78P0914	32 K	6ch	—	—	1ch	8ch	—	2ch	54	4.5 V	○

OVERVIEW OF FUNCTION

Part Number		μPD78081	μPD78082
Item			
Internal memory	ROM	8K bytes	16K bytes
	Internal high-speed RAM	256 bytes	384 bytes
Memory space		64K bytes	
General registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)	
Instruction cycle		On-chip instruction execution time selective function 0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs/12.8 μs (at main system clock of 5.0 MHz)	
Instruction set		• 16-bit operation • Multiplcation/division (8 bits × 8 bits,16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, boolean operation) • BCD adjustment, etc.	
I/O ports		Total : 33 • CMOS input : 1 • CMOS I/O : 32	
A/D converter		8-bit resolution × 8 channels	
Serial interface		3-wire serial I/O / UART mode selectable : 1 channel	
Timer		• 8-bit timer/event counter : 2 channels • Watchdog timer : 1 channel	
Timer output		2 (8-bit PWM output)	
Clock output		19.5 kHz, 39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz, 1.25 MHz, 2.5 MHz, 5.0 MHz (at main system clock of 5.0 MHz)	
Buzzer output		1.2 kHz, 2.4 kHz, 4.9 kHz, 9.8 kHz (at main system clock of 5.0 MHz)	
Vectored interrupts	Maskable interrupts	Internal : 8 external : 3	
	Non-maskable interrupts	Internal : 1	
	Software interrupts	Internal : 1	
Supply voltage		V _{DD} = 1.8 to 5.5 V	
Operating ambient temperature		T _A = −40 to + 85 °C	
Package		• 42-pin plastic shrink DIP (600 mil) • 44-pin plastic QFP (10 × 10 mm)	

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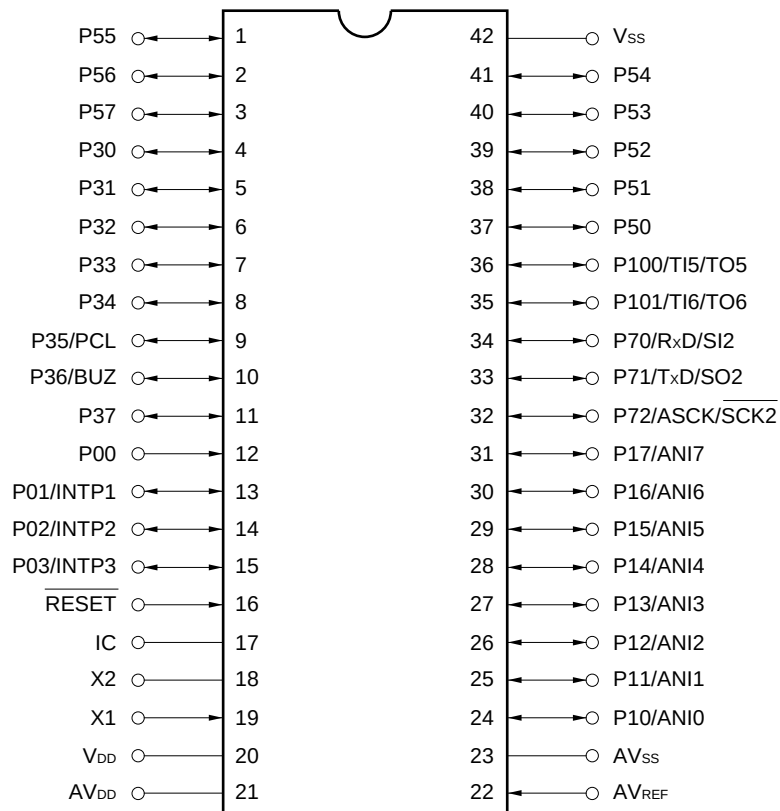
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1. PIN CONFIGURATIONS (TOP VIEW)

• 42-pin plastic shrink DIP (600 mil)

μPD78081CU-xxx

μPD78082CU-xxx



Cautions 1. Connect IC (Internally Connected) pin directly to V_{SS}.

2. Connect AV_{DD} pin to V_{DD}.

3. Connect AV_{SS} pin to V_{SS}.

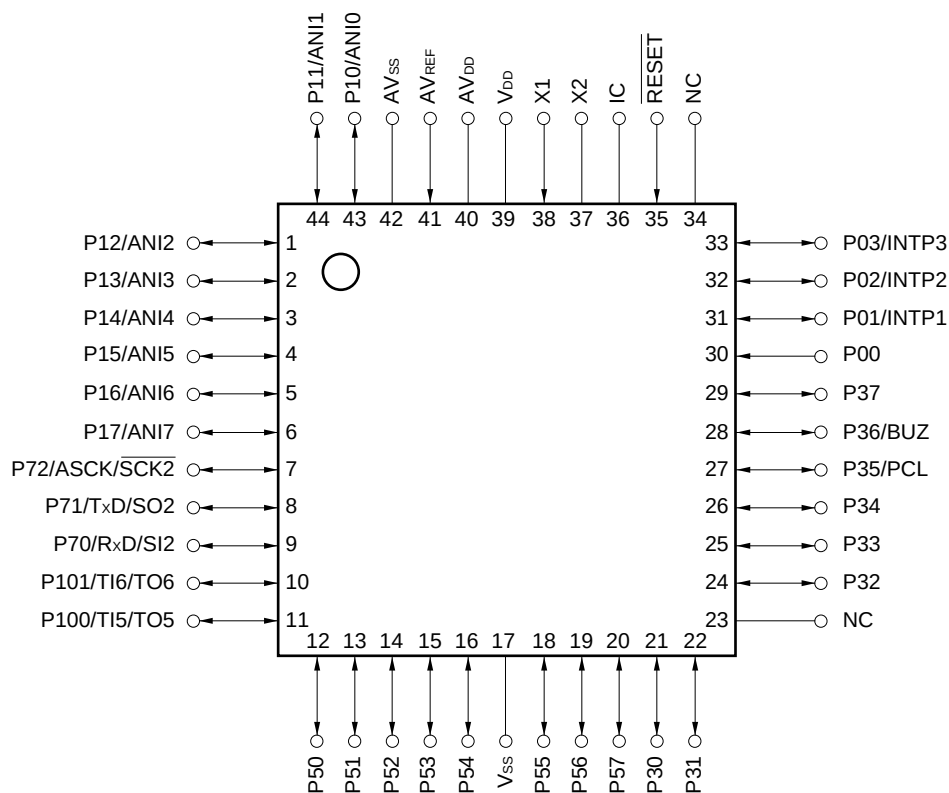
• 44-pin plastic QFP (10 × 10 mm)

μPD78081GB-xxx-3B4

μPD78081GB-xxx-3BS-MTX

μPD78082GB-xxx-3B4

μPD78082GB-xxx-3BS-MTX



Cautions 1. Connect IC (Internally Connected) pin directly to V_{SS}.

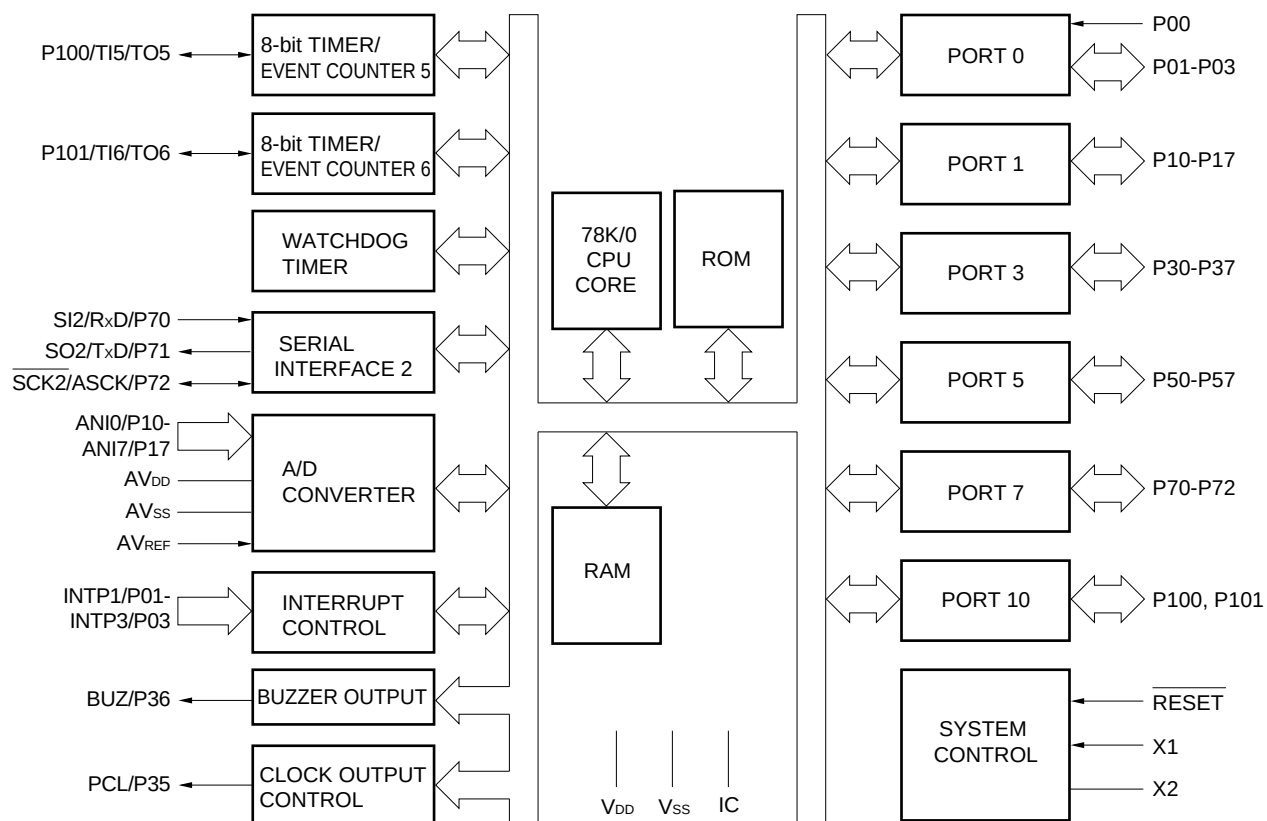
2. Connect AV_{DD} pin to V_{DD}.

3. Connect AV_{SS} pin to V_{SS}.

4. Connect NC (Non-connection) pin to V_{SS} for noise protection (It can be left open).

P00 to P03	: Port 0	PCL	: Programmable Clock
P10 to P17	: Port 1	BUZ	: Buzzer Clock
P30 to P37	: Port 3	X1, X2	: Crystal (Main System Clock)
P50 to P57	: Port 5	$\overline{\text{RESET}}$	: Reset
P70 to P72	: Port 7	ANI0-ANI7	: Analog Input
P100, P101	: Port 10	AV _{DD}	: Analog Power Supply
INTP1 to INTP3	: Interrupt from Peripherals	AV _{SS}	: Analog Ground
TI5, TI6	: Timer Input	AV _{REF}	: Analog Reference Voltage
TO5, TO6	: Timer Output	V _{DD}	: Power Supply
SI2	: Serial Input	V _{SS}	: Ground
SO2	: Serial Output	IC	: Internally Connected
SCK2	: Serial Clock	NC	: Non-connection
RxD	: Receive Data		
TxD	: Transmit Data		
ASCK	: Asynchronous Serial Clock		

2. BLOCK DIAGRAM



Remark The internal ROM and internal high-speed RAM capacities depend on the product.

3. PIN FUNCTIONS

3.1 Port pins

Pin Name	Input/Output	Function		After Reset	Shared by:
P00	Input	Port 0	Input only	Input	—
P01	Input/output	4-bit input/output port	Input/output is specifiable bit-wise. When used as the input port, it is possible to connect a pull-up resistor by software.	Input	INTP1
P02					INTP2
P03					INTP3
P10-P17	Input/output	Port 1 8-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to connect a pull-up resistor by software. Note		Input	ANI0-ANI7
P30-P34	Input/output	Port 3	8-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to connect a pull-up resistor by software.	Input	—
P35		8-bit input/output port			PCL
P36		Input/output is specifiable bit-wise.			BUZ
P37		When used as the input port, it is possible to connect a pull-up resistor by software.			—
P50-P57	Input/output	Port 5 8-bit input/output port Can drive up to seven LEDs directly. Input/output is specifiable bit-wise. When used as the input port, it is possible to connect a pull-up resistor by software.		Input	—
P70	Input/output	Port 7	3-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to connect a pull-up resistor by software.	Input	SI2/RxD
P71		3-bit input/output port			SO2/TxD
P72		Input/output is specifiable bit-wise.			SCK2/ASCK
P100	Input/output	Port 10	2-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to connect a pull-up resistor by software.	Input	TI5/TO5
P101		2-bit input/output port			TI6/TO6

Note When P10/ANI0-P17/ANI7 pins are used as the analog inputs for the A/D converter, set the port 1 to the input mode. The on-chip pull-up resistor is automatically disabled.

3.2 Non-port pins

Pin Name	Input/Output	Function	After Reset	Shared by:
INTP1	Input	External interrupt input by which the active edge (rising edge, falling edge, or both rising and falling edges) can be specified.	Input	P01
INTP2				P02
INTP3				P03
SI2	Input	Serial interface serial data input.	Input	P70/RxD
SO2	Output	Serial interface serial data output.	Input	P71/TxD
SCK2	Input/Output	Serial interface serial clock input/output.	Input	P72/ASCK
RxD	Input	Asynchronous serial interface serial data input.	Input	P70/SI2
TxD	Output	Asynchronous serial interface serial data output.	Input	P71/SO2
ASCK	Input	Asynchronous serial interface serial clock input.	Input	P72/SCK2
TI5	Input	External count clock input to 8-bit timer (TM5).	Input	P100/TO5
TI6		External count clock input to 8-bit timer (TM6).		P101/TO6
TO5	Output	8-bit timer output.	Input	P100/TO5
TO6				P101/TO6
PCL	Output	Clock output. (for main system clock trimming)	Input	P35
BUZ	Output	Buzzer output.	Input	P36
ANI0-ANI7	Input	A/D converter analog input.	Input	P10-P17
AV _{REF}	Input	A/D converter reference voltage input.	—	—
AV _{DD}	—	A/D converter analog power supply. Connected to V _{DD} .	—	—
AV _{SS}	—	A/D converter ground potential. Connected to V _{SS} .	—	—
RESET	Input	System reset input.	—	—
X1	Input	Main system clock oscillation crystal connection.	—	—
X2	—		—	—
V _{DD}	—	Positive power supply.	—	—
V _{SS}	—	Ground potential.	—	—
IC	—	Internal connection. Connect directly to V _{SS} .	—	—
NC	—	Does not internally connected. Connect to V _{SS} . (It can be left open)	—	—

3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

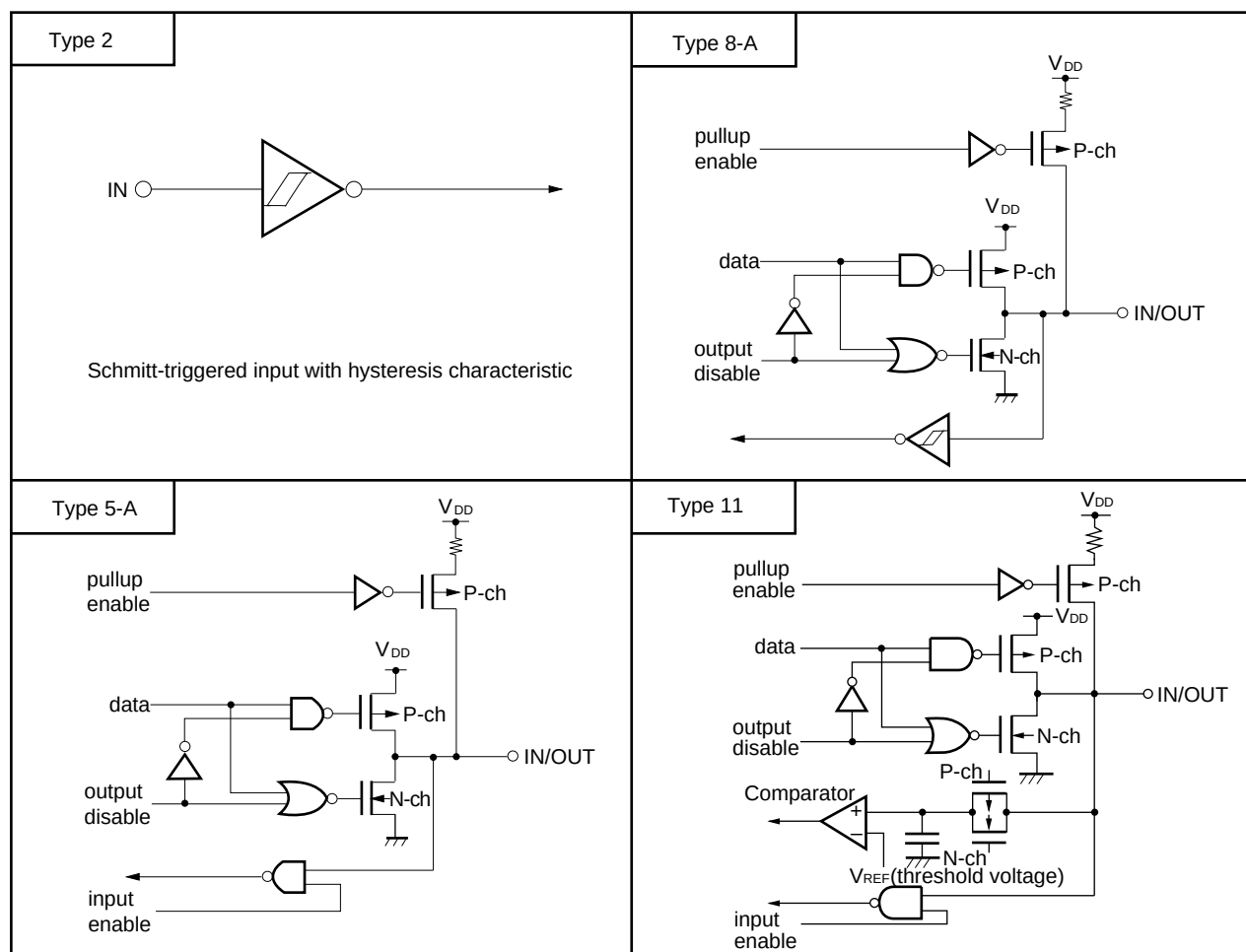
The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 3-1.

For the input/output circuit configuration of each type, refer to **Figure 3-1**.

Table 3-1. Types of Pin Input/Output Circuits

Pin Name	Input/Output Circuit Type	I/O	Recommended Connection for Unused Pins
P00	2	Input	Connect to V _{SS} .
P01/INTP1	8-A	Input/output	Connect to V _{SS} via a resistor individually.
P02/INTP2			
P03/INTP3			
P10/ANI0-P17/ANI7	11	Input/output	Connect to V _{DD} or V _{SS} via a resistor individually.
P30-P32	5-A		
P33, P34	8-A		
P35/PCL	5-A		
P36/BUZ			
P37			
P50-P57	5-A		
P70/SI2/RxD	8-A		
P71/SO2/TxD	5-A		
P72/ $\overline{\text{SCK2}}$ /ASCK	8-A		
P100/TI5/TO5	8-A		
P101/TI6/TO6			
$\overline{\text{RESET}}$	2	Input	—
AV _{REF}	—	—	Connect to V _{SS} .
AV _{DD}			Connect to V _{DD} .
AV _{SS}			Connect to V _{SS} .
IC			Connect to V _{SS} .
NC			Connect to V _{SS} (It can be left open).

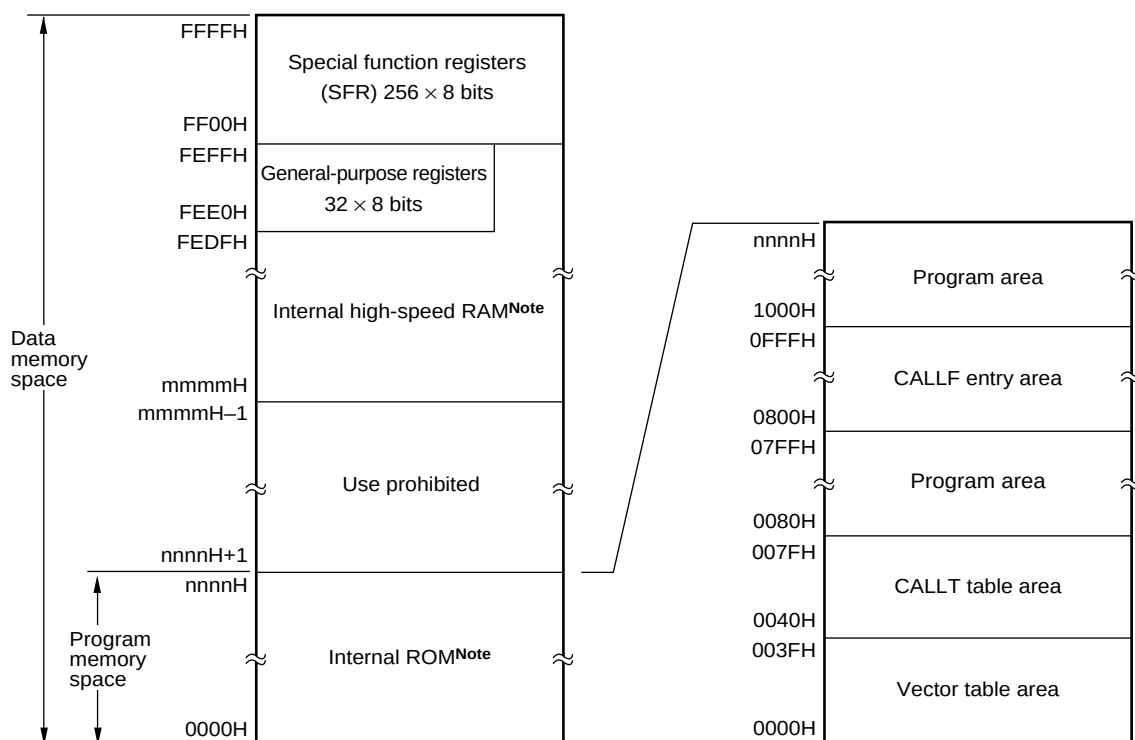
Figure 3-1. Pin Input/Output Circuits



4. MEMORY SPACE

The memory map of the μPD78081, 78082 is shown in Figure 4-1.

Figure 4-1. Memory Map



Note The internal ROM and internal high-speed RAM capacities depend on the product. (See the following table.)

Part Number	Internal ROM Last Address nnnnH	Internal High-speed RAM Starting Address mmmH
μPD78081	1FFFH	FE00H
μPD78082	3FFFH	FD80H

5. PERIPHERAL HARDWARE FUNCTIONS

5.1 Ports

Input/output ports are classified into two types.

- CMOS input (P00) : 1
 - CMOS input/output (P01 to P03, Port 1, Port 3, Port 5, Port 7, Port 10) : 32
-
- Total : 33

Table 5-1. Functions of Ports

Port Name	Pin Name	Function
Port 0	P00	Input only.
	P01 to P03	Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.
Port 1	P10 to P17	Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.
Port 3	P30 to P37	Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.
Port 5	P50 to P57	Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software. LED can be driven directly up to 7 pins.
Port 7	P70 to P72	Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.
Port 10	P100, P101	Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.

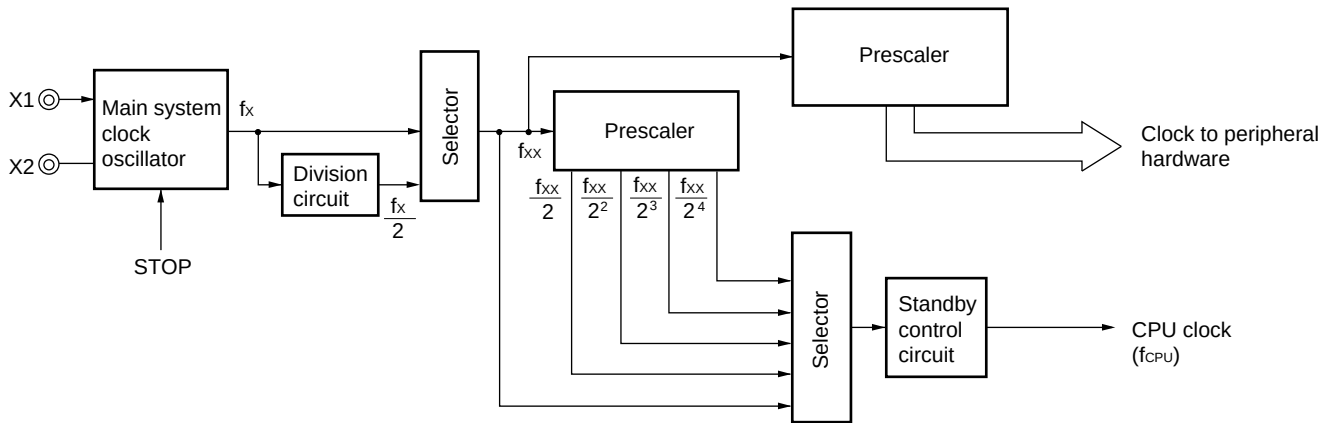
5.2 Clock Generator

Main system clock generator is incorporated.

It is possible to change the instruction execution time.

- 0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs/12.8 μs (at main system clock frequency of 5.0 MHz)

Figure 5-1. Clock Generator Block Diagram



5.3 Timer/Event Counter

There are the following three timer/event counter channels:

- 8-bit timer/event counter : 2 channels
- Watchdog timer : 1 channel

Table 5-2. Types and Functions of Timer/Event Counters

		8-bit Timer/Event Counter 5, 6	Watchdog Timer
Type	Interval timer	2 channels	1 channel
	External event counter	2 channels	—
Function	Timer output	2 output	—
	PWM output	2 output	—
	Square wave output	2 output	—
	Interrupt request	2	1

Figure 5-2. 8-Bit Timer/Event Counter 5, 6 Block Diagram

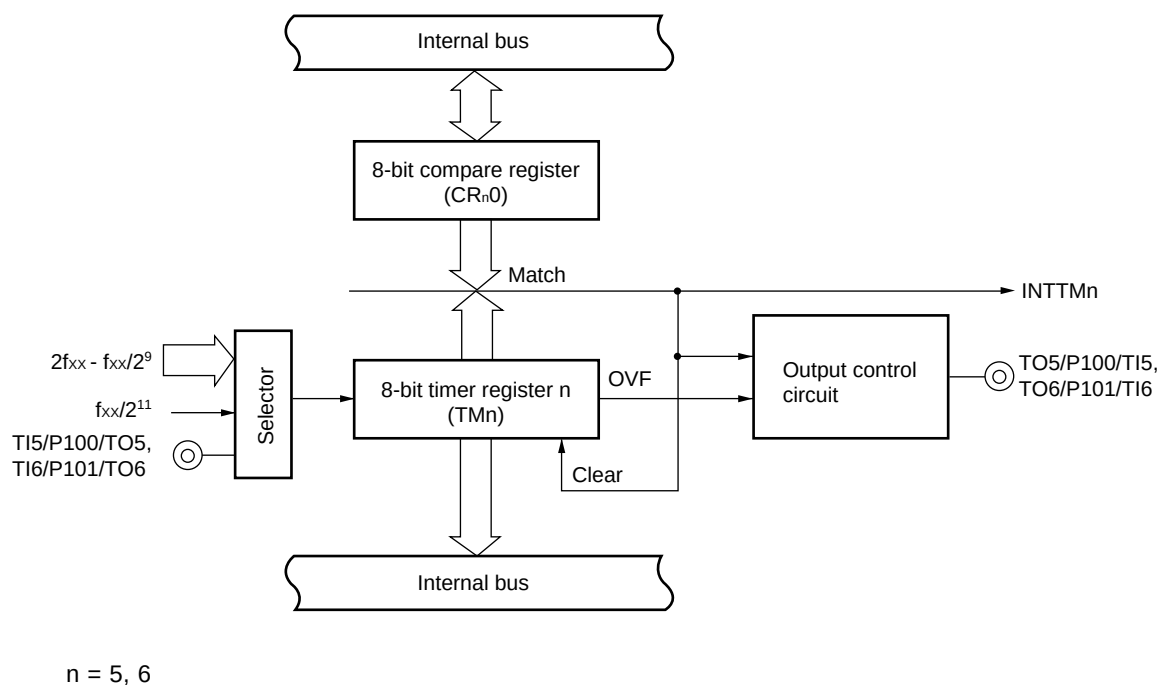
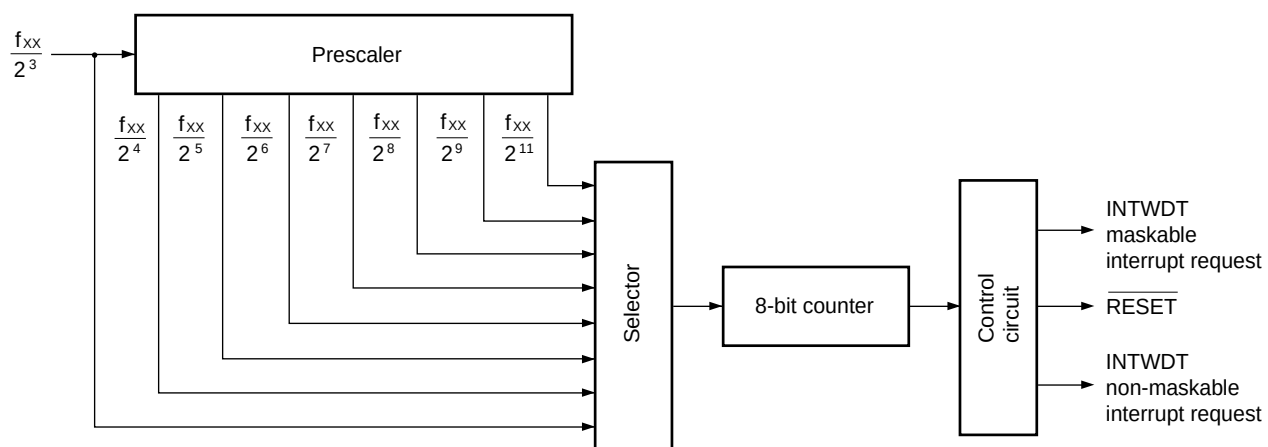


Figure 5-3. Watchdog Timer Block Diagram

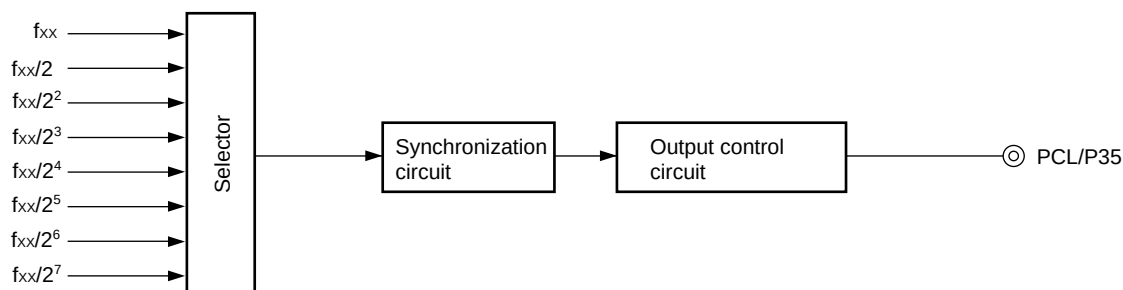


5.4 Clock Output Control Circuit

This circuit can output clocks of the following frequencies:

- 19.5 kHz/39.1 kHz/78.1 kHz/156 kHz/313 kHz/625 kHz/1.25 MHz/2.5 MHz/5.0 MHz (at main system clock frequency of 5.0 MHz)

Figure 5-4. Clock Output Control Circuit Block Diagram

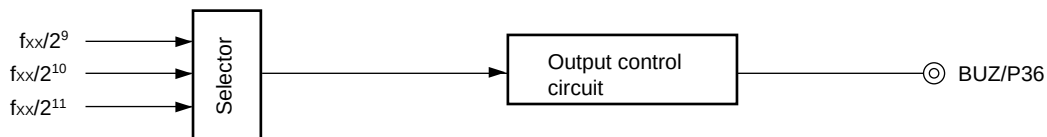


5.5 Buzzer Output Control Circuit

This circuit can output clocks of the following frequencies that can be used for driving buzzers:

- 1.2 kHz/2.4 kHz/4.9 kHz/9.8 kHz (at main system clock frequency of 5.0 MHz)

Figure 5-5. Buzzer Output Control Circuit Block Diagram



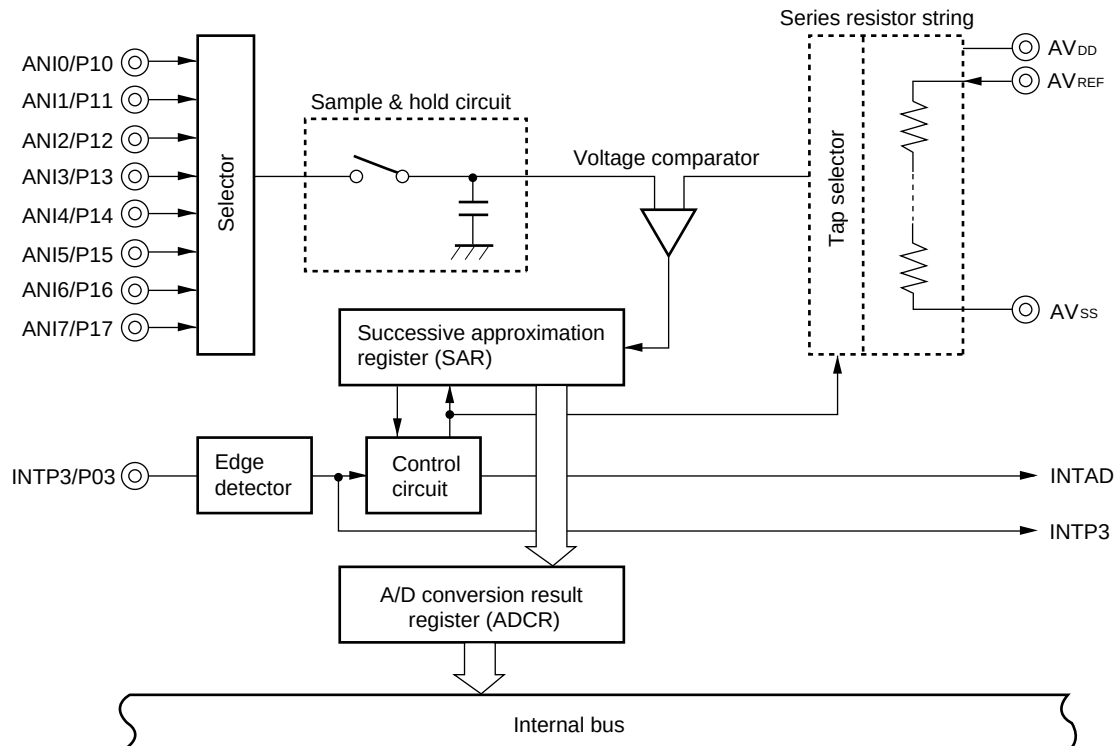
5.6 A/D Converter

The A/D converter consists of eight 8-bit resolution channels.

A/D conversion can be started by the following two methods:

- Hardware starting
- Software starting

Figure 5-6. A/D Converter Block Diagram



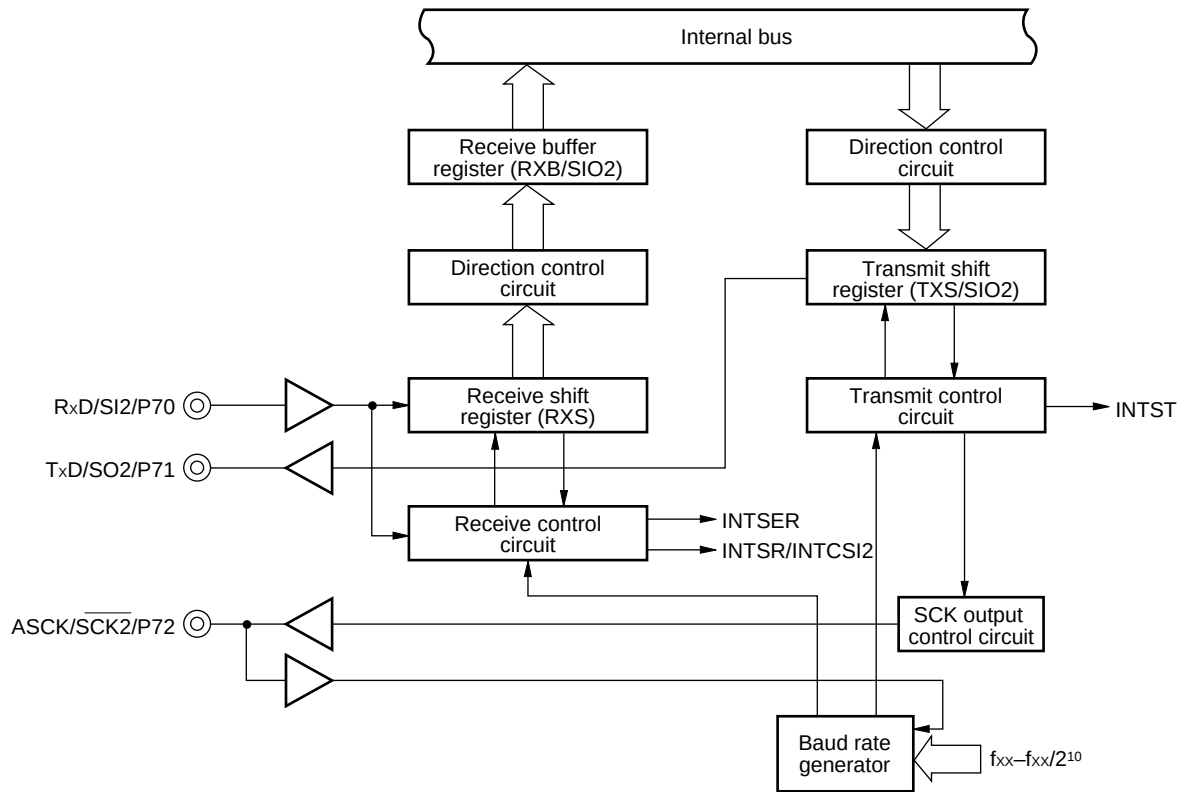
5.7 Serial Interface

There is one on-chip serial interface channel synchronous with the clock.

The serial interface channel 2 operates in the following two modes:

- 3-wire serial I/O mode : Starting bit MSB/LSB switching possible
- Asynchronous serial interface (UART) mode : On-chip dedicated baud rate generator

Figure 5-7. Serial Interface Channel 2 Block Diagram



6. INTERRUPT FUNCTIONS

A total of 13 interrupt functions are provided, divided into the following three types.

- Non-maskable interrupt : 1
- Maskable interrupt : 11
- Software interrupt : 1

Table 6-1. List of Interrupt Factors

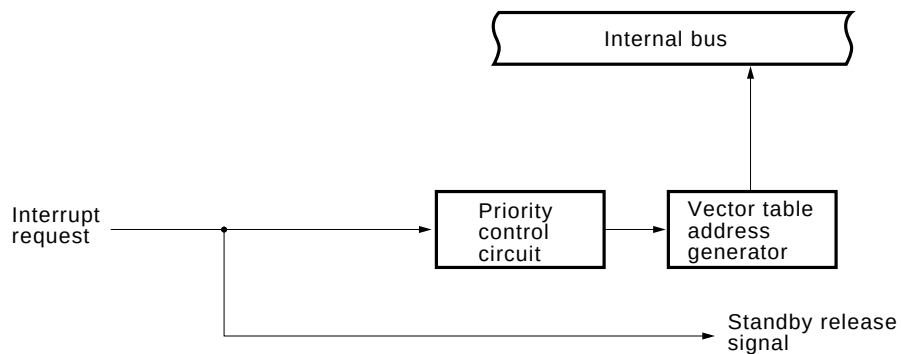
Interrupt Type	Note 1 Default Priority	Interrupt Factor		Internal/ External	Vector Table Address	Note 2 Basic Structure Type
		Name	Trigger			
Non-maskable	–	INTWDT	Overflow of watchdog timer (When the watchdog timer mode 1 is selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Overflow of watchdog timer (When the interval timer mode is selected)			(B)
	1	INTP1	Pin input edge detection	External	0008H	(C)
	2	INTP2			000AH	
	3	INTP3			000CH	
	4	INTSER	Occurrence of serial interface channel 2 UART reception error	Internal	0018H	(B)
	5	INTSR	Completion of serial interface channel 2 UART reception		001AH	
		INTCSI2	Completion of serial interface channel 2 3-wire transfer			
	6	INTST	Completion of serial interface channel 2 UART transmission		001CH	
	7	INTAD	Completion of A/D conversion		0028H	
	8	INTTM5	Generation of matching signal of 8-bit timer/event counter 5		002AH	
	9	INTTM6	Generation of matching signal of 8-bit timer/event counter 6		002CH	
Software	–	BRK	Execution of BRK instruction	Internal	003EH	(D)

Notes 1. Default priority is the priority order when several maskable interruptions are generated at the same time. 0 is the highest order and 9 is the lowest order.

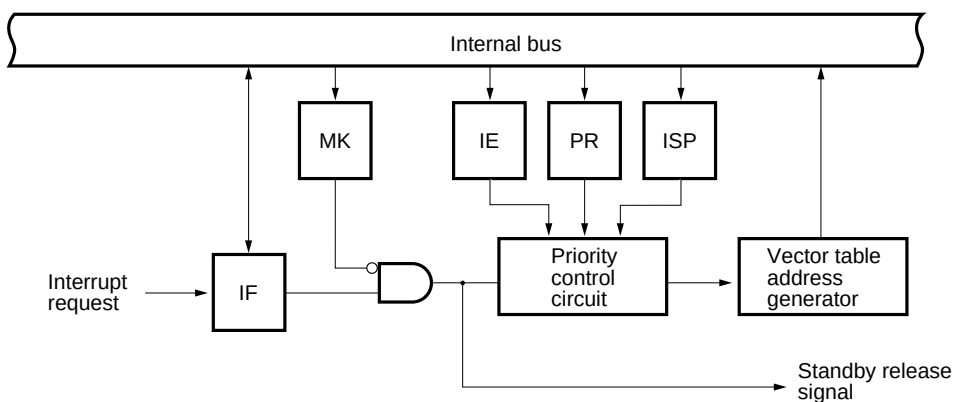
2. Basic structure types (A) to (D) correspond to (A) to (D) in Figure 6-1.

Figure 6-1. Interrupt Function Basic Configuration (1/2)

(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt

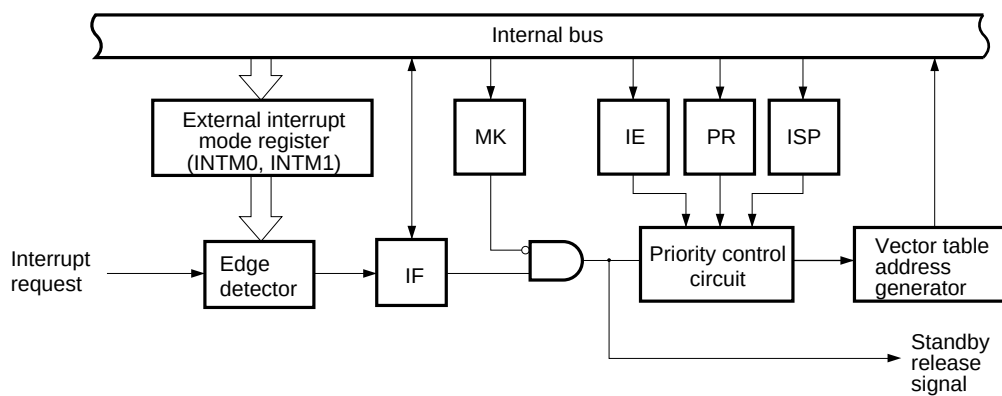
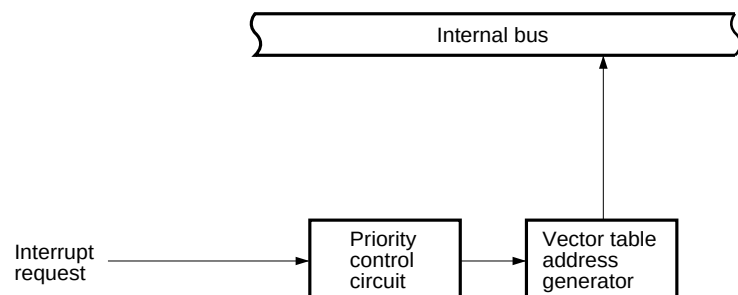


Figure 6-1. Interrupt Function Basic Configuration (2/2)

(D) Software interrupt



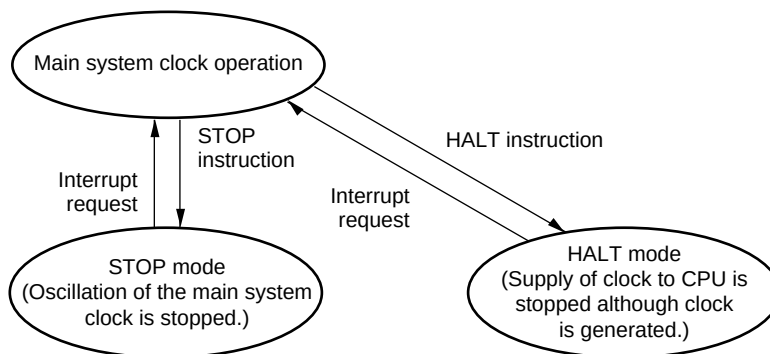
- IF : Interrupt request flag
- E : Interrupt enable flag
- ISP : In-service priority flag
- MK : Interrupt mask flag
- PR : Priority specification flag

7. STANDBY FUNCTION

The standby function intends to reduce current consumption. It has the following two modes:

- HALT mode : In this mode, the CPU operation clock is stopped. The average current consumption can be reduced by intermittent operation by combining this mode with the normal operation mode.
- STOP mode : In this mode, oscillation of the main system clock is stopped. All the operations performed on the main system clock are suspended, and power consumption becomes extremely small.

Figure 7-1. Standby Function



8. RESET FUNCTION

There are the following two reset methods.

- External reset input by RESET pin
- Internal reset by watchdog timer runaway time detection

9. INSTRUCTION SET

(1) 8-bit instructions

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

2nd Operand 1st Operand	#byte	A	r ^{Note}	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL + byte] [HL + B] [HL + C]	\$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP											INC DEC
B, C											DBNZ		
sfr	MOV	MOV											
saddrMOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP										DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]		MOV											

Note Except r = A

2nd Operand 1st Operand	#byte	A	r	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL + byte] [HL + B] [HL + C]	\$addr16	1	None
[HL]		MOV											ROR4 ROL4
[HL + byte] [HL + B] [HL + C]		MOV											
X													MULU
C													DIVUW

(2) 16-bit instructions

MOVW, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

2nd Operand 1st Operand	#word	AX	rp ^{Note}	sfrp	saddrp	!addr16	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW ^{Note}						INCW DECW PUSH POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
!addr16		MOVW						
SP	MOVW	MOVW						

Note Only when rp = BC, DE, HL

(3) Bit manipulation instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

2nd Operand 1st Operand	A.bit	sfr.bit	saddr.bit	PSW.bit	[HL].bit	CY	\$addr16	None
A.bit						MOV1 BT BF BTCLR		SET1 CLR1
sfr.bit						MOV1 BT BF BTCLR		SET1 CLR1
saddr.bit						MOV1 BT BF BTCLR		SET1 CLR1
PSW.bit						MOV1 BT BF BTCLR		SET1 CLR1
[HL].bit						MOV1 BT BF BTCLR		SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1

(4) Call instructions/Branch instructions

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

2nd Operand 1st Operand	AX	!addr16	!addr11	[addr5]	\$addr16
Basic instruction	BR	CALL BR	CALLF	CALLT	BR BC BNC BZ BNZ
Compound instruction					BT BF BTCLR DBNZ

(5) Other instructions

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

★ 10. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Test Conditions		Ratings	Unit
Supply voltage	V _{DD}			−0.3 to +7.0	V
	AV _{DD}			−0.3 to V _{DD} + 0.3	V
	AV _{REF}			−0.3 to V _{DD} + 0.3	V
	AV _{SS}			−0.3 to +0.3	V
Input voltage	V _I			−0.3 to V _{DD} + 0.3	V
Output voltage	V _O			−0.3 to V _{DD} + 0.3	V
Analog input voltage	V _{AN}	P10-P17	Analog input pins	AV _{SS} − 0.3 to AV _{REF} + 0.3	V
Output current, high	I _{OH}	Per pin		−10	mA
		Total of P10-P17, P50-P54, P70-P72, P100, P101		−15	mA
		Total of P01-P03, P30-P37, P55-P57 −15		mA	
Output current, low	I _{OL} ^{Note}	Per pin	Peak value	30	mA
			r.m.s. value	15	mA
		Total of P50-P54	Peak value	100	mA
			r.m.s. value	70	mA
		Total of P55-P57	Peak value	100	mA
			r.m.s. value	70	mA
		Total of P10-P17, P70-P72, P100, P101	Peak value	50	mA
			r.m.s. value	20	mA
		Total of P01-P03, P30-P37	Peak value	50	mA
			r.m.s. value	20	mA
Operating ambient temperature	T _A			−40 to +85	°C
Storage temperature	T _{stg}			−65 to +150	°C

Note The r.m.s. value should be calculated as follows: [r.m.s. value] = [Peak value] × √Duty

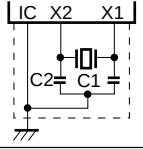
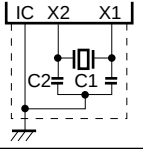
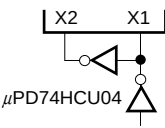
Caution If the absolute maximum rating of even one of the above parameters is exceeded, the quality of the product may be degraded. The absolute maximum ratings are therefore the rated values that may, if exceeded, physically damage the product. Be sure to use the product with all the absolute maximum ratings observed.

Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C _{IN}	f = 1 MHz, Unmeasured pins returned to 0 V.				15	pF
I/O capacitance	C _{IO}	f = 1 MHz, Unmeasured pins returned to 0 V.	P01-P03, P10-P17, P30-P37, P50-P57, P70-P72, P100, P101			15	pF

Remark Unless otherwise specified, shared pin characteristics are the same as port pin characteristics.

Main System Clock Oscillator Characteristics (T_A = -40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f _x) ^{Note 1}	V _{DD} = Oscillation voltage range	1.0		5.0	MHz
		Oscillation stabilization time ^{Note 2}	After V _{DD} came to MIN. of oscillation voltage range			4	ms
Crystal resonator		Oscillation frequency (f _x) ^{Note 1}		1.0		5.0	MHz
		Oscillation stabilization time ^{Note 2}	V _{DD} = 4.5 to 5.5 V			10 30	ms
External clock		X1 input frequency (f _x) ^{Note 1}		1.0		5.0	MHz
		X1 input high- and low-level widths (t _{xH} , t _{xL})		85		500	ns

Notes 1. Only the oscillator characteristics are shown. For the instruction execution time, refer to **AC Characteristics**.

2. Time required for oscillation to stabilize after a reset or the STOP mode has been released.

Caution When using the oscillation circuit of the main system clock, wire the portion enclosed in broken lines in the figures as follows to avoid adverse influences on the wiring capacitance:

- Keep the wiring length as short as possible.
- Do not cross the wiring over other signal lines.
- Do not route the wiring in the vicinity of lines through which a high fluctuating current flows.
- Always keep the ground point of the capacitor of the oscillation circuit at the same potential as V_{SS}.
- Do not connect the power source pattern through which a high current flows.
- Do not extract signals from the oscillation circuit.

DC Characteristics (T_A = -40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V _{IH1}	P10-P17, P30-P32, P35-P37, P50-P57, P71	V _{DD} = 2.7 to 5.5 V	0.7V _{DD}		V _{DD}	V
				0.8V _{DD}		V _{DD}	V
	V _{IH2}	P00-P03, P33, P34, P70, P72, P100, P101, $\overline{\text{RESET}}$	V _{DD} = 2.7 to 5.5 V	0.8V _{DD}		V _{DD}	V
				0.85V _{DD}		V _{DD}	V
	V _{IH3}	X1, X2	V _{DD} = 2.7 to 5.5 V	V _{DD} -0.5		V _{DD}	V
				V _{DD} -0.2		V _{DD}	V
Input voltage, low	V _{IL1}	P10-P17, P30-P32, P35-P37, P50-P57, P71	V _{DD} = 2.7 to 5.5 V	0		0.3V _{DD}	V
				0		0.2V _{DD}	V
	V _{IL2}	P00-P03, P33, P34, P70, P72, P100, P101, $\overline{\text{RESET}}$	V _{DD} = 2.7 to 5.5 V	0		0.2V _{DD}	V
				0		0.15V _{DD}	V
	V _{IL3}	X1, X2	V _{DD} = 2.7 to 5.5 V	0		0.4	V
				0		0.2	V
Output voltage, high	V _{OH}	V _{DD} = 4.5 to 5.5 V, I _{OH} = -1 mA		V _{DD} -1.0			V
		I _{OH} = -100 μA		V _{DD} -0.5			V
Output voltage, low	V _{OL}	P50-P57	V _{DD} = 2.0 to 4.5 V, I _{OL} = 10 mA			0.8	V
			V _{DD} = 4.5 to 5.5 V, I _{OL} = 15 mA		0.4	2.0	V
		P01-P03, P10-P17, P30-P37, P70-P72, P100, P101	V _{DD} = 4.5 to 5.5 V, I _{OL} = 1.6 mA			0.4	V
			I _{OL} = 400 μA			0.5	V
Input leak current, high	I _{LIH1}	V _{IN} = V _{DD}	P00-P03, P10-P17, P30-P37, P50-P57, P70-P72, P100, P101, $\overline{\text{RESET}}$			3	μA
	I _{LIH2}		X1, X2			20	μA
Input leak current, low	I _{LIL1}	V _{IN} = 0 V	P00-P03, P10-P17, P30-P37, P50-P57, P70-P72, P100, P101, $\overline{\text{RESET}}$			-3	μA
	I _{LIL2}		X1, X2			-20	μA
Output leak current, high	I _{LOH}	V _{OUT} = V _{DD}				3	μA
Output leak current, low	I _{LOL}	V _{OUT} = 0 V				-3	μA
Software pull-up resistor	R	V _{IN} = 0 V	P01-P03, P10-P17, P30-P37, P50-P57, P70-P72, P100, P101	15	40	90	kΩ

Remark Unless otherwise specified, shared pin characteristics are the same as port pin characteristics.

DC Characteristics (T_A = -40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Supply current ^{Note 1}	I _{DD1}	5.0-MHz crystal oscillation operating mode (f _{xx} = 2.5 MHz) ^{Note 2}	V _{DD} = 5.0 V ± 10% ^{Note 4}		4.5	13.5	mA
			V _{DD} = 3.0 V ± 10% ^{Note 5}		0.7	2.1	mA
			V _{DD} = 2.0 V ± 10% ^{Note 5}		0.4	1.2	mA
		5.0-MHz crystal oscillation operating mode (f _{xx} = 5.0 MHz) ^{Note 3}	V _{DD} = 5.0 V ± 10% ^{Note 4}		8.0	24.0	mA
			V _{DD} = 3.0 V ± 10% ^{Note 5}		0.9	2.7	mA
	I _{DD2}	5.0-MHz crystal oscillation HALT mode (f _{xx} = 2.5 MHz) ^{Note 2}	V _{DD} = 5.0 V ± 10%		1.4	4.2	mA
			V _{DD} = 3.0 V ± 10%		0.5	1.5	mA
			V _{DD} = 2.0 V ± 10%		280	840	μA
		5.0-MHz crystal oscillation HALT mode (f _{xx} = 5.0 MHz) ^{Note 3}	V _{DD} = 5.0 V ± 10%		1.6	4.8	mA
			V _{DD} = 3.0 V ± 10%		0.65	1.95	mA
	I _{DD3}	STOP mode	V _{DD} = 5.0 V ± 10%		0.1	30	μA
			V _{DD} = 3.0 V ± 10%		0.05	10	μA
			V _{DD} = 2.0 V ± 10%		0.05	10	μA

Notes 1. Not including AV_{REF}, AV_{DD} currents or port currents (including current flowing into internal pull-up resistors).

2. f_{xx} = f_x/2 operation (when oscillation mode selection register (OSMS) is set to 00H).

3. f_{xx} = f_x operation (when oscillation mode selection register (OSMS) is set to 01H).

4. High-speed mode operation (when processor clock control register (PCC) is set to 00H).

5. Low-speed mode operation (when processor clock control register (PCC) is set to 04H).

Remark f_{xx} : Main system clock frequency (f_x or f_x/2)

f_x : Main system clock oscillation frequency

AC Characteristics

(1) Basic Operation ($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = 1.8$ to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	$f_{XX} = f_X/2$ ^{Note1}	$V_{DD} = 2.7$ to 5.5 V	0.8		64	μs
				2.0		64	μs
		$f_{XX} = f_X$ ^{Note2}	$3.5 \text{ V} \leq V_{DD} \leq 5.5 \text{ V}$	0.4		32	μs
			$2.7 \text{ V} \leq V_{DD} < 3.5 \text{ V}$	0.8		32	μs
TI5, TI6 input frequency	f_{Ti}	$V_{DD} = 4.5$ to 5.5 V		0		4	MHz
				0		275	kHz
TI5, TI6 input high-/low-level widths	t_{TIH}	$V_{DD} = 4.5$ to 5.5 V		100			ns
	t_{TIL}			1.8			μs
Interrupt input high-/low-level widths	t_{INTH}	$V_{DD} = 2.7$ to 5.5 V		10			μs
	t_{INTL}			20			μs
RESET low-level width	t_{RSL}	$V_{DD} = 2.7$ to 5.5 V		10			μs
				20			μs

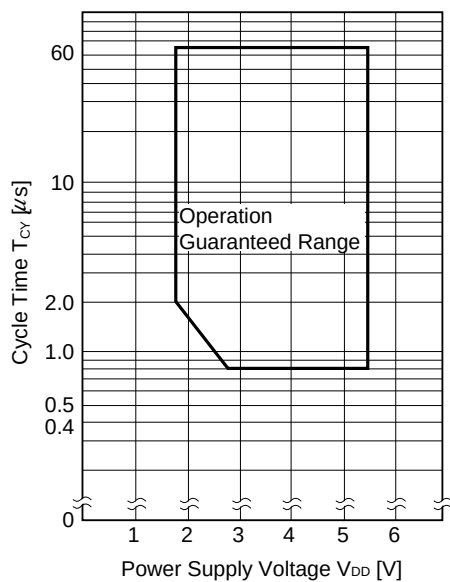
Notes 1. When oscillation mode selection register (OSMS) is set to 00H.

2. When OSMS is set to 01H.

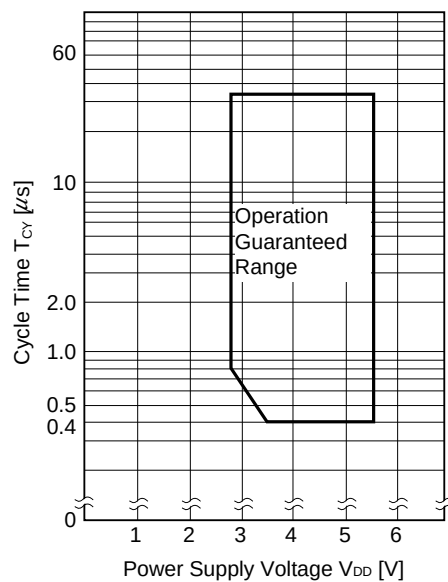
Remark f_{XX} : Main system clock frequency (f_X or $f_X/2$)

f_X : Main system clock oscillation frequency

T_{CY} vs V_{DD}
(Main System Clock $f_{XX} = f_X/2$ Operation)



T_{CY} vs V_{DD}
(Main System Clock $f_{XX} = f_X$ Operation)



(2) Serial Interface ($T_A = -40$ to $+85$ °C, $V_{DD} = 1.8$ to 5.5 V)(a) 3-wire serial I/O mode ($\overline{SCK2}$... Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK2}$ cycle time	t_{KCY1}	$4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	800			ns
		$2.7\text{ V} \leq V_{DD} < 4.5\text{ V}$	1600			ns
		$2.0\text{ V} \leq V_{DD} < 2.7\text{ V}$	3200			ns
			4800			ns
$\overline{SCK2}$ high/low-level width	t_{KH1}, t_{KL1}	$V_{DD} = 4.5$ to 5.5 V	$t_{KCY1}/2-50$			ns
			$t_{KCY1}/2-100$			ns
SI2 setup time (to $\overline{SCK2}\uparrow$)	t_{SIK1}	$4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	100			ns
		$2.7\text{ V} \leq V_{DD} < 4.5\text{ V}$	150			ns
		$2.0\text{ V} \leq V_{DD} < 2.7\text{ V}$	300			ns
			400			ns
SI2 hold time (from $\overline{SCK2}\uparrow$)	t_{KSI1}		400			ns
SO2 output delay time from $\overline{SCK2}\downarrow$	t_{KSO1}	$C = 100\text{ pF}$ Note			300	ns

Note C is the load capacitance of $\overline{SCK2}$, SO2 output line.

(b) 3-wire serial I/O mode ($\overline{SCK2}$... External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK2}$ cycle time	t_{KCY2}	$4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	800			ns
		$2.7\text{ V} \leq V_{DD} < 4.5\text{ V}$	1600			ns
		$2.0\text{ V} \leq V_{DD} < 2.7\text{ V}$	3200			ns
			4800			ns
$\overline{SCK2}$ high/low-level width	t_{KH2}, t_{KL2}	$4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	400			ns
		$2.7\text{ V} \leq V_{DD} < 4.5\text{ V}$	800			ns
		$2.0\text{ V} \leq V_{DD} < 2.7\text{ V}$	1600			ns
			2400			ns
SI2 setup time (to $\overline{SCK2}\uparrow$)	t_{SIK2}	$V_{DD} = 2.0$ to 5.5 V	100			ns
			150			ns
SI2 hold time (from $\overline{SCK2}\uparrow$)	t_{KSI2}		400			ns
SO2 output delay time from $\overline{SCK2}\downarrow$	t_{KSO2}	$C = 100\text{ pF}$ Note $V_{DD} = 2.0$ to 5.5 V			300	ns
					500	ns
$\overline{SCK2}$ rise/fall time	t_{R2}, t_{F2}				1000	ns

Note C is the load capacitance of SO2 output line.

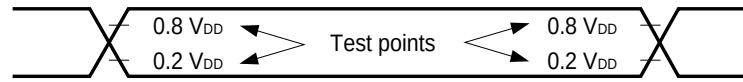
(c) UART mode (Dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		$4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			78125	bps
		$2.7\text{ V} \leq V_{DD} < 4.5\text{ V}$			39063	bps
		$2.0\text{ V} \leq V_{DD} < 2.7\text{ V}$			19531	bps
					9766	bps

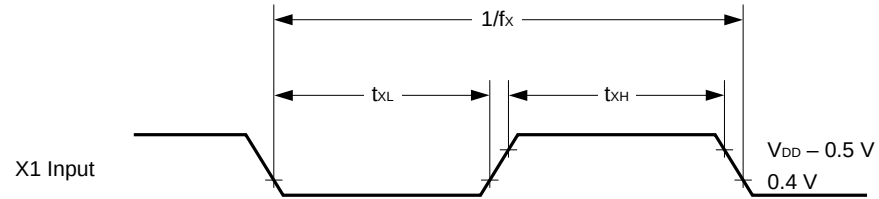
(d) UART mode (External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK cycle time	t_{KCY3}	$4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	800			ns
		$2.7\text{ V} \leq V_{DD} < 4.5\text{ V}$	1600			ns
		$2.0\text{ V} \leq V_{DD} < 2.7\text{ V}$	3200			ns
			4800			ns
ASCK high/low-level width	t_{KH3}, t_{KL3}	$4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	400			ns
		$2.7\text{ V} \leq V_{DD} < 4.5\text{ V}$	800			ns
		$2.0\text{ V} \leq V_{DD} < 2.7\text{ V}$	1600			ns
			2400			ns
Transfer rate		$4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			39063	bps
		$2.7\text{ V} \leq V_{DD} < 4.5\text{ V}$			19531	bps
		$2.0\text{ V} \leq V_{DD} < 2.7\text{ V}$			9766	bps
					6510	bps
ASCK rise/fall time	t_{R3}, t_{F3}				1000	ns

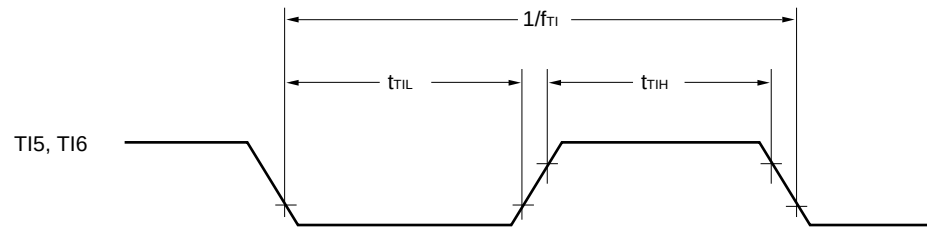
AC Timing Test Points (excluding X1 Input)



Clock Timing

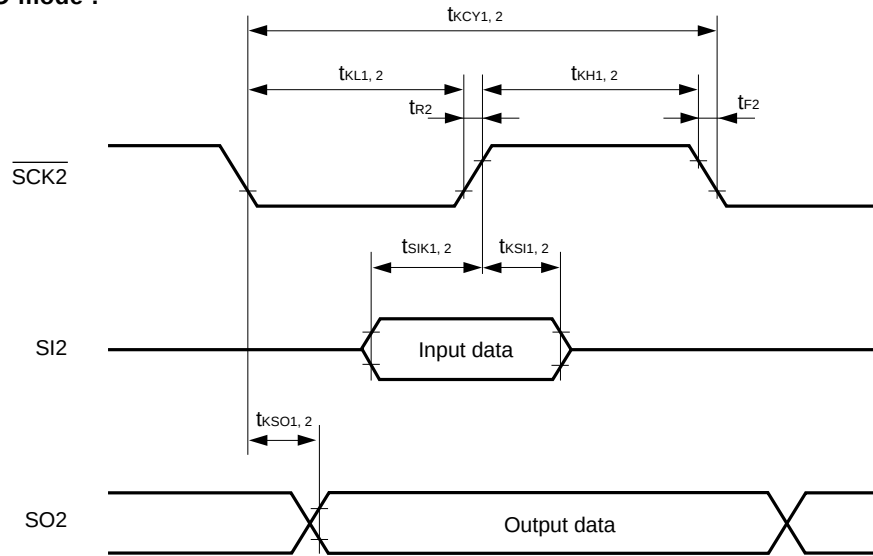


TI Timing

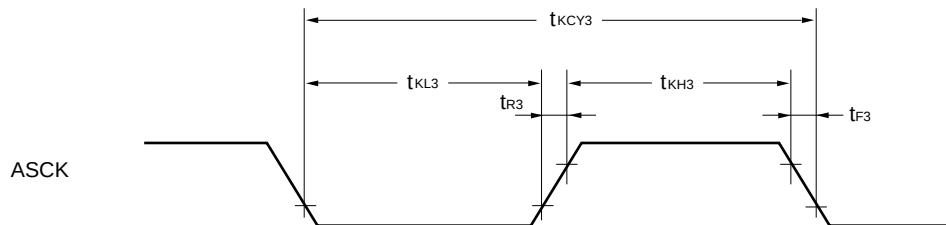


Serial Transfer Timing

3-wire serial I/O mode :



UART mode (external clock input) :



A/D CONVERTER CHARACTERISTICS ($T_A = -40$ to $+85$ °C, $\text{AV}_{\text{DD}} = \text{V}_{\text{DD}} = 1.8$ to 5.5 V, $\text{AV}_{\text{SS}} = \text{V}_{\text{SS}} = 0$ V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Overall error ^{Note}		$2.7 \text{ V} \leq \text{AV}_{\text{REF}} \leq \text{AV}_{\text{DD}}$			0.6	%
		$1.8 \text{ V} \leq \text{AV}_{\text{REF}} < 2.7 \text{ V}$			1.4	%
Conversion time	t_{CONV}	$2.0 \text{ V} \leq \text{AV}_{\text{DD}} \leq 5.5 \text{ V}$	19.1		200	μs
		$1.8 \text{ V} \leq \text{AV}_{\text{DD}} < 2.0 \text{ V}$	38.2		200	μs
Sampling time	t_{SAMP}		$12/f_{\text{xx}}$			μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF}	V
Reference voltage	AV_{REF}		1.8		AV_{DD}	V
Resistance between AV_{REF} and AV_{SS}	RA_{REF}		4	14		kΩ

Note Overall error excluding quantization error ($\pm 1/2$ LSB). It is indicated as a ratio to the full-scale value.

Remarks

1. f_{xx} : Main system clock frequency (f_x or $f_x/2$)
2. f_x : Main system clock oscillation frequency

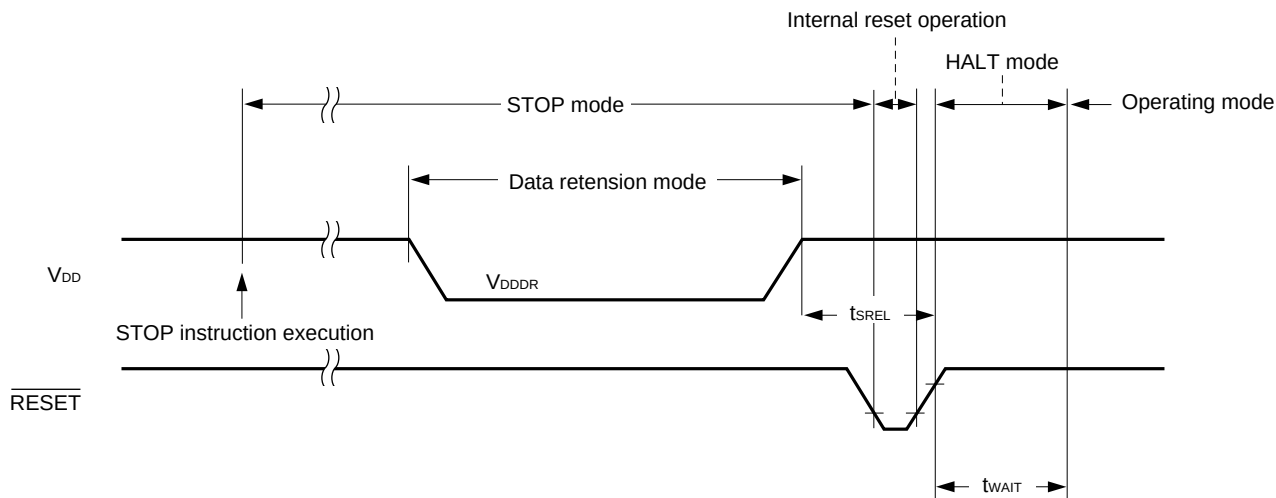
Data Memory Stop Mode Low Supply Voltage Data Retention Characteristics (TA = −40 to + 85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V _{DDDR}		1.8		5.5	V
Data retention power supply current	I _{DDDR}	V _{DDDR} = 1.8 V		0.1	10	μA
Release signal set time	t _{SREL}		0			μs
Oscillation stabilization wait time	t _{WAIT}	Release by $\overline{\text{RESET}}$		2 ¹⁷ /f _x		ms
		Release by interrupt		Note		ms

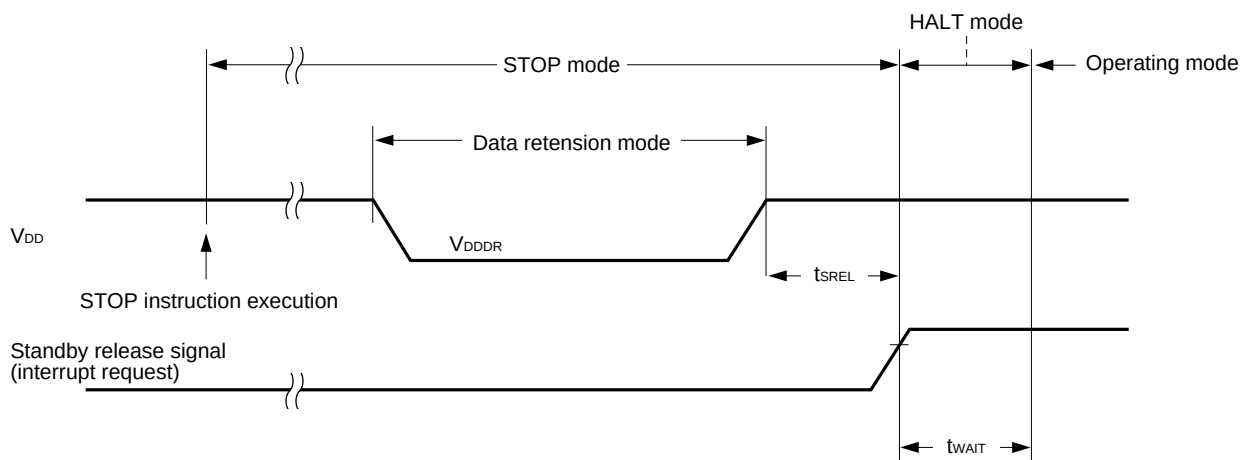
Note In combination with bits 0 to 2 (OSTS0 to OSTS2) of oscillation stabilization time select register (OSTS), selection of 2¹²/f_{xx} and 2¹⁴/f_{xx} to 2¹⁷/f_{xx} is possible.

Remark f_{xx} : Main system clock frequency (f_x or f_x/2)
f_x : Main system clock oscillation frequency

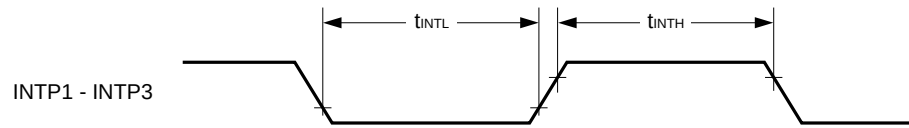
Data Retention Timing (STOP mode release by $\overline{\text{RESET}}$)



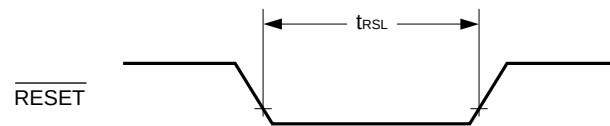
Data Retention Timing (Standby release signal: STOP mode release by interrupt signal)



Interrupt Input Timing

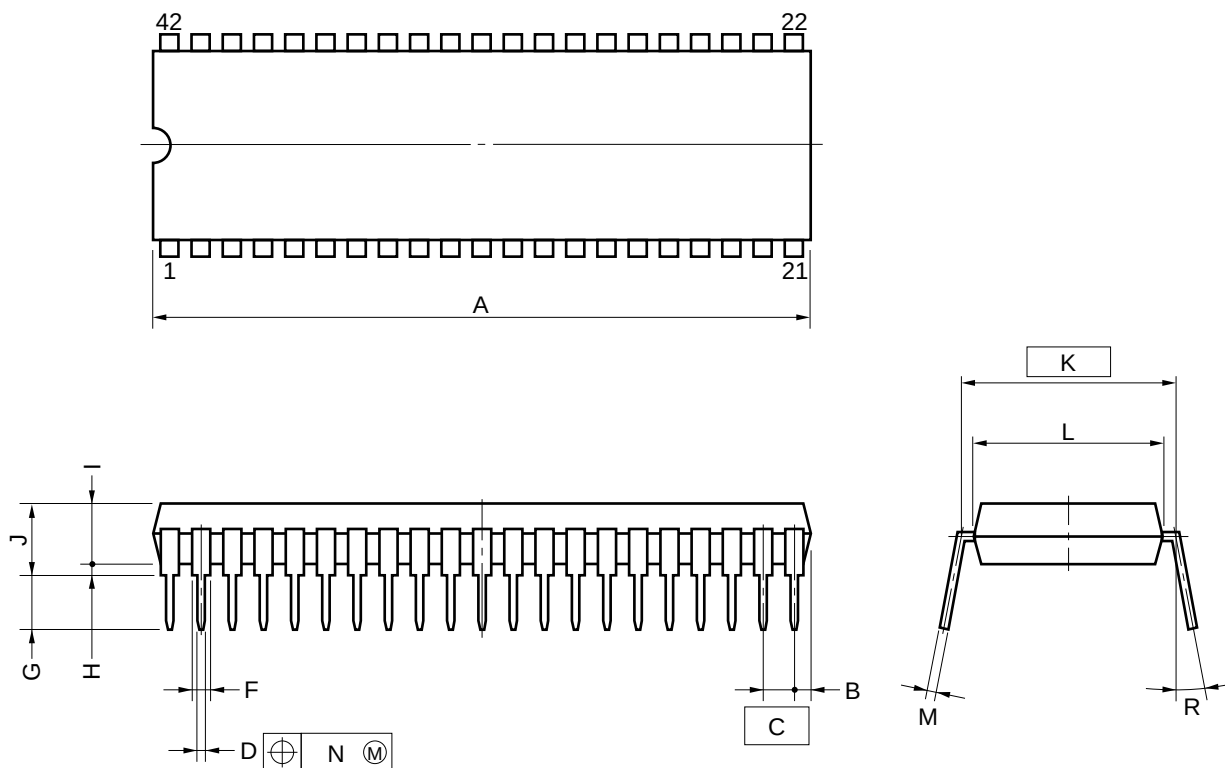


$\overline{\text{RESET}}$ Input Timing



11. PACKAGE DRAWINGS

42PIN PLASTIC SHRINK DIP (600 mil)



NOTES

- 1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.
- 2) Item "K" to center of leads when formed parallel.

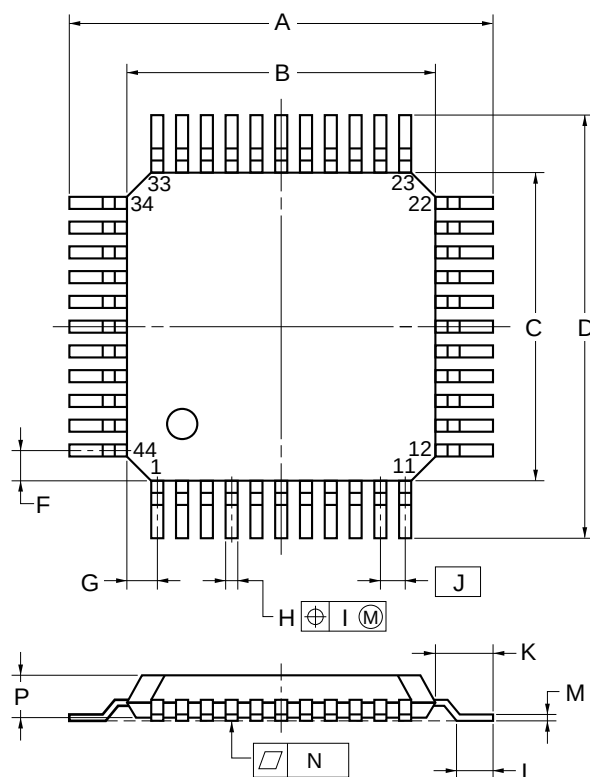
Remark The shape and material of the ES product is the same as the mass produced product.

ITEM	MILLIMETERS	INCHES
A	39.13 MAX.	1.541 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50±0.10	0.020 ^{+0.004} _{-0.005}
F	0.9 MIN.	0.035 MIN.
G	3.2±0.3	0.126±0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	15.24 (T.P.)	0.600 (T.P.)
L	13.2	0.520
M	0.25 ^{+0.10} _{-0.05}	0.010 ^{+0.004} _{-0.003}
N	0.17	0.007
R	0~15°	0~15°

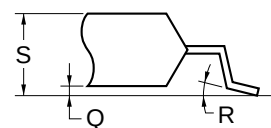
P42C-70-600A-1

μPD78081GB-xxx-3B4, 78082GB-xxx-3B4

44 PIN PLASTIC QFP (□10)



detail of lead end



NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

Remark The shape and material of the ES product is the same as the mass produced product.

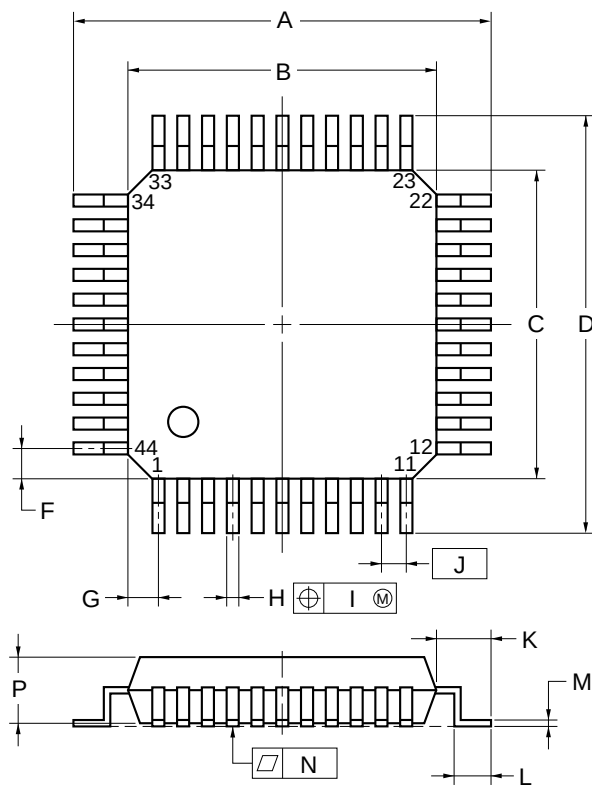
ITEM	MILLIMETERS	INCHES
A	13.6±0.4	0.535 ^{+0.017} _{-0.016}
B	10.0±0.2	0.394 ^{+0.008} _{-0.009}
C	10.0±0.2	0.394 ^{+0.008} _{-0.009}
D	13.6±0.4	0.535 ^{+0.017} _{-0.016}
F	1.0	0.039
G	1.0	0.039
H	0.35±0.10	0.014 ^{+0.004} _{-0.005}
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	0.071 ^{+0.008} _{-0.009}
L	0.8±0.2	0.031 ^{+0.009} _{-0.008}
M	0.15 ^{+0.10} _{-0.05}	0.006 ^{+0.004} _{-0.003}
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

P44GB-80-3B4-3

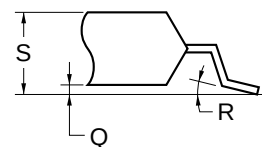
μPD78081GB-xxx-3BS-MTX, 78082GB-xxx-3BS-MTX



44 PIN PLASTIC QFP (□10)



detail of lead end



NOTE

Each lead centerline is located within 0.16 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

Remark The shape and material of the ES product is the same as the mass produced product.

ITEM	MILLIMETERS	INCHES
A	13.2±0.2	0.520 ^{+0.008} _{-0.009}
B	10.0±0.2	0.394 ^{+0.008} _{-0.009}
C	10.0±0.2	0.394 ^{+0.008} _{-0.009}
D	13.2±0.2	0.520 ^{+0.008} _{-0.009}
F	1.0	0.039
G	1.0	0.039
H	0.37 ^{+0.08} _{-0.07}	0.015 ^{+0.003} _{-0.004}
I	0.16	0.007
J	0.8 (T.P.)	0.031 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	0.031 ^{+0.009} _{-0.008}
M	0.17 ^{+0.06} _{-0.05}	0.007 ^{+0.002} _{-0.003}
N	0.10	0.004
P	2.7	0.106
Q	0.125±0.075	0.005±0.003
R	3° ^{+7°} _{-3°}	3° ^{+7°} _{-3°}
S	3.0 MAX.	0.119 MAX.

S44GB-80-3BS

★ 12. RECOMMENDED SOLDERING CONDITIONS

μPD78081 and 78082 should be soldered and mounted under the conditions recommended in the table below.

For detail of recommended soldering conditions, refer to the information document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, consult our sales personnel.

Table 12-1. Surface Mounting Type Soldering Conditions

μPD78081GB-XXX-3B4 : 44-pin plastic QFP (10 × 10 mm)

μPD78081GB-XXX-3BS-MTX : 44-pin plastic QFP (10 × 10 mm)

μPD78082GB-XXX-3B4 : 44-pin plastic QFP (10 × 10 mm)

μPD78082GB-XXX-3BS-MTX : 44-pin plastic QFP (10 × 10 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Duration: 30 sec. max. (at 210°C or above), Number of times: 3 times max.	IR35-00-3
VPS	Package peak temperature: 215°C, Duration: 40 sec. max. (at 200°C or above), Number of times: 3 times max.	VP15-00-3
Wave soldering	Soldering bath temperature: 260°C max., Duration: 10 sec. max., Number of times: once, Preheating temperature: 120°C max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C max. Duration: 3 sec. max. (per device side)	—

Caution Use of more than one soldering methods should be avoided (except in the case of partial heating).

Table 12-2. Hole-Through Type Soldering Conditions

μPD78081CU-XXX : 42-pin plastic shrink DIP (600 mil)

μPD78082CU-XXX : 42-pin plastic shrink DIP (600 mil)

Soldering Method	Soldering Conditions
Wave soldering (only pins)	Solder temperature: 260°C max., Duration: 10 sec. max.
Partial heating	Pin temperature: 300°C max., Duration: 3 sec. max. (per pin)

Caution Apply wave soldering only to the pins and be careful so as not to bring solder into direct contact with the package.

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available to support development of systems using the μPD78081, 78082.

Language Processing Software

RA78K/0 ^{Notes 1, 2, 3, 4}	Assembler package common to the 78K/0 series
CC78K/0 ^{Notes 1, 2, 3, 4}	C compiler package common to the 78K/0 series
DF78083 ^{Notes 1, 2, 3, 4}	Device file used for the μPD78083 subseries
CC78K/0-L ^{Notes 1, 2, 3, 4}	C compiler library source file common to the 78K/0 series

PROM Writing Tools

PG-1500	PROM programmer
PA-78P083CU PA-78P083GB	Programmer adapter connected to the PG-1500
PG-1500 Controller ^{Notes 1, 2}	Control program for the PG-1500

Debugging Tools

IE-78000-R	In-circuit emulator common to the 78K/0 series
IE-78000-R-A ^{Note 8}	In-circuit emulator common to the 78K/0 series (for integrated debugger)
IE-78000-R-BK	Break board common to the 78K/0 series
IE-78078-R-EM	Emulation board common to the μPD78078 subseries
EP-78083CU-R EP-78083GB-R	Emulation probe for the μPD78083 subseries
EV-9200G-44	Socket mounted on the target system board prepared for 44-pin plastic QFP
SM78K0 ^{Notes 5, 6, 7}	System simulator common to the 78K/0 series
ID78K0 ^{Notes 4, 5, 6, 7, 8}	Integrated debugger for IE-78000-R-A
SD78K/0 ^{Notes 1, 2}	Screen debugger for the IE-78000-R
DF78083 ^{Notes 1, 2, 5, 6, 7}	Device file used for the μPD78083 subseries

Notes 1. Based on PC-9800 series (MS-DOS™)

2. Based on IBM PC/AT™ and its compatibles (PC DOS™/IBM DOS™/MS-DOS)

3. Based on HP9000 series 300™ (HP-UX™)

4. Based on HP9000 series 700™ (HP-UX), SPARCstation™ (SunOS™), and EWS4800 series (EWS-UX/V)

5. Based on PC-9800 series (MS-DOS + Windows™)

6. Based on IBM PC/AT and its compatibles (PC DOS/IBM DOS/MS-DOS + Windows)

7. Based on NEWS™ (NEWS-OS™)

8. Under development

Remarks 1. Please refer to the **78K/0 Series Selection Guide (U11126E)** for information on the third party development tools.

2. Use the RA78K/0, CC78K/0, SM78K0, ID78K0, and SD78K/0 in combination with the DF78083.

Real-Time OS

MX78K0 ^{Notes 1, 2, 3, 4}	OS used for the 78K/0 series
------------------------------------	------------------------------

Fuzzy Inference Development Support System

FE9000 ^{Note 1} /FE9200 ^{Note 5}	Fuzzy knowledge data creating tool
FT9080 ^{Note 1} /FT9085 ^{Note 2}	Translator
FI78K0 ^{Notes 1, 2}	Fuzzy inference module
FD78K0 ^{Notes 1, 2}	Fuzzy inference debugger

Notes 1. Based on PC-9800 series (MS-DOS)

2. Based on IBM PC/AT and compatibles (PC DOS/IBM DOS/MS-DOS)

3. Based on HP9000 series 300 (HP-UX)

4. Based on HP9000 series 700 (HP-UX), SPARCstation (SunOS), and EWS4800 series (EWS-UX/V)

5. Based on IBM PC/AT (PC DOS/IBM DOS/MS-DOS + Windows)

Remark Please refer to the **78K/0 Series Selection Guide (U11126E)** for information on the third party development tools.

APPENDIX B. RELATED DOCUMENTS

Documents Related to Devices

Document	Document No.	
	Japanese	English
μPD78083 Subseries User's Manual	IEU-886	IEU-1407
78K/0 Series User's Manual-Instruction	IEU-849	IEU-1372
78K/0 Series Instruction Table	U10903J	—
78K/0 Series Instruction Set	U10904J	—
μPD78083 Subseries Special-Function Register Table	IEM-5599	—
78K/0 Series Application Note-Fundamental (III)	IEA-767	10182E

Documents on Development Tools (User's Manuals)

Document		Document No.	
		Japanese	English
RA78K Series Assembler Package	Operation	EEU-809	EEU-1399
	Language	EEU-815	EEU-1404
RA78K Series Structured Assembler Preprocessor		EEU-817	EEU-1402
CC78K Series C Compiler	Operation	EEU-656	EEU-1280
	Language	EEU-655	EEU-1284
CC78K/0 C Compiler Application Note	Programing Know-how	EEA-618	EEA-1208
CC78K Series Library Source File		EEU-777	—
PG-1500 PROM Programmer		EEU-651	EEU-1335
PG-1500 Controller PC-9800 Series (MS-DOS) Base		EEU-704	EEU-1291
PG-1500 Controller IBM PC Series (PC-DOS) Base		EEU-5008	U10540E
IE-78000-R		EEU-810	U11376E
IE-78000-R-A		U10057J	U10057E
IE-78000-R-BK		EEU-867	EEU-1427
IE-78078-R-EM		U10775J	EEU-1504
EP-78083		EEU-5003	EEU-1529
SM78K0 System Simulator	Reference	EEU-5002	U10181E
SM78K Series System Simulator	Third party's user open interface specifications	U10092J	U10092E
ID78K/0 Integrated Debugger	Reference	U11151J	—
SD78K/0 Screen Debugger	Introduction	EEU-852	—
PC-9800 Series (MS-DOS) Base	Reference	U10952J	—
SD78 K/0 Screen Debugger	Introduction	EEU-5024	EEU-1414
IBM PC/AT (PC DOS) Base	Reference	U11279J	EEU-1413

Caution The above documents are subject to change without notice. Be sure to use the latest documents for design or for any other similar purpose.

Documents on Embedded Software (User's Manuals)

Document		Document No.	
		Japanese	English
78K/0 Series OS MX78K0	Fundamental	EEU-5010	—
Fuzzy Knowledge Data Creation Tool		EEU-829	EEU-1438
78K/0, 78K/II, 87AD Series Fuzzy Inference Development Support System Translator		EEU-862	EEU-1444
78K/0 Series Fuzzy Inference Development Support System Fuzzy Inference Module		EEU-858	EEU-1441
78K/0 Series Fuzzy Inference Development Support System Fuzzy Inference Debugger		EEU-921	EEU-1458

Other Documents

Document		Document No.	
		Japanese	English
IC Package Manual		C10943X	
Semiconductor Device Mounting Technology Manual		C10535J	C10535E
Quality Grade on NEC Semiconductor Devices		IEI-620	IEI-1209
NEC Semiconductor Device Reliability/Quality Control System		C10983J	C10983E
Electrostatic Discharge (ESD) Test		MEM-539	—
Semiconductor Device Quality Assurance Guide		MEI-603	MEI-1202
Microcontroller-Related Product Guide – Third Party Products –		MEI-604	—

Caution The above documents are subject to change without notice. Be sure to use the latest documents for design or for any other similar purpose.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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