

Recent Additions

CD54AC109/3A
CD54ACT109/3A

HARRIS SEMICONDUCTOR

T-46-07-07

Dual "J-K" Flip-Flop with Set and Reset

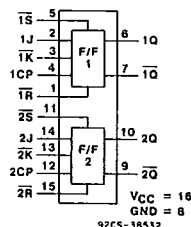
Positive-Edge-Triggered (J, $\bar{K}$)

The RCA CD54AC109 and CD54ACT109 are dual "J-K" flip-flops with set and reset that utilize the new RCA ADVANCED CMOS LOGIC technology. These flip-flops have independent J, $\bar{K}$, Set, Reset, and Clock inputs and Q and $\bar{Q}$ outputs. The CD54AC/ACT109 changes state on the positive-going transition of the clock. Set and Reset are accomplished asynchronously by low-level inputs.

The CD54AC109 and CD54ACT109 are supplied in 16-lead dual-in-line ceramic packages (F suffix).

Package Specifications

(See Section 11, Fig. 11)



FUNCTIONAL DIAGRAM

Static Electrical Characteristics (Limits with black dots (•) are tested 100%.)

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
				+25		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	
Quiescent Supply Current (FF) I_{CC}	V_{CC} or GND	0	5.5	—	4•	—	80•	μA

The complete static electrical test specification consists of the above by-type static tests combined with the standard static tests in the beginning of this section.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
J, CP, $\bar{C}P$	1
$\bar{K}$	0.53
$\bar{S}$, $\bar{R}$	0.58

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

Burn-In Test-Circuit Connections

Identical to CD54HC/HCT109/3A, page 5-43.

HARRIS SEMICONDUCTOR

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CD54AC109/3A

CD54ACT109/3A

SWITCHING CHARACTERISTICS: AC Series; $t_r, t_f = 3 \text{ ns}$, $C_L = 50 \text{ pF}$ (Worst Case)

CHARACTERISTICS	SYMBOL	V_{CC} (V)	-55 to +125°C		UNITS
			MIN.	MAX.	
Propagation Delays: CP ($\overline{CP}$) to Q, $\overline{Q}$	t_{PLH}	1.5	—	129	ns
	t_{PHL}	3.3*	2.7	14.4	
		5†	1.7	10.3*	
$\overline{S}, \overline{R}$ to Q, $\overline{Q}$	t_{PLH}	1.5	—	153	ns
	t_{PHL}	3.3	3.2	17.1	
		5	2.1	12.2*	
Power Dissipation Capacitance	$C_{PD\&}$	—			pF
Input Capacitance	C_i	—	—	10	pF

SWITCHING CHARACTERISTICS: ACT Series; $t_r, t_f = 3 \text{ ns}$, $C_L = 50 \text{ pF}$ (Worst Case)

CHARACTERISTICS	SYMBOL	V_{CC} (V)	-55 to +125°C		UNITS
			MIN.	MAX.	
Propagation Delays: CP ($\overline{CP}$) to Q, $\overline{Q}$	t_{PLH}	5†	1.7	10.3*	ns
	t_{PHL}	5	2.3	13.5*	
Power Dissipation Capacitance	$C_{PD\&}$	—			pF
Input Capacitance	C_i	—	—	10	pF

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*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

(Limits with black dots (•) are tested 100%.)

§ $C_{PD\&}$ is used to determine the dynamic power consumption per flip-flop.For AC, $P_D = C_{PD\&} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$

For ACT, $P_D = C_{PD\&} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o) + V_{CC} \Delta I_{CC}$ where
 f_i = input frequency
 f_o = output frequency
 C_L = output load capacitance
 V_{CC} = supply voltage

CD54AC112/3A

CD54ACT112/3A

Dual "J-K" Flip-Flop with Set and Reset

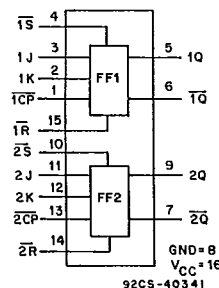
Negative-Edge-Triggered (J, K)

The RCA CD54AC112 and CD54ACT112 are dual "J-K" flip-flops with set and reset that utilize the new RCA ADVANCED CMOS LOGIC technology. These flip-flops have independent J, K, $\overline{Set}$, $\overline{Reset}$, and Clock inputs and Q and $\overline{Q}$ outputs. The CD54AC/ACT112 changes state on the negative-going transition of the clock pulse. Set and Reset are accomplished asynchronously by low-level inputs.

The CD54AC112 and CD54ACT112 are supplied in 16-lead dual-in-line ceramic packages (F suffix).

Package Specifications

(See Section 11, Fig. 11)



FUNCTIONAL DIAGRAM