

Data sheet acquired from Harris Semiconductor SCHS237B

September 1998 - Revised May 2002

# **Dual 4-Input Multiplexer**

### **Features**

- Buffered Inputs
- Typical Propagation Delay
  - 6.3ns at  $V_{CC} = 5V$ ,  $T_A = 25^{\circ}C$ ,  $C_L = 50pF$
- Exceeds 2kV ESD Protection MIL-STD-883, Method 3015
- SCR-Latchup-Resistant CMOS Process and Circuit Design
- Speed of Bipolar FAST™/AS/S with Significantly Reduced Power Consumption
- Balanced Propagation Delays
- AC Types Feature 1.5V to 5.5V Operation and Balanced Noise Immunity at 30% of the Supply
- ±24mA Output Drive Current
  - Fanout to 15 FAST™ ICs
  - Drives 50 $\Omega$  Transmission Lines

## Description

The 'AC153 and 'ACT153 are dual 4-input multiplexers that utilize Advanced CMOS Logic technology. One of the four sources for each section is selected by the common Select inputs, S0 and S1. When the Enable inputs  $(\overline{1E}, \overline{2E})$  are HIGH, the outputs are in the low state.

### **Ordering Information**

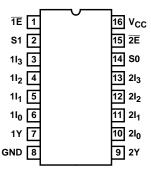
PART NUMBER	TEMP. RANGE ( <sup>O</sup> C)	PACKAGE
CD54AC153F3A	-55 to 125	16 Ld CERDIP
CD74AC153E	0 to 70°C, -40 to 85	16 Ld PDIP
CD74AC153M96	0 to 70°C, -40 to 85	16 Ld SOIC
CD54ACT153F3A	-55 to 125	16 Ld CERDIP
CD74ACT153E	0 to 70°C, -40 to 85	16 Ld PDIP
CD74ACT153M	0 to 70°C, -40 to 85	16 Ld SOIC

#### NOTES:

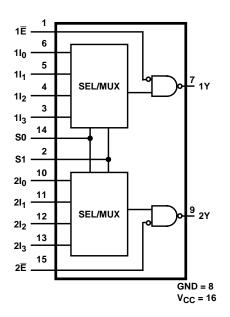
- 1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
- Wafer and die for this part number is available which meets all electrical specifications. Please contact your local TI sales office or customer service for ordering information.

#### **Pinout**

CD54AC153, CD54ACT153 (CERDIP) CD74AC153, CD74ACT153 (PDIP, SOIC) TOP VIEW



# Functional Diagram



TRUTH TABLE

SELECT	INPUTS	DATA INPUTS				ENABLE INPUTS	OUTPUT
<b>S</b> 1	S0	nl <sub>0</sub>	nl <sub>1</sub>	nl <sub>2</sub>	nl <sub>3</sub>	nE	nY
Х	Х	Х	Х	Х	Х	Н	L
L	L	L	Х	Х	Х	L	L
L	L	Н	Х	Х	Х	L	Н
L	Н	Х	L	Х	Х	L	L
L	Н	Х	Н	Х	Х	L	Н
Н	L	Х	Х	L	Х	L	L
Н	L	Х	Х	Н	Х	L	Н
Н	Н	Х	Х	Х	L	L	L
Н	Н	Х	Х	Х	Н	L	Н

Select inputs S1 and S0 are common to both sections. H = High Level, L = Low Level, X = Don't Care, Z = High Impedance.

### **Absolute Maximum Ratings**

DC Supply Voltage, V <sub>CC</sub> 0.5V to 6V
DC Input Diode Current, I <sub>IK</sub>
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$
DC Output Diode Current, I <sub>OK</sub>
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$
DC Output Source or Sink Current per Output Pin, IO
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$
DC $V_{CC}$ or Ground Current, $I_{CC}$ or $I_{GND}$ (Note 3) $\pm 100 \text{mA}$

#### **Thermal Information**

Thermal Resistance (Typical, Note 5)	$\theta_{JA}$ (oC/W)
PDIP Package	90
SOIC Package	160
Maximum Junction Temperature (Plastic Package)	150 <sup>0</sup> C
Maximum Storage Temperature Range	65°C to 150°C
Maximum Lead Temperature (Soldering 10s)	300°C

### **Operating Conditions**

· · · · · ·
Temperature Range, T <sub>A</sub> :
CD5455°C to 125°C
CD740°C to 70°C and -40°C to 85°C
Supply Voltage Range, V <sub>CC</sub> (Note 4)
AC Types1.5V to 5.5V
ACT Types
DC Input or Output Voltage, $V_I$ , $V_O$ 0V to $V_{CC}$
Input Rise and Fall Slew Rate, dt/dv
AC Types, 1.5V to 3V 50ns (Max)
AC Types, 3.6V to 5.5V 20ns (Max)
ACT Types, 4.5V to 5.5V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

#### NOTES:

- 3. For up to 4 outputs per device, add  $\pm 25 \text{mA}$  for each additional output.
- 4. Unless otherwise specified, all voltages are referenced to ground.
- 5.  $\theta_{\mbox{\scriptsize JA}}$  is measured with the component mounted on an evaluation PC board in free air.

### **DC Electrical Specifications**

			TEST CONDITIONS V <sub>CC</sub>		V <sub>CC</sub> 25°C		V <sub>CC</sub> 25°C -40°C 85°C				C TO 5°C	
PARAMETER	SYMBOL	V <sub>I</sub> (V)	I <sub>O</sub> (mA)	(V)	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	
AC TYPES					-		-					
High Level Input Voltage	V <sub>IH</sub>	-	-	1.5	1.2	-	1.2	-	1.2	-	V	
				3	2.1	-	2.1	-	2.1	-	V	
				5.5	3.85	-	3.85	-	3.85	-	V	
Low Level Input Voltage	V <sub>IL</sub>	-	-	1.5	-	0.3	-	0.3	-	0.3	V	
				3	-	0.9	-	0.9	-	0.9	V	
				5.5	-	1.65	-	1.65	-	1.65	V	
High Level Output Voltage	Voн	V <sub>IH</sub> or V <sub>IL</sub>	-0.05	1.5	1.4	-	1.4	-	1.4	-	V	
			-0.05	3	2.9	-	2.9	-	2.9	-	V	
			-0.05	4.5	4.4	-	4.4	-	4.4	-	V	
			-4	3	2.58	-	2.48	-	2.4	-	V	
			-24	4.5	3.94	-	3.8	-	3.7	-	V	
			-75 (Note 6, 7)	5.5	-	-	3.85	-	-	-	V	
			-50 (Note 6, 7)	5.5	-	-	-	-	3.85	-	V	

### DC Electrical Specifications (Continued)

		1	ST ITIONS	v <sub>cc</sub>	25°C		-40°C T0 85°C				
PARAMETER	SYMBOL	V <sub>I</sub> (V)	I <sub>O</sub> (mA)	(v)	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
Low Level Output Voltage	$V_{OL}$	V <sub>IH</sub> or V <sub>IL</sub>	0.05	1.5	-	0.1	-	0.1	-	0.1	V
			0.05	3	-	0.1	-	0.1	-	0.1	V
			0.05	4.5	-	0.1	-	0.1	-	0.1	V
			12	3	-	0.36	-	0.44	-	0.5	V
			24	4.5	-	0.36	-	0.44	-	0.5	V
			75 (Note 6, 7)	5.5	-	-	-	1.65	-	-	V
			50 (Note 6, 7)	5.5	-	-	-	-	-	1.65	V
Input Leakage Current	lį	V <sub>CC</sub> or GND	-	5.5	-	±0.1	-	±1	-	±1	μА
Quiescent Supply Current MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	-	8	-	80	-	160	μА
ACT TYPES											
High Level Input Voltage	V <sub>IH</sub>	-	-	4.5 to 5.5	2	-	2	-	2	-	V
Low Level Input Voltage	V <sub>IL</sub>	-	-	4.5 to 5.5	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage	Voн	V <sub>IH</sub> or V <sub>IL</sub>	-0.05	4.5	4.4	-	4.4	-	4.4	-	V
			-24	4.5	3.94	-	3.8	-	3.7	-	V
			-75 (Note 6, 7)	5.5	-	-	3.85	-	-	-	V
			-50 (Note 6, 7)	5.5	-	-	-	-	3.85	-	V
Low Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.05	4.5	-	0.1	-	0.1	-	0.1	V
			24	4.5	-	0.36	-	0.44	-	0.5	V
			75 (Note 6, 7)	5.5	-	-	-	1.65	-	-	V
			50 (Note 6, 7)	5.5	-	-	-	-	-	1.65	V
Input Leakage Current	lį	V <sub>CC</sub> or GND	-	5.5	-	±0.1	-	±1	-	±1	μΑ
Quiescent Supply Current MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	-	8	-	80	-	160	μΑ
Additional Supply Current per Input Pin TTL Inputs High 1 Unit Load	Δl <sub>CC</sub>	V <sub>CC</sub> -2.1	-	4.5 to 5.5	-	2.4	-	2.8	-	3	mA

#### NOTES:

- 6. Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
- 7. Test verifies a minimum  $50\Omega$  transmission-line-drive capability at  $85^{o}C$ ,  $75\Omega$  at  $125^{o}C$ .

### **ACT Input Load Table**

INPUT	UNIT LOAD
S0, S1, nl0, nl1	1
nE	0.47

NOTE: Unit load is  $\Delta I_{CC}$  limit specified in DC Electrical Specifications Table, e.g., 2.4mA max at 25°C.

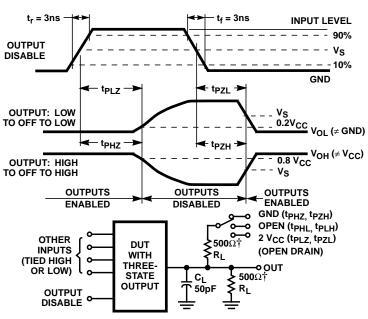
# **Switching Specifications** Input $t_r$ , $t_f$ = 3ns, $C_L$ = 50pF (Worst Case)

			-40 <sup>c</sup>	-40°C TO 85°C		-55	°C TO 12	5°C	
PARAMETER	SYMBOL	V <sub>CC</sub> (V)	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
AC TYPES									
Propagation Delay, S0, S1, to Y	t <sub>PLH</sub> , t <sub>PHL</sub>	1.5	-	-	227	-	-	250	ns
		3.3 (Note 9)	7.2	-	25.5	7	-	28	ns
		5 (Note 10)	5.2	-	18.2	5	-	20	ns
Propagation Delay, nl to Y	t <sub>PLH</sub> , t <sub>PHL</sub>	1.5	-	-	151	-	-	166	ns
		3.3	4.8	-	16.9	4.7	-	18.6	ns
		5	3.4	-	12.1	3.3	-	13.3	ns
Propagation Delay, nE to Y	t <sub>PLH</sub> , t <sub>PHL</sub>	1.5	-	-	134	-	-	148	ns
		3.3	4.3	-	15	4.1	-	16.5	ns
		5	3.1	-	10.7	3	-	11.8	ns
Input Capacitance	Cl	-	-	-	10	-	-	10	pF
Power Dissipation Capacitance	C <sub>PD</sub> (Note 11)	-	-	93	-	-	93	-	pF
ACT TYPES				•			•	•	
Propagation Delay, S0, S1, to Y	t <sub>PLH</sub> , t <sub>PHL</sub>	5 (Note 10)	5.7	-	20	5.5	-	22	ns
Propagation Delay, nl to Y	t <sub>PLH</sub> , t <sub>PHL</sub>	5	4.6	-	16.4	4.5	-	18	ns
Propagation Delay, nE to Y	t <sub>PLH</sub> , t <sub>PHL</sub>	5	3.2	-	11.5	3.2	-	12.6	ns
Input Capacitance	Cl	-	-	-	10	-	-	10	pF
Power Dissipation Capacitance	C <sub>PD</sub> (Note 11)	-	-	93	-	-	93	-	pF

#### NOTES:

- 8. Limits tested at 100%.
- 9. 3.3V Min at 3.6V, Max at 3V.
- 10. 5V Min at 5.5V, Max at 4.5V.

11.  $C_{PD}$  is used to determine the dynamic power consumption per multiplexer. AC:  $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ ACT:  $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$  where  $f_i$  = input frequency,  $C_L$  = output load capacitance,  $V_{CC}$  = supply voltage.



†FOR AC SERIES ONLY: WHEN V $_{\text{CC}}$  = 1.5V,  $R_{\text{L}}$  = 1k $\Omega$ 

FIGURE 1. THREE-STATE PROPAGATION DELAY WAVEFORMS AND TEST CIRCUIT

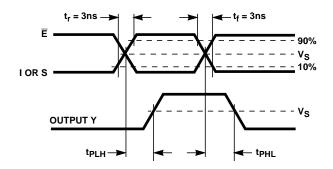
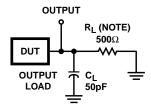


FIGURE 2. PROPAGATION DELAY TIMES AND TEST CIRCUIT



NOTE: For AC Series Only: When  $V_{CC}$  = 1.5V,  $R_L$  = 1k $\Omega$ .

	AC	ACT
Input Level	V <sub>CC</sub>	3V
Input Switching Voltage, V <sub>S</sub>	0.5 V <sub>CC</sub>	1.5V
Output Switching Voltage, V <sub>S</sub>	0.5 V <sub>CC</sub>	0.5 V <sub>CC</sub>

FIGURE 3. PROPAGATION DELAY TIMES

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