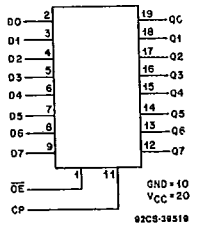
CD54AC574/3A
CD54ACT574/3A

Octal D-Type Flip-Flop, 3-State Positive-Edge-Triggered, Non-Inverting

T-46-07-11

The RCA CD54AC574/3A and CD54ACT574/3A are octal D-type, 3-state, positive-edge-triggered flip-flops that utilize the new RCA ADVANCED CMOS LOGIC technology. The eight flip-flops enter data into their registers on the LOW-to-HIGH transition of the clock (CP). The Output Enable ($\overline{OE}$) controls the 3-state outputs and is independent of the register operation. When the Output Enable ($\overline{OE}$) is HIGH, the outputs are in the high-impedance state. The CD54AC/ACT574/3A outputs are non-inverted.

The CD54AC574/3A and CD54ACT574/3A are supplied in 20-lead dual-in-line ceramic packages (F suffix).



FUNCTIONAL DIAGRAM & TERMINAL ASSIGNMENT

Package Specifications
See Section 11, Fig. 13

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Static Electrical Characteristics (Limits with black dots (•) are tested 100%.)

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
				+25		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	
3-State Leakage Current I_{OZ}	V_{IH} or V_{IL} V_O = V_{CC} or GND		5.5	—	±0.5•	—	±10•	μA
Quiescent Supply Current (MSI) I_{CC}	V_{CC} or GND	0	5.5	—	8•	—	160•	μA

The complete static electrical test specification consists of the above by-type static tests combined with the standard static tests in the beginning of this section.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
D, $\overline{OE}$	0.7
CP	1.17

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

Burn-In Test-Circuit Connections (Use Static II for /3A burn-in and Dynamic for Life Test.)

Static	STATIC BURN-IN I			STATIC BURN-IN II		
	OPEN	GROUND	V_{CC} (6V)	OPEN	GROUND	V_{CC} (6V)
CD54AC/ACT574	12-19	1-11	20	12-19	10	1-9,11,20
Dynamic	OPEN	GROUND	1/2 V_{CC} (3V)	V_{CC} (6V)	OSCILLATOR 50 kHz	OSCILLATOR 25 kHz
CD54AC/ACT574	—	1,10	12-19	20	11	2-9

NOTE: Each pin except V_{CC} and Gnd will have a resistor of 2k-47k ohms.

CD54AC574/3A
CD54ACT574/3A

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF (Limits with black dots (•) are tested 100%.)

CHARACTERISTICS	SYMBOL	V_{CC} (V)	-55 to +125°C		UNITS
			MIN.	MAX.	
Propagation Delays: Clock to Q	t_{PLH} t_{PHL}	1.5 3.3* 5†	— 4.5 3.2	135 15.1 10.8	ns
Output Enable	t_{PZL} t_{PZH}	1.5 3.3 5	— 6.5 4.4	181 21.8 14.5•	ns
Disable Time	t_{PLZ} t_{PHZ}	1.5 3.3 5	— 5.4 4.4	181 18.1 14.5•	ns
Power Dissipation Capacitance	C_{PD}§	—	60 Typ.		pF
Min. (Valley) V_{OH} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV}	5	4 Typ. @ 25°C		V
Max. (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP}	5	1 Typ. @ 25°C		V
Input Capacitance	C_I	—	—	10	pF
3-State Output Capacitance	C_O	—	—	15	pF

SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF (Limits with black dots (•) are tested 100%.)

CHARACTERISTICS	SYMBOL	V_{CC} (V)	-55 to +125°C		UNITS
			MIN.	MAX.	
Propagation Delays Clock to Q	t_{PLH} t_{PHL}	5†	3.4	11.2•	ns
Output Enable and Disable to Q	t_{PLZ} t_{PHZ} t_{PZL} t_{PZH}	5	4.4	14.5•	ns
Power Dissipation Capacitance	C_{PD}§	—	72 Typ.		pF
Min. (Valley) V_{OH} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV}	5	4 Typ. @ 25°C		V
Max. (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP}	5	1 Typ. @ 25°C		V
Input Capacitance	C_I	—	—	10	pF
3-State Output Capacitance	C_O	—	—	15	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption per flip-flop.
For AC, $P_D = C_{PD} V_{CC}^2 f_i + \Sigma V_{CC}^2 f_o C_L$
For ACT, $P_D = C_{PD} V_{CC}^2 f_i + \Sigma V_{CC}^2 f_o C_L + V_{CC} \Delta I_{CC}$ where f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage