PRELIMINARY PRODUCT INFORMATION

NEC

MOS INTEGRATED CIRCUIT

μPD78P0018Y

8-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μPD78P0018Y is a member of the μPD780018Y subseries of the 78K/0 series products, in which the internal mask ROM of the μPD780018Y is replaced with a one-time PROM or EPROM.

Because this device can be programmed by users, it is ideally suited for applications involving the evaluation of systems in development stages, small-scale productions of many different products, and rapid development and time-to-market of a new product.

Caution The μPD78P0018YKL-T is not disigned to guarantee the reliability required for use in mass-production. Please use it only for performance evaluation during testing and test production runs.

The details of functions are described in the user's manuals. Be sure to read the following manuals before designing.

μPD780018, 780018Y Subseries User's Manual: Planned
78K/0 Series User's Manual: Instructions : IEU-1372

FEATURES

- Pin-compatible with mask ROM version (except V_{PP} pin)
- Internal PROM: 60 Kbytes [Note]
  - μPD78P0018YKL-T: Reprogrammable (ideally suited for system evaluation)
  - μPD78P0018YGF: One-time programmable (ideally suited for small-scale production)
- Internal high-speed RAM: 1024 bytes
- Internal expansion RAM: 1024 bytes
- Buffer RAM : 32 bytes
- Operable in the same supply voltage range as the mask ROM version (V_{DD} = 2.7 to 5.5 V)

Note The internal PROM capacity can be changed by setting the internal memory size switching register (IMS).

Remark Refer to **1. DIFFERENCES BETWEEN THE μPD78P0018Y AND MASK ROM VERSIONS** for the differences between PROM versions and mask ROM versions.

In this document, “PROM” is used in parts common to one-time PROM versions and EPROM versions.

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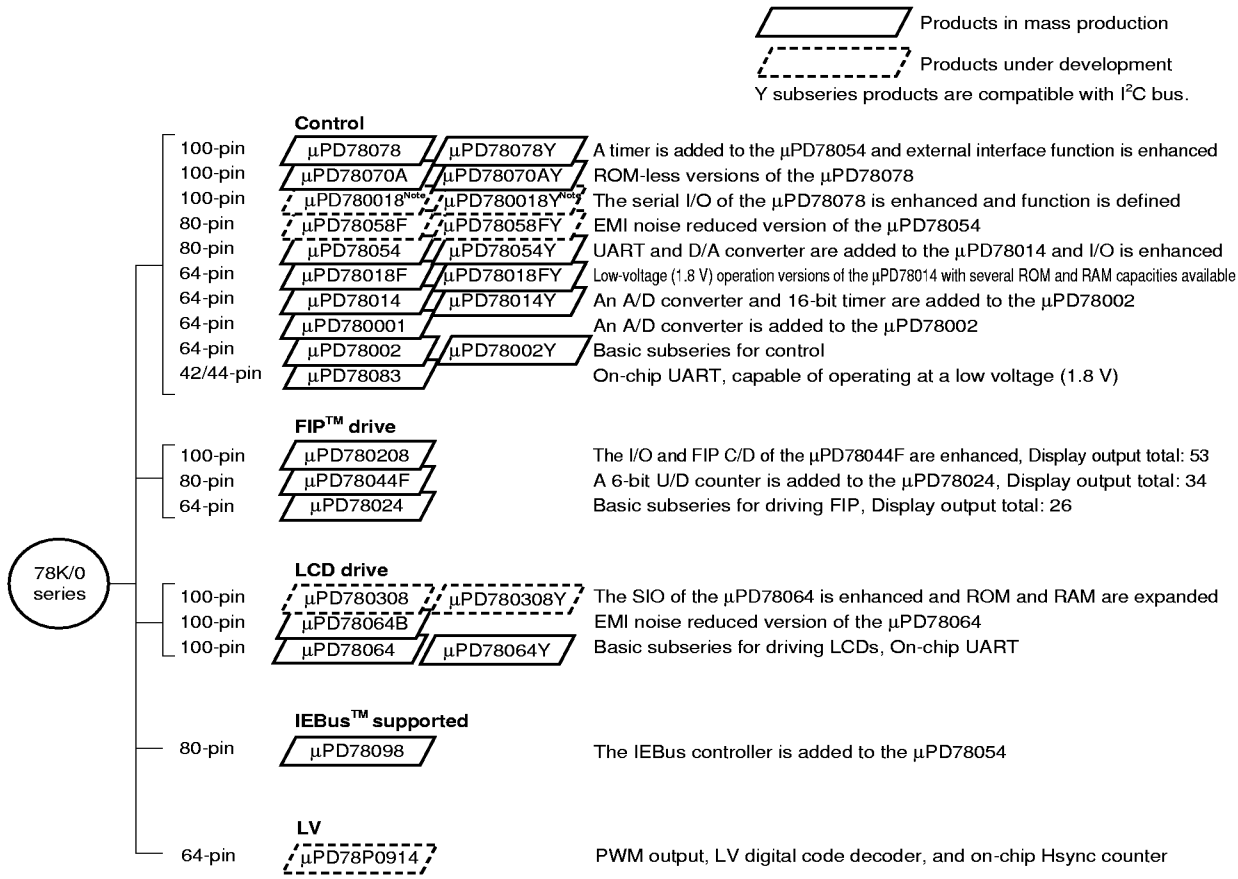
ORDERING INFORMATION

Part Number	Package	Internal ROM	Quality Grades
μPD78P0018YGF-3BA	100-pin plastic QFP (14 × 20 mm)	One-Time PROM	Standard
μPD78P0018YKL-T	100-pin ceramic WQFN	EPROM	Not Applied (only for performance evaluation)

Please refer to "**Quality Grades on NEC Semiconductor Devices**" **(Document number C11531E)** published by NEC Corporation to know the specification of quality grade on the devices and its recommended applicaions.

78K/0 Series Development



The following table lists the main functional differences between subseries products.

Subseries name \ Function		ROM capacity	Timer				8-bit A/D	8-bit D/A	Serial interface	I/O	V_{DD} MIN. value	External expansion
			8-bit	16-bit	Watch	WDT						
Control	μPD78078	32 K-60 K	4ch	1ch	1ch	1ch	8ch	2ch	3ch (UART : 1ch)	88	1.8 V	Available
	μPD78070A	–								61	2.7 V	
	μPD780018	48 K-60 K						–	2ch	88		
	μPD78058F	48 K-60 K	2ch					2ch	3ch (UART : 1ch)	69		
	μPD78054	16 K-60 K									2.0 V	
	μPD78018F	8 K-60 K						–	2ch	53	1.8 V	
	μPD78014	8 K-32 K									2.7 V	
	μPD780001	8 K		–	–				1ch	39		–
	μPD78002	8 K-16 K			1ch		–			53		Available
	μPD78083				–		8ch		1ch (UART : 1ch)	33	1.8 V	–
FIP driving	μPD780208	32 K-60 K	2ch	1ch	1ch	1ch	8ch	–	2ch	74	2.7 V	–
	μPD78044F	16 K-40 K								68		
	μPD78024	24 K-32 K								54		
LCD driving	μPD780308	48 K-60 K	2ch	1ch	1ch	1ch	8ch	–	3ch (UART : 1ch)	57	1.8 V	–
	μPD78064B	32 K							2ch (UART : 1ch)		2.0 V	
	μPD78064	16 K-32 K										
IEBus supported	μPD78098	32 K-60 K	2ch	1ch	1ch	1ch	8ch	2ch	3ch (UART : 1ch)	69	2.7 V	Available
LV	μPD78P0914	32 K	6ch	–	–	1ch	8ch	–	2ch	54	4.5 V	Available

FUNCTION DESCRIPTION

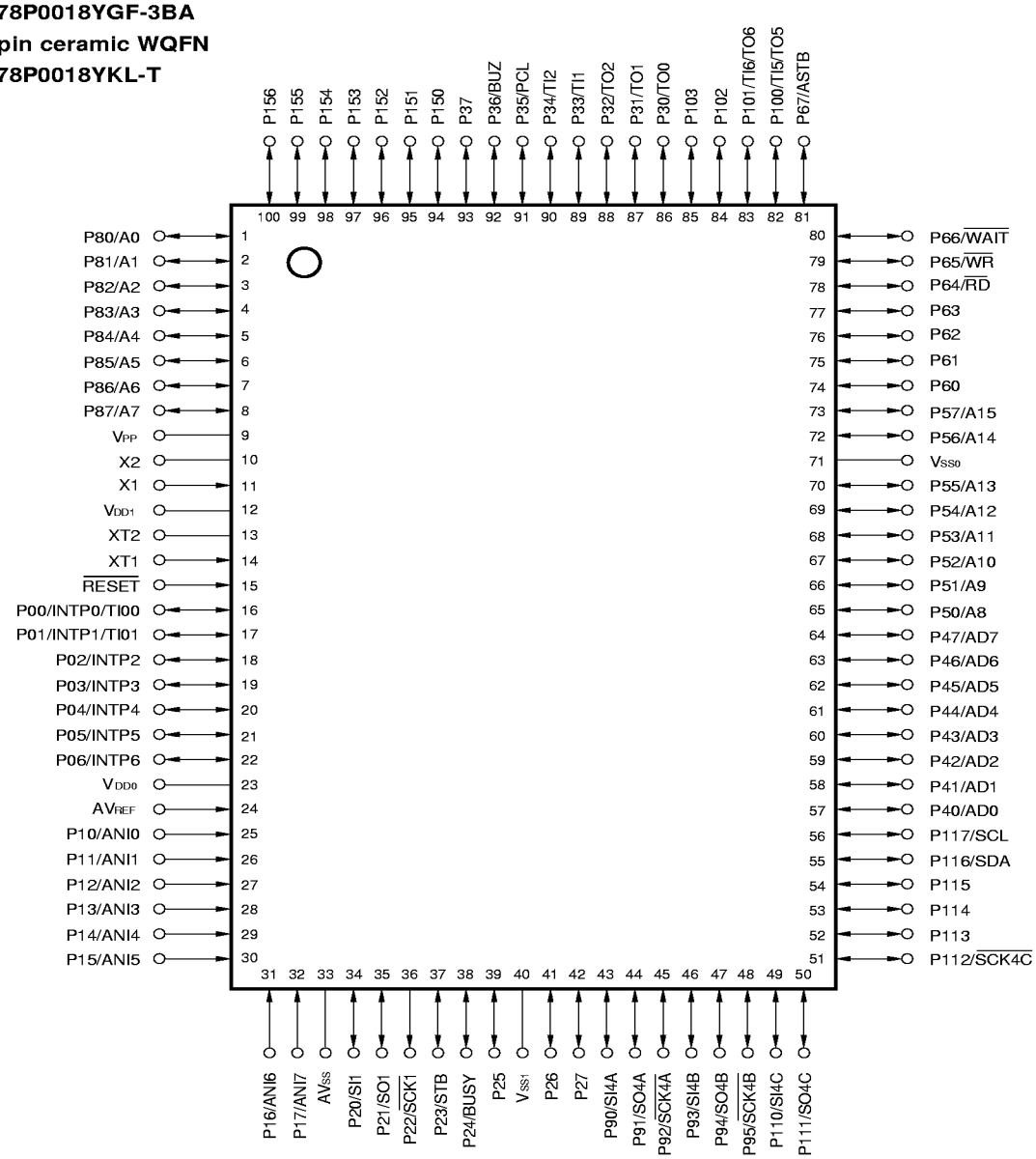
Item		Function
Internal memory		• PROM: 60 Kbytes [Note] • RAM High-speed RAM: 1024 bytes Expansion RAM: 1024 bytes Buffer RAM: 32 bytes
Memory space		64 Kbytes
General register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)
Instruction cycles		Instruction execution time variable function is integrated.
	When main system clock is selected	0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs (@ 5.0-MHz operation)
	When subsystem clock is selected	122 μs (@ 32.768-kHz operation)
Instruction set		• 16-bit operation • Multiply/divide (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulate (set, reset, test, Boolean operation) • BCD adjust, etc.
I/O ports		Total: 88 • CMOS input: 9 • CMOS input/output: 79
A/D converter		• 8-bit resolution × 8 channels
Serial interface		• 3-wire/Serial I/O mode (with automatic transmitting/receiving function): 1 channel • 3-wire Serial I/O mode (with time-sharing transporting function): 1 channel
Timer		• 16-bit timer/event counter: 1 channel • 8-bit timer/event counte: 4 channels • Watch timer: 1 channel • Watchdog timer: 1 channel
Timer output		5 pins (14-bit PWM output enable: 1 pin, 8-bit PWM output enable: 2 pins)
Clock output		39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz, 1.25 MHz, 2.5 MHz, and 5.0 MHz (@ 5.0-MHz operation with main system clock) 32.768 kHz (@ 32.768-kHz operation with subsystem clock)
Buzzer output		2.4 kHz, 4.9 kHz and 9.8 kHz (@ 5.0-MHz operation with main system clock)
Vectored interrupt	Maskable interrupt	Internal: 12, External: 7
	Non-maskable interrupt	Internal: 1
	Software interrupt	1
Test input		Internal: 1, External: 1
Operating supply voltage range		V_{DD} = 2.7 to 5.5 V
Package		• 100-pin plastic QFP (14 × 20 mm) • 100-pin ceramic WQFN

Note Internal PROM capacity can be changed by setting the internal memory size switching register (IMS).

PIN CONFIGURATION (TOP VIEW)

(1) Normal operating mode

- **100-pin plastic QFP (14 × 20 mm)**
  μPD78P0018YGF-3BA
- **100-pin ceramic WQFN**
  μPD78P0018YKL-T



Cautions 1. Connect V_{PP} pin directly to V_{SS0}.

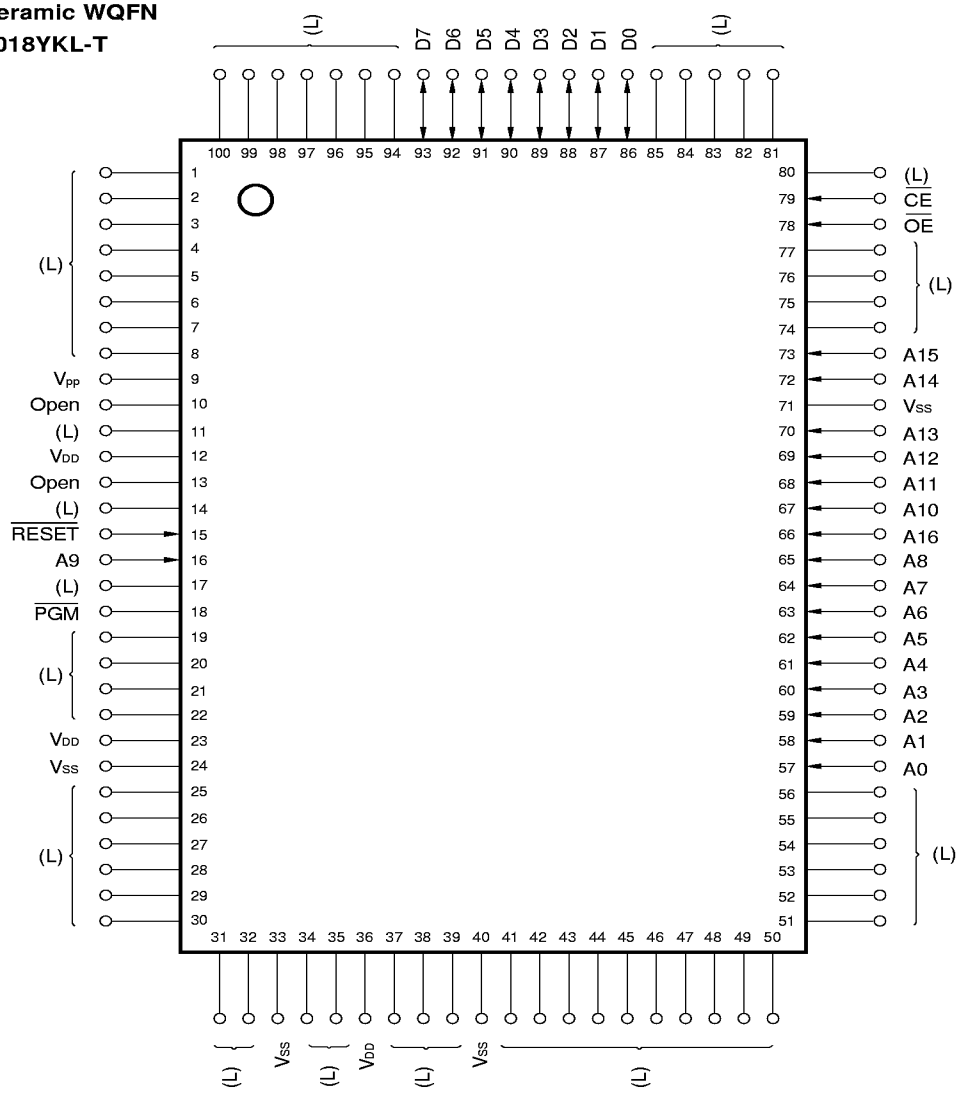
2. Connect AV_{SS} pin to V_{SS0}.

Remark When the μPD78P0018 is used in application fields which need to reduce noise from microcontroller inside, noise reduction, such as supplying voltage to V_{DD0} and V_{DD1} individually and connecting V_{SS0} and V_{SS1} to different ground lines, is recommended.

P00 to P06:	Port 0	SCL:	Serial Clock
P10 to P17:	Port 1	SDA:	Serial Data
P20 to P27:	Port 2	PCL:	Programmable Clock
P30 to P37:	Port 3	BUZ:	Buzzer Clock
P40 to P47:	Port 4	STB:	Strobe
P50 to P57:	Port 5	BUSY:	Busy
P60 to P67:	Port 6	AD0 to AD7:	Address/ Data Bus
P80 to P87:	Port 8	A0 to A15:	Address Bus
P90 to P95:	Port 9	$\overline{RD}$:	Read Strobe
P100 to P103:	Port 10	$\overline{WR}$:	Write Strobe
P110 to P117:	Port 11	$\overline{WAIT}$:	Wait
P150 to P156:	Port 15	ASTB:	Address Strobe
INTP0 to INTP6:	Interrupt From Peripherals	X1, X2:	Crystal (Main System Clock)
TI00, TI01:	Timer Input	XT1, XT2:	Crystal (Subsystem Clock)
TI1,TI2, TI5, TI6:	Timer Input	$\overline{RESET}$:	Reset
TO0 to TO2, TO5, TO6:	Timer Output	ANI0 to ANI7:	Analog Input
SI1, SI4A, SI4B, SI4C:	Serial Input	AV_{SS}:	Analog Ground
SO1, SO4A, SO4B,		AV_{REF}:	Analog Reference Voltage
SO4C:	Serial Output	V_{DD0}, V_{DD1}:	Power Supply
$\overline{SCK1}$, $\overline{SCK4A}$,		V_{PP}:	Programming Power Supply
$\overline{SCK4B}$, $\overline{SCK4C}$:	Serial Clock	V_{SS0}, V_{SS1}:	Ground

(2) PROM programming mode

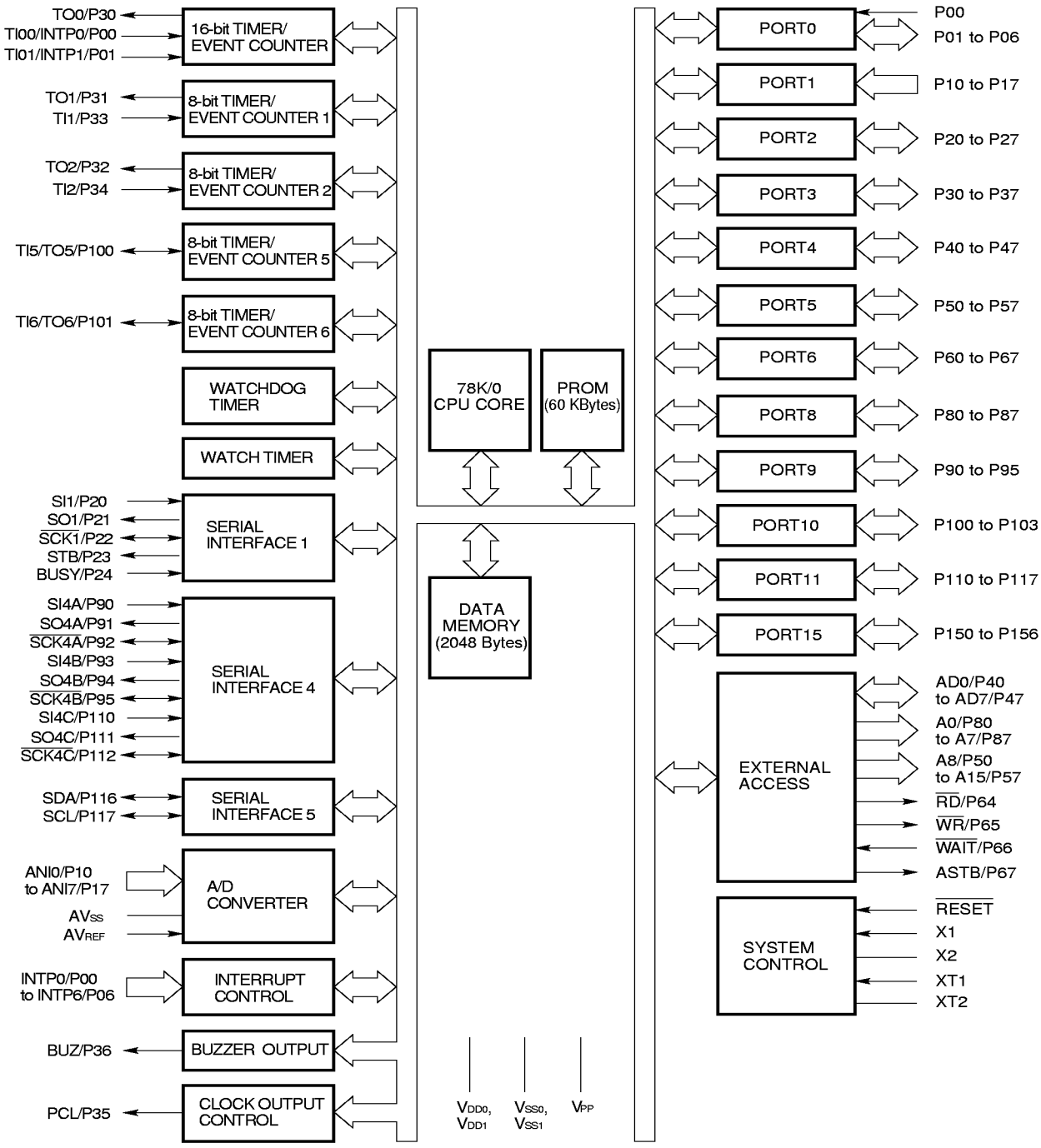
- **100-pin plastic QFP (14 × 20 mm)**
  μPD78P0018YGF-3BA
- **100-pin ceramic WQFN**
  μPD78P0018YKL-T



Cautions 1. (L): Individually connect to VSS via a pull-down resistor.
2. VSS: Connect to GND.
3. $\overline{\text{RESET}}$: Set to low level.
4. Open: No connection

A0 to A16:	Address Bus	$\overline{\text{RESET}}$:	Reset
D0 to D7:	Data Bus	VDD:	Power Supply
$\overline{\text{CE}}$:	Chip Enable	VPP:	Programming Power Supply
$\overline{\text{OE}}$:	Output Enable	VSS:	Ground
$\overline{\text{PGM}}$:	Program		

BLOCK DIAGRAM



CONTENTS

1. DIFFERENCES BETWEEN THE μPD78P0018Y AND MASK ROM VERSIONS

The μPD78P0018Y is a single-chip microcontroller with an on-chip one-time PROM or with an on-chip EPROM which has program write, erasure and rewrite capability.

It is possible to make all the functions except for PROM specification to the same as those of mask ROM versions by setting the internal memory size switching register.

Differences between the μPD78P0018Y and mask ROM versions are shown in **Table 1-1**.

Table 1-1. Differences between the μPD78P0018 and Mask ROM Versions

Parameter	μPD78P0018Y	Mask ROM Versions
ROM structure	One-time PROM/EPROM	Mask ROM
ROM capacity	60 Kbytes	μPD78P0016Y : 48 Kbytes μPD78P0018Y : 60 Kbytes
Setting the internal ROM capacity by the internal memory size switching register	Available Note	Not available
IC pin	No	Yes
V_{PP} pin	Yes	No

Note The internal PROM becomes to 60 Kbytes after the $\overline{\text{RESET}}$ input.

2. PIN FUNCTION LIST

2.1 PINS IN NORMAL OPERATING MODE

(1) Port pins (1/3)

Pin Name	Input/Output	Function		After Reset	Alternate Function
P00	Input	Port 0 7-bit input/output port	Input only	Input	INTP0/TI00
P01	Input/output		Input/output is specifiable bit-wise. When used as the input port, it is possible to use an on-chip pull-up resistor by software.	Input	INTP1/TI01
P02					INTP2
P03					INTP3
P04					INTP4
P05					INTP5
P06					INTP6
P10 to P17	Input	Port 1 8-bit input port It is possible to use an on-chip pull-up resistor by software. Note		Input	ANI0 to ANI7
P20	Input/output	Port 2 8-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to use an on-chip pull-up resistor by software.		Input	SI1
P21					SO1
P22					$\overline{SCK1}$
P23					STB
P24					BUSY
P25 to P27					—
P30	Input/output	Port 3 8-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to use an on-chip pull-up resistor by software.		Input	TO0
P31					TO1
P32					TO2
P33					TI1
P34					TI2
P35					PCL
P36					BUZ
P37					—

Note When P10/ANI0 to P17/ANI7 pins are used as the analog inputs for A/D converter, a pull-up resistor becomes automatically unused.

(1) Port pins (2/3)

Pin Name	Input/Output	Function	After Reset	Alternate Function
P40 to P47	Input/output	Port 4 8-bit input/output port Input/output is specifiable as 8-bit unit. When used as the input port, it is possible to use an on-chip pull-up resistor by software. Set test input flag (KRIF) to 1 by falling edge detection.	Input	AD0 to AD7
P50 to P57	Input/output	Port 5 8-bit input/output port It is possible to directly drive LEDs. Input/output is specifiable bit-wise. When used as the input port, it is possible to use an on-chip pull-up resistor by software.	Input	A8 to A15
P60	Input/output	Port 6 8-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to use an on-chip pull-upresistor by software.	Input	—
P61				—
P62				—
P63				—
P64				$\overline{RD}$
P65				$\overline{WR}$
P66				$\overline{WAIT}$
P67				ASTB
P80 to P87	Input/output	Port 8 8-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to use an on-chip pull-up resistor by software.	Input	A0 to A7
P90	Input/output	Port 9 6-bit input/output port Input/output is specifiablebit-wise. When used as the input port, it is possible to use an on-chip pull-up resistor by software.	Input	SI4A
P91				SO4A
P92				$\overline{SCK4A}$
P93				SI4B
P94				SO4B
P95				$\overline{SCK4B}$

(1) Port pins (3/3)

Pin Name	Input/Output	Function	After Reset	Alternate Function
P100	Input/output	Port 10 4-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to use an on-chip pull-up resistor by software.	Input	TI5/TO5
P101				TI6/TO6
P102, P103				—
P110	Input/output	Port 11 8-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to use an on-chip pull-up resistor by software.	Input	SI4C
P111				SO4C
P112				SCK4C
P113 to P115				—
P116				SDA
P117				SCL
P150 to P156	Input/output	Port 15 7-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to use an on-chip pull-up resistor by software.	Input	—

(2) Non-port pins (1/3)

Pin Name	Input/Output	Function	After Reset	Alternate Function
INTP0	Input	External interrupt inputs, with specifiable valid edges (rising edge, falling edge, and both rising and falling edges).	Input	P00/TI00
INTP1				P01/TI01
INTP2				P02
INTP3				P03
INTP4				P04
INTP5				P05
INTP6				P06
SI1	Input	Serial data input of the serial interface	Input	P20
SI4A				P90
SI4B				P93
SI4C				P110
SO1	Output	Serial data output of the serial interface	Input	P21
SO4A				P91
SO4B				P94
SO4C				P111
$\overline{SCK1}$	Input/output	Serial clock input/output of the serial interface	Input	P22
$\overline{SCK4A}$				P92
$\overline{SCK4B}$				P95
$\overline{SCK4C}$				P112
SCL				P117
STB	Output	Automatic transmitting/receiving strobe output of the serial interface	Input	P23
BUSY	Input	Automatic transmitting/receiving busy input of the serial interface	Input	P24
TI00	Input	External count clock input to 16-bit timer (TM0)	Input	P00/INTP0
TI01		Capture trigger signal input to capture register (CR00)		P01/INTP1
TI1		External count clock input to 8-bit timer (TM1)		P33
TI2		External count clock input to 8-bit timer (TM2)		P34
TI5		External count clock input to 8-bit timer (TM5)		P100/TO5
TI6		External count clock input to 8-bit timer (TM6)		P101/TO6

(2) Non-port pins (2/3)

Pin Name	Input/Output	Function	After Reset	Alternate Function
TO0	Output	16-bit timer output (alternate function as 14-bit PWM output)	Input	P30
TO1		8-bit timer output		P31
TO2				P32
TO5		8-bit timer output (alternate function as 8-bit PWM output)		P100/TI5
TO6				P101/TI6
PCL	Output	Clock output (for trimming main system clock and subsystem clock)	Input	P35
BUZ	Output	Buzzer output	Input	P36
AD0 to AD7	Input/output	Low-order address/data bus when expanding memory to the outside.	Input	P40 to P47
A0 to A7	Output	Low-order address bus when expanding memory to the outside.	Input	P80 to P87
A8 to A15	Output	High-order address bus when expanding memory to the outside.	Input	P50 to P57
$\overline{RD}$	Output	Strobe signal output for the external memory read operation	Input	P64
$\overline{WR}$		Strobe signal output for the external memory write operation	Input	P65
$\overline{WAIT}$	Input	Wait insertion when accessing external memory	Input	P66
ASTB	Output	Strobe output to externally latches address information which is output to ports 4, 5, and 8 for accessing external memory.	Input	P67
ANI0 to ANI7	Input	Analog input of A/D converter	Input	P10 to P17
AV_{REF}	Input	Reference voltage input of A/D converter (alternate function as analog supply voltage)	—	—
AV_{SS}	—	Ground potential of A/D converter. The same potential as V_{SS0}	—	—
$\overline{RESET}$	Input	System reset input	—	—

(2) Non-port pins (3/3)

Pin Name	Input/Output	Function	After Reset	Alternate Function
X1	Input	Crystal connection for main system clock oscillation	—	—
X2	—		—	—
XT1	Input	Crystal connection for subsystem clock oscillation	Input	—
XT2	—		—	—
V_{DD0}	—	Positive power supply for port	—	—
V_{SS0}	—	Ground potential for port	—	—
V_{DD1}	—	Positive power supply (except for port and analog)	—	—
V_{SS1}	—	Ground potential (except for port and analog)	—	—
V_{PP}	—	High-voltage applied during program write/verification Connected to V_{SS0} in normal operating mode	—	—

2.2 PINS IN PROM PROGRAMMING MODE

Pin Name	Input/Output	Function
$\overline{RESET}$	Input	PROM programming mode setting When +5 V or +12.5 V is applied to the V_{PP} pin and a low level signal is applied to the $\overline{RESET}$ pin, this chip is set in the PROM programming mode.
V_{PP}	Input	PROM programming mode setting and high-voltage applied during program write/ verification
A0 to A16	Input	Address bus
D0 to D7	Input/output	Data bus
$\overline{CE}$	Input	PROM enable input/program pulse input
$\overline{OE}$	Input	Read strobe input to PROM
$\overline{PGM}$	Input	Program/program inhibit input in PROM programing mode
V_{DD}	—	Positive power supply
V_{SS}	—	Ground potential

2.3 PIN INPUT/OUTPUT CIRCUITS AND RECOMMENDED CONNECTION OF UNUSED PINS

Types of input/output circuits of the pins and recommeded connection of unused pins are shown in **Table 2-1**. For the configuration of each type of input/output circuit, see **Figure 2-1**.

Table 2-1. Type of Input/Output Circuit of Each Pin (1/2)

Pin Name	Input/Output Circuit Type	Input/Output	Recommended Connection for Unused Pins
P00/INTP0/TI00	2	Input	Connect to V_{SS0}.
P01/INTP1/TI01	8-C	Input/output	Individually connect to V_{SS0} via a resistor.
P02/INTP2			
P03/INTP3			
P04/INTP4			
P05/INTP5			
P06/INTP6			
P10/ANI0 to P17/ANI7	9-B	Input	Individually connect to V_{DD0} or V_{SS0} via a resistor.
P20/SI1	8-C	Input/output	
P21/SO1	5-H		
P22/$\overline{SCK1}$	8-C		
P23/STB	5-H		
P24/BUSY	8-C		
P25 to P27	5-H		
P30/TO0 to P32/TO2			
P33/TI1	8-C		
P34/TI2			
P35/PCL	5-H		
P36/BUZ			
P37			
P40/AD0 to P47/AD7	5-N	Input/output	Individually connect to V_{DD0} via a resistor.
P50/A8 to P57/A15	5-H	Input/output	Individually connect to V_{DD0} or V_{SS0} via a resistor.
P60 to P63			
P64/$\overline{RD}$			
P65/$\overline{WR}$			
P66/$\overline{WAIT}$			
P67/ASTB			
P80/A0 to P87/A7			

Table 2-1. Type of Input/Output Circuit of Each Pin (2/2)

Pin Name	Input/Output Circuit Type	Input/Output	Recommended Connection for Unused Pins
P90/ISI4A	8-C	Input/output	Individually connect to V_{DD0} or V_{SS0} via a resistor.
P91/SO4A	5-H		
P92/$\overline{SCK4A}$	8-C		
P93/ISI4B			
P94/SO4B	5-H		
P95/$\overline{SCK4B}$	8-C		
P100/TI5/TO5			
P101/TI6/TO6			
P102, P103	5-H		
P110/SI4C	8-C		
P111/SO4C	5-H		
P112/$\overline{SCK4C}$	8-C		
P113 to P115	5-H		
P116/SDA	10-B		
P117/SCL			
P150 to P156	5-H		
$\overline{RESET}$	2	Input	—
XT1	16	—	Connect to V_{DD0}.
XT2			Leave open.
AV_{REF}	—		Connect to V_{SS0}.
AV_{SS}			
V_{PP}			Connect directly to V_{SS0}.

Figure 2-1. List of Pin Input/Output Circuits (1/2)

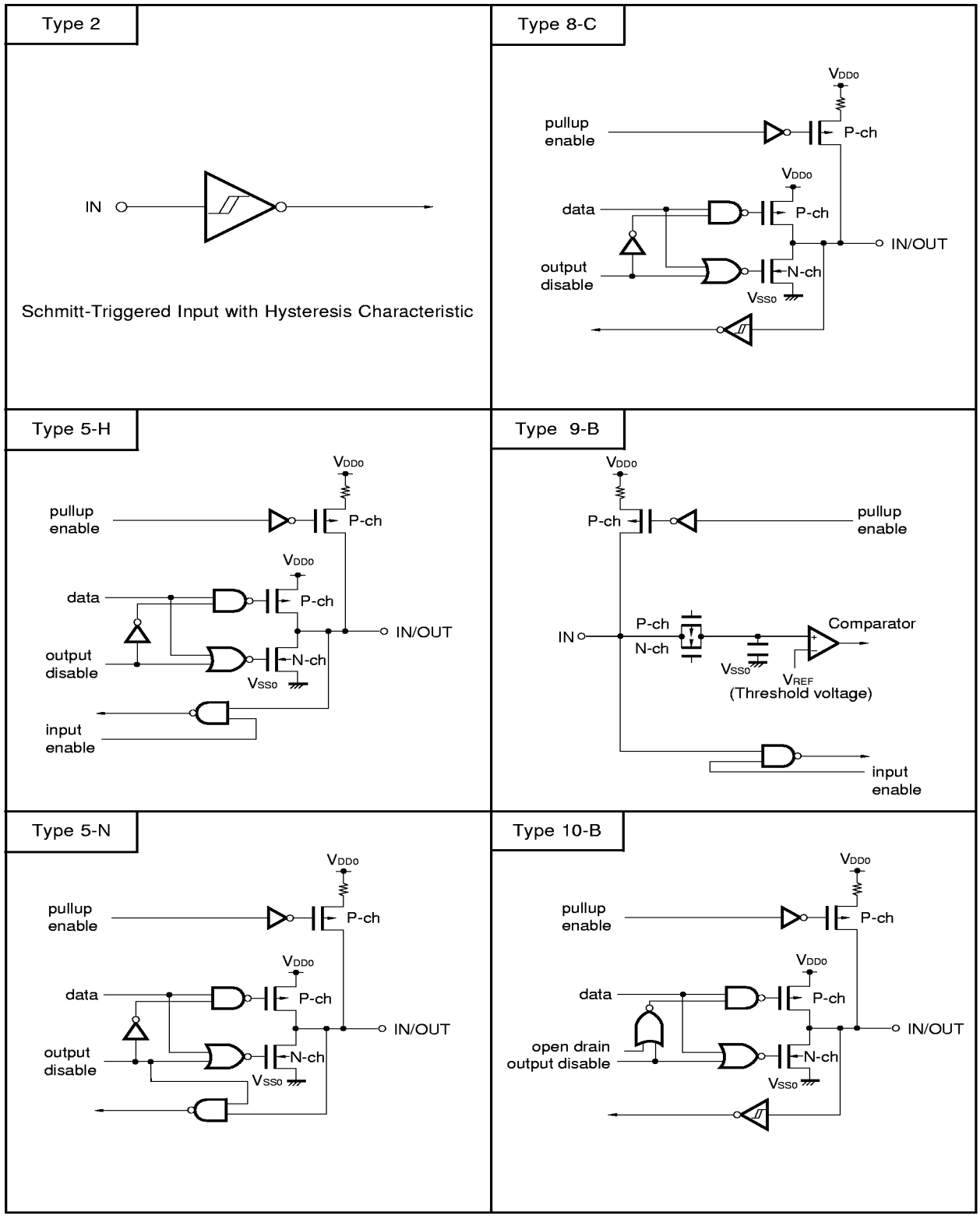
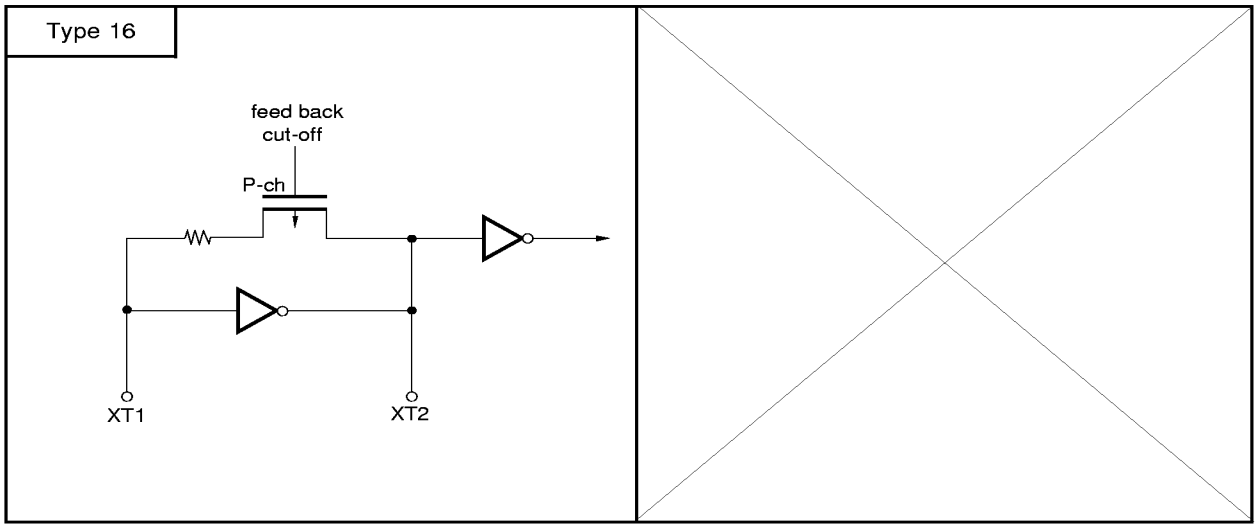


Figure 2-1. List of Pin Input/Output Circuits (2/2)



3. INTERNAL MEMORY SIZE SWITCHING REGISTER (IMS)

This is a register to disable use of part of internal memories by software. By setting this internal memory size switching register (IMS), it is possible to get the same memory mapping as that of the mask ROM versions with a different internal memory (ROM).

IMS is set with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets IMS to CFH.

Figure 3-1. Internal Memory Size Switching Register Format

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0	FFF0H	CFH	R/W

ROM3	ROM2	ROM1	ROM0	Selection of Internal ROM Capacity
1	1	0	0	48 Kbytes
1	1	1	1	60 Kbytes
Other than above				Setting prohibited

RAM2	RAM1	RAM0	Selection of Internal High-Speed RAM Capacity
1	1	0	1024 bytes
Other than above			Setting prohibited

Table 3-1 shows the setting values of IMS which makes the memory mapping the same as that of the mask ROM version.

Table 3-1. Internal Memory Size Switching Register Setting Values

Target Mask ROM Versions	IMS Setting
μPD780016Y	CCH
μPD780018Y	CFH

4. INTERNAL EXPANSION RAM SIZE SWITCHING REGISTER (IXS)

This register is used to set the internal expansion RAM capacity by software. By setting this internal expansion RAM size register (IXS), it is possible to get the same memory mapping as that of the mask ROM versions with a different internal expansion RAM.

IXS is set with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets IXS to 0AH.

Figure 4-1. Internal Expansion RAM Size Switching Register Format

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
IXS	0	0	0	0	IXRAM3	IXRAM2	IXRAM1	IXRAM0	FFF4H	0AH	W

IXRAM3	IXRAM2	IXRAM1	IXRAM0	Internal expansion RAM capacity selection
1	0	1	0	1024 bytes
Other than above				Setting prohibited

Table 4-1 shows the setting values of IXS which make the memory mapping the same as that of the mask ROM versions.

Table 4-1. Internal Expansion RAM Size Switching Register Setting Values

Target Mask ROM Versions	IXS Setting
μPD780016Y	0AH
μPD780018Y	

5. PROM PROGRAMMING

The μPD78P0018 has an on-chip 60-Kbyte PROM as a program memory. For programming, set the PROM programming mode by the V_{PP} and $\overline{RESET}$ pins. For connecting unused pins, refer to **PIN CONFIGURATION (2) PROM programming mode**.

Caution Programs must be written in addresses 0000H to EFFFH (the last address EFFFH must be specified). They cannot be written by a PROM programmer which cannot specify the write address.

5.1 OPERATING MODES

When +5 V or +12.5 V is applied to the V_{PP} pin and the low-level signal is applied to the $\overline{RESET}$ pin, the PROM programming mode is set. This mode will become the operating mode as shown in **Table 5-1** when the $\overline{CE}$, $\overline{OE}$, and $\overline{PGM}$ pins are set as shown.

Further, when the read mode is set, it is possible to read the contents of the PROM.

Table 5-1. Operating Modes of PROM Programming

Pin / Operating Mode	$\overline{RESET}$	V_{PP}	V_{DD}	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	D0 to D7
Page data latch	L	+12.5 V	+6.5 V	H	L	H	Data input
Page write				H	H	L	High-impedance
Byte write				L	H	L	Data input
Program verify				L	L	H	Data output
Program inhibit				×	H	H	High-impedance
				×	L	L	
Read		+5 V	+5 V	L	L	H	Data output
Output disable				L	H	×	High-impedance
Standby				H	×	×	High-impedance

Remark × : L or H

(1) Read mode

Read mode is set if $\overline{CE}$ = L, $\overline{OE}$ = L is set.

(2) Output disable mode

Data output becomes high-impedance, and is in the output disable mode, if $\overline{OE}$ = H is set.

Therefore, it allows data to be read from any device by controlling the $\overline{OE}$ pin, if multiple μPD78P0018s are connected to the data bus.

(3) Standby mode

Standby mode is set if $\overline{CE}$ = H is set.

In this mode, data outputs become high-impedance irrespective of the $\overline{OE}$ status.

(4) Page data latch mode

Page data latch mode is set if $\overline{CE}$ = H, $\overline{PGM}$ = H, $\overline{OE}$ = L are set at the beginning of page write mode.

In this mode, 1 page 4-byte data is latched in an internal address/data latch circuit.

(5) Page write mode

After 1 page 4 bytes of addresses and data are latched in the page data latch mode, a page write is executed by applying a 0.1 ms program pulse (active low) to the $\overline{PGM}$ pin with $\overline{CE}$ = H, $\overline{OE}$ = H. Then, program verification can be performed, if $\overline{CE}$ = L, $\overline{OE}$ = L are set.

If programming is not performed by a one-time program pulse, X (X ≤ 10) write and verification operations should be executed repeatedly.

(6) Byte write mode

Byte write is executed when a 0.1 ms program pulse (active low) is applied to the $\overline{PGM}$ pin with $\overline{CE}$ = L, $\overline{OE}$ = H. Then, program verification can be performed if $\overline{OE}$ = L is set.

If programming is not performed by a one-time program pulse, X (X ≤ 10) write and verification operations should be executed repeatedly.

(7) Program verify mode

Program verify mode is set if $\overline{CE}$ = L, $\overline{PGM}$ = H, $\overline{OE}$ = L are set.

In this mode, check if a write operation is performed correctly, after the write.

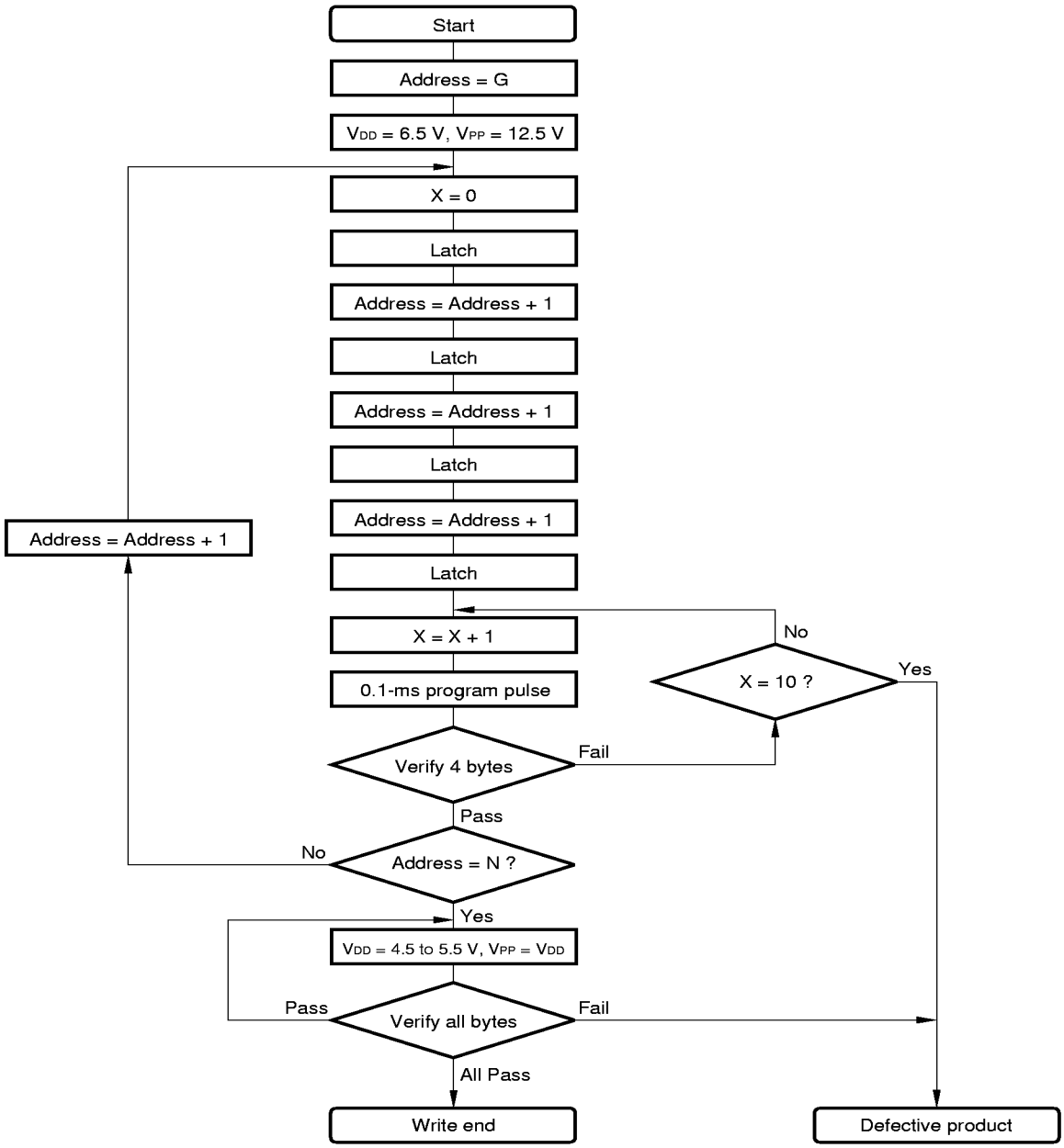
(8) Program inhibit mode

Program inhibit mode is used when the $\overline{OE}$ pin, V_{PP} pin and D0 to D7 pins of multiple μPD78P0018s are connected in parallel and a write is performed to one of those devices.

When a write operation is performed, the page write mode or byte write mode described above is used. At this time, a write is not performed to a device which has the $\overline{PGM}$ pin driven high.

5.2 PROM WRITE PROCEDURE

Figure 5-1. Page Program Mode Flow Chart



Remarks 1. G = Start address
2. N = Program last address

Figure 5-2. Page Program Mode Timing

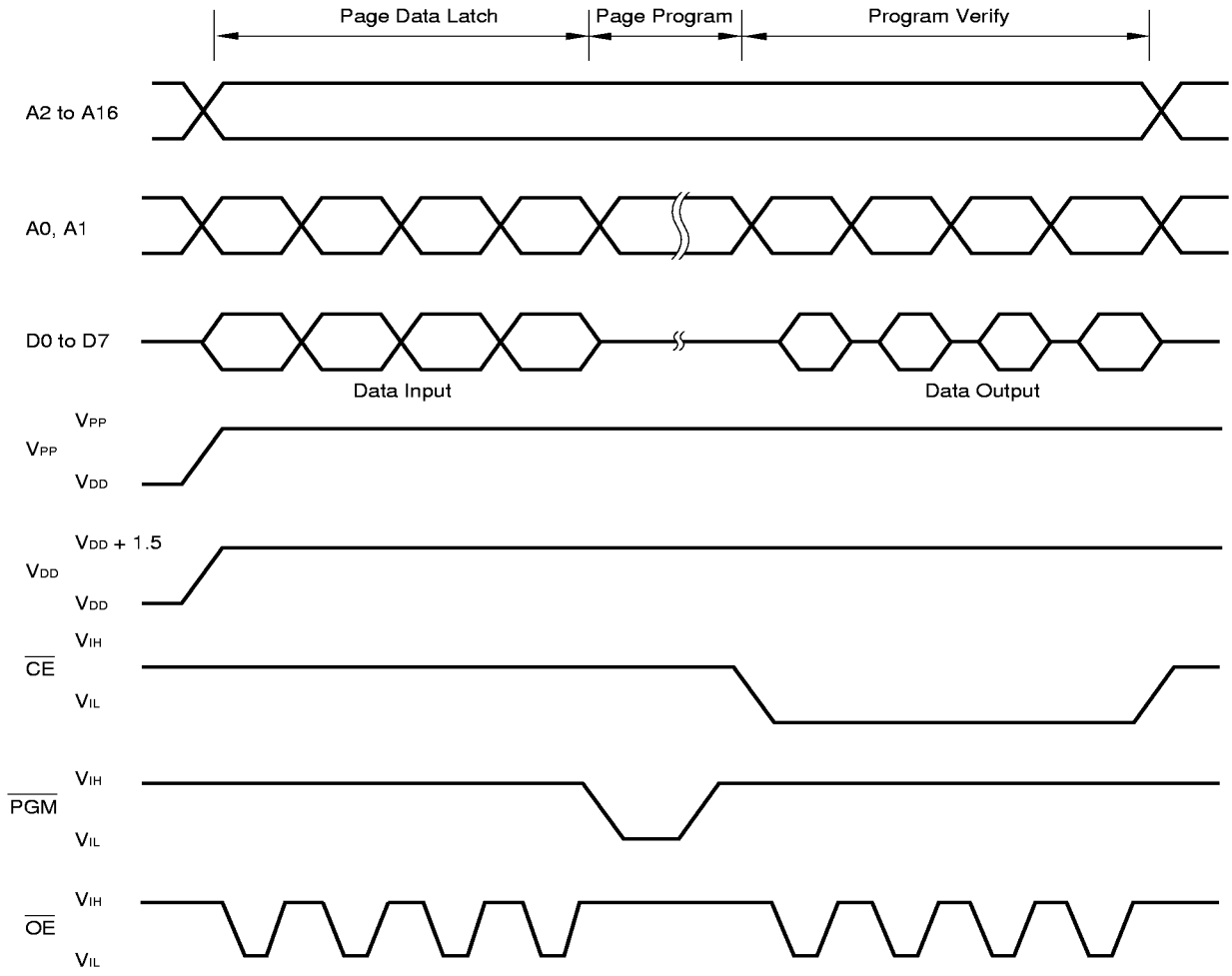
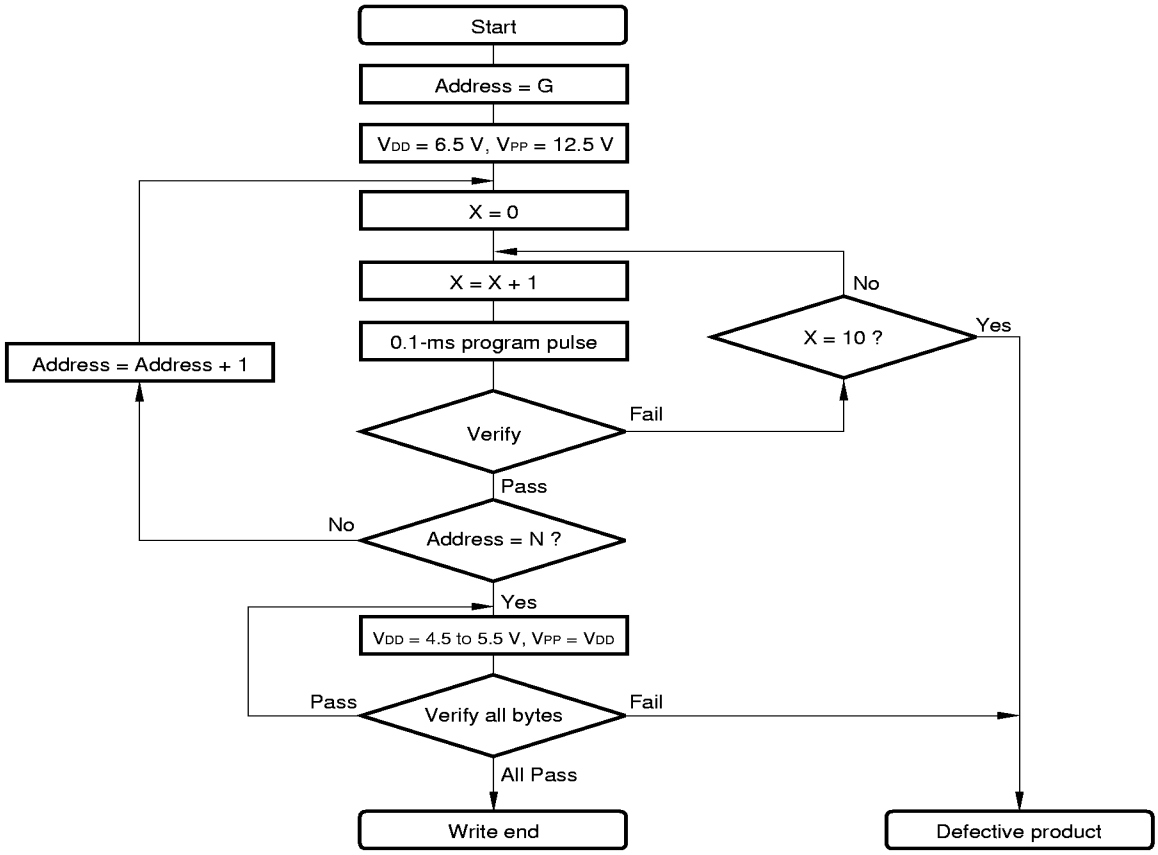
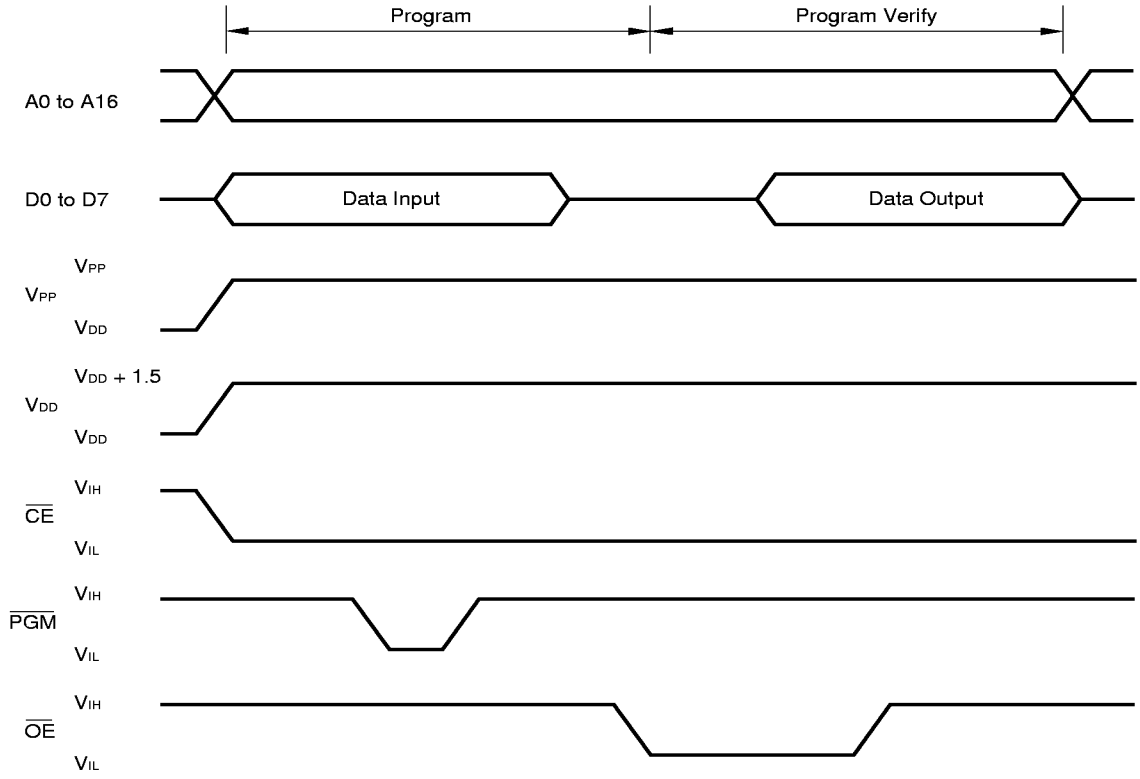


Figure 5-3. Byte Program Mode Flow Chart



Remarks **1.** G = Start address
2. N = Program last address

Figure 5-4. Byte Program Mode Timing



Cautions 1. V_{DD} should be applied before V_{PP} and cut after V_{PP}.
2. V_{PP} must not exceed +13.5 V including overshoot.
3. Reliability may be adversely affected if removal/reinsertion is performed while +12.5 V is being applied to V_{PP}.

5.3 PROM READ PROCEDURE

The contents of PROM are readable to the external data bus (D0 to D7) according to the read procedure shown below.

(1) Fix the $\overline{\text{RESET}}$ pin at low level, supply +5 V to the V_{PP} pin, and connect all other unused pins as shown in **PIN CONFIGURATION (2) PROM programming mode**.

(2) Supply +5 V to the V_{DD} and V_{PP} pins.

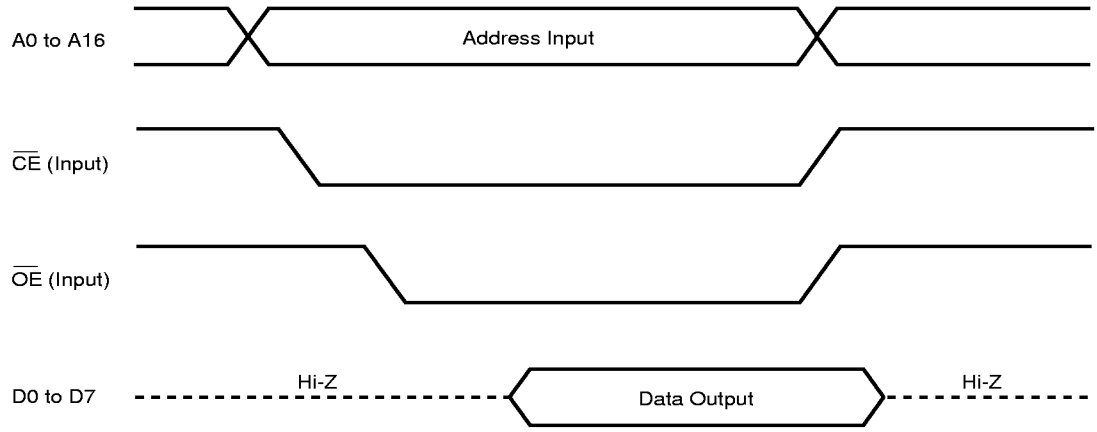
(3) Input address of read data into the A0 to A16 pins.

(4) Read mode

(5) Output data to D0 to D7 pins.

The timings of the above steps (2) to (5) are shown in **Figure 5-5**.

Figure 5-5. PROM Read Timings



6. PROGRAM ERASURE (μPD78P0018YKL-T ONLY)

The μPD78P0018YKL-T is capable of erasing (FFH) the data written in a program memory and rewriting.

To erase the programmed data, exposing the erasure window to light having a wavelength of shorter than about 400 nm. Normally, irradiate ultraviolet rays of 254 nm wavelength. Volume of exposing required to completely erase the programmed data is as follows:

- UV intensity × erasing time : 30 W•s/cm² or more
- Erasure time : 40 min. at least (When a UV lamp of 12 mW/cm² is used. However, a longer time may be needed because of deterioration in performance of the UV lamp, contamination of the erasure window, etc.)

When erasing the contents of data, set up the UV lamp within 2.5 cm from the erasing window. Further, if a filter is provided for a UV lamp, irradiate the ultraviolet rays after removing the filter.

7. OPAQUE FILM ON ERASURE WINDOW (μPD78P0018YKL-T ONLY)

To protect from unintentional erasure by rays other than that of the lamp for erasing EPROM contents, or to protect internal circuit other than EPROM from misoperating by rays, stick a protection seal on the erasure window when EPROM contents erasure is not performed.

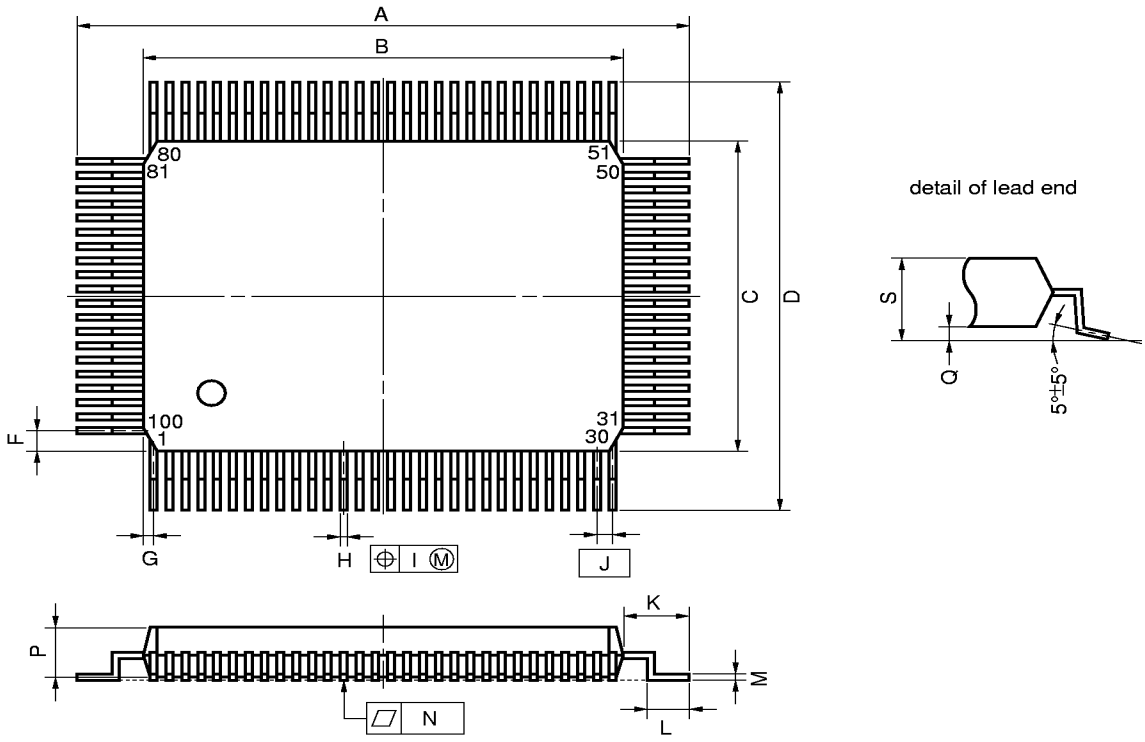
8. ONE-TIME PROM VERSION SCREENING

The one-time PROM version (μPD78P0018YGF-3BA) can not be tested completely by NEC before it is shipped, because of its structure. It is recommended to perform screening to verify PROM after writing necessary data and performing high-temperature storage under the condition below.

Storage Temperature	Storage Time
125 °C	24 hours

9. PACKAGE DRAWINGS

100 PIN PLASTIC QFP (14 × 20)



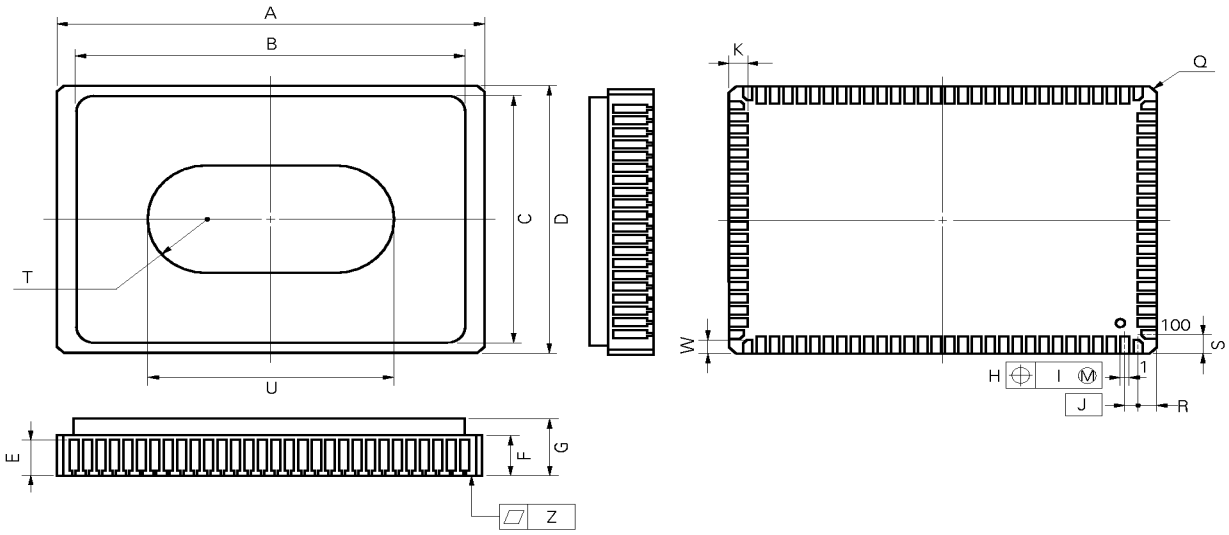
P100GF-65-3BA1-2

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	$0.795^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	0.8	0.031
G	0.6	0.024
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.65 (T.P.)	0.026 (T.P.)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

100 PIN CERAMIC WQFN



X100KW-65A-1

ITEM	MILLIMETERS	INCHES
A	20.6±0.4	0.811±0.016
B	19.0	0.748
C	13.8	0.543
D	14.6±0.4	0.575±0.016
E	1.94	0.076
F	2.14	0.084
G	3.5 MAX,	0.138 MAX.
H	0.45±0.10	$0.018^{+0.004}_{-0.005}$
I	0.06	0.003
J	0.65	0.026
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
Q	C 0.3	C 0.012
R	0.875	0.034
S	1.125	0.044
T	R 3.17	R 0.125
U	12.0	0.472
W	0.75±0.2	$0.030^{+0.008}_{-0.009}$
Z	0.10	0.004

NOTE
Each lead centerline is located within 0.06 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

APPENDIX A. DEVELOPMENT TOOLS

The following support tools are available for system development using the μPD78P0018Y.

Language Processing Software

RA78K/0 Notes 1, 2, 3, 4	78K/0 series common assembler package
CC78K/0 Notes 1, 2, 3, 4	78K/0 series common C compiler package
DF780018 Notes 1, 2, 3, 4, 8	μPD780018 subseries device file
CC78K/0-L Notes 1, 2, 3, 4	78K/0 series common C compiler library source file

PROM Writing Tools

PG-1500	PROM programmer
PA-78P0018GF Note 8 PA-78P0018KL-T Note 8	Programmer adapter connected to the PG-1500
PG-1500 controller Notes 1, 2	PG-1500 control program

Debugging Tools

IE-78000-R	78K/0 series common in-circuit emulator
IE-78000-R-A Note 8	78K/0 series common in-circuit emulator (for integrated debugger)
IE-78000-R-BK	78K/0 series common break board
IE-780018-R-EM Note 8	μPD780018 subseries common emulation board
EP-78064GF-R	Emulation probe common to the μPD78064 subseries
EV-9200GF-100	Socket for mounting on target system board created for 100-pin plastic QFP (14 × 20 mm) use
EV-9900	Jig used to remove the μPD78P0018YKL-T from the EV-9200GF-100
SM78K0 Notes 5, 6, 7	78K/0 series common simulator
ID78K0 Notes 4, 5, 6, 7, 8	Integrated debugger for the IE-78000-R-A
SD78K/0 Notes 1, 2	Screen debugger for the IE-78000-R
DF780018 Notes 1, 2, 4, 5, 6, 7, 8	μPD780018 subseries device file

Real-time Operating System

RX78K/0 Notes 1, 2, 3, 4	78K/0 series common real-time Operating System
MX78K/0 Notes 1, 2, 3, 4	78K/0 series common Operating System

Fuzzy Inference Development Support System

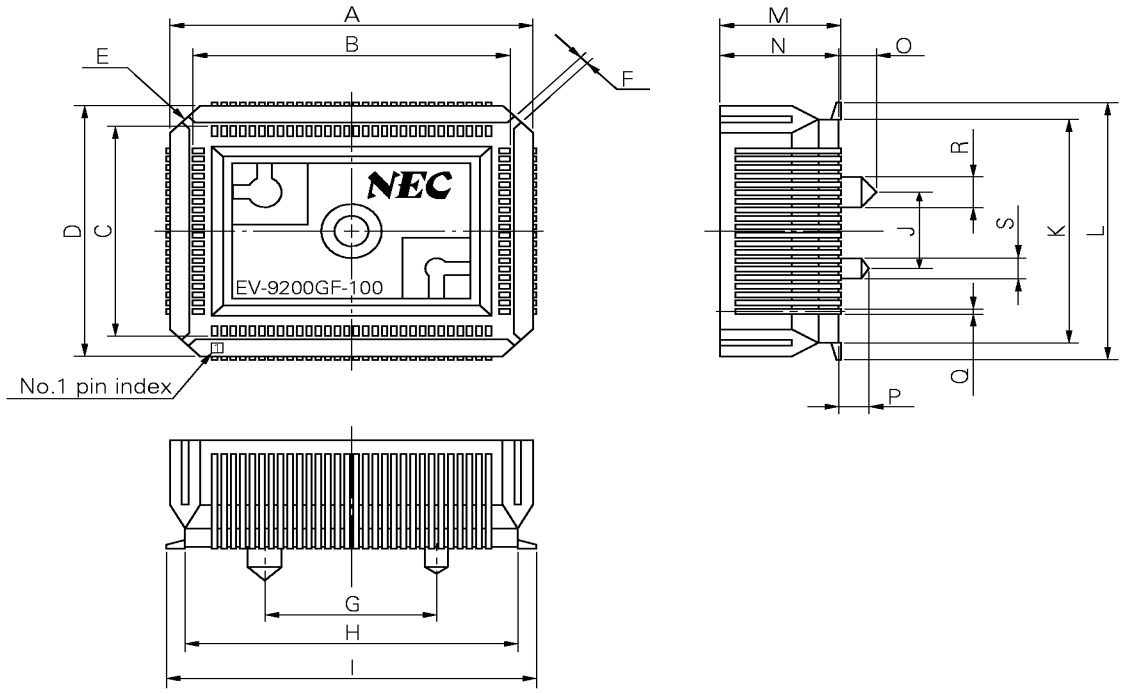
FE9000 Note 1/FE9200 Note 6	Fuzzy knowledge data creation tool
FT9080 Note 1/FT9085 Note 2	Translator
FI78K0 Notes 1, 2	Fuzzy inference module
FD78K0 Notes 1, 2	Fuzzy inference debugger

Notes **1.** PC-9800 series (MS-DOS™) based
2. IBM PC/AT™ and the compatible (PC DOS™/IBM DOS™/MS-DOS) based
3. HP9000 series 300™ (HP-UX™) based
4. HP9000 series 700™ (HP-UX) based, SPARCstation™ (SunOS™) based, EWS4800 series (EWS-UX/V) based
5. PC-9800 series (MS-DOS + Windows™) based
6. IBM PC/AT and the compatible (PC DOS/IBM DOS/MS-DOS + Windows) based
7. NEWS™ (NEWS-OS™) based
8. Under development

Remarks **1.** For development tools manufactured by third parties, see **78K/0 Series Selection Guide (U11126E)**.
2. RA78K/0, CC78K/0, SM78K0, ID78K0, SD78K/0, and RX78K/0 are used with DF780018.

Conversion Socket (EV-9200GF-100) Drawing and Footprints

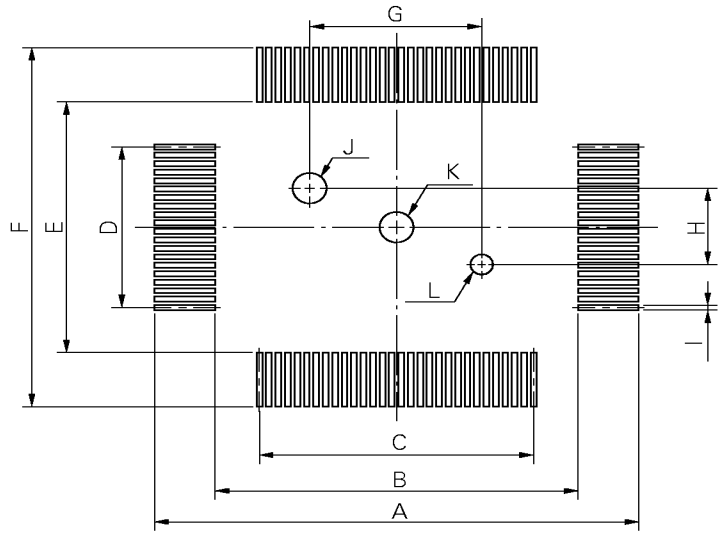
Figure A-1. Socket Drawing of EV9200GF-100 (Reference)



EV-9200GF-100-G0

ITEM	MILLIMETERS	INCHES
A	24.6	0.969
B	21	0.827
C	15	0.591
D	18.6	0.732
E	4-C 2	4-C 0.079
F	0.8	0.031
G	12.0	0.472
H	22.6	0.89
I	25.3	0.996
J	6.0	0.236
K	16.6	0.654
L	19.3	076
M	8.2	0.323
N	8.0	0.315
O	2.5	0.098
P	2.0	0.079
Q	0.35	0.014
R	φ2.3	φ0.091
S	φ1.5	φ0.059

Figure A-2. EV-9200GF-100 Footprints (Reference)



EV-9200GF-100-P1

ITEM	MILLIMETERS	INCHES
A	26.3	1.035
B	21.6	0.85
C	0.65±0.02 × 29=18.85±0.05	$0.026^{+0.001}_{-0.002} \times 1.142 = 0.742^{+0.002}_{-0.002}$
D	0.65±0.02 × 19=12.35±0.05	$0.026^{+0.001}_{-0.002} \times 0.748 = 0.486^{+0.003}_{-0.002}$
E	15.6	0.614
F	20.3	0.799
G	12±0.05	$0.472^{+0.003}_{-0.002}$
H	6±0.05	$0.236^{+0.003}_{-0.002}$
I	0.35±0.02	$0.014^{+0.001}_{-0.001}$
J	φ2.36±0.03	$\phi 0.093^{+0.001}_{-0.002}$
K	φ2.3	φ0.091
L	φ1.57±0.03	$\phi 0.062^{+0.001}_{-0.002}$

Caution Dimensions of mount pad for EV-9200 and that for target device (QFP) may be different in some parts. For the recommended mount pad dimensions for QFP, refer to "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (C10535E).

APPENDIX B. RELATED DOCUMENTS

Documents related to devices

Document Name	Document No.	
	Japanese Version	English Version
μPD780018, 780018Y Subseries User's Manual	Planned	Planned
μPD780016Y, 780018Y Preliminary Product Information	Planned	Planned
μPD78P0018Y Preliminary Product Information	U11603J	This document
78K/0 Series User's Manual: Instructions	IEU-849	IEU-1372
78K/0 Series Instruction Use Table	U10903J	—
78K/0 Series Instruction Set	U10904J	—
μPD780018Y Subseries Special Register Use Table	Planned	—

Documents related to development tools (User's Manuals)

Document Name		Document No.	
		Japanese Version	English Version
RA78K Series Assembler Package	Operation	EEU-809	EEU-1399
	Language	EEU-815	EEU-1404
RA78K Series Structured Assembler Preprocessor		EEU-817	EEU-1402
CC78K Series C Compiler	Operation	EEU-656	EEU-1280
	Language	EEU-655	EEU-1289
CC78K C Compiler Application Note	Programming Know-how	EEA-618	EEA-1208
CC78K Series Library Source File		EEU-777	—
PG-1500 PROM Programmer		EEU-651	EEU-1335
PG-1500 Controller PC-9800 Series (MS-DOS) based		EEU-704	EEU-1291
PG-1500 Controller IBM PC Series (PC DOS) based		EEU-5008	U10540E
IE-78000-R		EEU-810	U11376E
IE-78000-R-A		U10057J	U10057E
IE-78000-R-BK		EEU-867	EEU-1427
IE-780018-R-EM		Planned	Planned
EP-78064		EEU-934	EEU-1469
SM78K0 System Simulator	Reference	EEU-5002	U10181E
SM78K Series System Simulator	External Parts User-open Interface Spec	U10092J	U10092E
ID78K0 Integrated Debugger	Reference	U11151J	—
SD78K/0 Screen Debugger PC-9800 Series (MS-DOS) based	Instruction	EEU-852	—
	Reference	U10952J	—
SD78K/0 Screen Debugger IBM PC/AT (PC DOS) based	Instruction	EEU-5024	EEU-1414
	Reference	U11279J	EEU-1413

Caution The contents of the above documents are subject to change without notice. Be sure to use the latest edition for designing.

Documents related to embedded software (User's Manuals)

Document Name		Document No.	
		Japanese Version	English Version
78K/0 Series Real-tIme Operating System	Basic	EEU-912	—
	Install	EEU-911	—
	Technical	EEU-913	—
78K/0 Series Operating System MX78K0	Basic	EEU-5010	—
Fuzzy Knowledge Data Creation Tool		EEU-829	EEU-1438
78K/0, 78K/II, 87AD Series Fuzzy Inference Development Support System Translator		EEU-862	EEU-1444
78K/0 Series Fuzzy Inference Development Support System Fuzzy Inference Module		EEU-858	EEU-1441
78K/0 Series Fuzzy Inference Development Support System Fuzzy Inference Debugger		EEU-921	EEU-1458

Other documents

Document Name	Document No.	
	Japanese Version	English Version
IC Package Manual	C10943X	
Semiconductor Device Mounting Technology Manual	C10535J	C10535E
Quality Grades of NEC Semiconductor Devices	IEI-620	IEI-1209
NEC Semiconductor Device Reliability/Quality Control System	U10983J	U10983E
Electrostatic Discharge (ESD) Test	MEM-539	IEI-1201
Guide to Quality Assurance for Semiconductor Devices	MEI-603	MEI-1202
Microcomputer Product Series Guide	MEI-604	—

Caution The contents of the above documents are subject to change without notice. Be sure to use the latest edition for designing.