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μPD78218A Family **(μPD78217A/218A/P218A)** **8-Bit, K-Series Microcontrollers** **With A/D Converter, Real-Time Output Ports**

July 1993

Description

The μPD78217A, μPD78218A, and μPD78P218A are members of the K-Series® of microcontrollers and are designed for real-time embedded control applications. The μPD78218A family is pin compatible with the μPD78214 family and offers increased internal memory with enhanced timer and macro service facilities. These 8-bit, single-chip microcontrollers have a minimum instruction time of 333 ns at 12 MHz (500 ns for the μPD78217A). They feature 8-bit hardware multiply and divide instructions, four banks of main registers, an advanced interrupt handling facility, a powerful set of memory mapped on-chip peripherals, and the ability to address up to 1M bytes of external data memory. On board memory includes 1024 bytes of RAM, 32K bytes of mask ROM, or 32K bytes of UV EPROM or one-time programmable (OTP) ROM.

The advanced interrupt handling facility provides two levels of programmable hardware priority control and two separate methods of servicing interrupt requests: vectored and macro service. The macro service facility reduces the overhead involved in servicing peripheral interrupts by transferring data between the memory-mapped special function registers (SFRs) and memory without the use of time consuming interrupt service routines. In addition, the macro service facility can be initialized to automatically alter timer compare register values or to repeatedly output a prespecified pattern at a fixed or variable rate. By using macro service to control the real-time output ports, the μPD78218A family can easily and accurately drive two independent stepper motors.

The combination of the macro service facility, four banks of main registers, extended data memory address space, and powerful on-chip peripherals makes these devices ideal for applications in office automation, communication, HVAC, and industrial control.

Features

- Complete single-chip microcontroller
 - 8-bit ALU
 - Program memory (ROM)
 - μPD78217A: ROMless
 - μPD78218A/P218A: 32K bytes
 - Data memory (RAM): 1024 bytes
- Pin compatible with μPD78214 family
- Powerful instruction set
 - 8-bit unsigned multiply and divide
 - 16-bit arithmetic instructions
 - 1-bit and 8-bit logic instructions
- Minimum instruction time
 - 333 ns at 12 MHz (μPD78218A/P218A)
 - 500 ns at 12 MHz (μPD78217A)
- Memory expansion
 - 8085 bus-compatible
 - 64K program address space
 - 1M data address space
- Large I/O capacity
 - Up to 54 I/O port lines on μPD78218A/P218A
 - Up to 36 I/O port lines on μPD78217A
 - Software programmable pullup resistors
- Memory-mapped on-chip peripherals (special function registers)
- Timer/counter unit
 - 16-bit timer 0:
 - Two 16-bit compare registers
 - One 16-bit capture register
 - One external interrupt/capture line
 - 8-bit timer 1:
 - One 8-bit compare register
 - One 8-bit capture/compare register
 - One external interrupt/capture line
 - 8-bit timer/counter 2:
 - Two 8-bit compare registers
 - One 8-bit capture register
 - One external interrupt/capture line
 - One external event counter line
 - 8-bit timer 3:
 - One 8-bit compare register
- Four 8-bit precision timer-controlled pulse-width modulated (PWM) output lines
- Two 4-bit (or one 8-bit) real-time output ports
- Eight-channel 8-bit A/D converter
- Programmable priority interrupt controller (two levels)
- Two methods of interrupt service
 - Vectored interrupts
 - Macro service mode with choice of three different types

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Features (cont)

- Two-channel serial communication interface
 - Asynchronous serial interface (UART)
 - Dedicated baud rate generator
 - Clock-synchronized interface
 - Full-duplex, three-wire mode
 - NEC serial bus interface (SBI) mode
- Refresh output for pseudostatic RAM
- STOP and HALT standby functions
- 5-volt CMOS technology

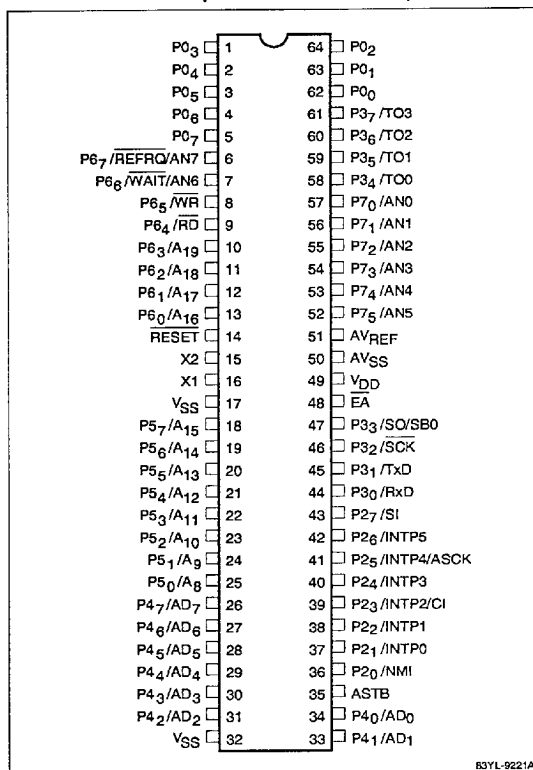
Ordering Information

Part Number	Package	Package Drawing	ROM
μPD78217ACW	64-pin plastic shrink DIP	(P64C-70-750A, C)	ROMless
μPD78217AGC	64-pin plastic QFP	(P64GC-80-AB8-2)	
μPD78218ACW-xxx	64-pin plastic shrink DIP	(P64C-70-750A, C)	32K mask ROM
μPD78218AGC-xxx	64-pin plastic QFP	(P64GC-80-AB8-2)	
μPD78P218ACW	64-pin plastic shrink DIP	(P64C-70-750A, C)	32K OTP ROM
μPD78P218AGC	64-pin plastic QFP	(P64GC-80-AB8-2)	
μPD78P218ADW	64-pin shrink cerdip w/ window	(P64DW-70-750A1)	32K UV EPROM

Note: xxx indicates ROM code suffix

Pin Configurations

64-Pin Shrink DIP (Plastic or Ceramic)



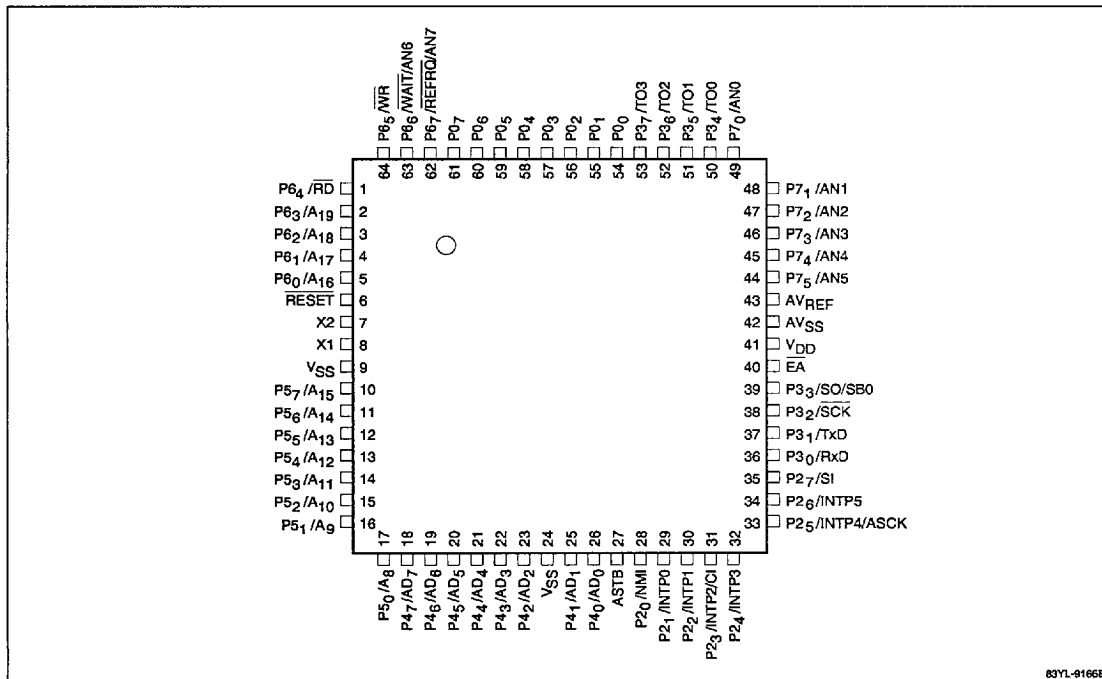
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Pin Configurations (cont)

64-Pin Plastic QFP



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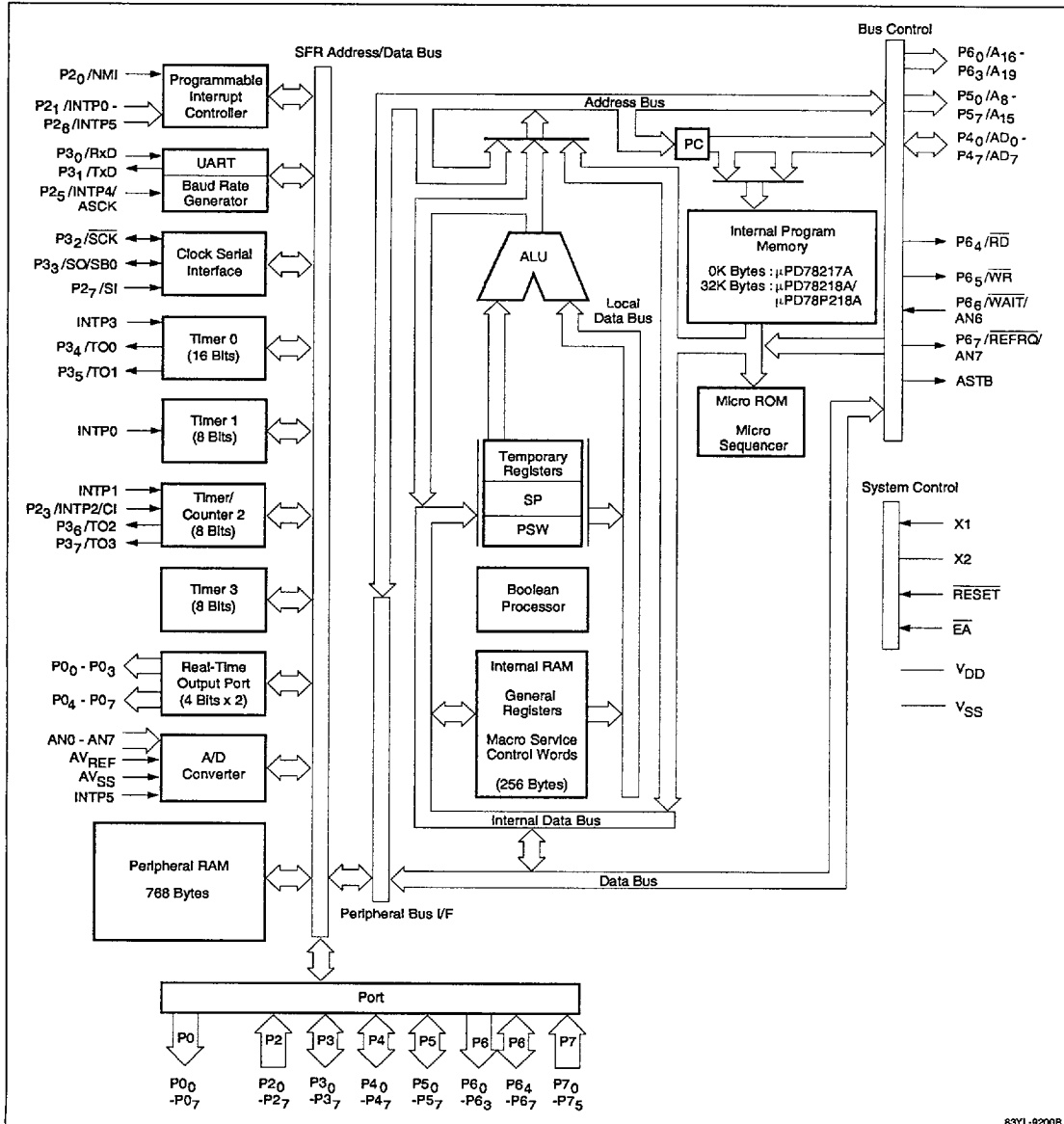
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Pin Functions; Normal Operating Mode

Symbol	First Function	Symbol	Second Function
P0 ₀ - P0 ₇	Port 0; 8-bit tristate output port/real time output port		
P2 ₀	Port 2; 8-bit input port	NMI	External nonmaskable interrupt
P2 ₁		INTP0	Maskable external interrupts
P2 ₂		INTP1	
P2 ₃		INTP2	Maskable external interrupt
		CI	External clock input to timer/counter 2
P2 ₄		INTP3	Maskable external interrupt
P2 ₅		INTP4	Maskable external interrupt
		ASCK	Asynchronous serial clock input
P2 ₆		INTP5	Maskable external interrupt
P2 ₇		SI	Serial data input for three-wire serial I/O mode
P3 ₀	Port 3; 8-bit, bit-selectable tristate input/output port	RxD	Asynchronous serial receive data input
P3 ₁		TxD	Asynchronous serial transmit data output
P3 ₂		SCK	Serial shift clock input/output
P3 ₃		SO	Serial data output for three-wire serial I/O mode
		SBO	I/O bus for NEC serial bus interface (SBI)
P3 ₄ - P3 ₇		TO0 - TO3	Timers T0 to T3 outputs
P4 ₀ - P4 ₇	Port 4; 8-bit tristate input/output port	AD ₀ - AD ₇	Low-order 8-bit multiplexed address/data bus
P5 ₀ - P5 ₇	Port 5; 8-bit, bit-selectable tristate input/output port	A ₈ - A ₁₅	High-order 8-bit address bus
P6 ₀ - P6 ₃	Port 6; 4-bit output port	A ₁₆ - A ₁₉	Extended memory address bus
P6 ₄	Port 6; 4-bit, bit-selectable tristate input/output port	RD	External memory read strobe
P6 ₅		WR	External memory write strobe
P6 ₆		WAIT	External memory wait signal input
P6 ₇		AN6	Analog voltage input to A/D converter
		REFRQ	Refresh pulse output used by external pseudostatic memory
		AN7	Analog voltage input to A/D converter
P7 ₀ - P7 ₅	Port 7; 6-bit input port	AN0 - AN5	Analog voltage inputs to A/D converter
ASTB	Address strobe output used to latch the low-order 8 address for external memory		
RESET	External system reset input		
EA	Internal ROM or external memory control signal input. Low-level input selects external memory. High-level input selects internal ROM. A low-level input on a μPD78218A or μPD78P218A places the device in ROMless mode and external memory is accessed		
X1	Crystal/ceramic resonator connection or external clock input		
X2	Crystal/ceramic resonator connection or inverse of external clock		
AVREF	A/D converter reference voltage		
AVSS	A/D converter ground		
VDD	+5 volt power supply input		
VSS	Power supply ground		
NC	No connection		

Block Diagram



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μPD78218A and μPD78214 Differences

The μPD78218A family is a pin compatible enhanced version of the μPD78214 family. Some of the enhancements include a larger internal program ROM and data RAM memory space, an improved 16-bit timer 0, and an enhanced macro service facility. Table 1 highlights the differences between the μPD78218A and μPD78214 families.

Table 1. Differences Between the μPD78218A and μPD78214 Families

Item	μPD78218A Family	μPD78214 Family
Maximum on-chip ROM	32K bytes	16K bytes
Maximum on-chip RAM	1024 bytes	512 bytes
16-bit timer	Software-triggered one-shot pulse output	Not available
Macro service counter	8/16-bit selectable (except Type A transfers)	8-bit only
Type C macro service pointer, MPT and MPD	Increments full 16 bits	Increments only lower 8 bits
Macro service execution times	Execution times differ; refer to hardware user's manual	Execution times differ; refer to hardware user's manual
PUSH PSW instruction	Execution times differ; refer to software user's manual	Execution times differ; refer to software user's manual
Oscillation stabilization time when exiting STOP mode	Time equivalent to NMI active pulse width plus 16 bits of dedicated counter or 15 bits of dedicated counter	Time equivalent to NMI active pulse width plus 16 bits of dedicated counter
A/D converter reference voltage	3.6 V to V _{DD}	3.4 V to V _{DD}
Programmable device operating voltage	5 V ±0.3 V	5 V ±10%
Package	64-pin plastic shrink DIP	64-pin plastic shrink DIP
	64-pin plastic QFP	64-pin plastic QFP
	64-pin shrink cerdip w/window	64-pin shrink cerdip w/window
		64-pin plastic QUIP
		68-pin PLCC
		74-pin plastic QFP

FUNCTIONAL DESCRIPTION

Central Processing Unit (CPU)

The μPD78218A family CPU features 8- and 16-bit arithmetic including an 8 x 8-bit unsigned multiply and 16 x 8-bit unsigned divide (producing a 16-bit quotient and an 8-bit remainder). The multiply executes in 3.67 μs and the divide in 12.36 μs at 12 MHz (4.00 and 12.69 μs respectively for μPD78217A).

A CALLT vector table and a CALLF program area decrease the number of bytes in the call instructions for commonly used subroutines. A 1-byte call instruction (CALLT) can access up to 32 subroutines through the addresses contained in the CALLT vector table. A 2-byte call instruction (CALLF) can access any routine beginning at a specific address in the CALLF area.

The internal system clock (f_{CLK}) is generated by dividing the oscillator frequency by two. Therefore, at the maximum oscillator frequency of 12 MHz, the internal system clock is 6 MHz. The minimum instruction execution time for an instruction fetched from internal ROM is 333 ns (500 ns when fetched from external memory).

Memory Space

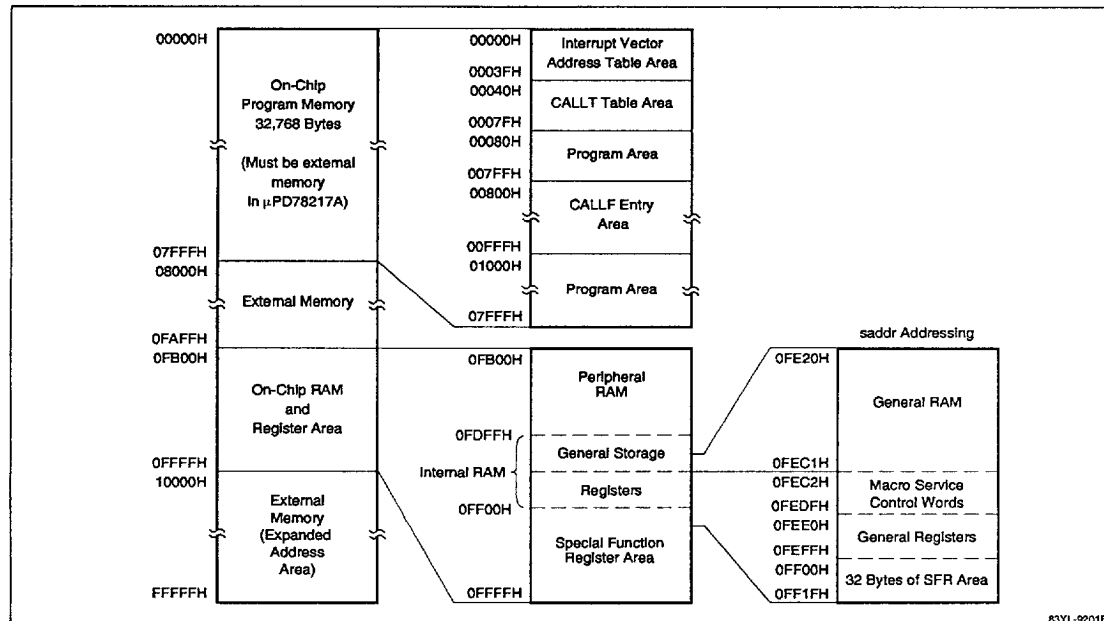
The μPD78218A family has a 1M byte address space (see figure 1). The first 64K bytes of this address space (00000H-0FFFFH) can be used as both program and data memory. The remaining 960K bytes of this address space (10000H-FFFFFH) can only be used as data memory and is known as expanded memory.

External Memory

The μPD78218A family has an 8-bit wide external data bus and a 16-bit wide external address bus (20-bit wide if expanded memory is enabled). The low-order 8 bits of the address bus are multiplexed to provide the 8-bit data bus and are supplied by I/O port 4. The high-order address bits of the 16-bit address bus are taken from port 5. If expanded memory is enabled, the expanded address nibble is provided by P6₀ to P6₃. Address latch, read, and write strobes are also provided.

The memory expansion mode register (MM) is used to enable external memory, to specify up to two additional wait states or the use of the WAIT input pin for the first 64K bytes of memory, and to enable the high-speed internal ROM fetch. Ports 4, 5, and 6 are available as general purpose I/O ports when only internal ROM is used and no external program or data space is required.

Figure 1. Memory Map



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Expanded Data Memory

The MM register is also used to enable the external expanded data memory space, addresses 10000H to FFFFFH. When the expanded data memory is enabled, the entire 1M byte address space is divided into 16 banks of 64K bytes each. The low-order 4-bits of the P6 or the PM6 registers are used as bank selection registers to supply the address information to A₁₆ to A₁₉. Data can easily be transferred from one memory bank to another by using the appropriate instructions. Address lines A₁₆ to A₁₉ are only active when an instruction that uses expanded addressing is being executed. A programmable wait control register (PW) allows the programmer to specify up to two additional wait states or the use of the WAIT input pin for expanded data memory space.

On-Chip RAM

The μPD78218A family has a total of 1024 bytes of on-chip RAM. The upper 256-byte area (FE00H-FEFFFH) features high-speed access and is known as "Internal RAM." The remaining 768 bytes (FB00H-FDFFFH) are accessed at the same speed as external memory and are known as "Peripheral RAM." The general register

banks and the macro service control words are stored in Internal RAM. The remainder of Internal RAM and any unused register bank locations are available for general storage.

On-Chip Program Memory

The μPD78218A contains 32K bytes of internal ROM respectively. The μPD78P218A contains 32K bytes of UV EPROM or one-time programmable ROM. Instructions from on-chip program memory can be fetched at high speed or at the same rate as from external memory. The μPD78217A does not have on-chip program memory.

CPU Control Registers

Program Counter. The program counter is a 16-bit binary counter register that holds the address of the next instruction to be executed. During reset, the program counter is loaded with the address stored in locations 0000H and 00001H.

Stack Pointer. The stack pointer is a 16-bit register that holds the address of the last item pushed onto the

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stack. It is decremented before new data is pushed onto the stack and incremented after data is popped off the stack.

Program Status Word. The program status word (PSW) is an 8-bit register that contains flags that are set or reset depending on the results of an instruction. This register can be written to or read from 8 bits at a time. The individual flags can also be manipulated on a bit-by-bit basis. The assignment of PSW bits follows.

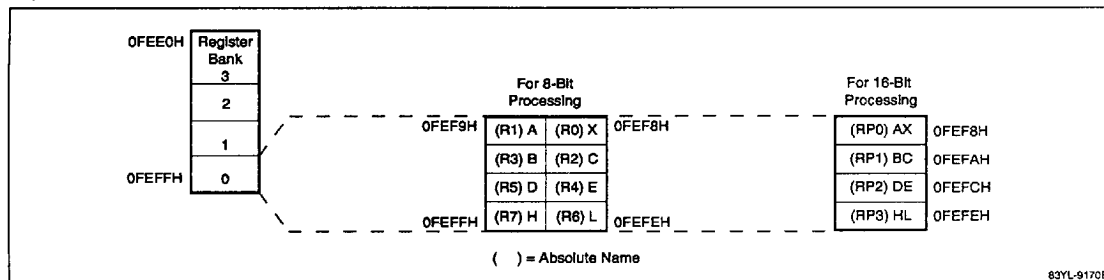
7							0
IE	Z	RBS1	AC	RBS0	0	ISP	CY

CY	Carry flag
ISP	Interrupt priority status flag
RBS0, RBS1	Register bank selection flags
AC	Auxiliary carry flag
Z	Zero flag
IE	Interrupt request enable flag

General Registers

The general-purpose registers (figure 2) consist of four banks of registers located at addresses FEE0H to FEFFH in Internal RAM. Each bank consists of eight 8-bit general registers that can also be used in pairs to function as four 16-bit registers. Two bits in the PSW (RBS0 and RBS1) specify which of the register banks is active. The bits are set under program control. Registers have both functional names (like A, X, B, C for 8-bit registers and AX, BC for 16-bit registers) and absolute names (like R1, R0, R3, R2 for 8-bit registers and RP0, RP1 for 16-bit registers). Each instruction determines whether a register is referred to by its functional or absolute name and whether it is 8 or 16 bits.

Figure 2. General Registers



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Addressing

The μPD78218A family features 1-byte addressing of both the special function registers and the portion of on-chip RAM from FE20H to FEFFH. The 1-byte sfr addressing accesses the entire SFR area, while the 1-byte saddr addressing accesses the first 32 bytes of the SFR area and 224 bytes of Internal RAM. The 16-bit SFRs and words of memory in these areas can be addressed by 1-byte saddrp addressing, which is valid for even addresses only. Since many instructions use 1-byte addressing, access to these locations is almost as fast and versatile as access to the general registers. There are seven addressing modes for data in main memory: direct, register, register indirect with autoincrement and decrement, saddr, SFR, based, and indexed. There are also both 8-bit and 16-bit immediate operands.

Special Function Registers

The input/output ports, timers, capture and compare registers, and mode and control registers for both the peripherals and the CPU are collectively known as special function registers. They are all memory-mapped between FF00H and FFFFH and can be accessed either by main memory addressing or by 1-byte sfr addressing. They are either 8 or 16 bits as required, and many of the 8-bit registers are capable of single-bit access as well. Locations FFD0H through FFD7H are known as the external SFR area. Registers in external circuitry interfaced and mapped to these addresses can be addressed with sfr addressing. Table 2 is a list of the special function registers.

Table 2. Special Function Registers

Address	Register (SFR)	Symbol	R/W	Access Units (Bits)			State After Reset
				1	8	16	
0FF00H	Port 0	P0	R/W	x	x	—	Undefined
0FF02H	Port 2	P2	R	x	x	—	Undefined
0FF03H	Port 3	P3	R/W	x	x	—	Undefined
0FF04H	Port 4	P4	R/W	x	x	—	Undefined
0FF05H	Port 5	P5	R/W	x	x	—	Undefined
0FF06H	Port 6	P6	R/W	x	x	—	x0H
0FF07H	Port 7	P7	R	x	x	—	Undefined
0FF0AH	Port 0 buffer register (low)	P0L	R/W	x	x	—	Undefined
0FF0BH	Port 0 buffer register (high)	P0H	R/W	x	x	—	Undefined
0FF0CH	Real-time output port control register	RTPC	R/W	x	x	—	00H
0FF10H-0FF11H	16-bit compare register 0 (16-bit timer 0)	CR00	R/W	—	—	x	Undefined
0FF12H-0FF13H	16-bit compare register (16-bit timer 0)	CR01	R/W	—	—	x	Undefined
0FF14H	8-bit compare register (8-bit timer 1)	CR10	R/W	—	x	—	Undefined
0FF15H	8-bit compare register (8-bit timer/counter 2)	CR20	R/W	—	x	—	Undefined
0FF16H	8-bit compare register (8-bit timer/counter 2)	CR21	R/W	—	x	—	Undefined
0FF17H	8-bit compare register (8-bit timer 3)	CR30	R/W	—	x	—	Undefined
0FF18H-0FF19H	16-bit capture register (16-bit timer 0)	CR02	R	—	—	x	Undefined
0FF1AH	8-bit capture register (8-bit timer/counter 2)	CR22	R	—	x	—	Undefined
0FF1CH	8-bit capture/compare register (8-bit timer 1)	CR11	R/W	—	x	—	Undefined
0FF20H	Port 0 mode register	PM0	W	—	x	—	FFH
0FF23H	Port 3 mode register	PM3	W	—	x	—	FFH
0FF25H	Port 5 mode register	PM5	W	—	x	—	FFH
0FF26H	Port 6 mode register	PM6	R/W	x	x	—	FxH
0FF30H	Capture/compare control register 0	CRC0	W	—	x	—	10H
0FF31H	Timer output control register	TOC	W	—	x	—	00H
0FF32H	Capture/compare control register 1	CRC1	W	—	x	—	00H
0FF34H	Capture/compare control register 2	CRC2	W	—	x	—	00H
0FF40H	Pullup resistor option register	PUO	R/W	x	x	—	00H
0FF43H	Port 3 mode control register	PMC3	R/W	x	x	—	00H
0FF50H-0FF51H	16-bit timer register 0	TM0	R	—	—	x	0000H
0FF52H	8-bit timer register 1	TM1	R	—	x	—	00H
0FF54H	8-bit timer register 2	TM2	R	—	x	—	00H
0FF56H	8-bit timer register 3	TM3	R	—	x	—	00H
0FF5CH	Prescaler mode register 0	PRM0	W	—	x	—	00H
0FF5DH	Timer control register 0	TMC0	R/W	—	x	—	00H
0FF5EH	Prescaler mode register 1	PRM1	W	—	x	—	00H
0FF5FH	Timer control register 1	TMC1	R/W	—	x	—	00H
0FF68H	A/D converter mode register	ADM	R/W	x	x	—	00H
0FF6AH	A/D conversion result register	ADCR	R	—	x	—	Undefined
0FF7DH	One-shot pulse output control register	OSPC	R/W	x	x	—	00H

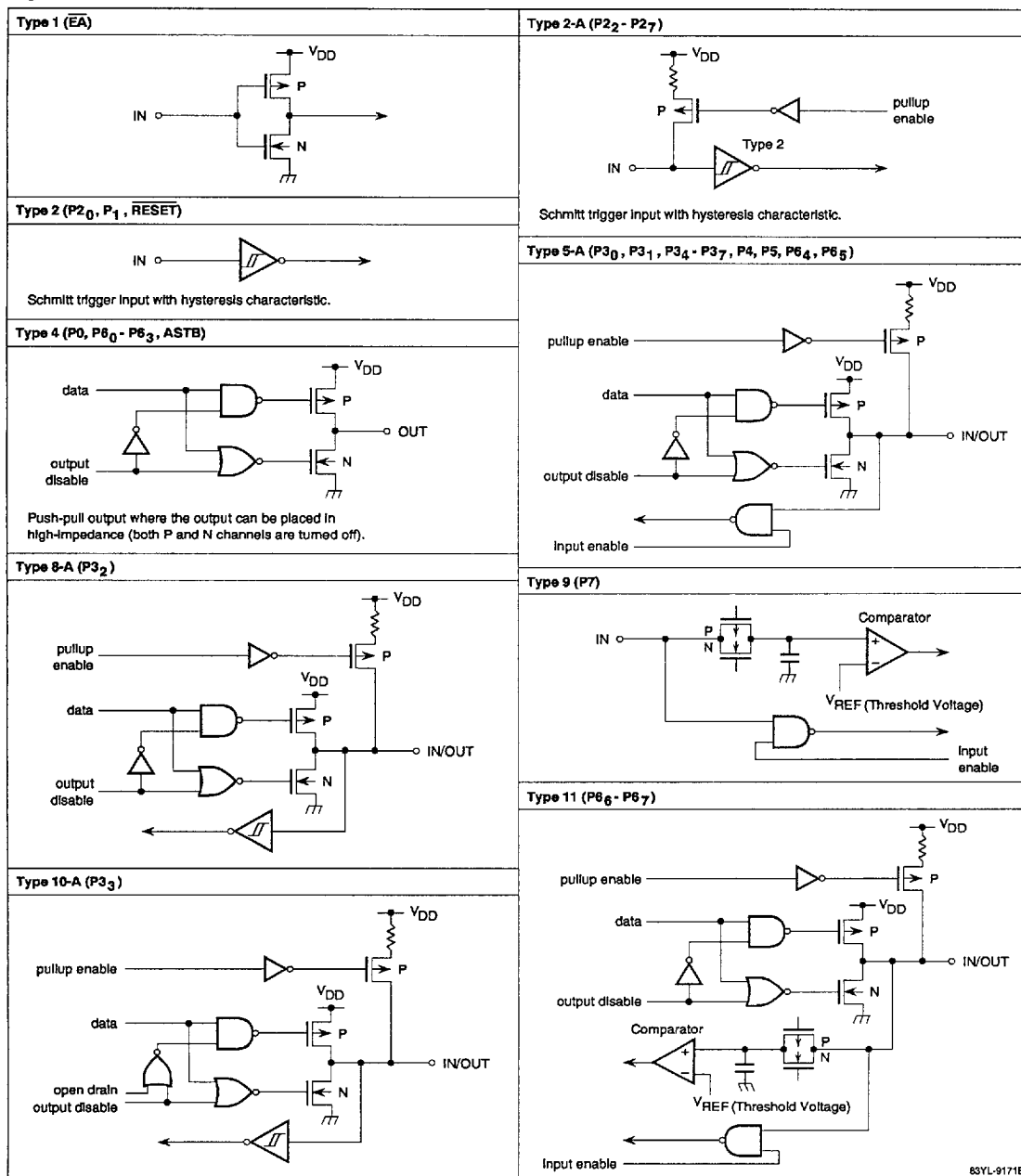
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Table 2. Special Function Registers (cont)

Address	Register (SFR)	Symbol	R/W	Access Units (Bits)			State After Reset
				1	8	16	
0FF80H	Clocked serial interface mode register	CSIM	R/W	x	x	—	00H
0FF82H	Serial bus interface control register	SBIC	R/W	x	x	—	00H
0FF86H	Serial shift register	SIO	R/W	—	x	—	Undefined
0FF88H	Asynchronous serial interface mode register	ASIM	R/W	x	x	—	80H
0FF8AH	Asynchronous serial interface status register	ASIS	R	x	x	—	00H
0FF8CH	Serial receive buffer: UART	RxB	R	—	x	—	Undefined
0FF8EH	Serial transmit shift register: UART	TxS	W	—	x	—	Undefined
0FF90H	Baud rate generator control register	BRGC	W	—	x	—	00H
0FFC0H	Standby control register	STBC	R/W	—	x	—	0000x000B
0FFC4H	Memory expansion mode register	MM	R/W	x	x	—	20H
0FFC5H	Programmable wait control register	PW	R/W	x	x	—	80H
0FFC6H	Refresh mode register	RFM	R/W	x	x	—	00H
0FFD0H-0FFDFH	External SFR area	—	R/W	x	x	—	Undefined
0FFE0H	Interrupt request flag register L	IF0L	R/W	x	x	—	00H
0FFE1H	Interrupt request flag register H	IF0H	R/W	x	x	—	00H
0FFE0H-0FFE1H	Interrupt request flag register	IF0	R/W	—	—	x	000H
0FFE4H	Interrupt mask flag register L	MK0L	R/W	x	x	—	FFH
0FFE5H	Interrupt mask flag register H	MK0H	R/W	x	x	—	FFH
0FFE4H-0FFE5H	Interrupt mask flag register	MK0	R/W	—	—	x	FFFH
0FFE8H	Priority specification flag register L	PR0L	R/W	x	x	—	FFH
0FFE9H	Priority specification flag register H	PR0H	R/W	x	x	—	FFH
0FFE8H-0FFE9H	Priority specification flag register	PR0	R/W	—	—	x	FFFH
0FFECH	Interrupt service mode specification flag register L	ISM0L	R/W	x	x	—	00H
0FFEDH	Interrupt service mode specification flag register H	ISM0H	R/W	x	x	—	00H
0FFECH-0FFEDH	Interrupt service mode specification flag register	ISM0	R/W	—	—	x	000H
0FFF4H	External interrupt mode register 0	INTM0	R/W	x	x	—	00H
0FFF5H	External interrupt mode register 1	INTM1	R/W	x	x	—	00H
0FFF8H	Interrupt status register	IST	R/W	x	x	—	00H

Figure 3. Pin I/O Circuits



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Input/Output Ports

There are up to 54 port lines on the μPD78218A/P218A and up to 36 port lines on the μPD78217A. (Ports 4, 5, and two bits of port 6 are not available on the μPD78217A since the μPD78217A must always use external memory.) Table 3 lists the features of each port and figure 3 shows the structure of each port pin. The pin levels of all port 2, 3, and 7 pins can always be read or tested regardless of the dual pin function.

Real-time Output Port

The real-time output port (RTPC) shares pins with port 0. It can be used as two independent 4-bit real-time output ports or one 8-bit real-time output port. In the

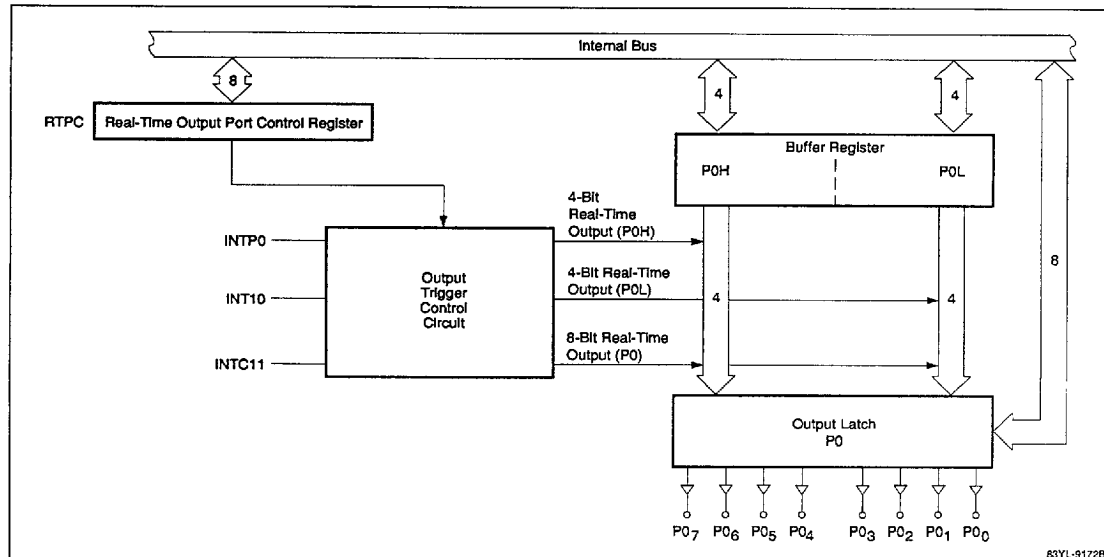
real-time output mode, data stored beforehand in the buffer registers, P0H and P0L, is transferred immediately to the output latch of P0 on the occurrence of a timer 1 interrupt (INTC10 or INTC11) or external interrupt (INTP0) (see figure 4). By using the real-time output port with the macro service function, port 0 can be used to output preprogrammed patterns at preprogrammed variable time intervals. In this mode, two independent stepper motors can accurately be driven at a fixed or variable rate.

Table 3. Digital Port Functions

Port	Operational Features	Configuration	Direct Drive Capability	Software Pullup Resistor Connection
Port 0	8-bit high impedance output		Transistor	
Port 2	8-bit Schmitt trigger input			In 6-bit units (P2 ₂ - P2 ₇)
Port 3	8-bit input or output	Bit selectable		Byte selectable, input bits only
Port 4	8-bit input or output	Byte selectable	LED	Byte selectable
Port 5	8-bit input or output	Byte selectable	LED	Byte selectable, input bits only
Port 6	4-bit output (bits 0 to 3) 4-bit input or output (bits 4 to 7)	Bit selectable		In 4-bit unit, input bits only
Port 7	6-bit input			

Note: Software pullup resistors can be internally connected only on a port-by-port basis to port bits set to input mode. Pullup resistors are not connected to port bits set to output mode.

Figure 4. Real-Time Output Port



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Analog-to-Digital (A/D) Converter

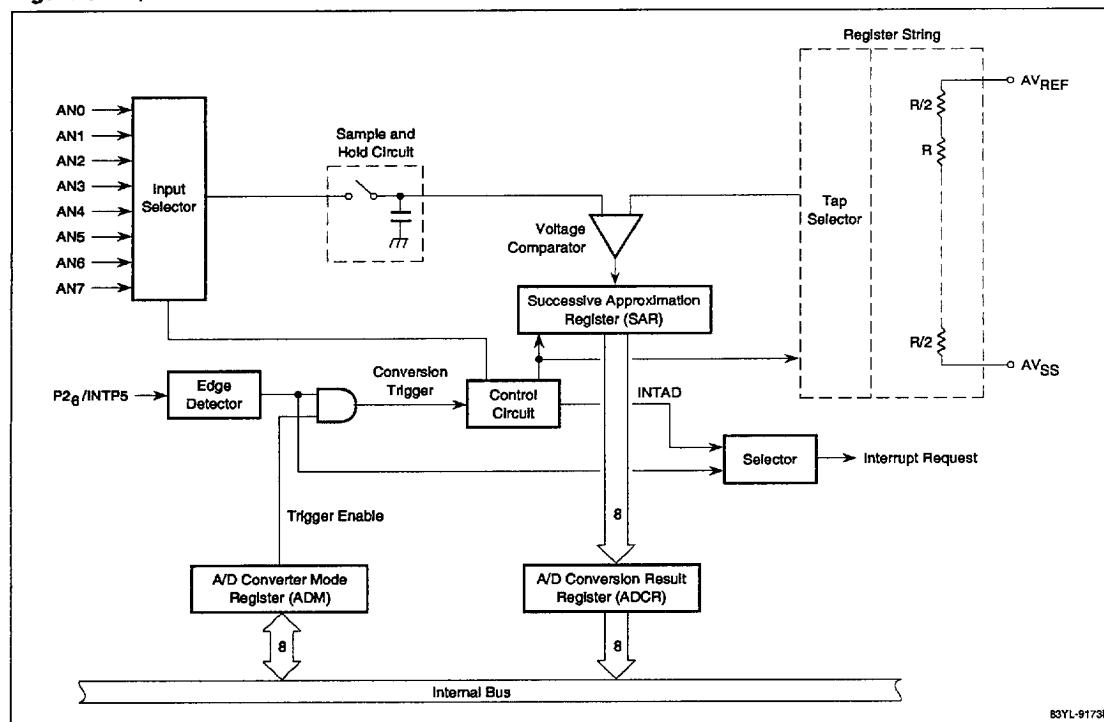
The μ PD78218A family A/D converter (see figure 5) uses the successive-approximation method for converting up to eight multiplexed analog inputs into 8-bit digital data. The conversion time per input is 30 μ s at 12 MHz operation. A/D conversion can be started by an external interrupt, INTP5, or under software control.

The A/D converter can operate in either scan mode or select mode. In scan mode, from one to eight sequential inputs can be programmed for conversion. The A/D converter selects each input in order, converts the data, stores it in the A/D conversion result (ADCR)

register, and generates an interrupt (INTAD). This converted data can be easily transferred to memory by using the macro service function.

In select mode, only one of the eight A/D inputs can be selected for conversion. The ADCR register is continually updated and can be read at any time. If the A/D converter is started by an external interrupt, an INTAD interrupt occurs at the completion of each conversion. If the A/D converter is started by software, no interrupts are generated.

Figure 5. A/D Converter



Serial Interface

The μPD78218A family has two independent serial interfaces. The first is a standard UART. The UART (figure 6) permits full-duplex operation and can be programmed for 7- or 8-bits of data after the start bit, followed by one or two stop bits. Odd, even, zero or no parity can also be selected. The serial clock for the UART can be provided by an on-chip baud rate generator or timer 3. By using either the internal system clock or an external clock input into the ASCK pin, the baud rate generator is capable of generating all of the commonly used baud rates. The UART generates three interrupts: INTST (transmission complete), INTSR (reception complete), and INTSER (reception error).

The second interface is an 8-bit clock-synchronized serial interface (figure 7). It can be operated in either a three-wire serial I/O mode or NEC serial bus interface (SBI) mode.

In the three-wire serial I/O mode, the 8-bit shift register (SIO) is loaded with a byte of data and eight clock pulses are generated. These eight pulses shift the byte of data out of the SO line (MSB first) and in from the SI line providing full-duplex operation. This interface can also be set to receive or to transmit data only. The INTCSI interrupt is generated after each 8-bit transfer. One of three internal clocks or an external clock clocks the data.

Figure 6. Asynchronous Serial Interface

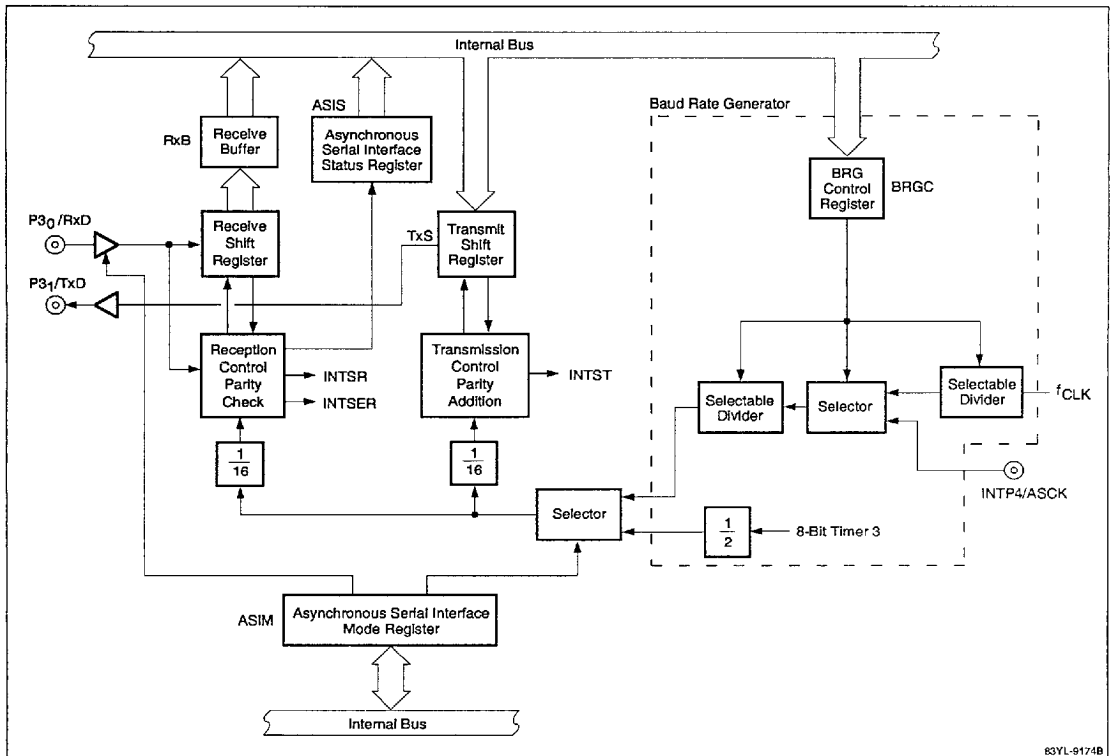


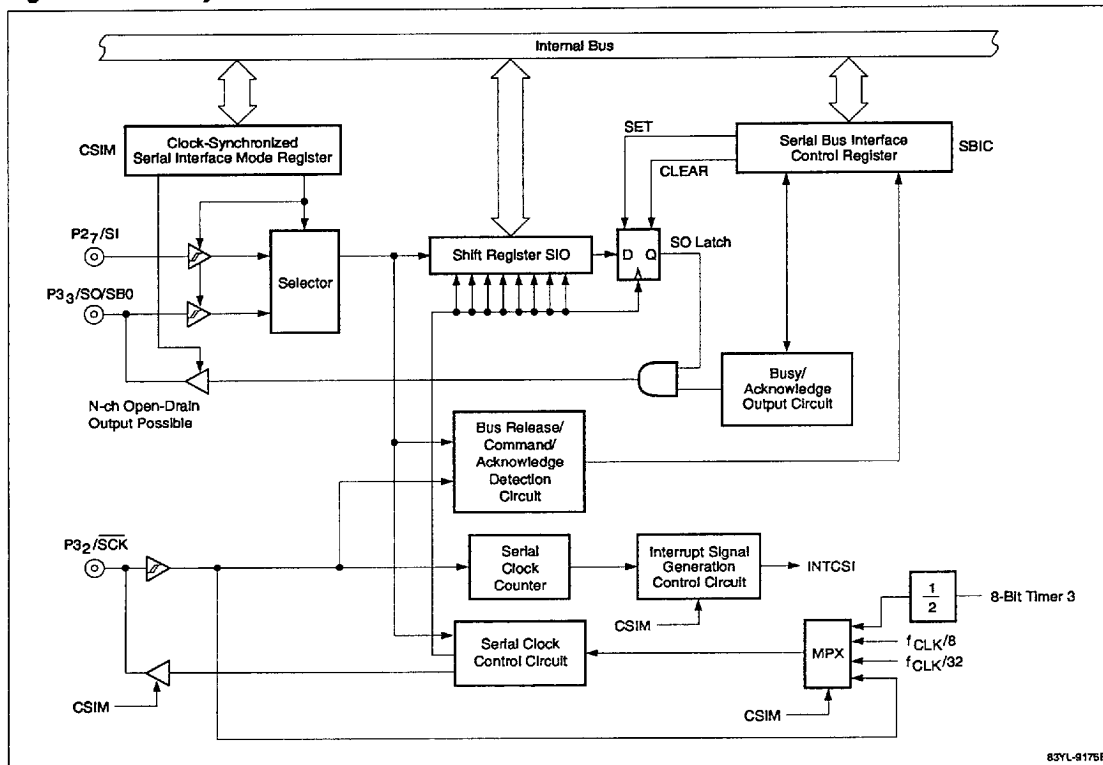
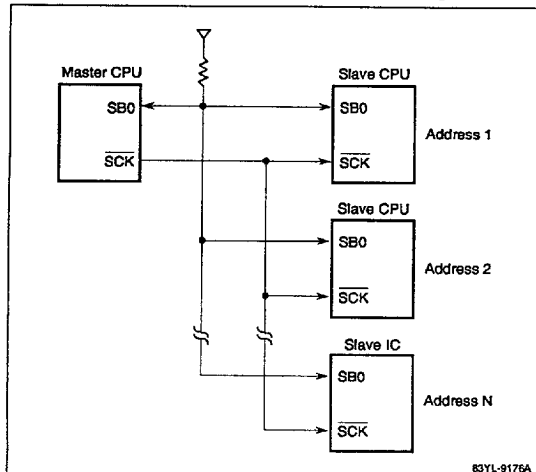
Figure 7. Clock-Synchronized Serial Interface

Figure 8. SBI Mode Master/Slave Configuration

The NEC SBI mode is a two-wire high-speed proprietary serial interface available on most devices in the NEC μ PD75xxx and μ PD78xxx product lines. Devices are connected in a master/slave configuration (see figure 8). There is only one master device at a time; all others

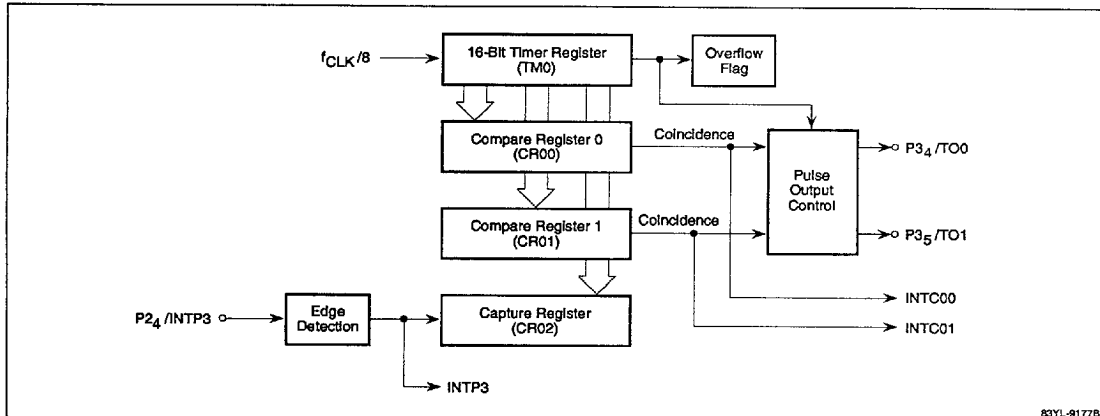
are slaves. The master sends addresses, commands, and data over the serial bus line (SB0) using a fixed hardware protocol synchronized with the SCK line. Each slave μ PD78218A family device can be programmed in software to respond to any one of 256 addresses. There are also 256 commands and 256 data types. Since all commands are user definable, any software protocol, simple or complex, can be defined. It is even possible to develop commands to change a slave into a master and the previous master into a slave.

Timers

The μ PD78218A family has one 16-bit timer and three 8-bit timers. The 16-bit timer counts the internal system clock ($f_{CLK}/8$) while the three 8-bit timers can be programmed to count a number of prescaled values of the internal system clock. One of the 8-bit timers can also count external events.

Timer 0 consists of a 16-bit timer (TM0), two 16-bit compare registers (CR00 and CR01), and a 16-bit capture register (CR02). Timer 0 can be used as two interval timers, to output a programmable square wave or two pulse-width modulated signals, to measure pulse widths, or to generate a software-triggered one-shot output pulse (see figure 9).

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Figure 9. 16-Bit Timer 0

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Timer 1 consists of an 8-bit timer (TM1), 8-bit compare register (CR10), and 8-bit capture/compare register (CR11). Timer 1 can be used as two interval timers or to measure pulse widths. In addition, it can be used to generate the output trigger for the real-time output port (see figure 10).

Timer/counter 2 consists of an 8-bit timer (TM2), two 8-bit compare registers (CR20 and CR21), and an 8-bit capture register (CR22). Timer/counter 2 can also be

used as two interval timers, to output a programmable square wave or two pulse-width modulated signals, or to measure pulse widths. In addition, it can be used to count external events sensed on the CI line or as a one-shot timer (see figure 11).

Timer 3 consists of an 8-bit timer (TM3) and an 8-bit compare register (CR30). Timer 3 can be used as an interval timer or as a clock for the clock-synchronized serial interface (see figure 12).

Figure 10. 8-Bit Timer 1

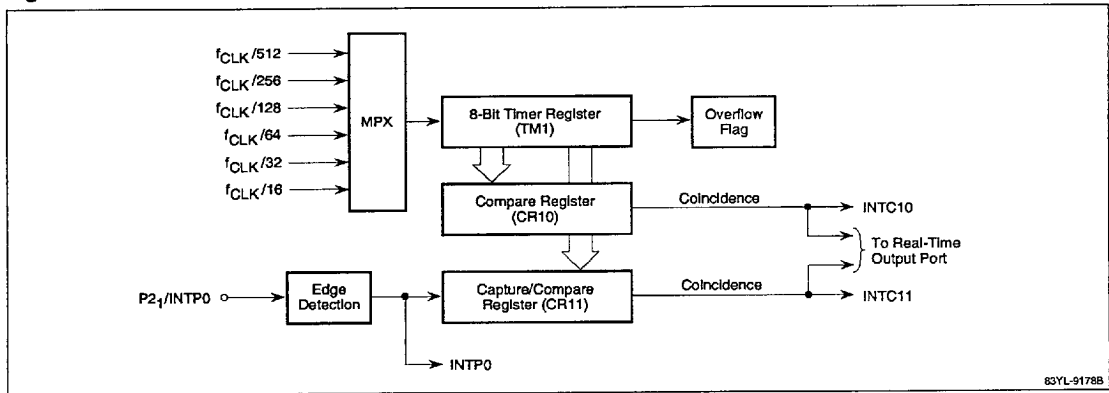


Figure 11. 8-Bit Timer/Counter 2

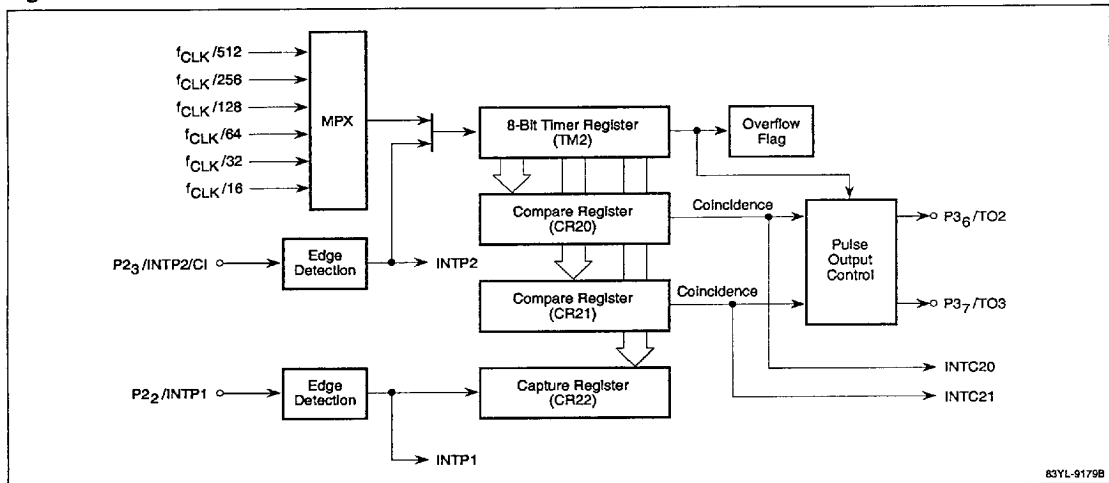
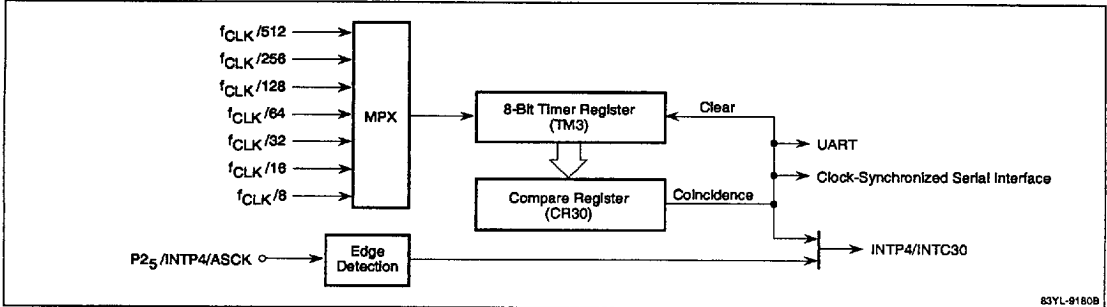


Figure 12. 8-Bit Timer 3



Interrupts

The μPD78218A family has 18 maskable hardware interrupt sources; 6 are external and 12 are internal. Since there are only 16 interrupt vectors and sets of control flags, 2 of the 6 external maskable interrupts, INTP4

and INTP5, share interrupt vectors and control flags with INTC30 and INTAD respectively. The active interrupt source for each shared vector must be chosen by the program. In addition, there is one nonmaskable interrupt and one software interrupt. The software interrupt, generated by the BRK instruction, is not maskable (see table 4).

Table 4. Interrupt Sources and Vector Addresses

Interrupt Request Type	Default Priority	Interrupt Request Generation Source	Macro Service Type	Vector Table Address
Software	None	BRK instruction execution	—	003EH
Nonmaskable	None	NMI (pin input edge detection)	—	0002H
Maskable	0	INTP0 (pin input edge detection)	A, B	0006H
	1	INTP1 (pin input edge detection)	A, B	0008H
	2	INTP2 (pin input edge detection)	A, B	000AH
	3	INTP3 (pin input edge detection)	B	000CH
	4	INTC00 (TM0-CR00 coincidence signal generation)	B	0014H
	5	INTC01 (TM0-CR01 coincidence signal generation)	B	0016H
	6	INTC10 (TM1-CR10 coincidence signal generation)	A, B, C	0018H
	7	INTC11 (TM1-CR11 coincidence signal generation)	A, B, C	001AH
	8	INTC21 (TM2-CR21 coincidence signal generation)	A, B	001CH
	9	INTP4 (pin input edge detection)	B	000EH
		INTC30 (TM3-CR30 coincidence signal generation)	A, B	
	10	INTP5 (pin input edge detection)	B	0010H
		INTAD (end of A/D conversion)	A, B	
	11	INTC20 (TM2-CR20 coincidence signal generation)	A, B	0012H
	12	INTSER (generation of asynchronous serial interface receive error)	—	0020H
	13	INTSR (end of asynchronous serial interface reception)	A, B	0022H
	14	INTST (end of asynchronous serial interface transmission)	A, B	0024H
	15	INTCSI (end of clocked serial interface transmission)	A, B	0026H

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Interrupt Servicing. The μPD78218A family provides two levels of programmable hardware priority control and two different methods of handling maskable interrupt requests: standard vectoring and macro service. The programmer can choose the priority and mode of servicing each maskable interrupt by using the interrupt control registers.

Interrupt Control Registers. The μPD78218A family has four 16-bit interrupt control registers. Each bit in each register is dedicated to one of the 16 active maskable interrupt sources. The interrupt request flag register (IF0) contains an interrupt request flag for each interrupt. The interrupt mask register (MK0) is used to enable or disable any interrupt. The interrupt service mode register (ISM0) specifies whether an interrupt is processed by vectoring or macro service. The priority flag register (PR0) can be used to specify a high or a low priority level for each interrupt.

Two other 8-bit registers are associated with interrupt processing. The interrupt status register (IST) indicates if a nonmaskable interrupt request on the NMI pin is being processed and can be used to allow nesting of nonmaskable interrupt requests. The IE and the ISP bits of the program status word are also used to control interrupts. If the IE bit is zero, all maskable interrupts, but not macro service, are disabled. The IE bit can be set or cleared using the EI and DI instructions, respectively, or by directly writing to the PSW. The IE bit is cleared each time an interrupt is accepted. The ISP bit is used by hardware to hold the priority level flag of the interrupt being serviced.

Interrupt Priority. The nonmaskable interrupt (NMI) has priority over all other interrupts. Two hardware controlled priority levels are available for the maskable interrupts. Either a high or a low priority level can be assigned by software to each of the maskable interrupts. Interrupt requests of a priority higher than the processor's current priority level are accepted; requests of the same or lower priority are held pending until the processor's priority state is lowered by program control within the current service routine or by a return instruction from the current service routine.

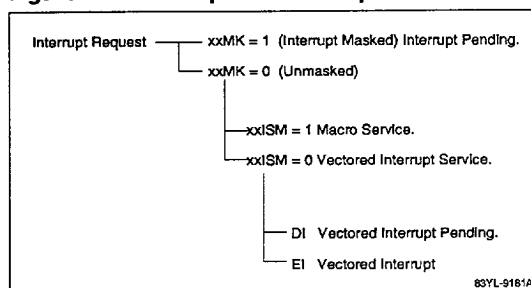
Interrupt requests programmed to be handled by macro service have priority over all vectored interrupt service regardless of the assigned priority level, and macro service requests are accepted even when the interrupt enable bit in the PSW is set to the disable state (see figure 13).

The default priorities listed in table 4 are fixed by hardware and are effective only when it is necessary to choose between two interrupt requests of the same

software assigned priority. For example, the default priorities would be used after the completion of a high priority routine, if two interrupts of the same priority routine were pending.

The software interrupt, initiated by the BRK instruction, is executed regardless of the processor's priority level and the state of the IE bit. It does not alter the processor's priority level.

Figure 13. Interrupt Service Sequence



Vectored Interrupt. When vectored interrupt is specified for a given interrupt request, (1) the program status word and the program counter are saved on the stack, (2) the processor's priority is set to that specified for the interrupt, (3) the IE bit in the PSW is set to zero, and (4) the routine whose address is in the interrupt vector table is entered. At the completion of the service routine, the RETI instruction (RETB instruction for the software interrupt) reverses the process and the μPD78218A family device resumes the interrupted routine.

Macro Service

When macro service is specified for a given interrupt, the macro service hardware temporarily stops the executing program and begins to transfer data between the special function register area and the memory space. One byte is transferred each interrupt. When the data transfer is complete, control is returned to the executing program, providing a completely transparent method of interrupt service. Macro service significantly improves response time and makes it unnecessary to save any registers.

For each request on the interrupt line, one operation is performed, and an 8- or 16-bit counter is decremented. When the counter reaches zero, a vectored interrupt service routine is entered according to the specified priority.

Macro service is provided for all of the maskable interrupt requests except INTSER, the asynchronous serial interface receive error interrupt request. Each interrupt request has a dedicated macro service control word stored in Internal RAM (see figure 14). The function to be performed is specified in the control word.

Figure 14. Macro Service Control Word Map

0FEDFH	Channel Pointer	} INTSR
0FEDEH	Mode Register	
0FEDDH	Channel Pointer	} INTST
0FEDCH	Mode Register	
0FEDBH	Channel Pointer	} INTCSI
0FEDA H	Mode Register	
0FED9H	Channel Pointer	} INTC10
0FED8H	Mode Register	
0FED7H	Channel Pointer	} INTC11
0FED6H	Mode Register	
0FED5H	Channel Pointer	} INTP4/INTC30
0FED4H	Mode Register	
0FED3H	Channel Pointer	} INTP5/INTAD
0FED2H	Mode Register	
0FED1H	Channel Pointer	} INTC00
0FED0H	Mode Register	
0FECFH	Channel Pointer	} INTC01
0FEC EH	Mode Register	
0FEC DH	Channel Pointer	} INTC20
0FEC CH	Mode Register	
0FECBH	Channel Pointer	} INTC21
0FEC AH	Mode Register	
0FEC9H	Channel Pointer	} INTP0
0FEC8H	Mode Register	
0FEC7H	Channel Pointer	} INTP1
0FEC6H	Mode Register	
0FEC5H	Channel Pointer	} INTP2
0FEC4H	Mode Register	
0FEC3H	Channel Pointer	} INTP3
0FEC2H	Mode Register	

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Table 5. Macro Service Type A Interrupts and Assigned SFRs

Interrupt Request	Source/Destination SFR
INTC10: TM1-CR10 coincidence	CR10: Timer 1 8-bit compare register
INTC11: TM1-CR11 coincidence	CR11: Timer 1 8-bit capture/compare register
INTC20: TM2-CR20 coincidence	CR20: Timer 2 8-bit compare register
INTC21: TM2-CR21 coincidence	CR21: Timer 2 8-bit compare register
INTC30: TM3-CR30 coincidence	CR30: Timer 3 8-bit compare register
INTSR: End of asynchronous serial interface reception	RxB: Serial receive buffer
INTST: End of asynchronous serial interface transmission	TxS: Serial transmit shift register
INTCSI: End of clocked serial interface transmission	SIO: Serial shift register
INTAD: End of A/D conversion	ADCR: A/D conversion result register
INTP0: External interrupt pin P0 ₁	CR11: Timer 1 8-bit capture/compare register
INTP1: External interrupt pin P0 ₂	CR22: Timer 2 8-bit capture register
INTP2: External interrupt pin P0 ₃	TM2: Timer 2 8-bit timer register

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Macro Service Type B. A byte of data is transferred in either direction between any specified special function register and a buffer anywhere in the 64K byte address space. The macro service counter can be programmed either to be an 8- or 16-bit counter. Macro service Type B transfers can be initiated by any maskable interrupt except INTSER.

Macro Service Type C. A byte of data is transferred from a buffer anywhere in the 64K byte address space to one of the 8-bit compare registers of timer 1. At the same time, a second byte of data is transferred from a buffer anywhere in the 64K byte address space to the real-time output port buffer. The macro service counter can be programmed either to be an 8- or 16-bit counter. Macro service Type C transfers can be initiated by INTC10 with data transferred to CR10 and P0L or P0H, or by INTC11 with data transferred to CR11 and P0L or P0H.

In addition, the macro service Type C transfer can be initialized to automatically alter timer compare register values or to repeatedly output a prespecified pattern at a fixed or variable rate. By using macro service Type C transfers to control the real-time output ports,

The μPD78218A family provides three different types of macro service transfers:

Macro Service Type A. A byte of data is transferred in either direction between a special function register, preassigned for each interrupt request, and a buffer in Internal RAM (FExx). Only the 8-bit macro service counter is available for Type A transfers. The preassigned SFRs for the 12 interrupt requests that support macro service Type A transfers are listed in table 5.

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the μ PD78218A family can easily and accurately drive two independent stepper motors.

Refresh

The refresh signal is used with any pseudostatic RAM equivalent of the NEC μ PD428128. The refresh cycle can be set to one of four intervals: 16, 32, 64, or $128/f_{\text{CLK}}$ (2.6, 5.3, 10.7, and 21.3 μ s at 12 MHz). The refresh cycle is timed to follow a read or write operation to avoid interference with external memory access cycles.

Standby Modes

HALT and STOP modes are provided to reduce power consumption when CPU action is not required. In HALT mode, the CPU is stopped but the system clock continues to run. The HALT mode is released by any unmasked interrupt, an external NMI, or an external reset pulse. In STOP mode, both the CPU and the system clock are stopped, further minimizing the power consumption. The STOP mode is released by either an external reset pulse or an external NMI. The

HALT and STOP modes are entered by programming the standby control register (STBC). This register is a protected location and can be written to only by a special instruction. If the third and fourth bytes of the instruction are not complements of each other, the data is not written and the next instruction is executed.

External Reset

The μ PD78218A family is reset by taking the $\overline{\text{RESET}}$ pin low. The $\overline{\text{RESET}}$ input pin contains a noise filter to protect against spurious system resets caused by noise. On power-up, the $\overline{\text{RESET}}$ pin must remain low until the power supply reaches its operating voltage and the oscillator has stabilized. During reset the program counter is loaded with the address contained in the reset vector table (address 0000H, 0001H); program execution starts at that address upon the $\overline{\text{RESET}}$ pin going high. While $\overline{\text{RESET}}$ is low, all external lines except V_{SS} , V_{DD} , AV_{SS} , AV_{REF} , X1, and X2 are in the high impedance state.

NEC**μPD78218A Family****ELECTRICAL SPECIFICATIONS****Absolute Maximum Ratings** $T_A = +25^{\circ}\text{C}$

Operating voltage, V_{DD}	-0.5 to +7.0 V
AV_{REF}	-0.5 to $V_{DD} + 0.5$ V
AV_{SS}	-0.5 to +0.5 V
Input voltage, V_{I1}	-0.5 to $V_{DD} + 0.5$ V
V_{I2} (Note 1)	-0.5 to $AV_{REF} + 0.5$ V
V_{I3} (Note 2 for μPD78P218A)	-0.5 to +13.5 V
Output voltage, V_O	-0.5 to $V_{DD} + 0.5$ V
Low-level output current, I_{OL}	
per pin	15 mA
total, all output pins	100 mA
High-level output current, I_{OH}	
per pin	-10 mA
total, all output pins	-50 mA
Operating temperature, T_{OPT}	-40 to +85°C
Storage temperature, T_{STG}	-65 to +150°C

Notes:

- (1) Pins $P7_0/AN0$ - $P7_5/AN5$, $P6_9/WAIT/AN6$, and $P6_7/REFRQ/AN7$ when used as the A/D converter input pins. However, the absolute maximum rating of V_{I1} must also be satisfied.
- (2) $P2_0/NMI$, EA/V_{pp} , and $P2_1/INTPO/Ag$ pins in the PROM programming mode

Exposure to absolute maximum ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC characteristics.

DC Characteristics $T_A = -40$ to $+85^{\circ}\text{C}$; $V_{SS} = 0$ V; $V_{DD} = +5$ V $\pm 10\%$ ($V_{DD} = +5$ V ± 0.3 V for μPD78P218A)

Item	Symbol	Min	Typ	Max	Unit	Conditions
Low-level input voltage	V_{IL}	0		0.8	V	
High-level input voltage	V_{IH1}	2.2		V_{DD}	V	Except the specified pins (Notes 1, 2)
	V_{IH2}	2.2		AV_{REF}	V	Specified pins (Note 1)
	V_{IH3}	0.8 V_{DD}		V_{DD}	V	Specified pins (Note 2)
Low-level output voltage	V_{OL1}			0.45	V	$I_{OL} = 2.0$ mA
	V_{OL2}			1.0	V	$I_{OL} = 8.0$ mA (Note 3)
High-level output voltage	V_{OH1}	$V_{DD} - 1.0$			V	$I_{OH} = -1.0$ mA
	V_{OH2}	$V_{DD} - 0.5$			V	$I_{OH} = -100$ μA
	V_{OH3}	2.0			V	$I_{OH} = -5.0$ mA (Note 4)
X1 low-level input current	I_{IL}			-100	μA	$0\text{V} \leq V_I \leq V_{IL}$
X1 high-level input current	I_{IH}			100	μA	$V_{IH3} \leq V_I \leq V_{DD}$
Input leakage current	I_{LI}			± 10	μA	$0\text{V} \leq V_I \leq V_{DD}$
Output leakage current	I_{LO}			± 10	μA	$0\text{V} \leq V_O \leq V_{DD}$
AV_{REF} current	AI_{REF}		1.5	5.0	mA	Operating mode, $f_{XX} = 12$ MHz
V_{DD} power supply current	I_{DD1}		20	40	mA	Operating mode, $f_{XX} = 12$ MHz
	I_{DD2}		7	20	mA	HALT mode, $f_{XX} = 12$ MHz

Operating Conditions

Oscillation Frequency, f_{XX}	T_A	V_{DD}
4 to 12 MHz	-40 to +85°C	+5 V $\pm 10\%$ (μPD78217A/218A), +5 V ± 0.3 V (μPD78P218A)

Capacitance $T_A = +25^{\circ}\text{C}$; $V_{DD} = V_{SS} = 0$ V

Item	Symbol	Max	Unit	Conditions
Input capacitance	C_I	20	pF	$f = 1$ MHz, pins not used for measurement are at 0 V
Output capacitance	C_O	20	pF	
Input/output capacitance	C_{IO}	20	pF	

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DC Characteristics (cont)

Item	Symbol	Min	Typ	Max	Unit	Conditions
Data retention voltage	V _{DDDR}	2.5		5.5	V	STOP mode
Data retention current	I _{DDDR}		2	20	μA	STOP mode; V _{DDDR} = 2.5 V
			5	50	μA	STOP mode; V _{DDDR} = 5 V ±10%
Pullup resistor	R _L	15	40	80	kΩ	V _I = 0 V

Notes:

- (1) Pins P7₀/AN0 - P7₅/AN5, P6₆/WA₁₇/AN6, and P6₇/REFRQ/AN7 when the pin is used as an A/D converter input pin.
- (2) X1, X2, RESET, P2₀/NMI, P2₁/INTP0, P2₂/INTP1, P2₃/INTP2/C1, P2₄/INTP3, P2₅/INTP4/ASCK, P2₆/INTP5, P2₇/SI, P3₂/SCK, P3₃/SO/SB0, and EA pins
- (3) Pins P4₀/AD₀ - P4₇/AD₇, and P5₀/A₈ - P5₇/A₁₅.
- (4) Pins P0₀ - P0₇.

AC Characteristics—Read/Write Operation

T_A = -40 to +85°C; V_{SS} = 0 V, f_{XX} = 12 MHz; C_L = 100 pF, V_{DD} = +5 V ±10% (V_{DD} = +5 V ±0.3 V for μPD78P218A)

Item	Symbol	Calculation Formula (2, 3)	Min	Max	Unit	Conditions
X1 input clock cycle time	t _{CYX}	—	82	250	ns	
Address setup time to ASTB ↓	t _{SAST}	t _{CYX} - 30	52		ns	
Address hold time from ASTB ↓ (Note 1)	t _{HSTA}	—	25		ns	
Address hold time from RD ↑	t _{HRA}	—	30		ns	
Address hold time from WR ↑	t _{HWA}	—	30		ns	
Address to RD ↓ delay time	t _{DAR}	2t _{CYX} - 35	129		ns	
Address float time to RD ↓	t _{FAR}	t _{CYX} /2 - 30	11		ns	
Address to data input time	t _{DAID}	(4+2n)t _{CYX} - 100		228	ns	No wait states
ASTB ↓ to data input time	t _{DSTID}	(3+2n)t _{CYX} - 65		181	ns	No wait states
RD ↓ to data input time	t _{DRID}	(2+2n)t _{CYX} - 64		100	ns	No wait states
ASTB ↓ to RD ↓ delay time	t _{DSTR}	t _{CYX} - 30	52		ns	
Data hold time from RD ↑	t _{HRID}	—	0		ns	
RD ↑ to address active time	t _{DRA}	2t _{CYX} - 40	124		ns	
RD ↑ to ASTB ↑ delay time	t _{DRST}	2t _{CYX} - 40	124		ns	
RD low-level width	t _{WRL}	(2+2n)t _{CYX} - 40	124		ns	No wait states
ASTB high-level width	t _{WSTH}	t _{CYX} - 30	52		ns	
Address to WR ↓ delay time	t _{DAW}	2t _{CYX} - 35	129		ns	
ASTB ↓ to data output time	t _{DSTOD}	t _{CYX} + 60		142	ns	
WR ↓ to data output time	t _{DWOD}	—		60	ns	
ASTB ↓ to WR ↓ delay time	t _{DSTW1}	t _{CYX} - 30	52		ns	
	t _{DSTW2}	2t _{CYX} - 35	129		ns	Refresh mode
Data setup time to WR ↑	t _{SODWR}	(3+2n)t _{CYX} - 100	146		ns	No wait states
Data setup time to WR ↓	t _{SODWF}	t _{CYX} - 60	22		ns	Refresh mode
Data hold time from WR ↑ (Note 1)	t _{HWOD}	—	20		ns	
WR ↑ to ASTB ↑ delay time	t _{DWST}	t _{CYX} - 40	42		ns	
WR low-level width	t _{WWL1}	(3+2n)t _{CYX} - 50	196		ns	No wait states
	t _{WWL2}	(2+2n)t _{CYX} - 50	114		ns	Refresh mode; No wait states
Address to WAIT ↓ input time	t _{DAWT}	3t _{CYX} - 100		146	ns	

AC Characteristics—Read/Write Operation (cont)

Item	Symbol	Calculation Formula (2, 3)	Min	Max	Unit	Conditions
ASTB $\downarrow$ to WAIT $\downarrow$ input time	t_{DSTWT}	$2t_{CYX} - 80$		84	ns	
WAIT hold time from ASTB $\downarrow$	t_{HSTWT}	$2Xt_{CYX} + 10$	174		ns	One external wait state
ASTB $\downarrow$ to WAIT $\uparrow$ delay time	t_{DSTWTH}	$2(1+X)t_{CYX} - 55$		273	ns	One external wait state
RD $\downarrow$ to WAIT $\downarrow$ input time	t_{DRWTL}	$t_{CYX} - 60$		22	ns	
WAIT hold time from RD $\downarrow$	t_{HRWT}	$(2X-1)t_{CYX} + 5$	87		ns	One external wait state
RD $\downarrow$ to WAIT $\uparrow$ delay time	t_{DRWTH}	$(2X+1)t_{CYX} - 60$		186	ns	One external wait state
WAIT $\uparrow$ to data input time	t_{DWTID}	$t_{CYX} - 20$		62	ns	
WAIT $\uparrow$ to WR $\uparrow$ delay time	t_{DWTW}	$2t_{CYX} - 10$	154		ns	
WAIT $\uparrow$ to RD $\uparrow$ delay time	t_{DWTR}	$t_{CYX} - 10$	72		ns	
WR $\downarrow$ to WAIT input time	t_{DWWTL}	$t_{CYX} - 60$		22	ns	Refresh disabled
WAIT hold time from WR $\downarrow$	t_{HWWT1}	$(2X-1)t_{CYX} + 5$	87		ns	One external wait state, refresh disabled
	t_{HWWT2}	$2(X-1)t_{CYX} + 5$	5		ns	One external wait state, refresh enabled
WR $\downarrow$ to WAIT $\uparrow$ delay time	t_{DWWTH1}	$(2X+1)t_{CYX} - 60$		186	ns	One external wait state; refresh disabled
	t_{DWWTH2}	$2Xt_{CYX} - 60$		104	ns	One external wait state; refresh enabled
RD $\uparrow$ to REFRQ $\downarrow$ delay time	t_{DRRFQ}	$2t_{CYX} - 10$	154		ns	
WR $\uparrow$ to REFRQ $\downarrow$ delay time	t_{DWRFQ}	$t_{CYX} - 10$	72		ns	
REFRQ low-level width	t_{WRFQL}	$2t_{CYX} - 44$	120		ns	
REFRQ $\uparrow$ to ASTB $\uparrow$ delay time	t_{DRFQST}	$4t_{CYX} - 48$	280		ns	

Notes:

(1) The hold time includes the time during which V_{OH} and V_{OL} are retained under the following load conditions: $C_L = 100$ pF and $R_L = 2$ k Ω .

(2) n indicates the number of internal wait states.

(3) X indicates the number of external wait states (1, 2, 3, ...)

Serial Port Operation

$T_A = -40$ to $+85^\circ\text{C}$; $V_{SS} = 0$ V; $f_{XX} = 12$ MHz; $C_L = 100$ pF; $V_{DD} = +5$ V $\pm 10\%$ ($V_{DD} = +5$ V ± 0.3 V for μ PD78P218A)

Item	Symbol	Min	Max	Unit	Conditions
Serial clock cycle time	t_{CYSK}	1.0		μ s	External clock input
		1.3		μ s	Internal clock/16 output
		5.3		μ s	Internal clock/64 output
Serial clock low-level width	t_{WSKL}	420		ns	External clock input
		556		ns	Internal clock/16 output
		2.5		μ s	Internal clock/64 output
Serial clock high-level width	t_{WSKH}	420		ns	External clock input
		556		ns	Internal clock/16 output
		2.5		μ s	Internal clock/64 output
SI, SBO setup time to $\overline{\text{SCK}}$ $\uparrow$	t_{SSK}	150		ns	
SI, SBO hold time from $\overline{\text{SCK}}$ $\uparrow$	t_{HSSK}	400		ns	

μPD78218A Family**NEC****Serial Port Operation (cont)**

Item	Symbol	Min	Max	Unit	Conditions
SO/SB0 output delay time from SCK ↓	t _{DSBSK1}	0	300	ns	CMOS push-pull output (3-line serial I/O mode)
	t _{DSBSK2}	0	800	ns	Open-drain output (SBI mode), R _L = 1 kΩ
SB0 high, hold time from SCK ↑	t _{HSBSK}	4		t _{CYX}	SBI mode
SB0 low, setup time to SCK ↓	t _{SSBSK}	4		t _{CYX}	SBI mode
SB0 low-level width	t _{WSBL}	4		t _{CYX}	
SB0 high-level width	t _{WSBH}	4		t _{CYX}	

A/D Converter Operation

T_A = -40 to +85°C; V_{SS} = AV_{SS} = 0 V; V_{DD} = +5 V ±10% (V_{DD} = +5 V ±0.3 V for μPD78P218A)

Item	Symbol	Min	Typ	Max	Unit	Conditions
Resolution		8			Bit	
Full-scale error *				0.4	%	AV _{REF} = 4.0 V to V _{DD} , T _A = -10 to +70°C
				0.8	%	AV _{REF} = 3.6 V to V _{DD} , T _A = -10 to +70°C
				0.8	%	AV _{REF} = 4.0 V to V _{DD}
Quantization error				±1/2	LSB	
Conversion time	t _{CONV}	360			t _{CYX}	82 ns ≤ t _{CYX} < 125 ns (FR bit of ADM register is 0)
		240			t _{CYX}	125 ns ≤ t _{CYX} < 250 ns (FR bit of ADM register is 1)
Sampling time	t _{SAMP}	72			t _{CYX}	82 ns ≤ t _{CYX} < 125 ns (FR bit of ADM register is 0)
		48			t _{CYX}	125 ns ≤ t _{CYX} < 250 ns (FR bit of ADM register is 1)
Analog input voltage	V _{IAN}	-0.3		AV _{REF} + 0.3	V	
Analog input impedance	R _{IAN}		1000		MΩ	
Analog reference voltage	AV _{REF}	3.6		V _{DD}	V	
AV _{REF} current	AI _{REF}		1.5	5.0	mA	Operating mode, f _{XX} = 12 MHz
			0.2	1.5	mA	STOP mode

* Quantization error is not included. Unit is defined as percent of full-scale value

Interrupt Timing Operation

T_A = -40 to +85°C; V_{SS} = 0 V, V_{DD} = +5 V ±10% (V_{DD} = +5 V ±0.3 V for μPD78P218A)

Item	Symbol	Min	Max	Unit	Conditions
NMI low-level width	t _{WNIL}	10		μs	
NMI high-level width	t _{WNIH}	10		μs	
INTP0-INTP5 low-level width	t _{WITL}	24		t _{CYX}	
INTP0-INTP5 high-level width	t _{WITH}	24		t _{CYX}	
RESET low-level width	t _{WRSL}	10		μs	
RESET high-level width	t _{WRSH}	10		μs	

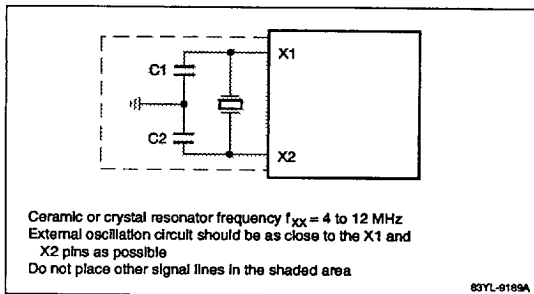
Data Retention Characteristics

$T_A = -40$ to $+85^\circ\text{C}$

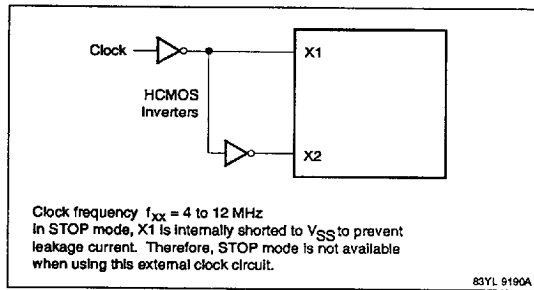
Item	Symbol	Min	Typ	Max	Unit	Conditions
Data retention voltage	V_{DDDR}	2.5		5.5	V	STOP mode
Data retention current	I_{DDDR}		2	20	μA	$V_{DDDR} = 2.5\text{ V}$
			5	50	μA	$V_{DDDR} = 5\text{ V} \pm 10\%$
V_{DD} rise time	t_{RVD}	200			μs	
V_{DD} fall time	t_{FVD}	200			μs	
V_{DD} retention time (from STOP mode setting)	t_{HVD}	0			ms	
STOP release signal input time	t_{DREL}	0			ms	
Oscillation stabilization wait time	t_{WAIT}	30			ms	Crystal resonator
		5			ms	Ceramic resonator
Low-level input voltage	V_{IL}	0		$0.1 V_{DDDR}$	V	Specified pins *
High-level input voltage	V_{IH}	$0.9 V_{DDDR}$		V_{DDDR}	V	Specified pins *

* RESET, $P2_0/\text{NMI}$, $P2_1/\text{INTP0}$, $P2_2/\text{INTP1}$, $P2_3/\text{INTP2/C1}$, $P2_4/\text{INTP3}$, $P2_5/\text{INTP4/ASCK}$, $P2_6/\text{ASCK}$, $P2_6/\text{INTP5}$, $P2_7/\text{SI}$, $P3_2/\text{SCK}$, $P3_3/\text{SO/ SB0}$, and $\overline{\text{EA}}$ pins.

Recommended Resonator Circuit



Recommended External Clock Circuit



Recommended Ceramic Resonators (μPD78217A/218A only)

Manufacturer	Frequency (MHz)	Part Number	C1 (pF)	C2 (pF)
Murata Mfg.	12	CSA12.0MTZ	30	30
		CST12.0MTW	None*	None*

*C1 and C2 are contained in the resonator.

External Clock Operation

$T_A = -40$ to $+85^\circ\text{C}$; $V_{DD} = +5\text{ V} \pm 10\%$; $V_{SS} = 0\text{ V}$

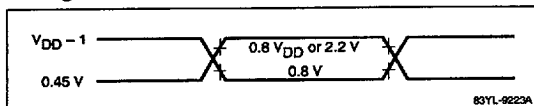
Item	Symbol	Min	Max	Unit	Conditions
X1 input low-level width	t_{WXL}	30	130	ns	
X1 input high-level width	t_{WXH}	30	130	ns	
X1 input rise time	t_{XR}	0	30	ns	
X1 input fall time	t_{XF}	0	30	ns	
X1 input clock cycle time	t_{CYX}	82	250	ns	

μ PD78218A Family

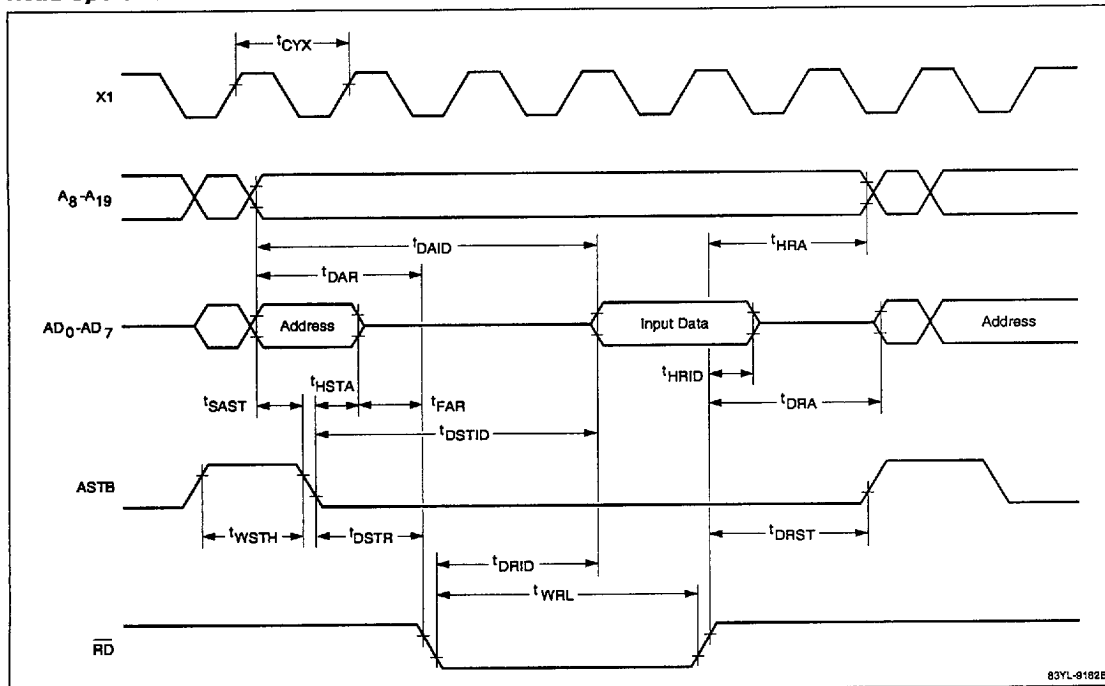
NEC

Timing Waveforms

Voltage Thresholds for AC Timing Measurements

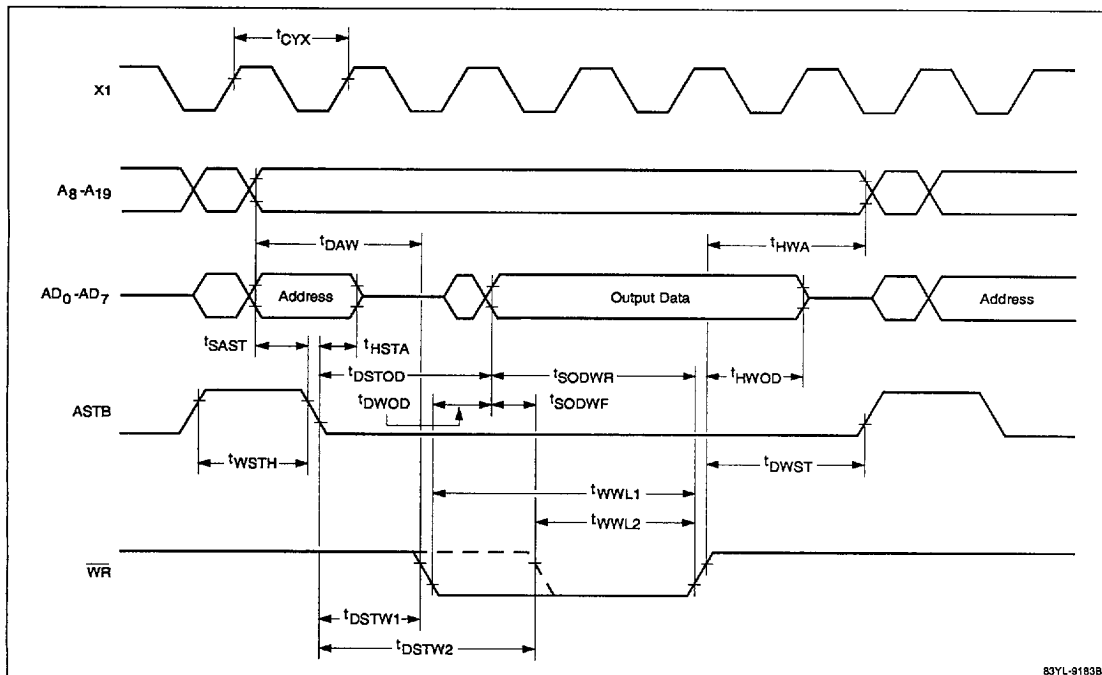


Read Operation



Timing Waveforms (cont)

Write Operation



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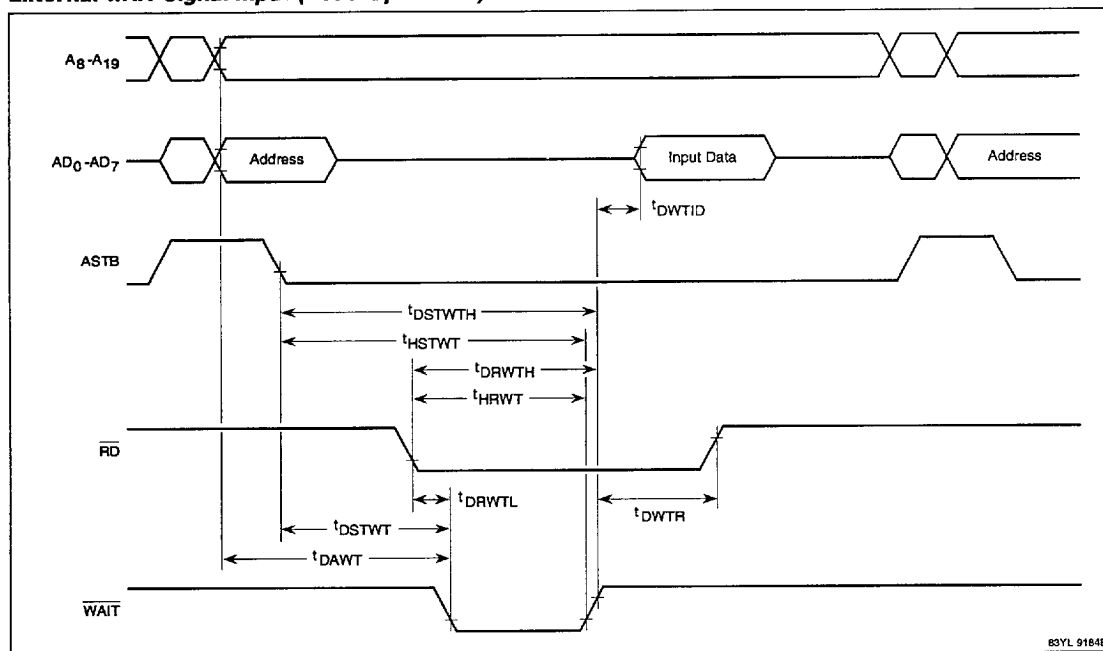
4b

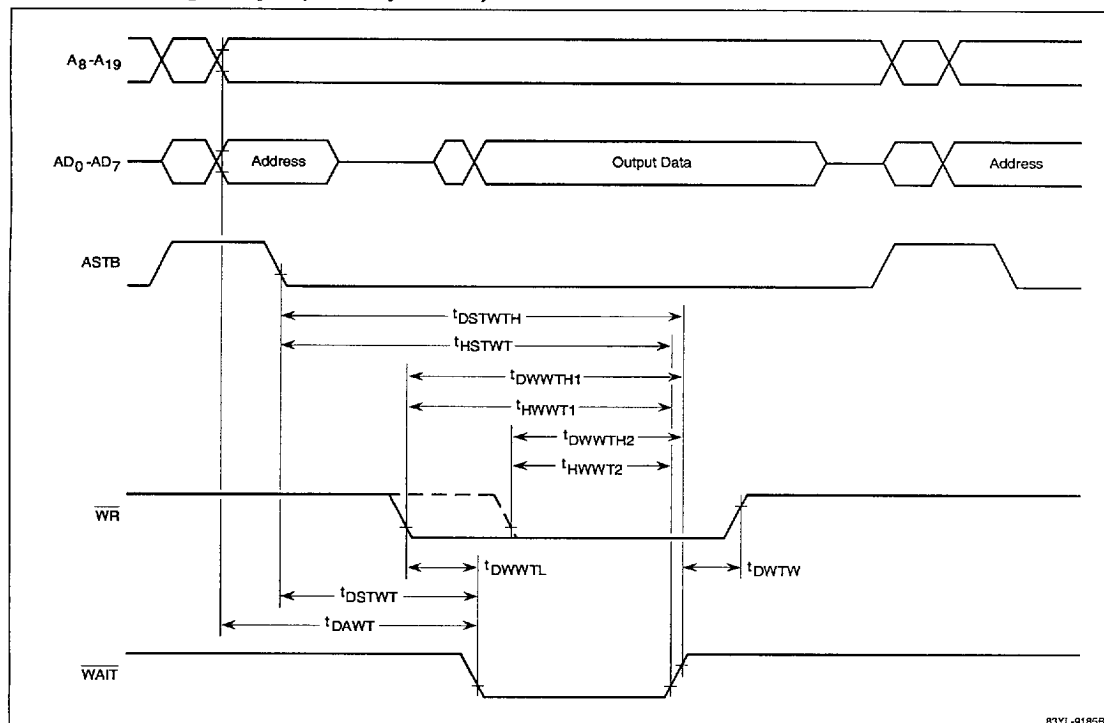
μPD78218A Family

NEC

Timing Waveforms (cont)

External WAIT Signal Input (Read Operation)



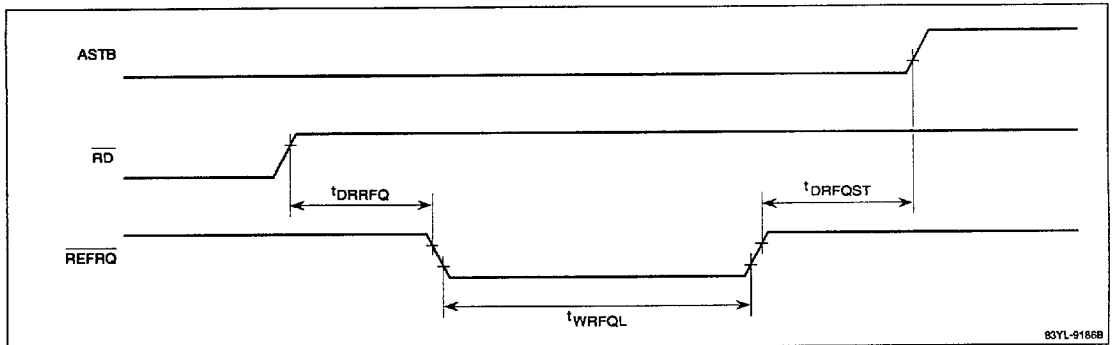
NEC **μ PD78218A Family****Timing Waveforms (cont)****External $\overline{\text{WAIT}}$ Signal Input (Write Operation)****4b**

μPD78218A Family

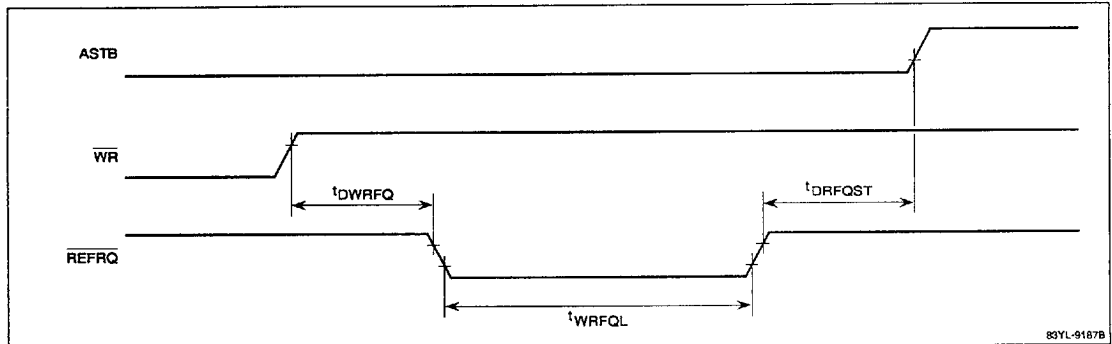
NEC

Timing Waveforms (cont)

Refresh After Read

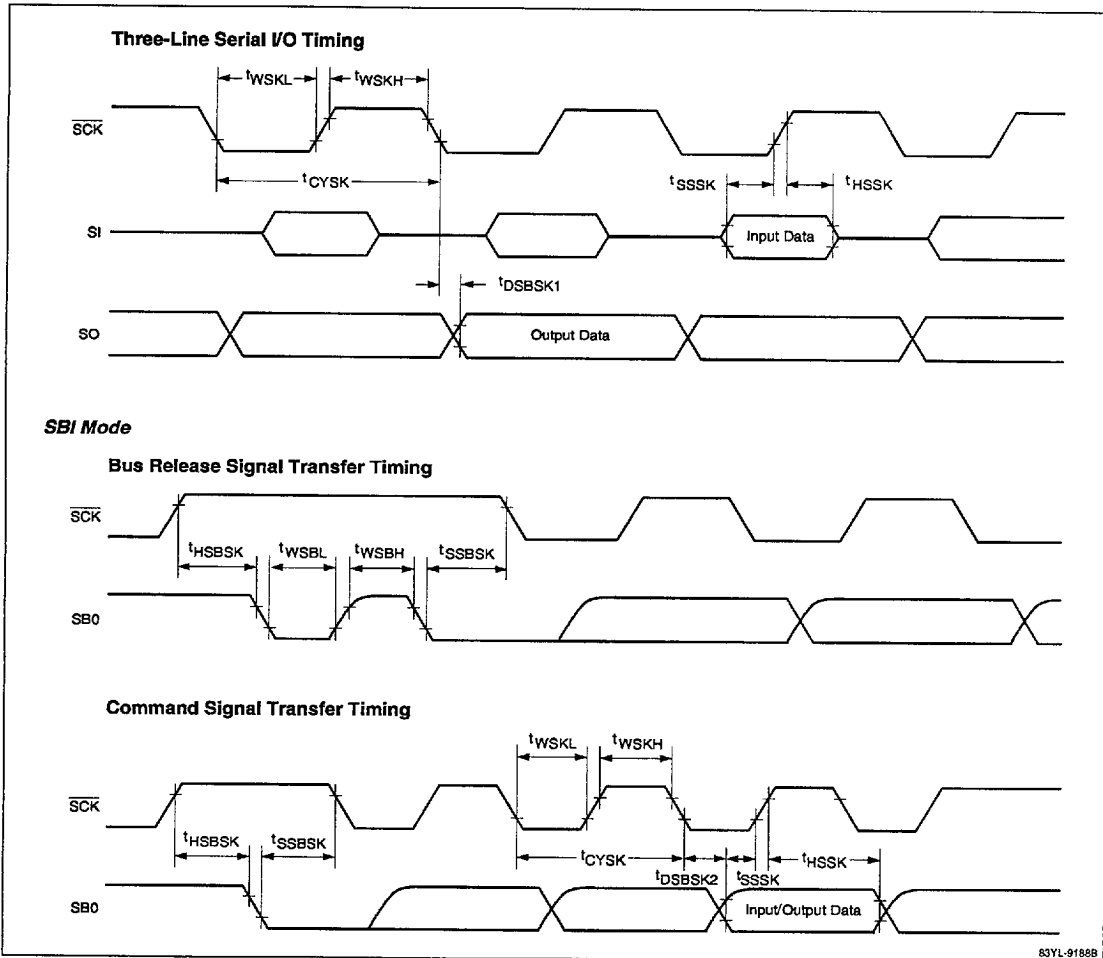


Refresh After Write

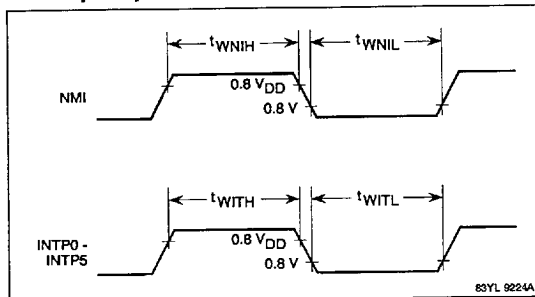
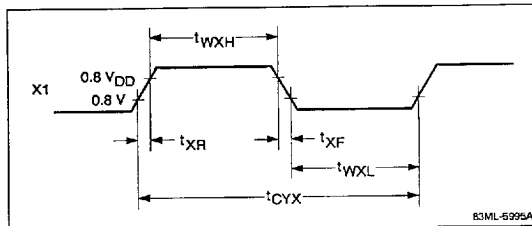
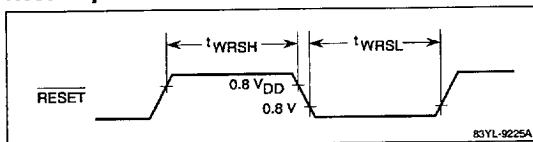
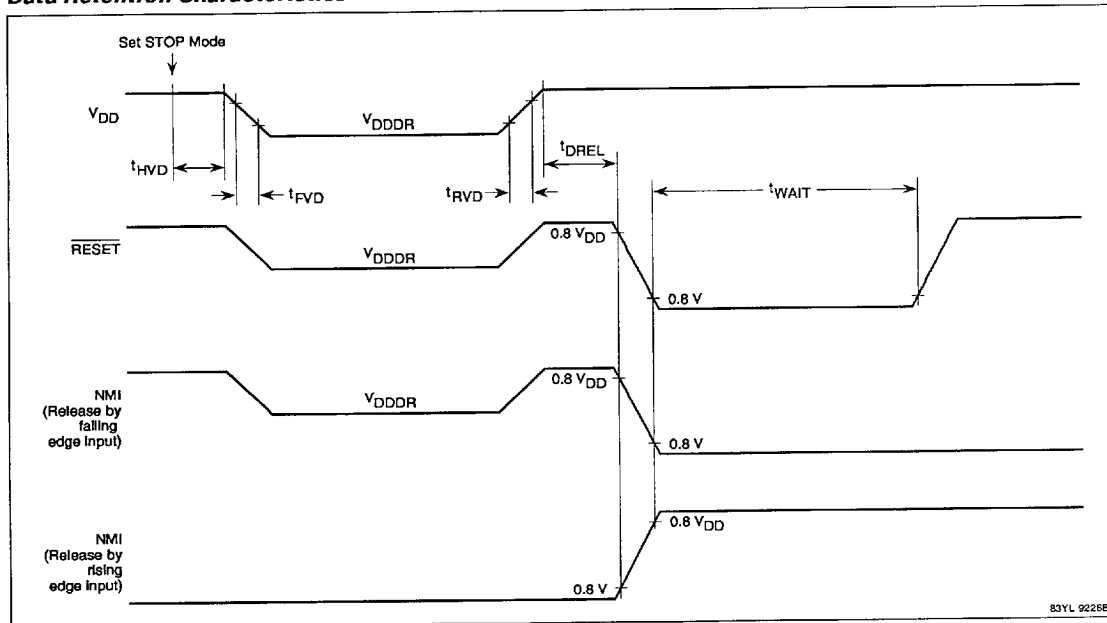


Timing Waveforms (cont)

Serial Operation



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μ PD78218A Family**NEC****Timing Waveforms (cont)****Interrupt Input****External Clock****Reset Input****Data Retention Characteristics**

NEC**μPD78218A Family****μPD78P218A PROGRAMMING**

In the μPD78P218A, the mask ROM of μPD78218A is replaced by a one-time programmable ROM (OTP ROM) or a reprogrammable, ultraviolet erasable ROM (UV EPROM). The ROM is 32,768 x 8 bits and can be programmed using a general-purpose PROM writer with a μPD27C256A programming mode.

The PA-78P214CW/GC are the socket adaptors used for configuring the μPD78P218A to fit a standard PROM socket.

Refer to tables 6 and 7 and figures 15 and 16 for special information applicable to PROM programming.

Table 6. Pin Functions During PROM Programming

Pin	Pin*	Function
P0 ₀ - P0 ₇	A ₀ - A ₇	Address input pins for PROM operations
P5 ₀ /A ₈	A ₈	Address input pin for PROM operations
P2 ₁ /INTP0	A ₉	Address input pin for PROM operations
P5 ₂ /A ₁₀ - P5 ₆ /A ₁₄	A ₁₀ - A ₁₄	Address input pins for PROM operations

Table 6. Pin Functions During PROM Programming (cont)

Pin	Pin*	Function
P4 ₀ /AD ₀ - P4 ₇ /AD ₇	D ₀ - D ₇	Data pins for PROM operations
P6 ₅ /WR	CE	Strobes data into the PROM
P6 ₄ /RD	OE	Enables a data read from the PROM
P2 ₀ /NMI	NMI	PROM programming mode is entered by applying +12.5 volts to this pin
RESET	RESET	PROM programming mode requires applying a low voltage to this pin
EA	V _{PP}	High voltage applied to this pin for program write/verify
V _{DD}	V _{DD}	Positive power supply pin
V _{SS}	V _{SS}	Ground

*Pin name in PROM programming mode.

Table 7. Summary of Operation Modes for PROM Programming

Mode	NMI	RESET	CE	OE	V _{PP}	V _{DD}	D ₀ - D ₇
Program write	+12.5 V	L	L	H	+12.5 V	+6 V	Data input
Program verify	+12.5 V	L	H	L	+12.5 V	+6 V	Data output
Program inhibit	+12.5 V	L	H	H	+12.5 V	+6 V	High Z
Read out	+12.5 V	L	L	L	+5 V	+5 V	Data output
Output disable	+12.5 V	L	L	H	+5 V	+5 V	High Z
Standby	+12.5 V	L	H	L/H	+5 V	+5 V	High Z

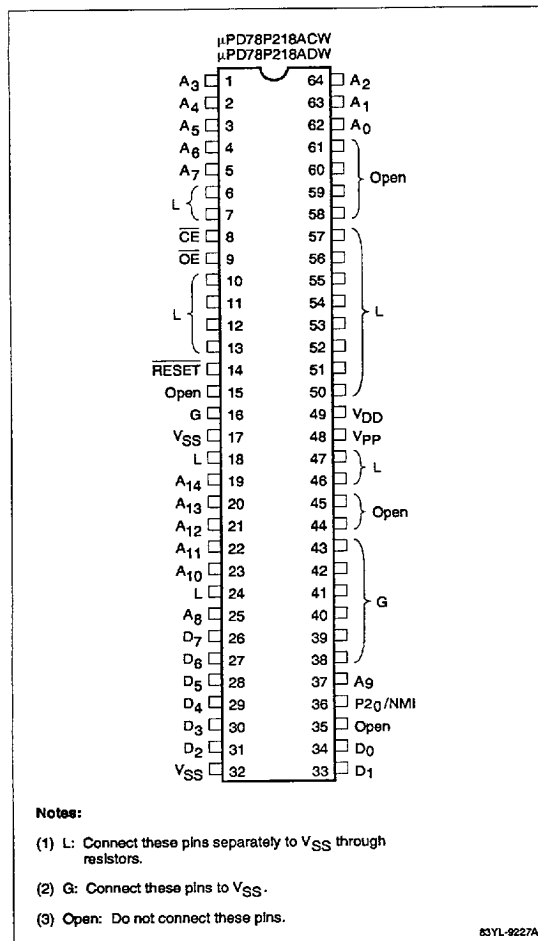
Note: When +12.5 V is applied to V_{PP} and +6 V to V_{DD}, both CE and OE cannot be set to low level (L) simultaneously.

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μPD78218A Family

NEC

Figure 15. Pin Functions in μPD78P218A PROM Programming Mode; 64-Pin Plastic and Ceramic Shrink DIP, 64-Pin Plastic QUIP



PROM Write Procedure

- (1) Set the pins not used for programming as indicated in figures 15 and 16. Connect the RESET pin to a low level, the V_{DD} and V_{PP} pins to +5 V, and apply +12.5 V to the NMI pin. The CE and OE pins should be high.
- (2) Apply +6 V to the V_{DD} pin and +12.5 V to the V_{PP} pin.
- (3) Provide the initial address to the A₀ to A₁₄ pins.

- (4) Provide write data.
- (5) Provide 1-ms program pulse (active low) to the CE pin.
- (6) This data is now verified with a pulse (active low) to the OE pin. If the data has been written, proceed to step 8; if not, repeat steps 4 to 6. If the data cannot be correctly written after 25 attempts, go to step 7.
- (7) Classify as defective and stop write operation.
- (8) Provide write data and supply program pulse (for additional writing) for 3 ms times the number of writes performed in step 5.
- (9) Increment the address.
- (10) Repeat steps 4 to 9 until the end address.

PROM Read Procedure

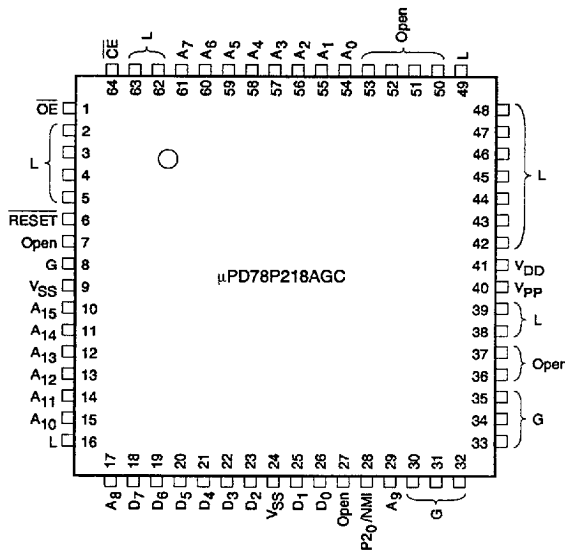
- (1) Set the pins not used for programming as indicated in figures 15 and 16. Fix the RESET pin to a low level, the V_{DD} and V_{PP} pins to +5 V, and apply +12.5 V to the NMI pin. The CE and OE pins should be high.
- (2) Input the address of the data to be read to pins A₀-A₁₄.
- (3) Read mode is entered with a pulse (active low) on both the CE and OE pins.
- (4) Data is output to the D₀ to D₇ Pins.

EPROM Erasure

Data in an EPROM is erased by exposing the quartz window in the ceramic package to light having a wavelength shorter than 400 nm, including ultraviolet rays, direct sunlight, and fluorescent light. To prevent unintentional erasure, mask the window.

Typically, data is erased by 254-nm ultraviolet rays. A minimum lighting level of 15 Ws/cm² (ultraviolet ray intensity x exposure time) is required to completely erase written data. Erasure by an ultraviolet lamp rated at 12 mW/cm² takes approximately 15 to 20 minutes. Remove any filter on the lamp and place the device within 2.5 cm of the lamp tubes.

Figure 16. Pin Functions in μPD78P218A PROM Programming Mode; 64-Pin Plastic QFP



Notes:

- (1) L: Connect these pins separately to V_{SS} through resistors.
- (2) G: Connect these pins to V_{SS} .
- (3) Open: Do not connect these pins.

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DC Programming Characteristics

$T_A = 25 \pm 5^\circ\text{C}$; $V_{IP} = 12.5 \pm 0.5\text{ V}$ applied to NMI pin; $V_{SS} = 0\text{ V}$

Parameter	Symbol	Symbol*	Min	Typ	Max	Unit	Condition
High-level input voltage	V_{IH}	V_{IH}	2.4		$V_{DDP} + 0.3$	V	
Low-level input voltage	V_{IL}	V_{IL}	-0.3		0.8	V	
Input leakage current	I_{LIP}	I_{LI}			10	μA	$0 \leq V_I \leq V_{DDP}$
High-level output voltage	V_{OH1}	V_{OH1}	2.4			V	$I_{OH} = -400\text{ }\mu\text{A}$
	V_{OH2}	V_{OH2}	$V_{DD} - 0.7$			V	$I_{OH} = -100\text{ }\mu\text{A}$
Low-level output voltage	V_{OL}	V_{OL}			0.45	V	$I_{OL} = 2.1\text{ mA}$
Output leakage current	I_{LO}				10	μA	$0 \leq V_O \leq V_{DDP}$, $\overline{OE} = V_{IH}$
NMI pin high-voltage input current	I_{IP}				± 10	μA	
V_{DDP} power voltage	V_{DDP}	V_{CC}	5.75	6.0	6.25	V	Program memory write mode
			4.5	5.0	5.5	V	Program memory read mode
			12.2	12.5	12.8	V	Program memory write mode
V_{PP} power voltage	V_{PP}	V_{PP}				V	Program memory read mode
				$V_{PP} = V_{DDP}$		V	Program memory read mode

μPD78218A Family**NEC****DC Programming Characteristics (cont)**

Parameter	Symbol	Symbol*	Min	Typ	Max	Unit	Condition
V _{DDP} power current	I _{DDP}	I _{CC}		5	30	mA	Program memory write mode
				5	30	mA	Program memory read mode CE = V _{IL} , V _I = V _{IH}
V _{PP} power current	I _{PP}	I _{PP}		5	30	mA	Program memory write mode CE = V _{IL} , OE = V _{IH}
				1	100	μA	Program memory read mode

*Corresponding symbols of the μPD27C256A.

AC Programming Characteristics (Write Mode)T_A = 25 ± 5°C; V_{IP} = 12.5 ± 0.5 V applied to NMI pin; V_{SS} = 0 V; V_{DD} = 6 ± 0.25 V; V_{PP} = 12.5 ± 0.3 V

Parameter	Symbol	Symbol*	Min	Typ	Max	Unit	Conditions
Address setup time to $\overline{CE}$ ↓	t _{SAC}	t _{AS}	2			μs	
Data input to $\overline{OE}$ ↓ delay time	t _{DDO0}	t _{OES}	2			μs	
Input data setup time to $\overline{CE}$ ↓	t _{SIDC}	t _{DS}	2			μs	
Address hold time from $\overline{CE}$ ↑	t _{HCA}	t _{AH}	2			μs	
Input data hold time from $\overline{CE}$ ↑	t _{HCID}	t _{DH}	2			μs	
Output data hold time from $\overline{OE}$ ↑	t _{HOOD}	t _{DF}	0		130	ns	
V _{PP} setup time to $\overline{CE}$ ↓	t _{SVPC}	t _{VPS}	1			ms	
V _{DDP} setup time to $\overline{CE}$ ↓	t _{SVDC}	t _{VCS}	1			ms	
Initial program pulse width	t _{WL1}	t _{pw}	0.95	1.0	1.05	ms	
Additional program pulse width	t _{WL2}	t _{OPW}	2.85		78.75	ms	
NMI high-voltage input setup time to $\overline{CE}$ ↓	t _{SPC}		2			μs	
$\overline{OE}$ ↓ to data output time	t _{DOOD}	t _{OE}			150	ns	

*Corresponding symbols of the μPD27C256A.

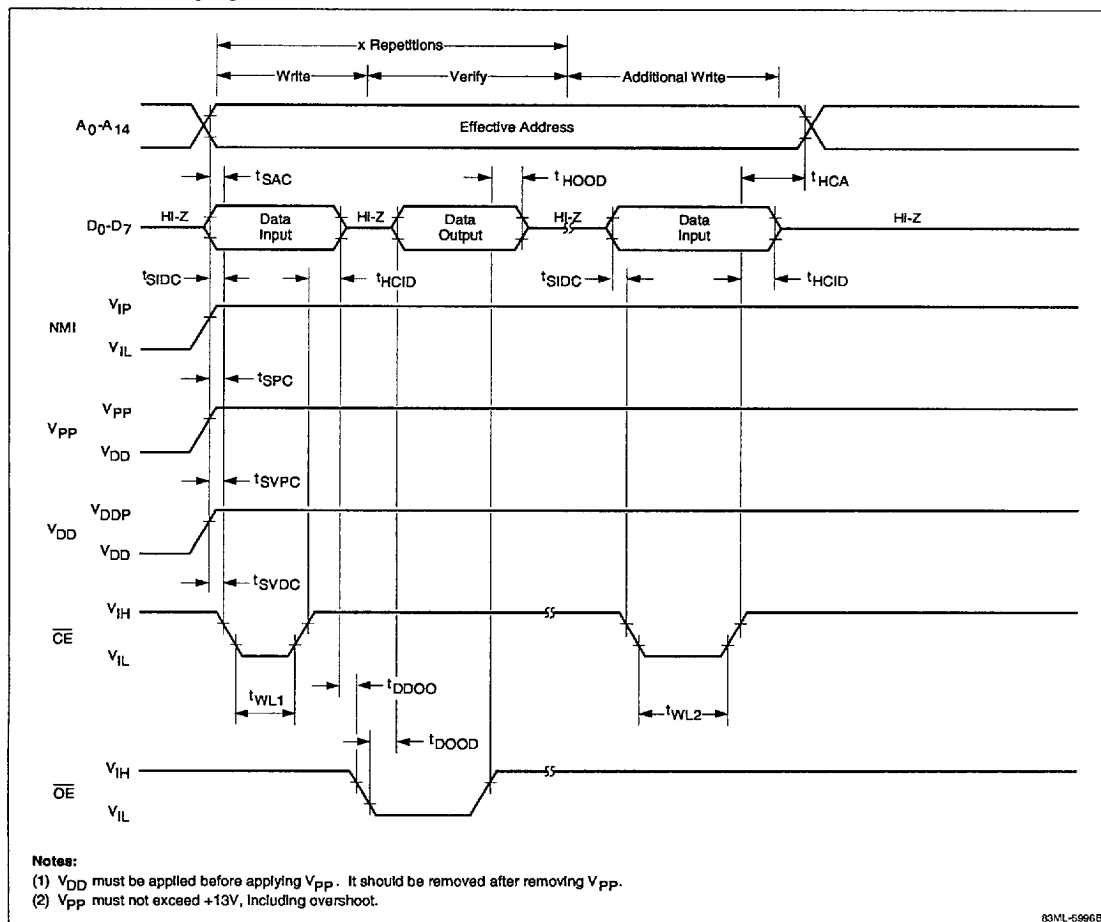
AC Programming Characteristics (Read Mode)T_A = 25 ± 5°C; V_{IP} = 12.5 ± 0.5 V applied to NMI pin; V_{SS} = 0 V; V_{DD} = 5 ± 0.5 V; V_{PP} = V_{DDP}

Parameter	Symbol	Symbol*	Min	Typ	Max	Unit	Condition
Address to data output time	t _{DAOD}	t _{ACC}			200	ns	$\overline{CE} = \overline{OE} = V_{IL}$
$\overline{CE}$ ↓ to data output time	t _{DCOD}	t _{CE}			200	ns	$\overline{OE} = V_{IL}$
$\overline{OE}$ ↓ to data output time	t _{DOOD}	t _{OE}			75	ns	$\overline{CE} = V_{IL}$
Data hold time from $\overline{OE}$ ↑	t _{HCOD}	t _{DF}	0		60	ns	$\overline{CE} = V_{IL}$
Data hold time from address	t _{HAOD}	t _{OH}	0			ns	$\overline{CE} = \overline{OE} = V_{IL}$

* Corresponding symbols of the μPD27C256A.

PROM Timing Diagrams

PROM Write/Verifying Mode



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μPD78218A Family

NEC

PROM Read Mode

