NEC

Design Manual

CB-9 Family
VX/VM Type

0.35 μm CMOS Cell-Based IC

Memory Macro (Compiled Type)

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[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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MAJOR REVISIONS IN THIS EDITION

Page	Description
pp. 71 of previous edition	**CHAPTER 4 HIGH-SPEED DUAL-PORT (1R/W + 1R/W) RAM (SYNCHRONOUS TYPE)** was deleted.
p. 18	**Table 1-2 Typical Values of Memory Macros (8 bits × 512 words)** was changed.
p. 33	**1.8 Notes on Using Each Macro** was added.
p. 134	**8.4 Macro Size** was chagned.
p. 155	**Table A-7 High-Speed ROM (Synchronous Type)** was changed.

The mark ★ shows major revised points.

PREFACE

This manual describes the general information, design technique, and points to be noted when you design circuits using the memory macros (compiled type) of the CB-9 Family VX/VM Type.

Thoroughly read this manual to smoothly design LSIs.
Be sure to observe the points described in this manual (general information, notes, and limitations); otherwise, the quality and performance of the LSI may be degraded or malfunction may occur.

For the overall circuit designing, **CB-9 Family VX/VM Type Design Manual (A12745E)** is also available. Please read it first, and then read this manual.

If you require an application where the restrictions described in this manual are not observed, or if you have any questions, consult NEC.

Related documents

Some of the related documents listed below are preliminary editions but not so specified here.

CB-9 Family VX/VM Type Design Manual	(A12745E)
CB-9 Family VX/VM Type Memory Macro (Compiled Type) Design Manual	(This manual)
CB-9 Family VX/VM Type Memory Macro (Fixed Type) Design Manual	(A13899E)
CB-9 Family VX/VM Type Analog Macro (High-Speed D/A Converter) Design Manual	(A13820E)
CB-9 Family VX/VM Type Analog Macro (PLL) Design Manual	(A13947E)
CB-9 Family VX/VM Type Analog Macro (General-purpose A/D, D/A Converter) Design Manual	(A14021E)
CB-9 Family VX/VM Type CPU, Peripheral Design Manual	(A14304E)
CB-9 Family VX/VM Type CPU Core, Memory Controller Design Manual	(A13195E)
CB-9 Family VX/VM Type (CMOS 3.3V) Block Library	(A12793E)
CB-9 Family VX/VM Type (CMOS 2.0V) Block Library	(A12794E)
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Design For Test User's Manual	(A14357E)

When designing your system, be sure to use the latest documents.
Contact your local NEC sales office or representative office.

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CHAPTER 1 OVERVIEW

1.1 General

The memory macros of the CB-9 family VX/VM type are the compiled type and fixed type of macros.
A compiled type memory macro can automatically/generate a memory of the size suitable to your system by using software called a memory compiler.
For the details of the fixed-type memory macro, refer to **CB-9 Family VX/VM Type Memory Macro (Fixed Type) Design Manual (A13899E)**.

1.2 Types of Memory Macros

For the CB-9 family VX/VM type, seven types of memory macros are provided as shown in Table 1-1.
Select the macro best-suited to your system, taking into consideration the features of each type of memory and your application.

Table 1-1 Types of Memory Macros

Type	Compiled Range	Remark
High-speed single-port RAM (synchronous type)	1 to 32 bits, 32 to 2K words (variable in 1-bit/8-word units)	I/O separation type
High-speed dual-port (1R/W + 1R) RAM (synchronous type)	1 to 32 bits, 32 to 2K words (variable in 1-bit/16-word units)	I/O separation type
High-density single-port RAM (synchronous type)	1 to 32 bits, 32 to 8K words (variable in 1-bit/32-word units)	I/O separation type
High-density dual-port (1R + 1W) RAM (synchronous type)	1 to 32 bits, 32 to 1K words (variable in 1-bit/8-word units)	–
Super high-speed single-port RAM (synchronous type)	1 to 16 bits, 64 to 1K words (variable in 1-bit/64-word units)	I/O separation type
Register file (dual-port)	4 to 64 bits, 8 to 512 words (variable in 1-bit/4-word units)	–
High-speed ROM (synchronous type)	1 to 64 bits, 64 to 8K words (variable in 1-bit/32-word units)	–

Table 1-2 Typical Values of Memory Macros (8 bits × 512 words)

Type	Note 1 Number of Grids	Note 2 Access Time (t_{ACC})		Cycle Time (t_{RC})	
		3.3 V	2.0 V	3.3 V	2.0 V
High-speed single-port RAM (synchronous type)	37440	3.68 ns	8.24 ns	6.32 ns	14.40 ns
High-speed dual-port (1R/W + 1R) RAM (synchronous type)	59675	3.80 ns	–	7.46 ns	–
High-density single-port RAM (synchronous type)	26460	8.06 ns	17.77 ns	9.14 ns	19.22 ns
High-density dual-port (1R + 1W) RAM (synchronous type)	54239	7.45 ns	19.08 ns	14.10 ns	36.20 ns
Super high-speed single-port RAM (synchronous type)	37115	2.98 ns	–	3.98 ns	–
Register file (dual-port)	60680	Note 3 18.63 ns	Note 3 41.51 ns	Note 4 18.56 ns	Note 4 41.37 ns
★ High-speed ROM (synchronous type)	15834	5.53 ns	12.74 ns	8.86 ns	17.36 ns

Notes 1. Including macro circumferential wiring area
2. External capacitance is calculated as 0.2 pF.
3. Read access time (t_{RA})
4. Read cycle time (t_{RC})

1.3 Macro Area

The macro area is a function of the number of grids used.
The number of grids is the index which indicates the circuit area for a cell-based IC, and is calculated as follows:

$$\text{Number of grids} = \text{X grids (size in X direction)} \times \text{Y grids (size in Y direction)}$$

For example, the circuit size shown in Figure 1-1 is expressed as 35 grids.
The actual chip area is the total of this macro area and the wiring area.

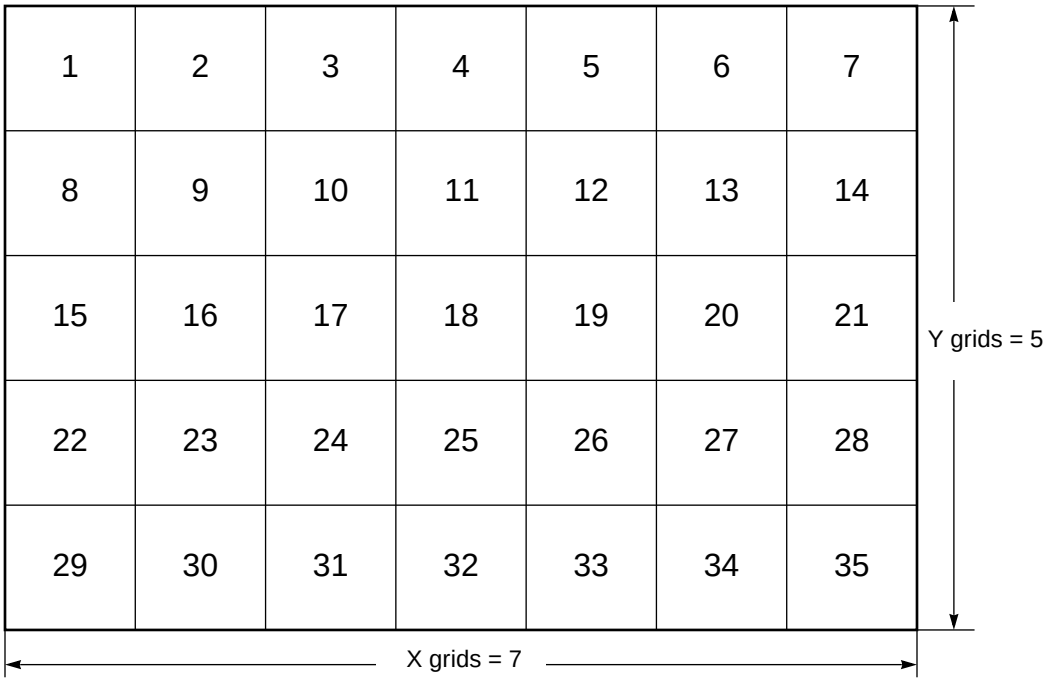


Figure 1-1 Concept of Grids

For the area of each macro, refer to **Macro Size** in **2.4**, **3.4**, **4.4**, **5.4**, **6.4, 7.4**, **8.4.**

1.4 Designing for Testing

In designing an ASIC circuit, test designing is very important. This section describes how to test a memory macro, which is necessary for designing a cell-based IC including memory macro covered by this manual.

1.4.1 Testing method

A memory macro has a relatively large circuit scale, and is regarded as a type of a core. Because its operation is simple in comparison with the CPUs, the user can design its test pattern.
Although memory macro performs simple operations even if its capacity is large, it is not easy to design the test pattern for memory if the memory is incorporated in the user circuit. A pattern to check all the functions of a RAM is particularly complicated.
Although the following three methods are available to test the memory macro, use (1) or (2) in principle.
When using (3), the testability (failure detection rate) of the memory is determined depending on your pattern design. Therefore, consult NEC in advance.

Table 1-3 Test Method of Each Macro

Test Method	Macro To Be Tested	Number of Test Patterns
(1) BIST (Built in Self Test)	RAM	0
(2) Separate test circuit (test bus)	Register file, ROM	Register file: Number of words × 36 + 2
(3) Tests using other than BIST, separate test circuit	All macros. However, this is regarded as special test. In principle, do not use such tests.	

(1) BIST (Built-in Self Test)

BIST is a method of testing by which a test pattern is automatically generated inside a circuit. An external source can test the circuit simply by applying a test mode signal and test clock to the circuit. This method is effective for testing circuits with a regular structure, such as RAM circuits.
Test patterns for BIST are not included in the total number of test patterns of the tester; therefore the limit on the number of user patterns can be relaxed.
For details of BIST, refer to **CHAPTER 9 BIST**.

(2) Separate test circuit

Register file: Test pattern created by NEC can be used.
ROM : User must create a pattern which dumps internal addresses.
Because the memory macro is provided with separate test circuits and test pins, a pattern can be easily designed using a circuit that can be externally accessed.
This test pattern is applied via the memory macro test pins. Therefore, when designing a circuit, make sure that all the test pins can be manipulated from the external pins so that all the bits of the memory can be directly accessed from the external pins.

(3) Tests using other than BIST and separate test circuit

In this case, you must create a detailed test pattern for the memory macro by yourself.
Because there is no special circuit for testing, redundant circuit design is not necessary. Instead, design a pattern that can check all the bits and the details of decoders and so on inside the macro.

1.4.2 Notes on designing test circuit

The following points (1) through (3) must be noted when designing test circuit using BIST or separate test.

(1) Test pins and external pins must be of the same logic (separate test circuit only)
Do not insert a sequential circuit such as a flop-flop between an external pin and a test pin. Do not invert a signal between them. It is not necessary to consider about BIST because it is automatically connected.

(2) Consideration of floating prevention of data output pins
Outputs pins such as DO(b:0) and TDO(b:0)[Note] go into a high-impedance state when not selected. Consequently, a floating level may be input to the block to which output is connected, causing malfunctioning or through current due to intermediate level input. Design circuits so that floating output is not directly input to the other blocks. For the prevention of floating, refer to **CB-9 Family VX/VM Type Design Manual (A12745E)**.
Because the test data output pin (TDO (b:0)) in BIST circuit design is automatically prevented from floating, it is not necessary to take it into consideration.

Note Refer to **2.2 Pin Function List**, **3.2 Pin Function List**, **4.2 Pin Function List**, **5.2 Pin Function List**, **6.2 Pin Function List**, **7.2 Pin Function List**, and **8.2 Pin Function List**.

(3) Specification of memory macro operation mode (BUNRI, TEST, BUB)
Specify the modes of BUNRI, TEST, and PUB by combination of the high and low levels input from an external pin to the test pin. Do not insert a sequential circuit such as a flip-flop between the external pin and test pin.

1.4.3 Test pattern

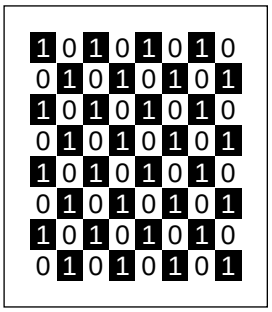
(1) RAM
The RAM test pattern offered by NEC can be used. When a test circuit is not used, the user must create a test pattern. The test pattern of the RAM usually conducts the following tests from the viewpoint of testability (failure detection rate).

- **Marching test**

  This is a method to sequentially reads patterns in the flow called marching.
  It tests the overall functions including the decoder, as well as the functions of the memory cells.

- **Checkerboard test**

  This is a method writes data in checkerboard pattern to check the mutual interference and retention function of the memory cells.
  In this case, the data must be arranged in checkerboard pattern when viewed from the physical layout of the memory cell.



(2) ROM

The ROM test pattern is checked by reading all the internal data once.
Normally, output all the data from the test bus to the external pins in the order of address. When ROM is used, prepare a test pattern for this purpose. Create a ROM code in any of the following formats.
In principle, submit the ROM code on a floppy disk to NEC to prevent any mistakes.

Caution Create the internal code as an 8-bit ASCII code. Input alphanumeric characters (single-byte) by using a text editor or word processor software.

- **NINCF format (for simulation with V.sim™)**

  In this NEC original NINCF format, ROM data of any size can be written.
  This format is a fixed column format. Exercise care that the columns are not misaligned.
  For details of the NINCF format, refer to the following pages.

- **Extended Intel HEX format**

  The ROM data can be written in the world standard extended Intel HEX format. In this case, be sure to specify data for all the addresses in the ROM.
  Write the data in ascending order of address.

Caution The assembler may output often jumps from address to address, in other words, some data addresses are skipped.

1.5 Format of ROM Code

NINCF or HEX can be used as the interface data format of ROM code.

All the bits of the ROM code must be defined to be 0 or 1. For example, if the actually used area is 990 bytes when a 1K-byte ROM is used, be sure to specify the remaining 34 bytes in the interface file.

NINCF format : NEC original format.
Data of any bit length can be handled.
HEX format : World standard format for ROM code.
Only byte data is handled. In the extended HEX format, 16-bit data can be handled.

1.5.1 Embedding ROM code in simulation system

ROM cannot be used simply by registering it in a simulation library. It is also necessary to embed the ROM code in a simulator before simulation.
How to embed the ROM code differs depending on the simulator. Here are some examples.

V.sim : NINCF format only.
Embedded when simulation is started by mr command.
Verilog™ : HEX or binary format.
$READMEMH or $READMEMB is included in data.

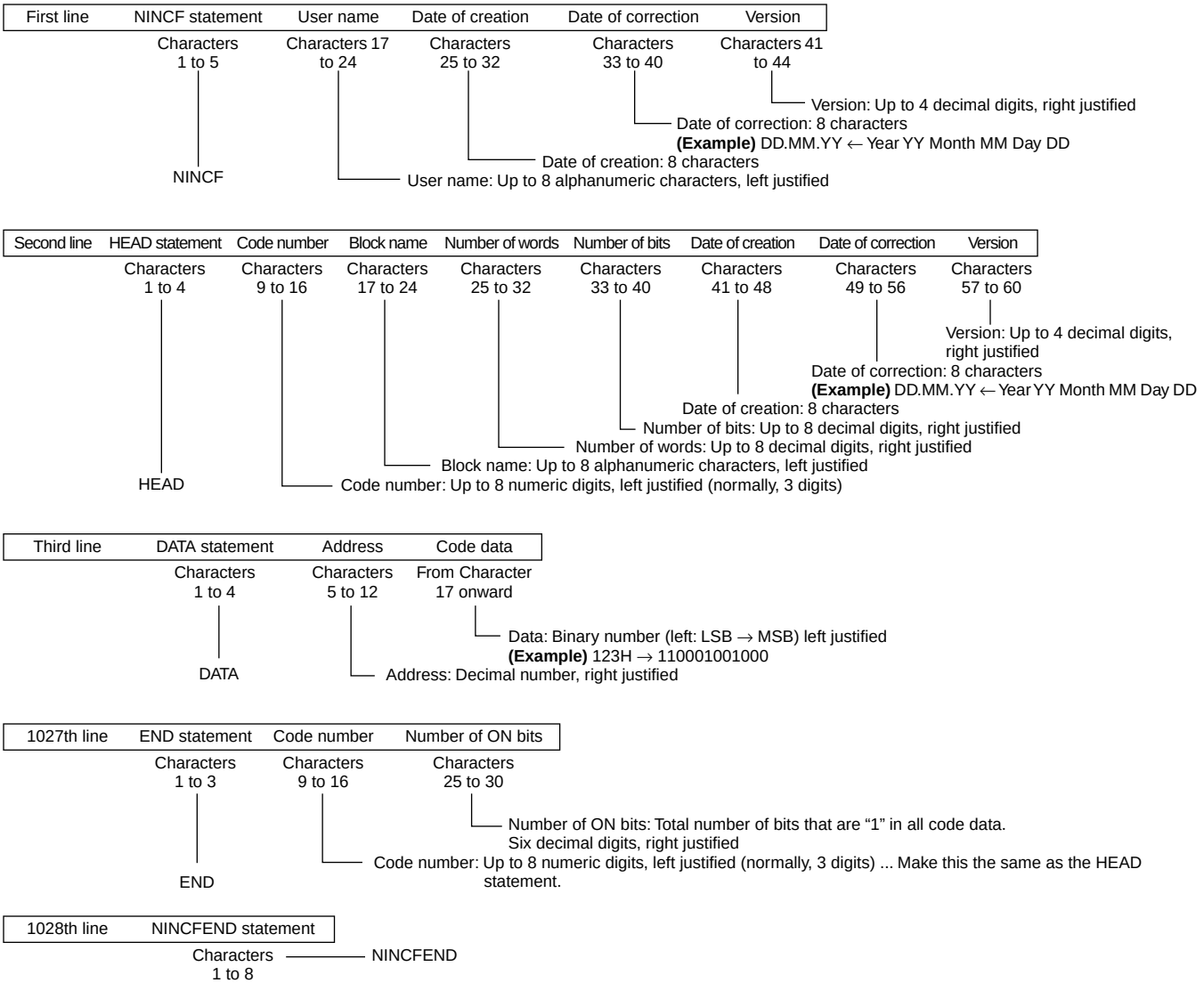
1.5.2 NINCF

NINCF is a format-fixed text file in the format shown on the next page.
This file can be created by inputting single-byte characters (ASCII codes) with a text editor, but should be created automatically to avoid mistakes.
A program that can be automatically converted from the HEX format is also available.

An example where 1K-byte ROM is used is shown below.

(Example)

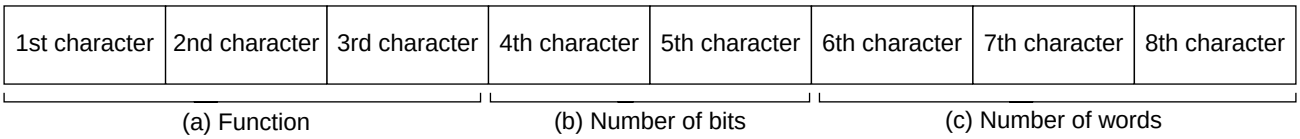
```
                Character
                          1 1 1 1 1 1 1 1 1 1 2 2 2 2 2 2 2 2 2 2 3 3 3 3 3 3 3 3 3 3 4 4 4 4 4 4 4 4 4 4 5 5 5 5 5 5 5 5 5 5 6 6 6 6 6
                1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1 2 3 4
Line
   1  N I N C F                    N A K A        2 1 / 0 9 / 9 1 2 1 / 0 9   9 1       1
   2  H E A D        0 0 1         1 K B R O M              1 0 2 4              8 2 1 / 0 9 / 9 1 2 1 / 0 9 / 9 1       1
   3  D A T A          0           1 1 0 0 0 0 1 1
   4  D A T A          1           1 1 0 0 0 0 0 0
   5  D A T A          2           0 0 1 0 0 0 0 0
   6  D A T A          3           1 0 0 0 1 1 0 0
   7  D A T A          4           0 0 1 0 1 1 0 0
        .....
        .....
1025  D A T A        1 0 2 2       1 1 1 1 1 1 1 1
1026  D A T A        1 0 2 3       1 1 1 1 1 1 1 1
1027  E N D          0 0 1                                7 7 9 0
1028  N I N C F E N D
```



1.6 Block Names of Macro

The memory macro blocks are named according to certain rules and are classified by function, capacity, and physical shape. All the names of the compiled memory macros consist of eight characters.

1.6.1 RAM



The meanings of the respective characters of a macro name are described below.

(a) Function

The first character indicates the type of the macro, the second indicates the type of the RAM, and the third indicates the column configuration and the type of the I/O format.

Table 1-4 Block Indicating Function

1st through 3rd Characters	Function
WRV WUE	High-speed single-port RAM (synchronous type) High-speed dual-port (1R/W + 1R) RAM (synchronous type)
W8K, W8U, W8T WBV	High-density single-port RAM (synchronous type) High-density dual-port (1R + 1W) RAM (synchronous type)
WHV	Super high-speed single-port RAM (synchronous type)

(b) Number of bits

The fourth and fifth characters indicate the number of bits expressed as a 2-digit base-32 number notation in the range 0 to 1023. For the correspondence between the base-32 notation and numbers, refer to **1.6.4 Correspondence table for notation to the base of 32**.

Number of bits = 4th character × 32 + 5th character

4	5	Number of Bits	4	5	Number of Bits
0	0	Missing number	0	F	15
0	1	1	0	G	16
0	2	2	0	H	17
0	3	3	0	I	Missing number
0	4	4	0	J	18
0	5	5	:	:	:
0	6	6	0	Y	31
0	7	7	0	Z	Missing number
0	8	8	1	0	32
0	9	9	1	1	33
0	A	10	1	2	34
0	B	11	:	:	:
0	C	12	Y	Y	1023
0	D	13	Y	Z	Missing number
0	E	14	Z	–	Missing number

(c) Number of words

The sixth through eighth characters indicate the number of words expressed as a 3-digit base-32 number notation in the range 0 to 32767. For the correspondence between the base-32 notation and numbers, refer to **1.6.4 Correspondence table for notation to the base of 32**.

Number of words = 6th character × 1024 × 7th character × 32 + 8th character

6	7	8	Number of words
0	0	0	Missing number
0	0	1	1
0	0	2	2
0	0	3	3
0	0	4	4
0	0	5	5
0	0	6	6
0	0	7	7
0	0	8	8
0	0	9	9
0	0	A	10
0	0	B	11
0	0	C	12
0	0	D	13
0	0	E	14
0	0	F	15
0	0	G	16
0	0	H	17
0	0	I	Missing number
0	0	J	18
:	:	:	:
0	0	X	30
0	0	Y	31
0	0	Z	Missing number
0	1	0	32
0	1	1	33
0	1	2	34
:	:	:	:
0	Y	Y	1023
0	Y	Z	Missing number
0	Z	–	Missing number
1	0	0	1024
:	:	:	:
Y	Y	Y	32767
Y	Y	Z	Missing number
Y	Z	–	Missing number
Z	–	–	Missing number

1.6.2 Register file

- **Block name**
  - Dual-port type: NZR (x1) (x2) (y1) (y2) A

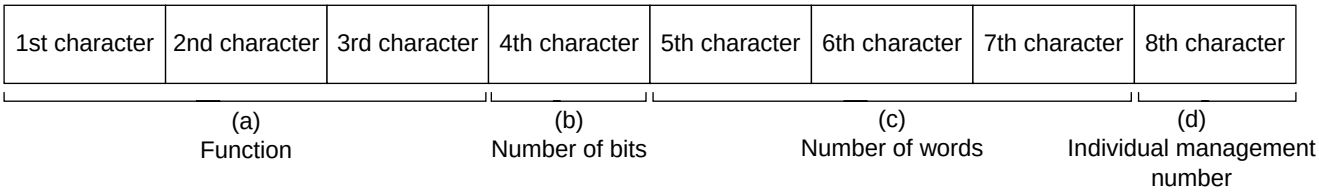
(x1) (x2)..... Expresses number of bits as a decimal number
(y1) (y2)..... Expresses number of words as a base-32 number

x1, x2 ..... Tens and units digits of number of bits
y1, y2 ..... Digits of 32^1 and 32^0 of number of words expressed by the following characters. Note, however, that I, O, Q, and Z are not used.

(x1) (x2)	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16
(y1) (y2)	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	0G
(x1) (x2)	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
(y1) (y2)	0H	0J	0K	0L	0M	0N	0P	0R	0S	0T	0U	0V	0W	0X	0Y	10

Example Targeted register file — Supported macro name
64 words × 16 bits, dual port → NZR1620A

1.6.3 ROM

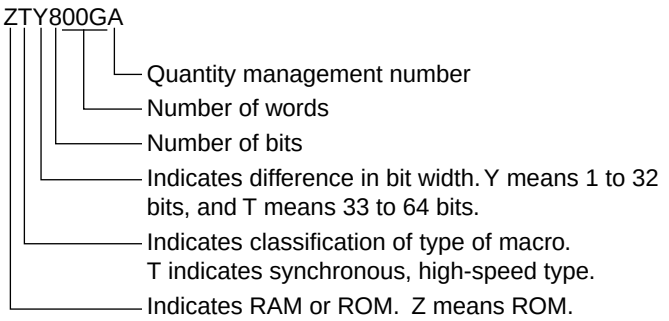


The meaning of each character is explained below.

(a) Function

The first character indicates the type of the macro, the second character indicates the ROM type, and the third character indicates the bit width.

Example High-speed ROM (synchronous type)



(b) Number of bits

The number of bits indicated by the third character varies depending on the bit width indicated by the third character, as indicated in the following tables. Characters I, O, and Q are not used.

- **If third character is Y**

Fourth Character	Number of Bits	Fourth Character	Number of Bits
0	Prohibited	K	19
1	1	L	20
2	2	M	21
3	3	N	22
:	:	O	Prohibited
9	9	P	23
A	10	Q	Prohibited
B	11	R	24
C	12	S	25
D	13	T	26
E	14	U	27
F	15	V	28
G	16	W	29
H	17	X	30
I	Prohibited	Y	31
J	18	Z	32

- **If third character is T**

Fourth Character	Number of Bits	Fourth Character	Number of Bits
0	Prohibited	K	51
1	33	L	52
2	34	M	53
3	35	N	54
:	:	O	Prohibited
9	41	P	55
A	42	Q	Prohibited
B	43	R	56
C	44	S	57
D	45	T	58
E	46	U	59
F	47	V	60
G	48	W	61
H	49	X	62
I	Prohibited	Y	63
J	50	Z	64

(c) Number of words

The fifth through seventh characters correspond to the low-order 3 digits of a base-32 number indicating the quotient of the number of real words divided by 32. The applicable range, however, is 32 words to 1M words. I, O, Q, and Z are not used in the alphabetic characters used in the base-32 number. For the correspondence between the base-32 numbers and numerals, refer to **1.6.4 Correspondence table for notation to the base of 32**.

5	6	7	Number of words
0	0	1	32
:	:	:	:
0	0	9	288
0	0	A	320
:	:	:	:
0	0	H	544
0	0	I	Missing number
0	0	J	576
0	0	N	704
0	0	O	Missing number
0	0	P	736
0	0	Q	Missing number
0	0	R	768
:	:	:	:
0	0	Z	Missing number
0	1	0	1024
:	:	:	:
0	2	0	2048
:	:	:	:
0	8	0	8192
:	:	:	:
0	G	0	16384
:	:	:	:
0	Y	Y	32736
0	Y	Z	Missing number
0	Z	–	Missing number
1	0	0	32768
:	:	:	:
Y	Y	Y	1048544
Y	Y	Z	Missing number
Y	Z	–	Missing number
Z	–	–	Missing number
0	0	0	1048576

Number of words = Fifth character $\times 32^3$ + sixth character $\times 32^2$ + seventh character $\times 32$

Example Where 5th, 6th, 7th character= 01J

J = 18

$32^3 \times 0 + 32^2 \times 1 + 32 \times 18 = 1600$ words

(d) Quantity management number

The eighth character indicates management information when two or more of the same type of ROM are used on one chip.

Value	Description
A	Indicates the first ROM on one chip
B	Indicates the second ROM of the same type on one chip
C	Indicates the third ROM of the same type on one chip
:	:
Y	:
Z	:
0	:
1	:
:	:
9	:

Caution Be sure to assign numbers in ascending order i.e.: A, B, C ... 9.

1.6.4 Correspondence table for notation to the base of 32

The following table shows the correspondence between base-32 and the decimal numbers 0 through 31. The base-32 notation are expressed using numerals and alphabetic characters, like hexadecimal numbers. However, the alphabetic characters I, O, Q, and Z are not used.

Table 1-5 Correspondence between Base-32 and Decimal Numbers

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F

16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
G	H	J	K	L	M	N	P	R	S	T	U	V	W	X	Y

1.6.5 Notes on bus name

Simulation display is performed in “descending order” in hexadecimal. For example, A(7:0) is expressed as A7, A6, ... A0.
Make sure that the mating bus name is also in descending order. If the bus name is in ascending order, connection sequence is reversed, causing problems.

1.7 Backup Memory Macros of Cell-Based IC

1.7.1 Backup function of RAM macros

(1) Operating voltage to which CB-9 family VX/VM type RAM macros apply

The CB-9 family VX/VM type provides RAM macros applicable to the following conditions.

- High-speed single-port RAM (synchronous type), high-density single-/dual-port (1R + 1W) RAM (synchronous type)
  Hold voltage: 1.6 to 3.6 V at operating voltage of 3.0 to 3.6 V, or 1.6 to 2.2 V at 1.8 to 2.2 V

- High-speed dual-port (1R/W + 1R) RAM (synchronous type)
  Hold voltage: 2.1 to 3.6 V at operating voltage of 3.0 to 3.6 V

- Super high-speed single-port RAM (synchronous type)
  Hold voltage: 2.5 to 3.6 V at operating voltage of 3.0 to 3.6 V

(2) BUB (backup) pin

When making backups of RAM macros, ensure that underfined data from the non-backup block is not propagated to inside the macros, corrupting the data.
Therefore, the RAM macros with the backup function are provided with the BUB (backup) pin to which a low-level signal can be input when making backups to protect data in the macros.

(3) Separation of main power supply and backup power supply

To back up the RAM macro, the main power supply and backup power supply must be separated when laying out the chip. Therefore, the layout TAT and development cost must be separately considered. To back up the entire chip, however, the power supply does not have to be separated.

(4) When not using backup

If BUB pins are not used, place the F091 (level generator) adjacent to the BUB pins of each RAM and clamp it high. Do not connect more than one BUB pin to one F091.

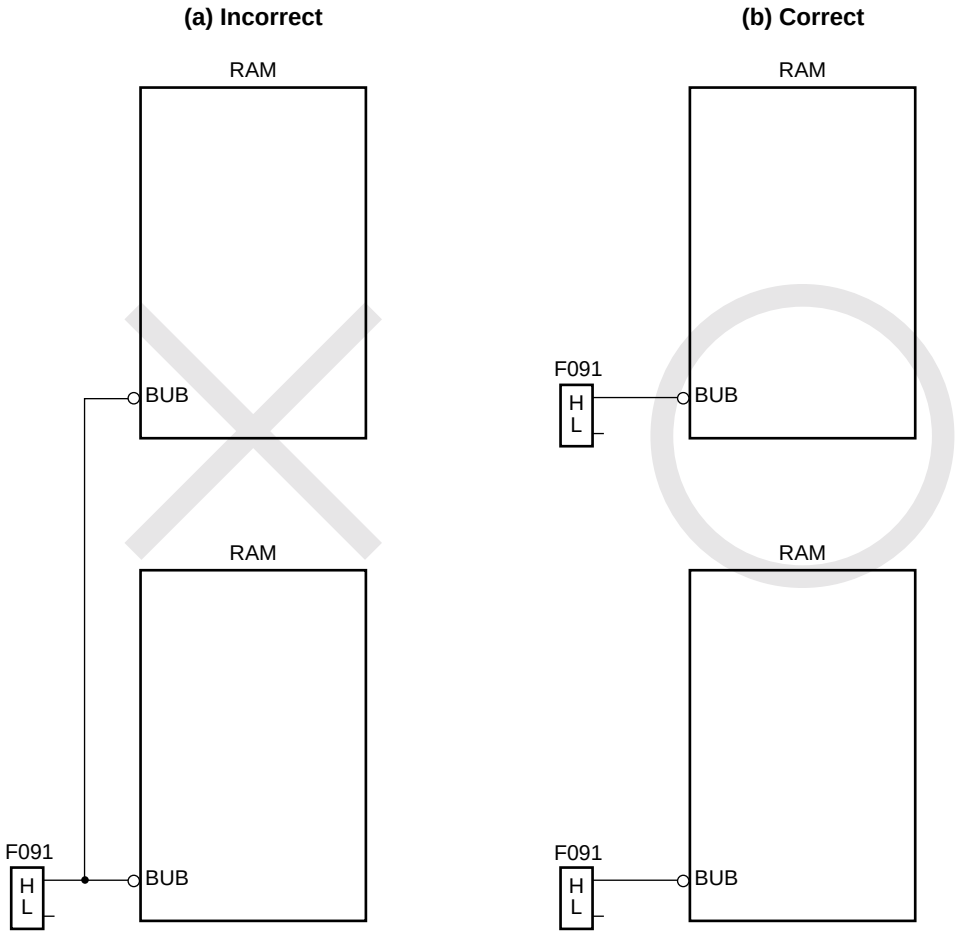


Figure 1-2 When Not Using Backup

1.7.2 Notes on backup of memory macro block

(1) Notes on designing power supply separation circuits (For circuit configuration, refer to **Figure 1-3 Power Supply Separation Circuit Configuration.**)

<1> To separate the power supply, the following three dedicated (external) pins are necessary.
- One each of BV_{DD} (backup V_{DD}) and BGND (backup GND) pins as dedicated power supply pins
- BUB (backup) pin

The BV_{DD} and BGND pins are necessary for layout and do not have to be wired when designing the circuit.

<2> Directly input the BUB pin of the memory macro from an external pin via input buffer (separate the power to the input buffer also). At this time, use FI01 as the input buffer.

<3> Inputting a low level signal to the BUB pin prevents undefined data from propagating to inside memory macros when the power is off, thus preventing data corruption.

(2) Note on selecting power supply

As an example, selecting power supply during a 3.3 V operation is shown below (the same applies during a 2.0 V operation).

<1> When the supply voltage level for memory backup is the same as that during the normal operation
(During normal operation: main power: 3.3 V, during backup: backup power = 3.3 V)
Turn OFF the main power.

<2> When the supply voltage level for memory backup is different from that during normal operation
(During normal operation: main power: 3.3 V, during backup: backup power = 3 V)
If the backup power (power to the memory macro block) is changed to 3 V before the main power is turned OFF, a potential difference from the non-backup block (blocks other than memory macro block) is generated, causing malfunction or destruction due to latchup. Change the supply voltage level in either of the following ways:

- First turn OFF the main power, and then change the backup power from 3.3 V to 3 V.
- Change the main power and backup power from 3.3 V to 3 V simultaneously, and then turn OFF the main power.

(3) Notes on using BSCAN when using backup function

The BUB pin must not be subject to BSCAN when the backup function is used.

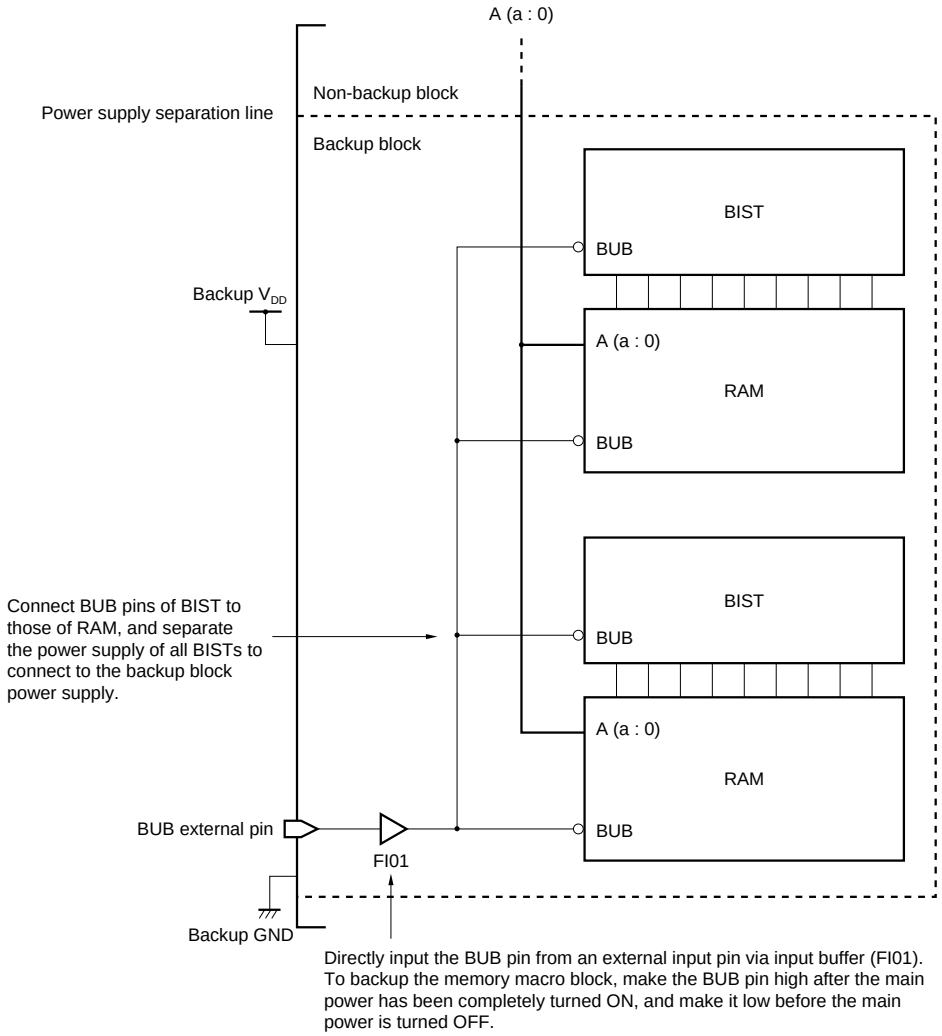


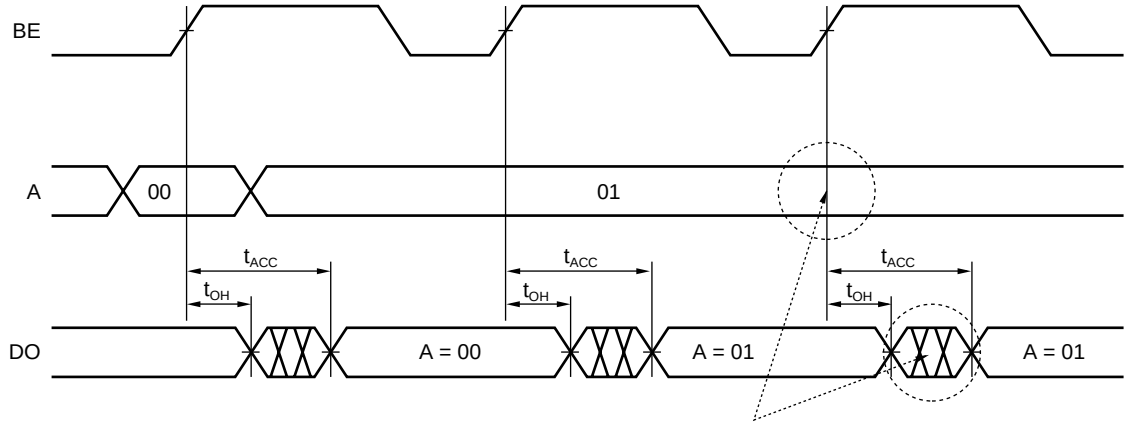
Figure 1-3 Power Supply Separation Circuit Configuration

1.8 Notes on Using Each Macro

If the address or input data changes when each RAM or ROM is read or written, note that the output data always has an undefined period (for details, refer to the timing charts in each chapter).

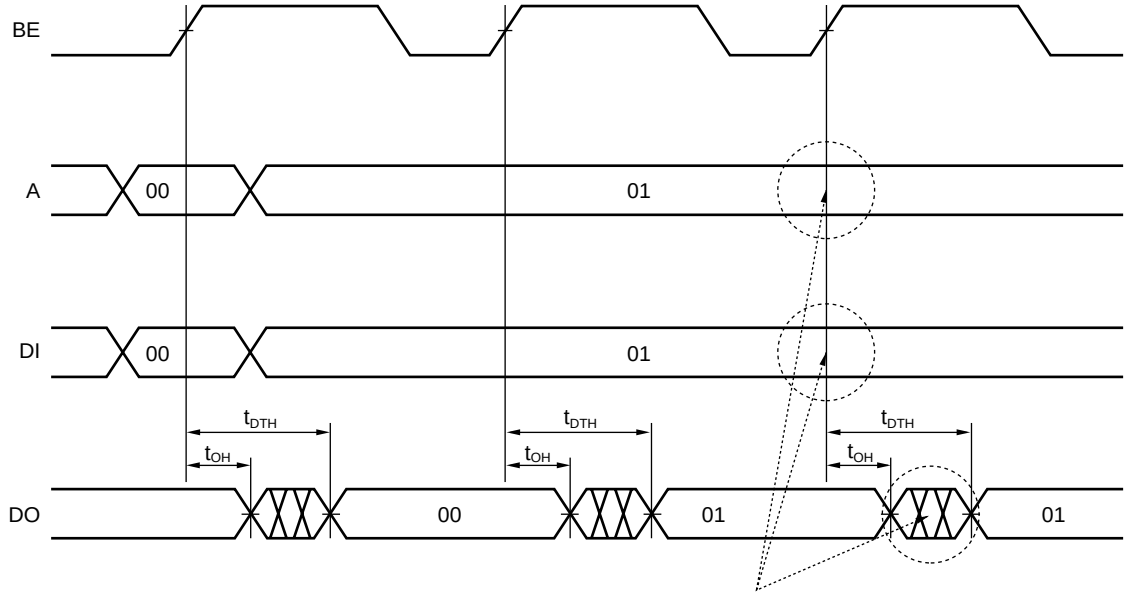
★ With the synchronous RAM, the output data has an undefined period at the rising edge of the clock even if the address and input data do not change. Observe each operation timing (refer to **Figure 1-4**).

Read cycle (CSB = low level, WEB = high level, OEB = low level)



Caution An undefined period is output to the output data (DO) even when the address (A) does not change.

Write cycle (CSB = low level, WEB = low level, OEB = low level)



Caution An undefined period is output to the output data (DO) even when the address (A) and input data (DI) do not change.

Remark t_{ACC}: Access time, t_{OH}: Output hold time, t_{DTH}: Write data through time

: Undefined

Figure 1-4 Read/Write Cycle of Synchronous RAM

1.9 Timing Limitations when Synchronous RAM Is Used

Observe the following timing limitations when using the synchronous RAM of the CB-9 family VX/VM type.

- **Synchronous RAM subject to timing limitations**
  - High-speed single-port RAM (synchronous type)
  - High-speed dual-port (1R/W + 1R) RAM (synchronous type)
  - High-density single-port RAM (synchronous type)
  - High-density dual-port (1R + 1W) RAM (synchronous type)
  - Super high-speed single-port RAM (synchronous type)

1.9.1 Prohibiting address change at same time as rising of clock input signal (BE)

If the address is changed at the same time as the rising of the clock (BE) when the synchronous RAM is read or written, the internal data of the RAM may be destroyed (refer to **Figure 1-5**).

It is recommended to change the address in synchronization with the falling of the clock (refer to **Figure 1-6**).

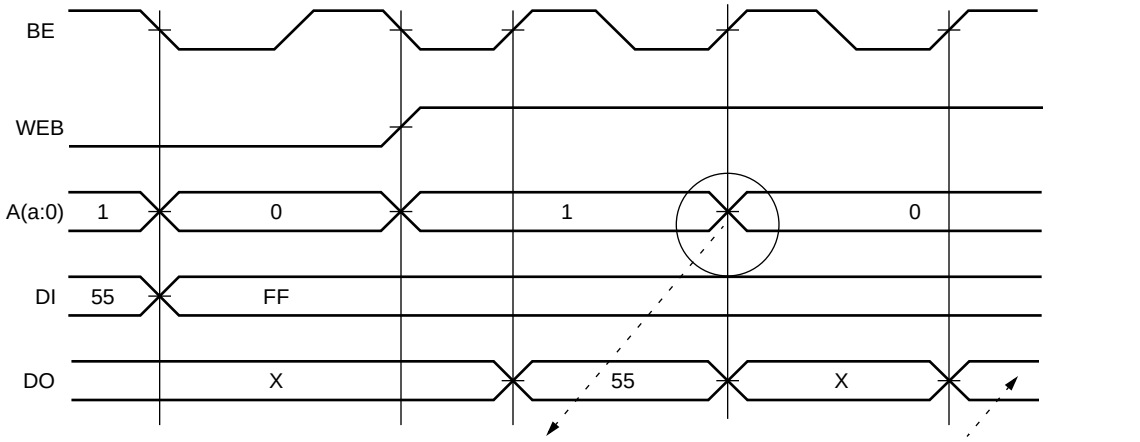


Figure 1-5 Read Cycle Timing

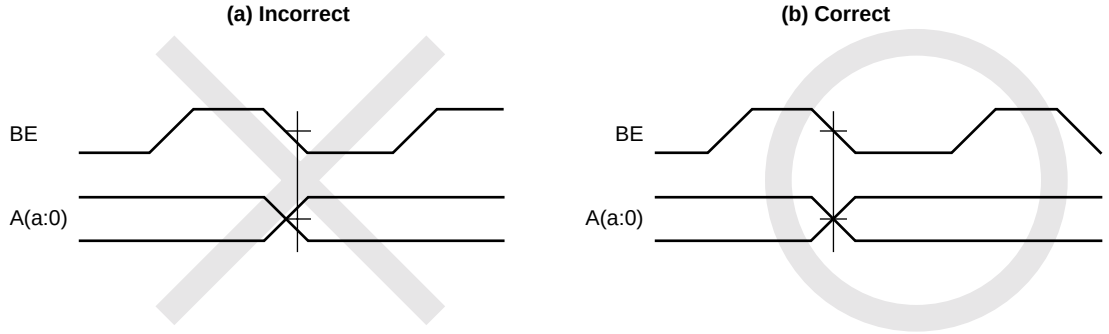


Figure 1-6 Timing to Change Clock and Address

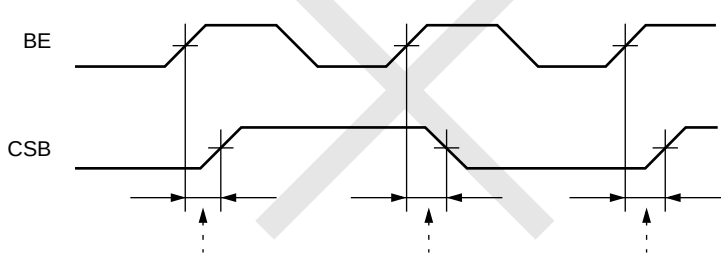
Caution Note that this limitation applies to the read/write port and write port of a dual-port RAM. However, this limitation does not apply to the read port.

1.9.2 Prohibiting changing of CSB signal while clock input signal (BE) is high

Do not change the CSB signal while the BE signal of the synchronous RAM is high. If the CSB signal is changed, the internal data of the RAM may be destroyed.

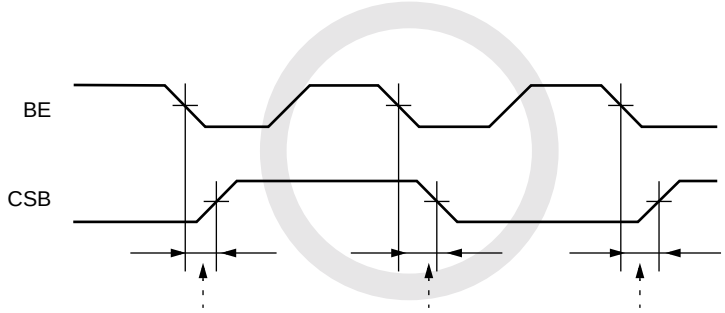
Change the CSB signal after the clock has fallen (refer to **Figure 1-7**).

(a) Incorrect



Do not change the CSB signal after BE has risen.

(b) Correct



Change the CSB signal after BE has fallen. (Satisfy the CSB setup time and CSB hold time)

Figure 1-7 Timing to Change Clock and CSB

Caution Note that this limitation applies to both the ports (A port and B port) of a dual-port RAM. However, this limitation does not apply to the read port.

1.9.3 Prohibiting changing of BUB while clock input signal (BE) is high

Do not change the BUB while the BE signal of the synchronous RAM is high.
If the BUB is changed, the data may be destroyed.

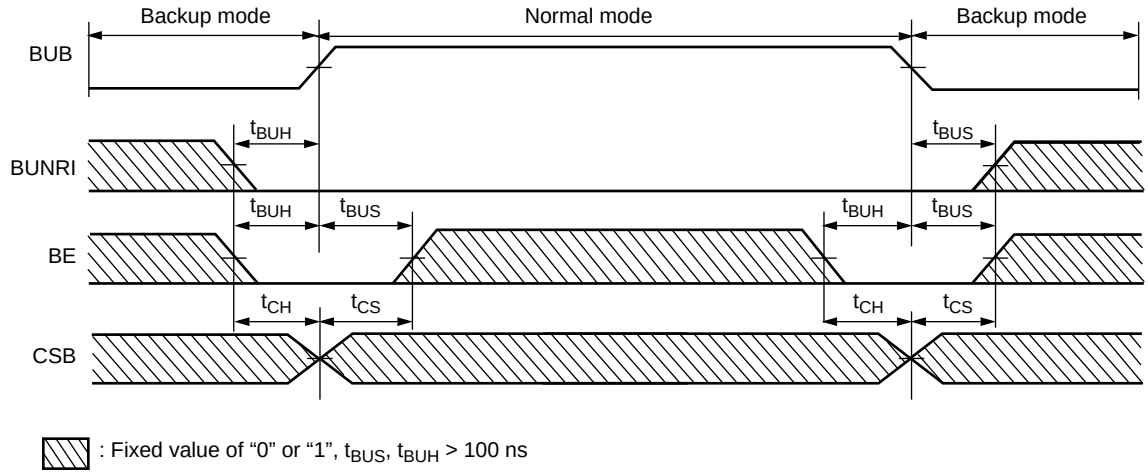


Figure 1-8 Timing to Change BE and BUB

1.9.4 Prohibiting changing of BUNRI while clock input signal (BE) is high

Do not change the BUNRI while the BE signal of the synchronous RAM is high.
If the BUNRI is changed, the data may be destroyed.

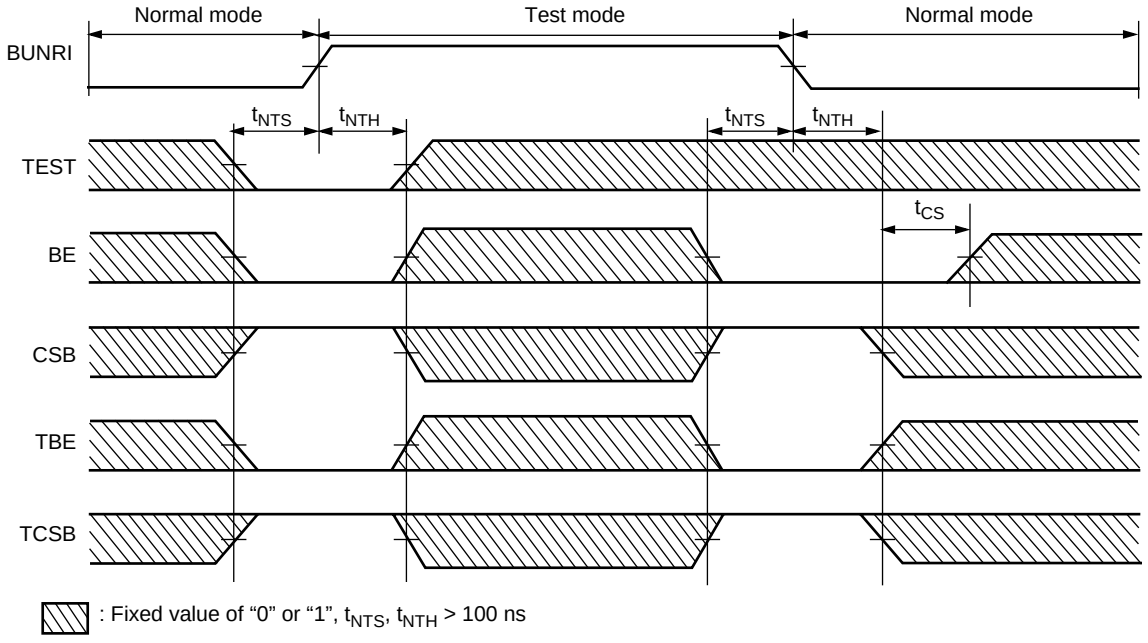


Figure 1-9 Timing to Change BE and BUNRI

CHAPTER 2 HIGH-SPEED SINGLE-PORT RAM (SYNCHRONOUS TYPE)

2.1 General

- Single-port SRAM (I/O separation type)
- Flexible memory size
  → High-efficiency macro location by memory compiler.
  Block name: WRVxxxxx
  Bit width: 1 to 32 bits (variable in 1-bit units)
  Number of words: 32 to 2K words (variable in 8-word units)
- Operating voltage: 3.3 ± 0.3 V, 2.0 ± 0.2 V
- Operating ambient temperature: –40 to +85°C
- Storage temperature: –65 to +150°C
- 0.35 μm CMOS technology

2.1.1 Compiled range

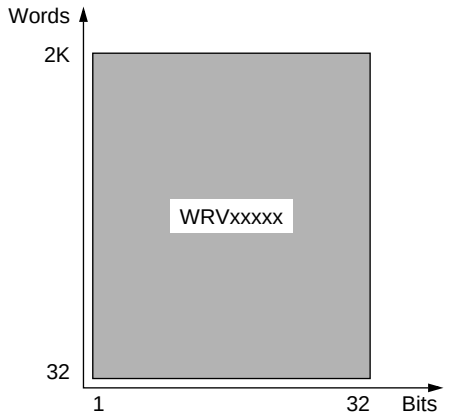
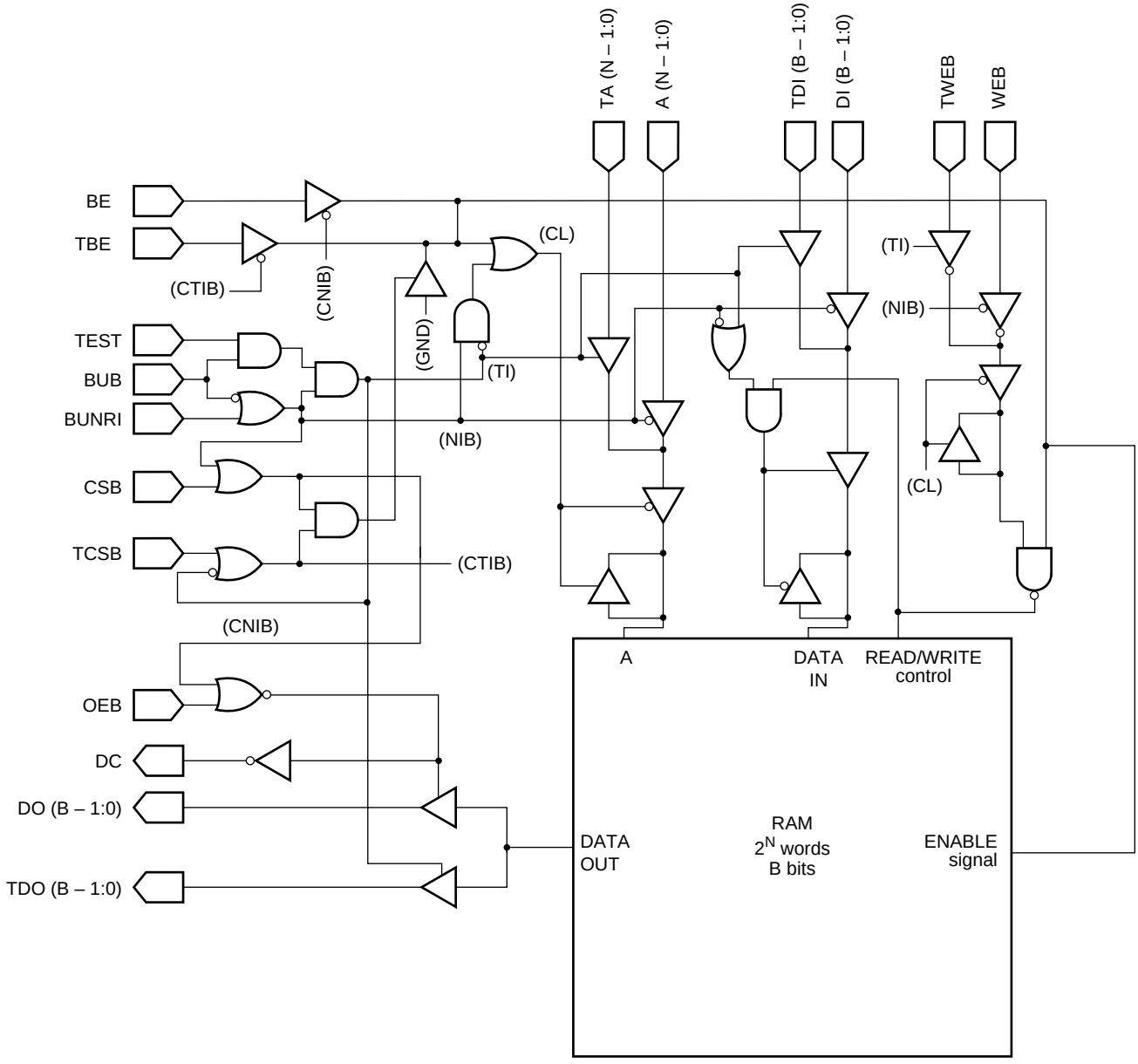


Figure 2-1 Compiled Range of High-Speed Single-Port RAM (Synchronous Type)

Table 2-1 Compiled Range of High-Speed Single-Port RAM (Synchronous Type)

Block Name	Minimum Size	Maximum Size	Step
WRVxxxxx	32 words × 1 bit	2K words × 32 bits	8 words/1 bit

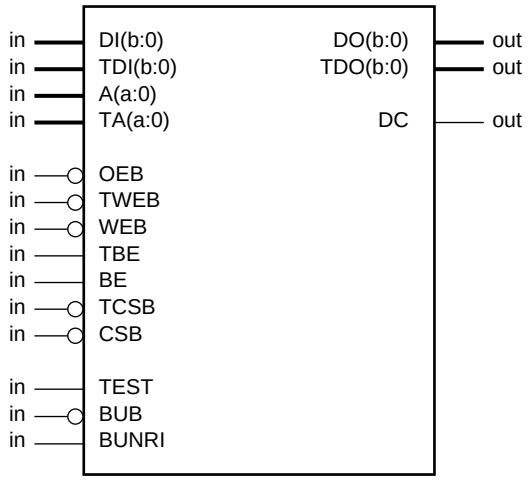
2.1.2 Equivalent circuit



Remark N: number of address lines, B: number of bits

Figure 2-2 Internal Equivalent Circuit

2.1.3 Symbol diagram



Remarks 1. A pin prefixed with “T” is a test pin.
2. “a” = (number of address lines) – 1, where $4 \le a \le 10$.
“b” = (number of bits) – 1, where $0 \le b \le 31$.

2.1.4 Pin capacitance

Pin Information GateDRC uses C_{IN} and C_{MAX} for fanin/fanout calculation.
Wiring capacitance = temporary wiring length × 0.18 (pF/mm)

Input		Output		
Pin Name/Symbol	**CIN (pF)**	**Pin Name/Symbol**	**CIN (pF)**	**CMAX (pF)**
DI(b:0)	0.01	DO(b:0)	0.05	6.0 (3.0)
TDI(b:0)	0.01	TDO(b:0)	0.05	6.0 (3.0)
A(a:0)	0.02	DC	–	1.5 (1.0)
TA(a:0)	0.02			
BE	0.07			
TBE	0.07			
CSB	0.01			
TCSB	0.01			
WEB	0.02			
TWEB	0.02			
OEB	0.02			
TEST	0.02			
BUB	0.03			
BUNRI	0.02			

Remarks 1. ( ) : Value at $V_{DD} = 2.0 \pm 0.2$ V.
2. “a” = (number of address lines) – 1, where $4 \le a \le 10$
“b” = (number of bits) – 1, where $0 \le b \le 31$

2.2 Pin Function List

Pin Name/Signal Name	Attribute	Mode	Function
DI(b:0)	I	Normal	Data input b = number of bits – 1
DO(b:0)	OZ	Normal	Data output b = number of bits – 1
A(a:0)	I	Normal	Address input a = number of address lines – 1 (determined by number of words)**Note**
BE	I	Normal	Clock input
CSB	I	Normal	Chip select input
WEB	I	Normal	Write enable input
OEB	I	Normal	Data output enable input
TDI(b:0)	I	Test	Data input b = number of bits – 1
TDO(b:0)	OZ	Test	Data output b = number of bits – 1
TA(a:0)	I	Test	Address input a = number of address lines – 1 (determined by number of words)**Note**
TBE	I	Test	Clock input
TCSB	I	Test	Chip select input
TWEB	I	Test	Write enable input
BUNRI	I	Mode selection	Separation test input BUNRI = 0: Normal mode BUNRI = 1: Test mode
TEST	I	Mode selection	Test mode input BUNRI = 1, TEST = 0 Separated from test bus (tests other macros) BUNRI = 1, TEST = 1 Selected as subject to test
BUB	I	Mode selection	Backup mode input BUB = 0: Backup mode BUB = 1: Normal mode, test mode
DC	O	Normal	Data control output DC = 0: DO(b:0) = 0, 1, undefined DC = 1: DO(b:0) = high impedance

Note Number of address lines = $\log_2$ (number of words) (rounded up at decimal place)

Remark The meanings of the symbols in the Attribute column are as follows:
I : input pin, OZ : 3-state output pin, O : output pin

2.3 Operation Truth Table

The meanings of the symbols in the following operation truth tables are as follows:

Hi-Z : High impedance
X : Undefined state not including high impedance
XZ : Undefined state including high impedance
Ax : Any data
DIx : Input data
[Ax] : Data in memory

BUB	BUNRI	TEST	Mode	Normal Pin Status			Test Pin Status	
				Input	Output	DC	Input	Output
0	XZ	XZ	Backup	XZ	Hi-Z	1	XZ	Hi-Z
1	0	X	Normal	Valid	Valid	Valid	XZ	Hi-Z
1	1	0	Test (non-select)	XZ	Hi-Z	1	XZ	Hi-Z
1	1	1	Test (select)	XZ	Hi-Z	1	Valid	Valid

Normal mode access

CSB	BE	WEB	OEB	A(a:0)	DI(b:0)	DO(b:0)	DC	Operation
0	↑	0	1	Ax	DIx	Hi-Z	1	Write (output off)
0	↑	0	0	Ax	DIx	[Ax] = DIx**Note**	0	Write (output on)
0	↑	1	0	Ax	X	[Ax]	0	Read
0	0	X	0	X	X	Hold	0	Precharge
0	X	X	1	X	X	Hi-Z	1	Output off
1	X	X	X	X	X	Hi-Z	1	Macro off

Note The data input from the DI(b:0) pin is output through.

Test mode access

TCSB	TBE	TWEB	TA(a:0)	TDI(b:0)	TDO(b:0)	Operation
0	↑	0	Ax	DIx	[Ax] = DIx**Note**	Write
0	↑	1	Ax	X	[Ax]	Read
0	0	X	X	X	Hold	Precharge
1	X	X	X	X	Hold	Macro off

Note The data input from the TDI(b:0) pin is output through.

2.4 Macro Size

Use the following expression to calculate the macro size.

Macro size = X × Y (grids)

W : number of words
B : number of bits
N : number of address lines (N = $\log_2$W (rounded up at decimal place))
α : Macro circumferential wiring area in X direction (73.53)
β : Macro circumferential wiring area in Y direction (7.353)

	B ≤ 16	B > 16
W = 32	X = 31.74 × B + 169.00 + α (grids) Y = 7.464 × 10^{-2} × W + 22.87 + β (grids)	X = 31.74 × B + 196.58 + α (grids) Y = 7.464 × 10^{-2} × W + 22.87 + β (grids)
W > 32	X = 31.74 × B + 6.24 × N + 136.36 + α (grids) Y = 7.464 × 10^{-2} × W + 25.52 + β (grids)	X = 31.74 × B + 6.24 × N + 163.93 + α (grids) Y = 7.464 × 10^{-2} × W + 25.52 + β (grids)

Remarks 1. Round up the fraction below the decimal place.
2. Not necessary to add α and β when not taking the macro circumferential wiring area into consideration.

2.5 Electrical Characteristics

Absolute maximum ratings

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	–0.5 to +4.6	V
Operating ambient temperature	T_A	–40 to +85	°C
Storage temperature	T_{stg}	–65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended operating range (V_{DD} = 3.3 ± 0.3 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}	3.0	3.3	3.6	V
Operating ambient temperature	T_A	–40		+85	°C

Recommended operating range (V_{DD} = 2.0 ± 0.2 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}	1.8	2.0	2.2	V
Operating ambient temperature	T_A	–40		+85	°C

2.6 Operating Current Consumption

The operating current consumption (I_{DD}) changes depending on the number of bits, number of words, number of address lines, and operating frequency of the memory. The value of the operating current consumption can be calculated by the following expression.

I_{DD} (TYP.) = I_{DDR} (TYP.) + I_{DDW} (TYP.)
I_{DD} (MAX.) = I_{DDR} (MAX.) + I_{DDW} (MAX.)

I_{DDR} and I_{DDW} in the above expression can be worked out by the expressions in the table below.

The meanings of the symbols in the tables below are as follows:
B: number of bits, W: number of words, N: number of address lines (N = $\log_2$W (rounded up at decimal place)),
f_R: read operating frequency (MHz), f_W: write operating frequency (MHz), C_L: external load capacitance (pF),
A: operation rate **Note 1** (100% = 1), DF: MAX data rate (MHz) of A (a:0), WEB, or DI (b:0) pin

(1) V_{DD} = 3.3 ± 0.3 V

TYP.
During read/write operation (α = 1.65 × B × C_L)

Operation	Expression	Unit
Read (I_{DDR})	$\{(1.19 \times N + 1.61 \times B - 3.23) \times 10^{-3} \times W + 1.20 \times N + 12.1 \times B + 11.2 + \alpha\} \times f_R \times A$	μA
Write (I_{DDW})	$\{(1.19 \times N + 1.71 \times B - 3.23) \times 10^{-3} \times W + 1.20 \times N + 9.11 \times B + 11.0 + \alpha\} \times f_W \times A$	μA

MAX.
During read/write operation (α = 1.8 × B × C_L)

Operation	Expression	Unit
Read (I_{DDR})	$\{(1.29 \times N + 4.27 \times B - 2.74) \times 10^{-3} \times W + 1.50 \times N + 13.1 \times B + 13 + \alpha\} \times f_R \times A$	μA
Write (I_{DDW})	$\{(1.29 \times N + 3.26 \times B - 2.74) \times 10^{-3} \times W + 1.50 \times N + 10.3 \times B + 12.7 + \alpha\} \times f_W \times A$	μA

In power-down mode **Note 2**

Condition	Expression	Unit
TYP.	$\{1.19 \times 10^{-3} \times W \times (N - 5) + 1.20 \times N + 0.370 \times B - 2.69\} \times DF$	μA
MAX.	$\{1.29 \times 10^{-3} \times W \times (N - 5) + 1.50 \times N + 0.441 \times B - 3.33\} \times DF$	μA

(2) V_{DD} = 2.0 ± 0.2 V

TYP.
During read/write operation (α = 1.0 × B × C_L)

Operation	Expression	Unit
Read (I_{DDR})	$\{(0.695 \times N + 0.94 \times B - 1.885) \times 10^{-3} \times W + 0.7 \times N + 7.06 \times B + 6.50 + \alpha\} \times f_R \times A$	μA
Write (I_{DDW})	$\{(0.695 \times N + 1.00 \times B - 1.885) \times 10^{-3} \times W + 0.7 \times N + 5.32 \times B + 6.44 + \alpha\} \times f_W \times A$	μA

MAX.
During read/write operation (α = 1.1 × B × C_L)

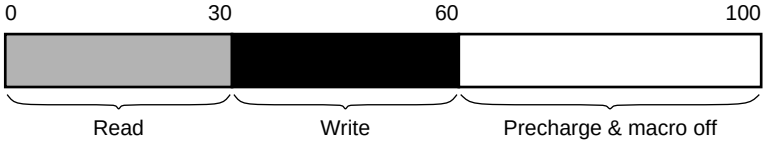
Operation	Expression	Unit
Read (I_{DDR})	$\{(0.746 \times N + 2.47 \times B - 1.59) \times 10^{-3} \times W + 0.87 \times N + 7.57 \times B + 7.55 + \alpha\} \times f_R \times A$	μA
Write (I_{DDW})	$\{(0.746 \times N + 1.89 \times B - 1.59) \times 10^{-3} \times W + 0.87 \times N + 5.95 \times B + 7.35 + \alpha\} \times f_W \times A$	μA

In power-down mode Note 2

Condition	Expression	Unit
TYP.	$\{1.94 + 0.216 \times B + (0.695 \times 10^{-3} \times W + 0.70) \times (N - 5)\} \times DF$	μA
MAX.	$\{2.41 + 0.255 \times B + (0.746 \times 10^{-3} \times W + 0.87) \times (N - 5)\} \times DF$	μA

Notes 1. This operation rate is the ratio of the read and write operations to the total operation period (read, write, precharge, and macro off) of the RAM.

Example The operation rate is 60% (0.6) if read operations account for 30% of the total operation period of RAM and write operations account for 30%.



2. Power-down mode indicates the precharge status or macro off status in **Normal mode access** in **2.3 Operation Truth Table**.

Remarks 1. If all the input signals of this RAM are fixed, the current consumption in the standby mode (I_{DD1}) = 0.
2. Calculate the read/write operating frequency (MHz) based on the following concept (read 50%, write 50% during read/write operation).

Example To read and write alternately every 1 clock at 50 MHz
Calculate I_{DDR} and I_{DDW} assuming the folllowing.
Read frequency : f_R = 25 MHz
Write frequency : f_W = 25 MHz

3. If OEB is fixed to H during write operation, α of I_{DDW} is 0 (in the write (output off) status for the normal mode access in the operation truth table).

2.7 Timing

2.7.1 Expressions

The timing values can be calculated by the following expressions (rounded at the third place below the decimal place. However, the output hold time is truncated).
The meanings of the symbols in the table below are as follows:
W: number of words, B: number of bits: N: number of address lines ($N = \log_2 W$ (rounded up at decimal place)),
C_L: external load capacitance (pF)

(1) $V_{DD} = 3.3 \pm 0.3$ V

Read/write operation (T_A = –40 to +85°C)

Parameter	Symbol	Expression	Unit
Cycle time	t_{RC}	Where $t_{BEH} > t_{PC}$: $t_{BEH} \times 2$ (clock duty: 50%) Where $t_{BEH} < t_{PC}$: $t_{PC} \times 2$ (clock duty: 50%)	ns
Access time	t_{ACC}	$3.10 + 3.21 \times 10^{-2} \times B + 4.94 \times 10^{-4} \times W + 3.40 \times 10^{-1} \times C_L$	ns
Output hold time	t_{OH}	$0.61 + 7.5 \times 10^{-3} \times B + 1.31 \times 10^{-4} \times W$	ns
BE high-level time	t_{BEH}	$2.67 + 3.21 \times 10^{-2} \times B + 3.84 \times 10^{-4} \times W$	ns
Precharge time	t_{PC}	$2.49 + 4.97 \times 10^{-2} \times B + 5.14 \times 10^{-4} \times W$	ns
Address setup time	t_{AS}	$1.10 + 4.69 \times 10^{-4} \times W$	ns
Address hold time	t_{AH}	$0.70 + 1.80 \times 10^{-2} \times N$	ns
Write data setup time	t_{DIS}	0	ns
Write data hold time	t_{DIH}	$0.88 + 1.87 \times 10^{-2} \times B$	ns
Write data through time	t_{DTH}	$2.52 + 1.61 \times 10^{-2} \times B + 3.40 \times 10^{-1} \times C_L$	ns
WEB setup time	t_{WS}	0.47	ns
WEB hold time	t_{WH}	$0.70 + 1.80 \times 10^{-2} \times N$	ns
CSB setup time	t_{CS}	0.79	ns
CSB hold time	t_{CH}	0	ns
CSB, OEB control			
Output floating time	t_{HZ}	$1.73 + 1.96 \times 10^{-2} \times B$	ns
Output active time	t_{LZ}	$1.71 + 2.25 \times 10^{-2} \times B$	ns
DC output delay time	t_{DC}	$1.59 + 1.61 \times 10^{-2} \times B + 9.40 \times 10^{-1} \times C_L$	ns

(2) V_{DD} = 2.0 ± 0.2 V

Read/write operation (T_A = –40 to +85°C)

Parameter	Symbol	Expression	Unit
Cycle time	t_{RC}	Where $t_{BEH} > t_{PC}$: $t_{BEH} \times 2$ (clock duty: 50%) Where $t_{BEH} < t_{PC}$: $t_{PC} \times 2$ (clock duty: 50%)	ns
Access time	t_{ACC}	$5.23 \times 10^{-2} \times B + 1.66 \times 10^{-3} \times W + 6.84 + 6.26 \times 10^{-1} \times C_L$	ns
Output hold time	t_{OH}	$1.83 \times 10^{-2} \times B + 3.315 \times 10^{-4} \times W + 0.925$	ns
BE high-level time	t_{BEH}	$5.23 \times 10^{-2} \times B + 1.57 \times 10^{-3} \times W + 5.97$	ns
Precharge time	t_{PC}	$6.69 \times 10^{-2} \times B + 8.95 \times 10^{-4} \times W + 5.68$	ns
Address setup time	t_{AS}	$8.44 \times 10^{-4} \times W + 1.95$	ns
Address hold time	t_{AH}	$2.64 \times 10^{-2} \times N + 1.17$	ns
Write data setup time	t_{DIS}	0	ns
Write data hold time	t_{DIH}	$2.98 \times 10^{-2} \times B + 1.47$	ns
Write data through time	t_{DTH}	$2.81 \times 10^{-2} \times B + 5.62 + 6.26 \times 10^{-1} \times C_L$	ns
WEB setup time	t_{WS}	0.89	ns
WEB hold time	t_{WH}	$2.64 \times 10^{-2} \times N + 1.17$	ns
CSB setup time	t_{CS}	1.51	ns
CSB hold time	t_{CH}	0	ns
CSB, OEB control			
Output floating time	t_{HZ}	$3.70 \times 10^{-2} \times B + 3.02$	ns
Output active time	t_{LZ}	$4.04 \times 10^{-2} \times B + 3.34$	ns
DC output delay time	t_{DC}	$3.57 \times 10^{-2} \times B + 3.12 + 1.77 \times C_L$	ns

2.7.2 Typical value (8 bits × 512 words)

(1) V_{DD} = 3.3 ± 0.3 V

Read/write operation (T_A = –40 to +85°C)

Parameter		Symbol	MIN.	TYP.	MAX.	Unit
Cycle time		t_{RC}	6.32			ns
Access time		t_{ACC}			3.68	ns
Output hold time		t_{OH}	0.73			ns
BE high-level time		t_{BEH}	3.13			ns
Precharge time		t_{PC}	3.16			ns
Address setup time		t_{AS}	1.35			ns
Address hold time		t_{AH}	0.87			ns
Write data setup time		t_{DIS}	0			ns
Write data hold time		t_{DIH}	1.03			ns
Write data through time		t_{DTH}			2.72	ns
WEB setup time		t_{WS}	0.47			ns
WEB hold time		t_{WH}	0.87			ns
CSB setup time		t_{CS}	0.79			ns
CSB hold time		t_{CH}	0			ns
CSB, OEB control						
	Output floating time	t_{HZ}	1.89			ns
	Output active time	t_{LZ}	1.89			ns
	DC output delay time	t_{DC}			1.91	ns

Remarks 1. The above values are calculated with an external load capacitance of 0.2 pF.
2. The meanings of the symbols in the above table are as follows:
MIN. : minimum value necessary for operating macro under worst condition
MAX. : delay time of macro output under worst condition

(2) V_{DD} = 2.0 ± 0.2 V

Read/write operation (T_A = –40 to +85°C)

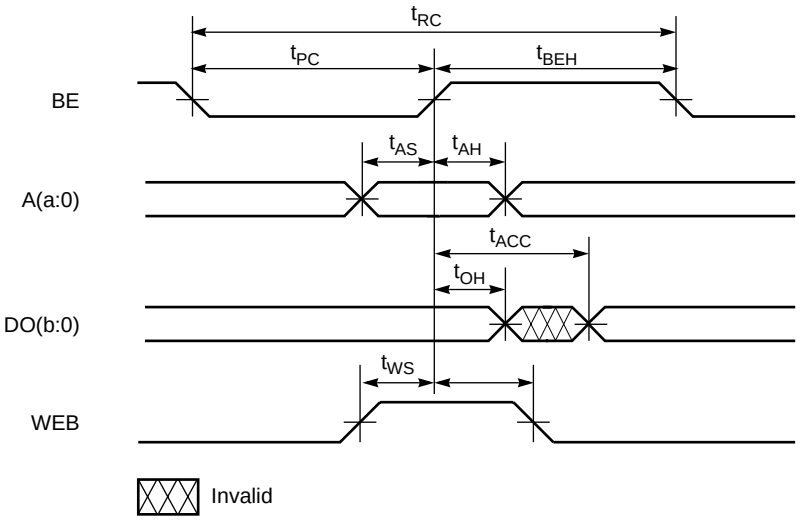
Parameter		Symbol	MIN.	TYP.	MAX.	Unit
Cycle time		t_{RC}	14.40			ns
Access time		t_{ACC}			8.24	ns
Output hold time		t_{OH}	1.24			ns
BE high-level time		t_{BEH}	7.20			ns
Precharge time		t_{PC}	6.68			ns
Address setup time		t_{AS}	2.39			ns
Address hold time		t_{AH}	1.41			ns
Write data setup time		t_{DIS}	0			ns
Write data hold time		t_{DIH}	1.71			ns
Write data through time		t_{DTH}			5.97	ns
WEB setup time		t_{WS}	0.89			ns
WEB hold time		t_{WH}	1.41			ns
CSB setup time		t_{CS}	1.51			ns
CSB hold time		t_{CH}	0			ns
CSB, OEB control						
	Output floating time	t_{HZ}	3.32			ns
	Output active time	t_{LZ}	3.67			ns
	DC output delay time	t_{DC}			3.64	ns

Remarks 1. The above values are calculated with an external load capacitance of 0.2 pF.
2. The meanings of the symbols in the above table are as follows:
MIN. : minimum value necessary for operating macro under worst condition
MAX. : delay time of macro output under worst condition

2.8 Timing Chart

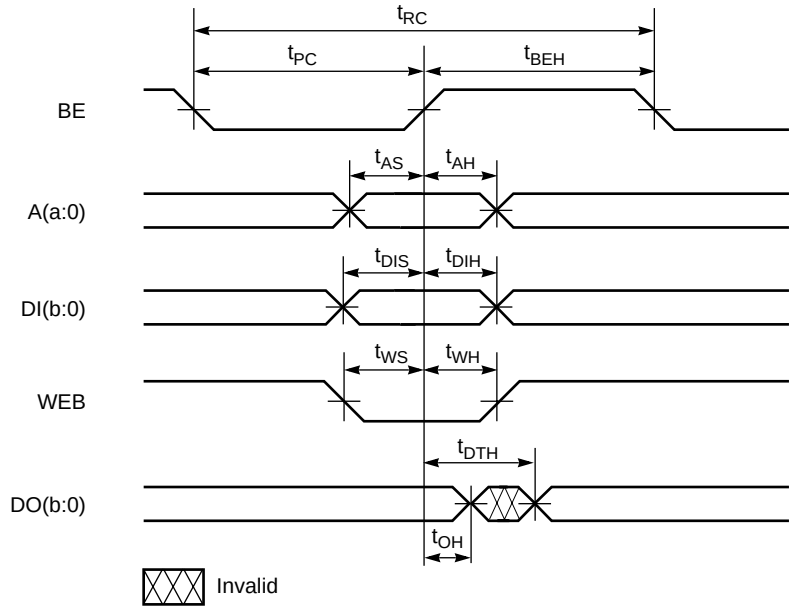
Read operation

Read cycle (CSB = low level, OEB = low level)



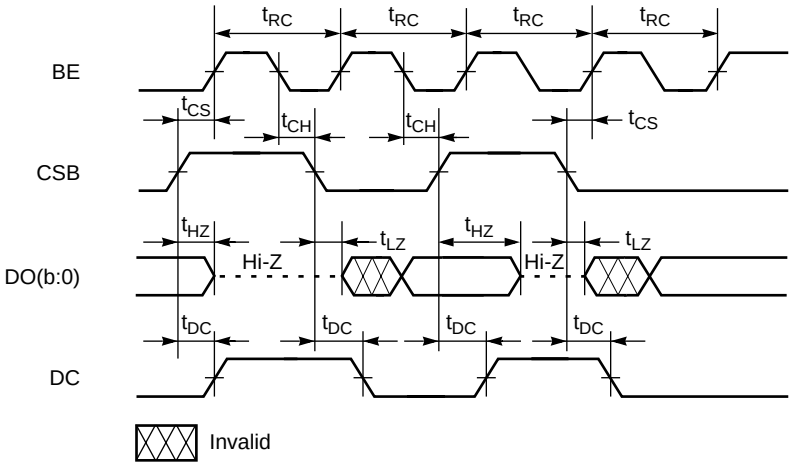
Write operation

Write cycle (CSB = low level, OEB = low level)

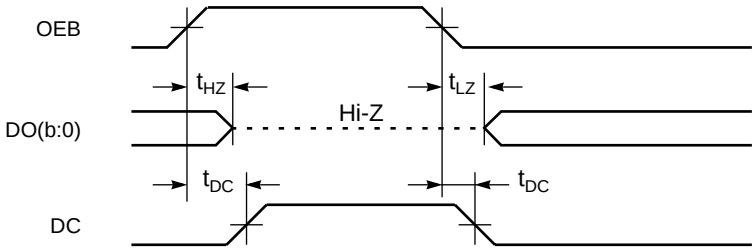


Read/write operation

(1) CSB control (OEB = low level)



(2) OEB control (CSB = low level)



2.9 Notes on Correct Use

(1) If a spike is input to the clock input pin while CSB = L, the data in the RAM may be destroyed. In this case, the addresses other than that when the spike was input may be also destroyed.

(2) When using a RAM macro of less than 2^N words, do not access a non-existent address. **Note**
Otherwise, the output data of the preceding cycle is not retained.

Note Specifically, this means an access to W+1 to 2^N where $W < 2^N$.
For example, when a RAM macro of 1 bit × 160 words is used and the number of address lines (N) is 8, 161 through 256 words are non-existent addresses.

(3) If a non-existent address is accessed, an overcurrent flows during read operation (WEB = H, BE = H) (the overcurrent does not flow during write operation or in macro off status). In addition, even when there are no non-existent addresses, an overcurrent flows immediately after power application until the address is confirmed. The overcurrent can be calculated by the following expression.

- **Overcurrent when non-existent address or uncertain address is accessed**
  $[V_{DD} = 3.3 \pm 0.3\ V]$
  ΔI_{DD} (TYP.) = 1.671 × (B + 1) [mA]
  ΔI_{DD} (MAX.) = 3.4226 × (B + 1) [mA]

Remark B: number of bits of RAM accessed

(4) Currently may continue to flow if the clock is stopped at a high level when power is applied, so be sure to either stop the clock while the clock pin is low, or input the clock first low then high (or high → low → high). If the clock is input at a low level even once, current will not flow no matter how the clock is subsequently stopped.

CHAPTER 3 HIGH-SPEED DUAL-PORT (1R/W + 1R) RAM (SYNCHRONOUS TYPE)

3.1 General

- Read/write port + read port

  Multi-function dual-port RAM (I/O separation type)
- Flexible memory size
  → High efficiency macro location by memory complier.
  Block name: WUExxxxx
  Bit width: 1 to 32 bits (variable in 1-bit units)
  Number of words: 32 to 2K words (variable in 16-word units)
- Operating voltage: 3.3 ± 0.3 V
- Operating ambient temperature: –40 to +85°C
- Storage temperature: –65 to +150°C
- 0.35 μm CMOS technology

3.1.1 Compiled range

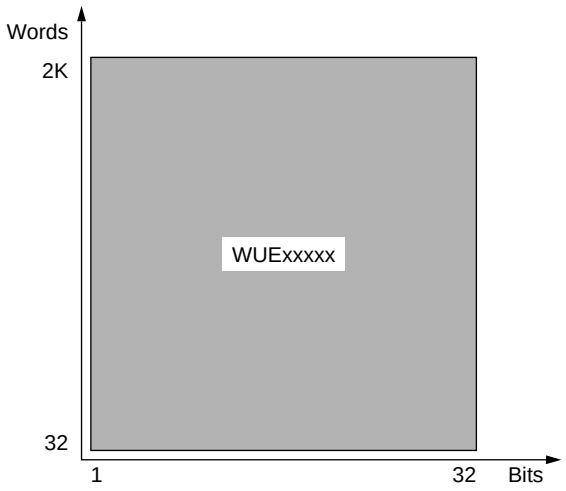
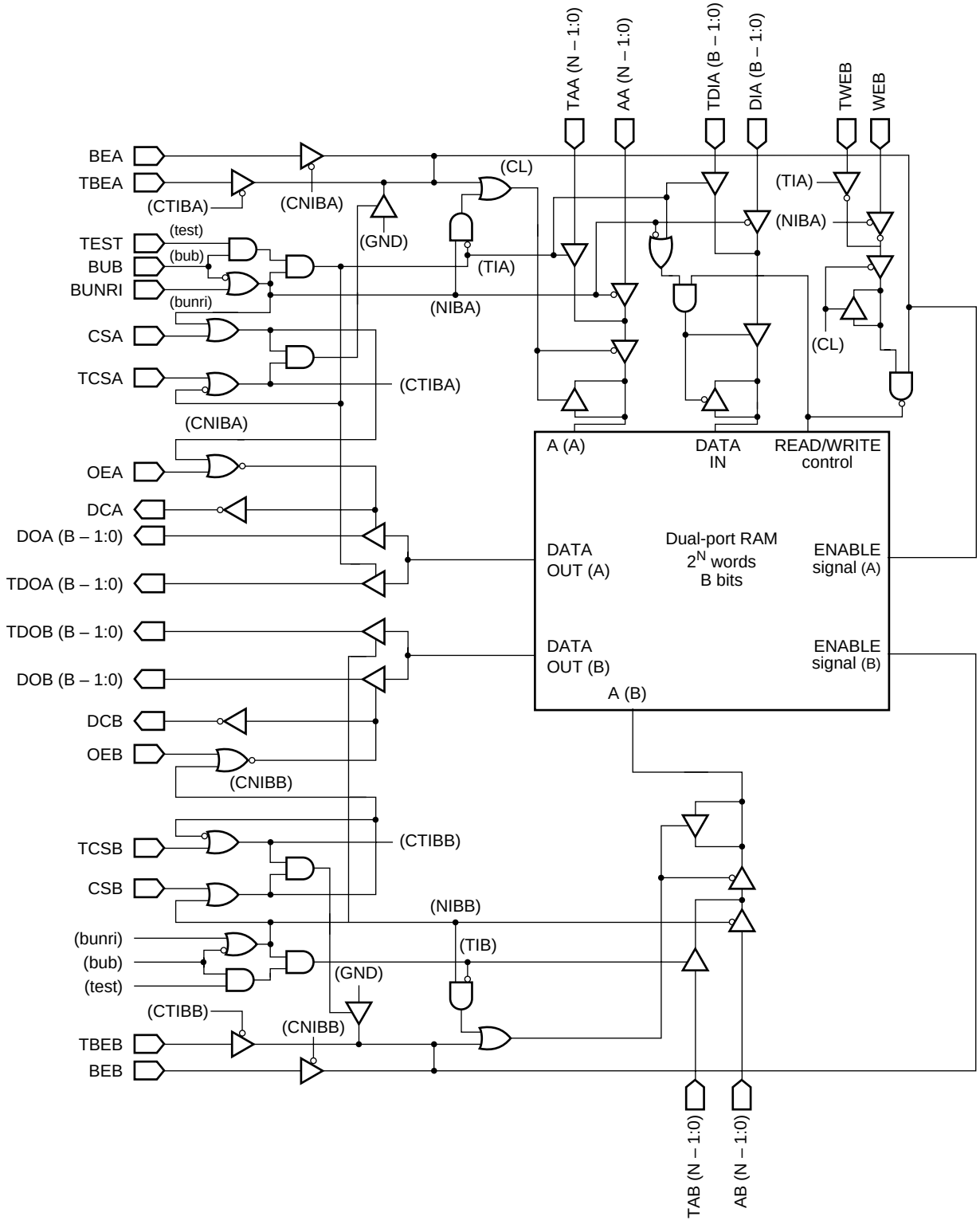


Figure 3-1 Compiled Range of High-Speed Dual-Port (1R/W + 1R) RAM (Synchronous Type)

Table 3-1 Compiled Range of High-Speed Dual-Port (1R/W + 1R) RAM (Synchronous Type)

Block Name	Minimum Size	Maximum Size	Step
WUExxxxx	32 words × 1 bit	2K words × 32 bits	16 words/1 bit

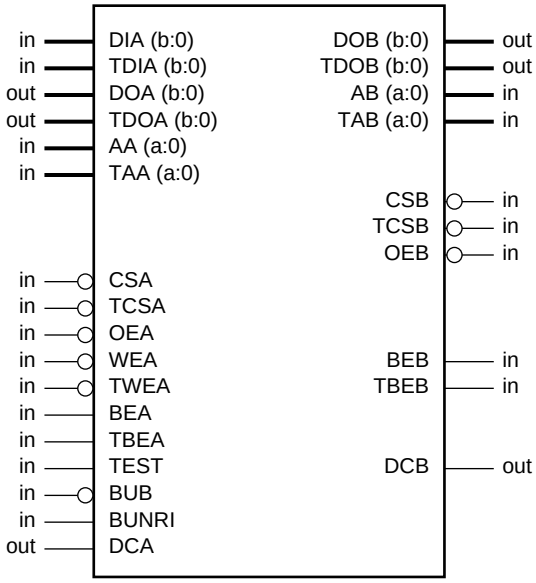
3.1.2 Equivalent circuit



Remark N: number of address lines, B: number of bits

Figure 3-2 Internal Equivalent Circuit

3.1.3 Symbol diagram



Remarks 1. A pin prefixed with “T” is a test pin.

2. “a” = (number of address lines) – 1, where $4 \leq a \leq 10$.
“b” = (number of bits) – 1, where $0 \leq b \leq 31$.

3.1.4 Pin capacitance

Pin Information GateDRC uses C_{IN} and C_{MAX} for fanin/fanout calculation.
Wiring capacitance = temporary wiring length × 0.18 (pF/mm)

Input		Output		
Pin Name/Symbol	**CIN (pF)**	**Pin Name/Symbol**	**CIN (pF)**	**CMAX (pF)**
DIA(b:0)	0.01	DOA(b:0)	0.133	6.0
TDIA(b:0)	0.01	TDOA(b:0)	0.133	6.0
AA(a:0)	0.02	DCA	–	1.5
TAA(a:0)	0.02	DOB(b:0)	0.133	6.0
BEA	0.06	TDOB(b:0)	0.133	6.0
TBEA	0.06	DCB	–	1.5
CSA	0.01			
TCSA	0.01			
WEA	0.02			
TWEA	0.02			
OEA	0.013			
AB(a:0)	0.02			
TAB(a:0)	0.02			
BEB	0.06			
TBEB	0.06			
CSB	0.01			
TCSB	0.01			
OEB	0.013			
TEST	0.028			
BUB	0.042			
BUNRI	0.028			

Remark “a” = (number of address lines) – 1, where $4 \leq a \leq 10$
“b” = (number of bits) – 1, where $0 \leq b \leq 31$

3.2 Pin Function List

Pin Name/ Signal Name	Attribute	Mode	Port	Function
DIA(b:0)	I	Normal	R/W	Data input b = number of bits – 1
DOA(b:0)	OZ	Normal	R/W	Data output b = number of bits – 1
AA(a:0)	I	Normal	R/W	Address input a = number of address lines – 1 (determined by number of words)**Note**
BEA	I	Normal	R/W	Clock input
CSA	I	Normal	R/W	Chip select input
WEA	I	Normal	R/W	Write enable input
OEA	I	Normal	R/W	Data output enable input
TDIA(b:0)	I	Test	R/W	Data input b = number of bits – 1
TDOA(b:0)	OZ	Test	R/W	Data output b = number of bits – 1
TAA(a:0)	I	Test	R/W	Address input a = number of address lines – 1 (determined by number of words)**Note**
TBEA	I	Test	R/W	Clock input
TCSA	I	Test	R/W	Chip select input
TWEA	I	Test	R/W	Write enable input
DCA	O	Normal	R/W	Data control output DCA = 0: DOA(b:0) = 0, 1, undefined DCA = 1: DOA(b:0) = high impedance
DOB(b:0)	OZ	Normal	R	Data output b = number of bits – 1
AB(a:0)	I	Normal	R	Address input a = number of address lines – 1 (determined by number of words)**Note**
BEB	I	Normal	R	Clock input
CSB	I	Normal	R	Chip select input
OEB	I	Normal	R	Data output enable
TDOB(b:0)	OZ	Test	R	Data output b = number of bits – 1
TAB(a:0)	I	Test	R	Address input a = number of address lines – 1 (determined by number of words)**Note**
TBEB	I	Test	R	Clock input
TCSB	I	Test	R	Chip select input
DCB	O	Normal	R	Data control output DCB = 0: DOB(b:0) = 0, 1, undefined DCB = 1: DOB(b:0) = high impedance
BUNRI	I	Mode selection	–	Separation test input BUNRI = 0: Normal mode BUNRI = 1: Test mode
TEST	I	Mode selection	–	Test mode input BUNRI = 1, TEST = 0 Separated from test bus (tests other macros) BUNRI = 1, TEST = 1 Selected as subject to test
BUB	I	Mode selection	–	Backup mode input BUB = 0: Backup mode BUB = 1: Normal mode, test mode

Note number of address lines = $\log_2$ (number of words) (rounded up at decimal place)

Remark The meanings of the symbols in the Attribute column are as follows:
I: input pin, OZ: 3-state output pin, O: output pin
The meanings of the symbols in the Port column are as follows:
R/W: read/write port, R: read port

3.3 Operation Truth Table

The operating timing between a read/write port and a read port is partially restricted. For details, refer to **3.8.3 Operation timing restrictions between read/write port and read port**.

The meanings of the symbols in the following operation truth tables are as follows:

Hi-Z : High impedance
X : Undefined state not including high impedance
XZ : Undefined state including high impedance
AAx, ABx : Any data
DIAx : Input data
[AAx], [ABx] : Data in memory

BUB	BUNRI	TEST	Mode	Normal Pin Status			Test Pin Status	
				Input	Output	DCA/DCB	Input	Output
0	XZ	XZ	Backup	XZ	Hi-Z	1	XZ	Hi-Z
1	0	X	Normal	Valid	Valid	Valid	XZ	Hi-Z
1	1	0	Test (non-select)	XZ	Hi-Z	1	XZ	Hi-Z
1	1	1	Test (select)	XZ	Hi-Z	1	Valid	Valid

Normal mode access

Read/write port

CSA	BEA	WEA	OEA	AA(a:0)	DIA(b:0)	DOA(b:0)	DCA	Operation
0	↑	0	1	AAx	DIAx	Hi-Z	1	Write (output off)
0	↑	0	0	AAx	DIAx	[AAx] = DIAx**Note**	0	Write (output on)
0	↑	1	0	AAx	X	[AAx]	0	Read
0	0	X	0	X	X	Hold	0	Precharge
0	X	X	1	X	X	Hi-Z	1	Output off
1	X	X	X	X	X	Hi-Z	1	Macro off

Note The data input from the DIA(b:0) pin is output through.

Read port

CSB	BEB	OEB	AB(a:0)	DOB(b:0)	DCB	Operation
0	↑	0	ABx	[ABx]	0	Read
0	0	0	X	Hold	0	Precharge
0	X	1	X	Hi-Z	1	Output off
1	X	X	X	Hi-Z	1	Macro off

Test mode access

Read/write port

TCSA	TBEA	TWEA	TAA(a:0)	TDIA(b:0)	TDOA(b:0)	Operation
0	↑	0	AAx	DIAx	[AAx] = DIAx[Note]	Write
0	↑	1	AAx	X	[AAx]	Read
0	0	X	X	X	Hold	Precharge
1	X	X	X	X	Hold	Macro off

Note The data input from the TDIA(b:0) pin is output through.

Read port

TCSB	TBEB	TAB(a:0)	TDOB(b:0)	Operation
0	↑	ABx	[ABx]	Read
0	0	X	Hold	Precharge
1	X	X	Hold	Macro off

3.4 Macro Size

Use the following expression to calculate the macro size.

Macro size = X × Y (grids)

W : number of words
B : number of bits
N : number of address lines (N = $\log_2$W (rounded up at decimal place))
INT : Maximum integer which does not exceed the value in parentheses (**Example** INT (8.9) = 8)
α : Macro circumferential wiring area in X direction (73.53)
β : Macro circumferential wiring area in Y direction (7.353)

B ≤ 16	X = INT (0.18 × B + 1.48) × 9.48 + 5.59 × B + 0.88 × W + 186.65 + α	(grids)
	Y = 5.59 × B + 0.7 × N + 17.88 + β	(grids)
B > 16	X = INT (0.18 × B + 1.48) × 9.48 + 5.59 × B + 0.88 × W + 186.65 + α	(grids)
	Y = 5.59 × B + 0.7 × N + 20.61 + β	(grids)

Remarks 1. Round up the fraction below the decimal place.
2. Not necessary to add α and β when not taking the macro circumferential wiring area into consideration.

3.5 Electrical Characteristics

Absolute maximum ratings

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	–0.5 to +4.6	V
Operating ambient temperature	T_A	–40 to +85	°C
Storage temperature	T_{stg}	–65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended operating range (V_{DD} = 3.3 ± 0.3 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}	3.0	3.3	3.6	V
Operating ambient temperature	T_A	–40		+85	°C

3.6 Operating Current Consumption

The operating current consumption (I_{DD}) changes depending on the number of bits, number of words, number of address lines, and operating frequency of the memory. The value of the operating current consumption can be calculated by the following expression.

I_{DD} (TYP.) = I_{DDR} (TYP.) + I_{DDW} (TYP.) + I_{DDR2} (TYP.)
I_{DD} (MAX.) = I_{DDR} (MAX.) + I_{DDW} (MAX.) + I_{DDR2} (MAX.)

I_{DDR}, I_{DDW}, and I_{DDR2} in the above expression can be worked out by the expressions in the table below.

The meanings of the symbols in the tables below are as follows:
B: number of bits, W: number of words, N: number of address lines (N = $\log_2$W(rounded up at decimal place)),
f_R: read operating frequency (MHz), f_W: write operating frequency (MHz), C_L: external load capacitance (pF),
A: operation rate **Note 1** (100% = 1)
DFa: MAX. data rate (MHz) of AA (a:0), WEA, or DIA (b:0) pin
DFb: MAX. data rate (MHz) of AB (a:0) pin

(1) V_{DD} = 3.3 ± 0.3 V

TYP.
During read/write operation (α = 1.65 × B × C_L)

Port	Operation	Expression	Unit
Read/write	Read (I_{DDR})	$\{(0.375 \times N + 0.882 \times B - 1.531) \times 10^{-3} \times W + 1.3 \times N + 9.24 \times B + 7.6 + \alpha\} \times f_R \times A$	μA
	Write (I_{DDW})	$\{(0.375 \times N + 1.76 \times B - 1.531) \times 10^{-3} \times W + 1.3 \times N + 6.99 \times B + 8.1 + \alpha\} \times f_W \times A$	μA
Read	Read (I_{DDR2})	$\{(0.375 \times N + 0.882 \times B - 1.531) \times 10^{-3} \times W + 1.3 \times N + 9.24 \times B + 7.6 + \alpha\} \times f_R \times A$	μA

MAX.
During read/write operation (α = 1.8 × B × C_L)

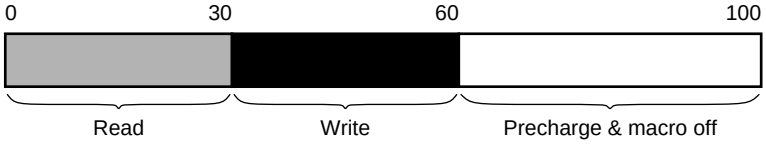
Port	Operation	Expression	Unit
Read/write	Read (I_{DDR})	$\{(0.536 \times N + 1.26 \times B - 2.189) \times 10^{-3} \times W + 1.85 \times N + 13.2 \times B + 10.95 + \alpha\} \times f_R \times A$	μA
	Write (I_{DDW})	$\{(0.536 \times N + 2.51 \times B - 2.189) \times 10^{-3} \times W + 1.85 \times N + 9.99 \times B + 11.55 + \alpha\} \times f_W \times A$	μA
Read	Read (I_{DDR2})	$\{(0.536 \times N + 1.26 \times B - 2.189) \times 10^{-3} \times W + 1.85 \times N + 13.2 \times B + 10.95 + \alpha\} \times f_R \times A$	μA

In power-down mode **Note 2**

Condition	Port	Expression	Unit
TYP.	Read/write	$\{0.903 \times 10^{-3} \times W \times (N - 5) + 1.05 \times N + 0.309 \times B - 2.33\} \times DFa$	μA
	Read	$\{0.903 \times 10^{-3} \times W \times (N - 5) + 1.05 \times N - 2.33\} \times DFb$	μA
MAX.	Read/write	$\{1.29 \times 10^{-3} \times W \times (N - 5) + 1.50 \times N + 0.441 \times B - 3.33\} \times DFa$	μA
	Read	$\{1.29 \times 10^{-3} \times W \times (N - 5) + 1.50 \times N - 3.33\} \times DFb$	μA

Notes 1. This operation rate is the ratio of the read and write operations to the total operation period (read, write, precharge, and macro off) of the RAM.

Example The operation rate is 60% (0.6) if read operations account for 30% of the total operation period of RAM and write operations account for 30%.



2. Power-down mode indicates the precharge status or macro off status in **Normal mode access** in **3.3 Operation Truth Table**.

Remarks 1. If all the input signals of this RAM are fixed, the current consumption in the standby mode (I_{DD1}) = 0.

2. Calculate the read/write operating frequency (MHz) based on the following concept (read 50%, write 50% during read/write operation).

Example To read and write alternately every 1 clock at 50 MHz
Calculate I_{DDR} and I_{DDW} assuming the following.
Read frequency: f_R = 25 MHz
Write frequency: f_W = 25 MHz

3. If OEB is fixed to H during write operation, α of I_{DDW} is 0 (in the write (output off) status in the normal mode access in the operation truth table).

3.7 Timing

3.7.1 Expressions

The timing values can be calculated by the following expressions (rounded at the third place below the decimal place. However, the output hold time is truncated).
The meanings of the symbols in the table below are as follows:
W: number of words, B: number of bits: N: number of address lines ($N = \log_2 W$ (rounded up at decimal place)),
C_L: external load capacitance (pF)

(1) $V_{DD} = 3.3 \pm 0.3$ V

Read/write operation (T_A = –40 to +85°C)

Parameter	Symbol	Expression	Unit
Cycle time	t_{RC}	Where $t_{BEH} > t_{PC}$: $t_{BEH} \times 2$ (clock duty: 50%) Where $t_{BEH} < t_{PC}$: $t_{PC} \times 2$ (clock duty: 50%)	ns
Access time	t_{ACC}	(W < 512) $3.15 + 15.0 \times 10^{-3} \times B + 8.04 \times 10^{-4} \times W + 1.63 \times 10^{-5} \times B \times W + 3.15 \times 10^{-1} \times C_L$ (W ≥ 512) $3.24 + 12.5 \times 10^{-3} \times B + 6.3 \times 10^{-4} \times W + 1.63 \times 10^{-5} \times B \times W + 3.15 \times 10^{-1} \times C_L$	ns
Output hold time	t_{OH}	$0.40 + 2.08 \times 10^{-3} \times B$	ns
BEA, BEB high-level time	t_{BEH_A} t_{BEH_B}	(W < 512) $3.15 + 15.0 \times 10^{-3} \times B + 8.04 \times 10^{-4} \times W + 1.63 \times 10^{-5} \times B \times W$ (W ≥ 512) $3.24 + 12.5 \times 10^{-3} \times B + 6.3 \times 10^{-4} \times W + 1.63 \times 10^{-5} \times B \times W$	ns
Precharge time	t_{PC}	(W < 512) $1.14 + 12.8 \times 10^{-3} \times B + 3.8 \times 10^{-4} \times W + 0.1 \times 10^{-4} \times B \times W$ (W ≥ 512) $0.58 + 17.0 \times 10^{-3} \times B + 1.26 \times 10^{-3} \times W + 0.22 \times 10^{-4} \times B \times W$	ns
Address setup time	t_{AS}	$1.16 + 6.25 \times 10^{-5} \times W$	ns
Address hold time	t_{AH}	$0.75 \times 10^{-1} + 0.15 \times 10^{-1} \times N$	ns
Write data setup time	t_{DIS}	0.13	ns
Write data hold time	t_{DIH}	$0.34 + 7.25 \times 10^{-3} \times B$	ns
Write data through time	t_{DTH}	$2.30 + 7.25 \times 10^{-3} \times B + 3.15 \times 10^{-1} \times C_L$	ns
WEA setup time	t_{WS}	0.21	ns
WEA hold time	t_{WH}	0	ns
CSA, CSB setup time	t_{CS}	0.62	ns
CSA, CSB hold time	t_{CH}	0	ns
CSA, CSB control time			
Output floating time	t_{HZ}	$1.75 + 7.92 \times 10^{-3} \times B$	ns
Output active time	t_{LZ}	$1.87 + 9.70 \times 10^{-3} \times B$	ns
DC output delay time	t_{DC}	$1.67 + 8.75 \times 10^{-3} \times B + 7.15 \times 10^{-1} \times C_L$	ns
OEA, OEB control time			
Output floating time	t_{HZ}	$1.10 + 8.75 \times 10^{-3} \times B$	ns
Output active time	t_{LZ}	$1.19 + 0.01 \times B$	ns
DC output delay time	t_{DC}	$1.08 + 8.75 \times 10^{-3} \times B + 7.15 \times 10^{-1} \times C_L$	ns

3.7.2 Typical value (8 bits × 512 words)

(1) V_{DD} = 3.3 ± 0.3 V

Read/write operation (T_A = –40 to + 85°C)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Cycle time	t_{RC}	7.46			ns
Access time	t_{ACC}			3.80	ns
Output hold time	t_{OH}	0.41			ns
BEA, BEB high-level time	t_{BEH_A} t_{BEH_B}	3.73			ns
Precharge time	t_{PC}	1.46			ns
Address setup time	t_{AS}	1.20			ns
Address hold time	t_{AH}	0.21			ns
Write data setup time	t_{DIS}	0.13			ns
Write data hold time	t_{DIH}	0.40			ns
Write data through time	t_{DTH}			2.43	ns
WEA setup time	t_{WS}	0.21			ns
WEA hold time	t_{WH}	0			ns
CSA, CSB setup time	t_{CS}	0.62			ns
CSA, CSB hold time	t_{CH}	0			ns
CSA, CSB control					
Output floating time	t_{HZ}	1.82			ns
Output active time	t_{LZ}	1.95			ns
DC output delay time	t_{DC}			1.89	ns
OEA, OEB control					
Output floating time	t_{HZ}	1.17			ns
Output active time	t_{LZ}	1.27			ns
DC output delay time	t_{DC}			1.30	ns

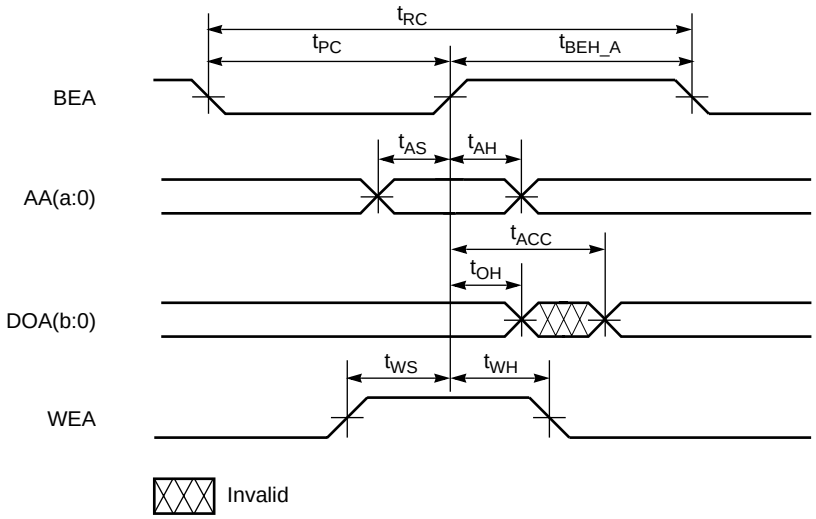
Remarks 1. The above values are calculated with an external load capacitance of 0.2 pF.
2. The meanings of the symbols in the above table are as follows:
MIN.: minimum value necessary for operating macro under worst condition
MAX.: delay time of macro output under worst condition

3.8 Timing Chart

3.8.1 Read/write port

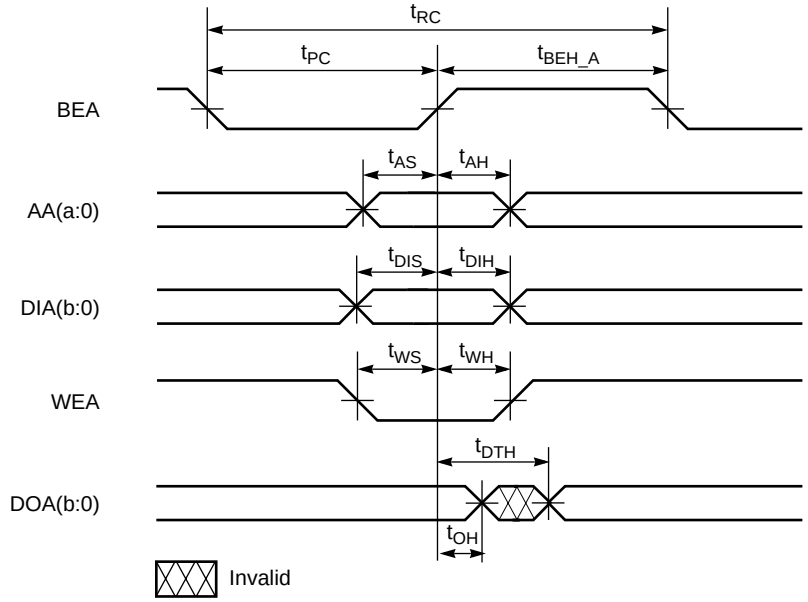
Read operation

Read cycle (CSA = low level, OEA = low level)



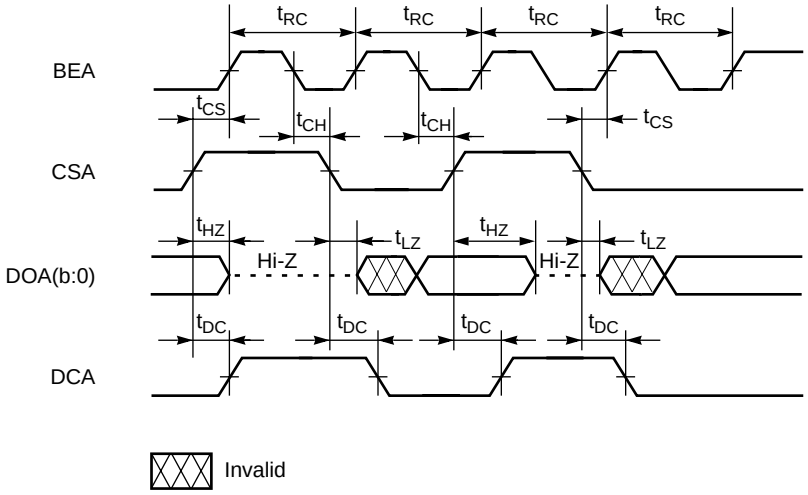
Write operation

Write cycle (CSA = low level, OEA = low level)

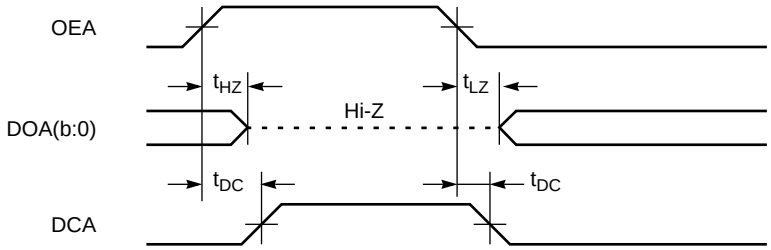


Read/write operation

(1) CSA control (OEA = low level)

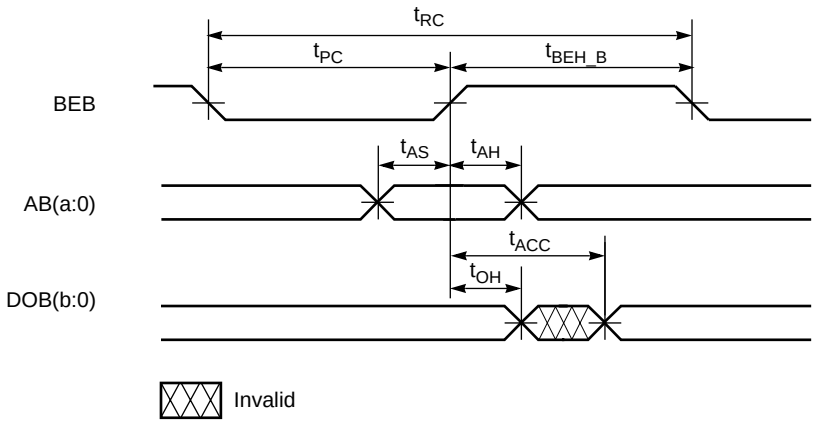


(2) OEA control (CSA = low level)

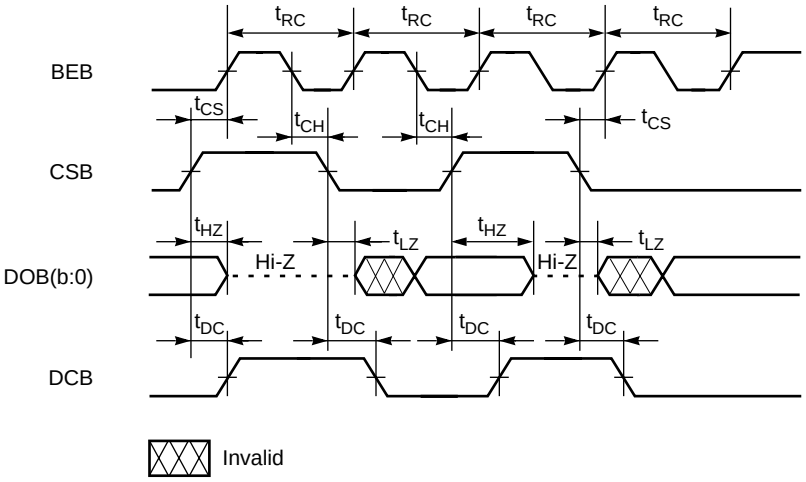


3.8.2 Read port

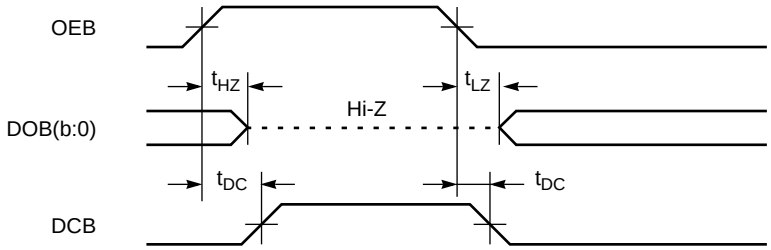
(1) Read cycle (CSB = low level, OEB = low level)



(2) CSB control (OEB = low level)



(3) OEB control (CSB = low level)



3.8.3 Operation timing restrictions between read/write port and read port

(1) When the read/write port and the read port access different addresses

There is no restriction imposed on the operation timing between the read/write port and the read port.
For the operation of each port, refer to the operating timing of **3.8.1 Read/write port** and **3.8.2 Read port**.

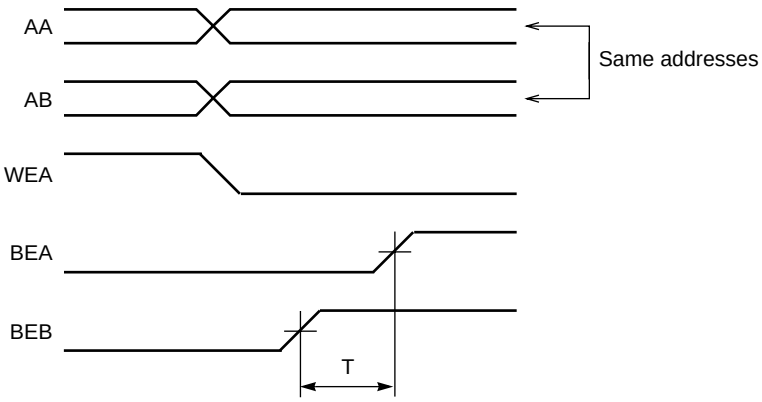
(2) When the read/write port and the read port access the same address

(a) When the read/write port performs a read operation

There is no restriction imposed on the operation timing between the read/write port and the read port.
For the operation of each port, refer to the operating timing of **3.8.1 Read/write port** and **3.8.2 Read port**.

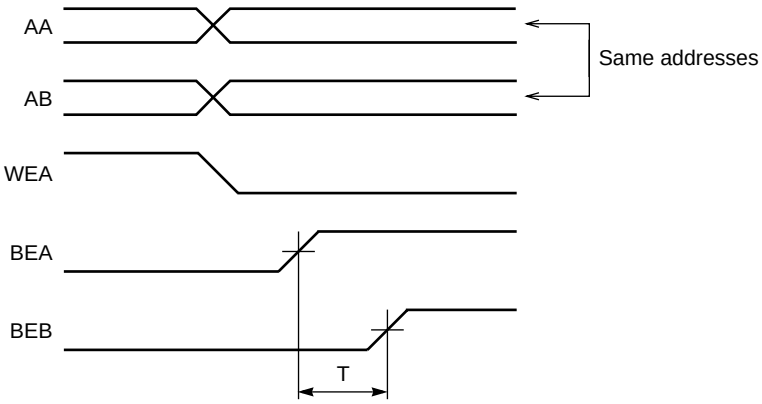
(b) When the read/write port performs a write operation

[If BEA (read/write port clock) rises after or at the same timing as BEB (read port clock) (Refer to the figure below.)]



Read Port Spec.	Operation Timing
If $T \leq t_{BEH\_B}$	Write operation from the read/write port is performed correctly. Output of the read port is undefined.
If $T > t_{BEH\_B}$	Write operation from the read/write port is performed correctly. The read port outputs the previous write data.

[If BEA (read/write port clock) rises before BEB (read port clock) (Refer to the figure below.)]



The operation timing is as follows:

Read/Write Port Spec.	Operation Timing
If $T \leq t_{BEH\_A}$	Write operation from the read/write port is performed correctly. Output of the read port is undefined.
If $T > t_{BEH\_A}$	Write operation from the read/write port is performed correctly. Output of the read port is also performed correctly.

For the operation of each port, refer to the operating timing of **3.8.1 Read/write port** and **3.8.2 Read port**.

3.9 Notes on Correct Use

(1) If a spike is input to the clock input pin while CSA or CSB = L, the data in the RAM may be destroyed. In this case, the addresses other than that when the spike was input may be also destroyed.

(2) When using a RAM macro of less than 2^N words, do not access a non-existent address **Note**. Otherwise, the output data of the preceding cycle is not retained.

Note Specifically, this means an access to W+1 to 2^N where $W < 2^N$. For example, when a RAM macro of 1 bit × 160 words is used and the number of address lines (N) is 8, 161 through 256 words are non-existent addresses.

(3) If a non-existent address is accessed, an overcurrent flows during read operation (WEA = H, BEA = H, BEB = H) (the overcurrent does not flow during write operation or in macro off status). In addition, even when there are no non-existent addresses, an overcurrent flows immediately after power application until the address is confirmed. The overcurrent can be calculated by the following expression.

- **Overcurrent when non-existent address or uncertain address is accessed**
  $[V_{DD} = 3.3 \pm 0.3\ V]$
  ΔI_{DD} (TYP.) $= 1.671 \times (B + 1)$ [mA]
  ΔI_{DD} (MAX.) $= 3.4226 \times (B + 1)$ [mA]

Remarks 1. B: Number of bits of RAM accessed
2. Calculate the overcurrent of the high-speed dual-port (1R/W+1R) RAM (synchronous type) for each port (read/write port, read port).

★ (4) Current may continue to flow if the clock is stopped at a high level when power is applied, so be sure to either stop the clock while the clock pin is low, or input the clock first low then high (or high → low → high). If the clock is input at a low level even once, current will not flow no matter how the clock is subsequently stopped.

3.10 Other Notes on Correct Use

Although this RAM has a read/write port and a read port, these ports can be also used as a write port and a read port.
The connections when the ports are used as a write port and a read port are shown below. For the operating timing, refer to the operating timing of **3.8.1 Read/write port** and **3.8.2 Read port**.

Pin Name	I/O	Connection
WEA	Input	Fixed to low level
DOA(b:0)	Output	Open

CHAPTER 4 HIGH-DENSITY SINGLE-PORT RAM (SYNCHRONOUS TYPE)

4.1 General

- Dedicated to VX/VM
- Single-port SRAM (I/O separation type)
- High-density integration
- Flexible memory size
  → High efficiency macro location by memory compiler.
  Block name: W8Kxxxxx, W8Uxxxxx
  Bit width: 1 to 32 bits (variable in 1-bit units)
  Number of words: 32 to 4096 words (variable in 32-word units)
  Block name: W8Txxxxx
  Bit width: 1 to 32 bits (variable in 1-bit units)
  Number of words: 4160 to 8192 words (variable in 64-word units)
- Operating voltage: 3.3 ± 0.3 V, 2.0 ± 0.2 V
- Operating ambient temperature: –40 to +85°C
- Storage temperature: –65 to +150°C
- 0.35 μm CMOS technology

4.1.1 Compiled range

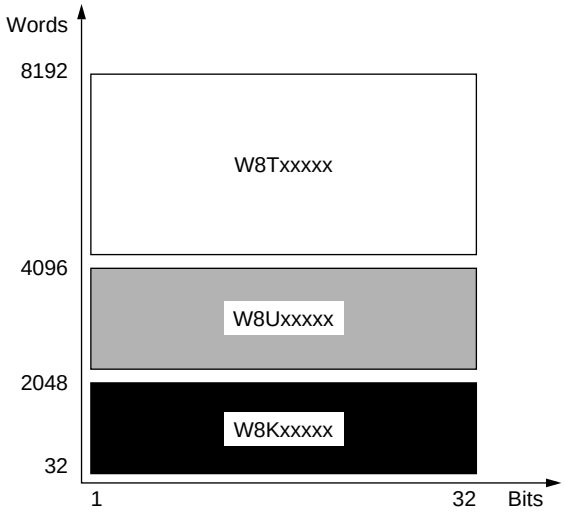
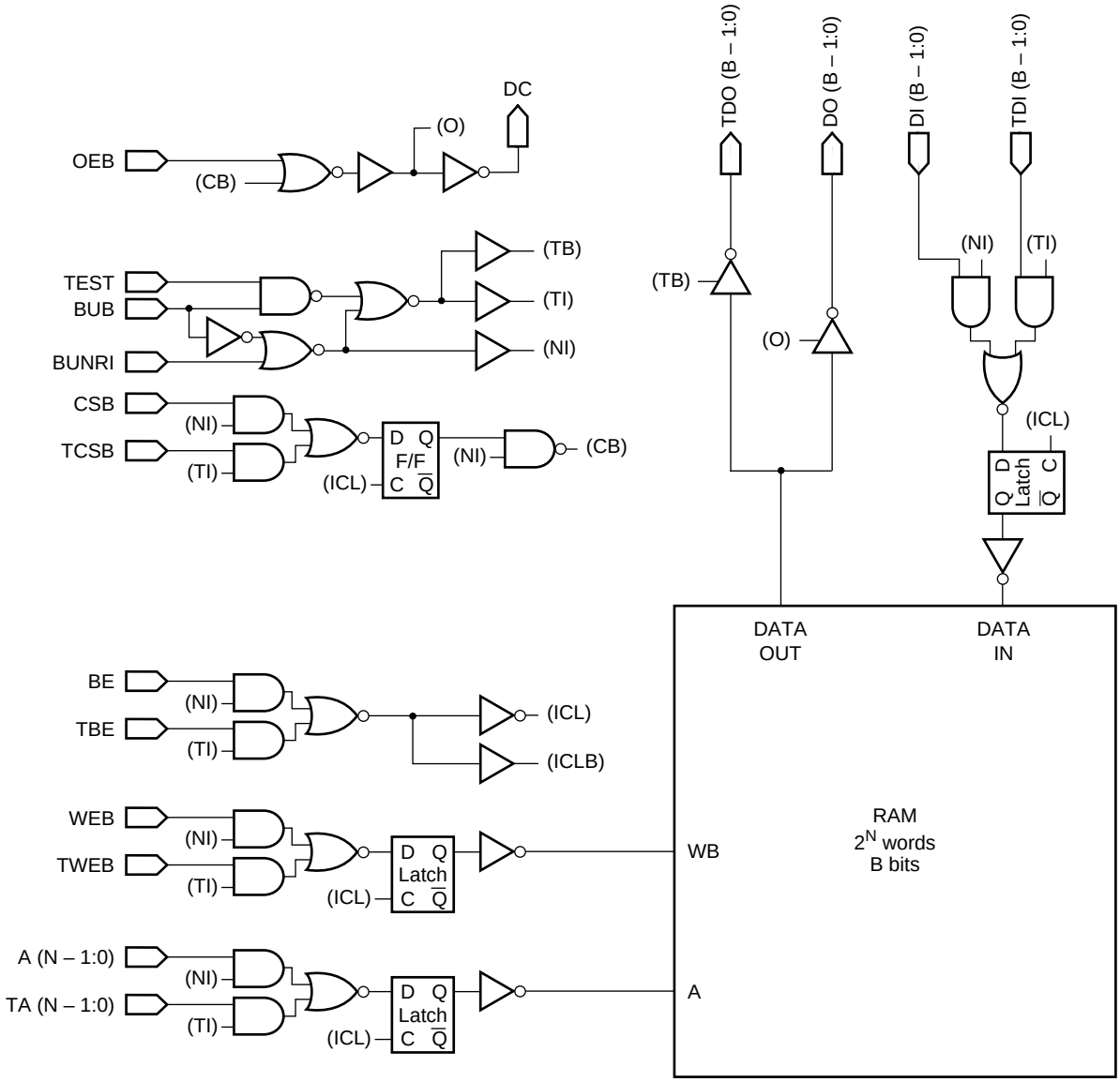


Figure 4-1 Compiled Range of High-Density Single-Port RAM (Synchronous Type)

Table 4-1 Compiled Range of High-Density Single-Port RAM (Synchronous Type)

Block Name	Minimum Size	Maximum Size	Step
W8Kxxxxx	32 words × 1 bit	2048 words × 32 bits	32 words/1 bit
W8Uxxxxx	2080 words × 1 bit	4096 words × 32 bits	32 words/1 bit
W8Txxxxx	4160 words × 1 bit	8192 words × 32 bits	64 words/1 bit

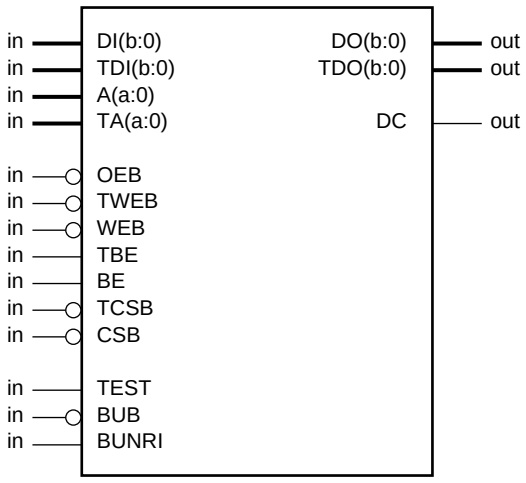
4.1.2 Equivalent circuit



Remark N: number of address lines, B: numbr of bits

Figure 4-2 Internal Equivalent Circuit

4.1.3 Symbol diagram



Remarks 1. A pin prefixed with “T” is a test pin.
2. “a” = (number of address lines) – 1, where $4 \le a \le 12$
“b” = (number of bits) – 1, where $0 \le b \le 31$.

4.1.4 Pin capacitance

Pin Information GateDRC uses C_{IN} and C_{MAX} for fanin/fanout calculation.
Wiring capacitance = temporary wiring length × 0.18 (pF/mm)

Input		Output		
Pin Name/Symbol	**CIN (pF)**	**Pin Name/Symbol**	**CIN (pF)**	**CMAX (pF)**
DI(b:0)	0.068	DO(b:0)	0.077	6.3167
TDI(b:0)	0.068			(2.0966)
A(a:0)	0.064	TDO(b:0)	0.077	6.3167
TA(a:0)	0.064			(2.0966)
BE	0.172	DC	–	1.7976
TBE	0.172			(0.6280)
CSB	0.064			
TCSB	0.064			
WEB	0.067			
TWEB	0.067			
OEB	0.064			
TEST	0.066			
BUB	0.067			
BUNRI	0.065			

Remarks 1. ( ): Value at $V_{DD} = 2.0 \pm 0.2$ V
2. “a” = (number of address lines) – 1, where $4 \le a \le 12$
“b” = (number of bits) – 1, where $0 \le b \le 31$

4.2 Pin Function List

Pin Name/ Signal Name	Attribute	Mode	Function
DI(b:0)	I	Normal	Data input b = number of bits – 1
DO(b:0)	OZ	Normal	Data output b = number of bits – 1
A(a:0)	I	Normal	Address input a = number of address lines – 1 (determined by number of words)**Note**
BE	I	Normal	Clock input
CSB	I	Normal	Chip select input
WEB	I	Normal	Write enable input
OEB	I	Normal	Data output enable input
TDI(b:0)	I	Test	Data input b = number of bits – 1
TDO(b:0)	OZ	Test	Data output b = number of bits – 1
TA(a:0)	I	Test	Address input a = number of address lines – 1 (determined by number of words)**Note**
TBE	I	Test	Clock input
TCSB	I	Test	Chip select input
TWEB	I	Test	Write enable input
BUNRI	I	Mode selection	Separation test input BUNRI = 0: Normal mode BUNRI = 1: Test mode
TEST	I	Mode selection	Test mode input BUNRI = 1, TEST = 0 Separated from test bus (tests other macros) BUNRI = 1, TEST = 1 Selected as subject to test
BUB	I	Mode selection	Backup mode input BUB = 0: Backup mode BUB = 1: Normal mode, test mode
DC	O	Normal	Data control output DC = 0: DO(b:0) = 0, 1, undefined DC = 1: DO(b:0) = high impedance

Note number of address lines = $\log_2$ (number of words) (rounded up at decimal place)

Remark The meanings of the symbols in the Attribute column are as follows:
I: input pin, OZ: 3-state output pin, O: output pin

4.3 Operation Truth Table

The meanings of the symbols in the following operation truth tables are as follows:

Hi-Z : High impedance
X : Undefined state not including high impedance
XZ : Undefined state including high impedance
Ax : Any data
DIx : Input data
[Ax] : Data in memory

BUB	BUNRI	TEST	Mode	Normal Pin Status			Test Pin Status	
				Input	Output	DC	Input	Output
0	XZ	XZ	Backup	XZ	Hi-Z	1	XZ	Hi-Z
1	0	X	Normal	Valid	Valid	Valid	XZ	Hi-Z
1	1	0	Test (non-select)	XZ	Hi-Z	1	XZ	Hi-Z
1	1	1	Test (select)	XZ	Hi-Z	1	Valid	Valid

Normal mode access

CSB	BE	WEB	OEB	A(a:0)	DI(b:0)	DO(b:0)	DC	Operation
0	↑	0	1	Ax	DIx	Hi-Z	1	Write (output off)
0	↑	0	0	Ax	DIx	[Ax] = DIx **Note**	0	Write (output on)
0	↑	1	0	Ax	X	[Ax]	0	Read
0	0	X	0	X	X	Hold	Hold	Precharge
0	X	X	1	X	X	Hi-Z	1	Output off
1	↑	X	X	X	X	Hi-Z	1	Macro off

Note The data input from the DI(b:0) pin is output through.

Test mode access

TCSB	TBE	TWEB	TA (a:0)	TDI(b:0)	TDO(b:0)	Operation
0	↑	0	Ax	DIx	[Ax] = DIx **Note**	Write
0	↑	1	Ax	X	[Ax]	Read
0	0	X	X	X	Hold	Precharge
1	↑	X	X	X	Hold	Macro off

Note The data input from the TDI(b:0) pin is output through.

4.4 Macro Size

Use the following expressions to calculate the macro size.

Macro size = X × Y (grids)

W : number of words
B : number of bits
α : Macro circumferential wiring area in X direction (73.53)
β : Macro circumferential wiring area in Y direction (7.353)

In case of 32 to 2048 words

$X = 26.81 \times B + X_1 + \alpha$ [grids]
$Y = 5.87 \times 10^{-2} \times W + Y_1 + \beta$ [grids]

$1 \leq B < 8$

Number of Words	32	64	96 to 128	160 to 256	288 to 480	512	544 to 1024	1056 to 2048
X_1	124.39	131.93	136.74	144.28	149.09	152.03	159.58	164.39
Y_1	21.61	21.61	21.61	21.61	21.61	21.90	22.00	22.00

$8 \leq B < 16$

Number of Words	32	64	96 to 128	160 to 256	288 to 512	544 to 1024	1056 to 2048
X_1	127.33	134.87	139.68	147.23	152.03	159.58	164.39
Y_1	21.90	21.90	21.90	21.90	21.90	22.00	22.00

$16 \leq B \leq 32$

Number of Words	32	64	96 to 128	160 to 256	288 to 512	544 to 1024	1056 to 2048
X_1	130.27	137.81	142.62	150.17	154.98	162.52	167.33
Y_1	22.19	22.19	22.19	22.19	22.19	22.30	22.30

In case of 2080 to 4096 words
$X = 53.62 \times B + 223.39 + \alpha$ [grids]
$Y = 0.203 \times B + 2.94 \times 10^{-2} \times W + 22.74 + \beta$ [grids]

In case of 4160 to 8192 words
$X = 107.24 \times B + 248.43 + \alpha$ [grids]
$Y = 0.203 \times B + 1.47 \times 10^{-2} \times W + 21.96 + \beta$ [grids]

Remarks 1. Round up the fraction below the decimal place.
2. Not necessary to add α and β when not taking the macro circumferential wiring area into consideration.

4.5 Electrical Characteristics

Absolute maximum ratings

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	–0.5 to +4.6	V
Operating ambient temperature	T_A	–40 to +85	°C
Storage temperature	T_{stg}	–65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended operating range (V_{DD} = 3.3 ± 0.3 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}	3.0	3.3	3.6	V
Operating ambient temperature	T_A	–40		+85	°C

Recommended operating range (V_{DD} = 2.0 ± 0.2 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}	1.8	2.0	2.2	V
Operating ambient temperature	T_A	–40		+85	°C

4.6 Operating Current Consumption

The operating current consumption (I_{DD}) changes depending on the number of bits, number of words, and operating frequency of the memory. The value of the operating current consumption can be calculated by the following expression.

I_{DD} (TYP.) = I_{DDR} (TYP.) + I_{DDW} (TYP.)
I_{DD} (MAX.) = I_{DDR} (MAX.) + I_{DDW} (MAX.)

I_{DDR} and I_{DDW} in the above expression can be worked out by the expressions in the table below.

The meanings of the symbols in the tables below are as follows:
B: number of bits, W: number of words, f_R: read operating frequency (MHz),
f_W: write operating frequency (MHz), C_L: external load capacitance (pF),
A: operation rate **Note** (100% = 1)

(1) V_{DD} = 3.3 ± 0.3 V

TYP. (α : 1.65 × C_L × B)

Number of Words	Operation	Expression	Unit
At 32 to 2048	Read (I_{DDR})	$\{(1.60 \times B + 23.22) \times 10^{-3} \times W + 5.23 \times B + 36.45 + \alpha\} \times f_R \times A$	μA
	Write (I_{DDW})	$\{(2.43 \times B + 23.03) \times 10^{-3} \times W + 6.08 \times B + 41.31 + \alpha\} \times f_W \times A$	μA
At 2080 to 4096	Read (I_{DDR})	$\{(0.38 \times B + 20.80) \times 10^{-3} \times W + 12.42 \times B + 54.55 + \alpha\} \times f_R \times A$	μA
	Write (I_{DDW})	$\{(0.96 \times B + 19.46) \times 10^{-3} \times W + 14.49 \times B + 44.58 + \alpha\} \times f_W \times A$	μA
At 4160 to 8192	Read (I_{DDR})	$\{(0.27 \times B + 8.72) \times 10^{-3} \times W + 17.78 \times B + 42.57 + \alpha\} \times f_R \times A$	μA
	Write (I_{DDW})	$\{(0.72 \times B + 7.58) \times 10^{-3} \times W + 21.77 \times B + 37.24 + \alpha\} \times f_W \times A$	μA

MAX. (α : 1.8 × C_L × B)

Number of Words	Operation	Expression	Unit
At 32 to 2048	Read (I_{DDR})	$\{(2.40 \times B + 24.73) \times 10^{-3} \times W + 6.09 \times B + 50.81 + \alpha\} \times f_R \times A$	μA
	Write (I_{DDW})	$\{(3.42 \times B + 23.92) \times 10^{-3} \times W + 6.99 \times B + 55.67 + \alpha\} \times f_W \times A$	μA
At 2080 to 4096	Read (I_{DDR})	$\{(0.76 \times B + 22.04) \times 10^{-3} \times W + 14.46 \times B + 65.67 + \alpha\} \times f_R \times A$	μA
	Write (I_{DDW})	$\{(1.29 \times B + 21.08) \times 10^{-3} \times W + 16.87 \times B + 58.19 + \alpha\} \times f_W \times A$	μA
At 4160 to 8192	Read (I_{DDR})	$\{(0.86 \times B + 7.21) \times 10^{-3} \times W + 19.82 \times B + 54.20 + \alpha\} \times f_R \times A$	μA
	Write (I_{DDW})	$\{(1.12 \times B + 7.87) \times 10^{-3} \times W + 25.59 \times B + 50.52 + \alpha\} \times f_W \times A$	μA

(2) V_{DD} = 2.0 ± 0.2 V

TYP. (α : 1.0 × C_L × B)

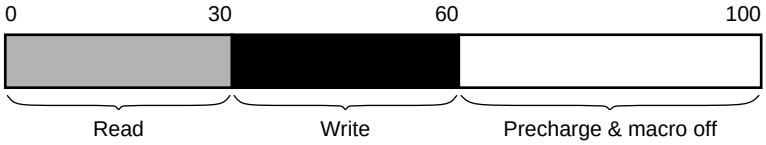
Number of Words	Operation	Expression	Unit
At 32 to 2048	Read (I_{DDR})	$\{(1.08 \times B + 13.15) \times 10^{-3} \times W + 2.86 \times B + 18.00 + \alpha\} \times f_R \times A$	μA
	Write (I_{DDW})	$\{(1.59 \times B + 13.12) \times 10^{-3} \times W + 3.33 \times B + 23.47 + \alpha\} \times f_W \times A$	μA
At 2080 to 4096	Read (I_{DDR})	$\{(0.33 \times B + 11.60) \times 10^{-3} \times W + 7.06 \times B + 28.71 + \alpha\} \times f_R \times A$	μA
	Write (I_{DDW})	$\{(0.62 \times B + 11.24) \times 10^{-3} \times W + 8.46 \times B + 22.13 + \alpha\} \times f_W \times A$	μA
At 4160 to 8192	Read (I_{DDR})	$\{(0.26 \times B + 4.71) \times 10^{-3} \times W + 10.41 \times B + 19.67 + \alpha\} \times f_R \times A$	μA
	Write (I_{DDW})	$\{(0.51 \times B + 4.01) \times 10^{-3} \times W + 12.52 \times B + 21.77 + \alpha\} \times f_W \times A$	μA

MAX. (α : 1.1 × C_L × B)

Number of Words	Operation	Expression	Unit
At 32 to 2048	Read (I_{DDR})	$\{(1.48 \times B + 16.25) \times 10^{-3} \times W + 3.35 \times B + 28.67 + \alpha\} \times f_R \times A$	μA
	Write (I_{DDW})	$\{(2.17 \times B + 14.39) \times 10^{-3} \times W + 3.87 \times B + 31.13 + \alpha\} \times f_W \times A$	μA
At 2080 to 4096	Read (I_{DDR})	$\{(0.45 \times B + 13.06) \times 10^{-3} \times W + 8.55 \times B + 32.60 + \alpha\} \times f_R \times A$	μA
	Write (I_{DDW})	$\{(0.80 \times B + 12.76) \times 10^{-3} \times W + 9.95 \times B + 26.12 + \alpha\} \times f_W \times A$	μA
At 4160 to 8192	Read (I_{DDR})	$\{(0.57 \times B + 4.21) \times 10^{-3} \times W + 11.87 \times B + 27.43 + \alpha\} \times f_R \times A$	μA
	Write (I_{DDW})	$\{(0.73 \times B + 4.18) \times 10^{-3} \times W + 14.99 \times B + 29.12 + \alpha\} \times f_W \times A$	μA

Note This operation rate is the ratio of the read and write operations to the total operation period (read, write, precharge, and macro off) of the RAM.

Example The operation rate is 60% (0.6) if read operations account for 30% of the total operation period of RAM and write operations account for 30%.



Remarks 1. If all the input signals of this RAM are fixed, the current consumption in the standby mode (I_{DD1}) = 0.

2. Calculate the read/write operating frequency (MHz) based on the following concept (read 50%, write 50% during read/write operation).

Example To read and write alternately every 1 clock at 50 MHz
Calculate I_{DDR} and I_{DDW} assuming the following.
Read frequency: f_R = 25 MHz
Write frequency: f_W = 25 MHz

3. If OEB is fixed to H during write operation, α of I_{DDW} is 0 (in the write (output off) status for the normal mode access in the operation truth table).

4.7 Timing

4.7.1 Expressions

The timing values can be calculated by the following expressions (rounded at the third place below the decimal place. However, the output hold time is truncated).

The meanings of the symbols in the table below are as follows:
W: number of words, B: number of bits, C_L: external load capacitance (pF)

(1) V_{DD} = 3.3 ± 0.3 V

In case of 32 to 2048 words (T_A = –40 to +85°C)

Parameter	Symbol	Expression	Unit
Cycle time	t_{RC}	Where $t_{ACC} > t_{BEH} + t_{PC}$: t_{ACC} Where $t_{ACC} < t_{BEH} + t_{PC}$: $t_{BEH} + t_{PC}$	ns
Access time	t_{ACC}	$6.83 + 4.86 \times 10^{-2} \times B + 1.33 \times 10^{-3} \times W + 1.72 \times 10^{-6} \times B \times W + 0.74 \times C_L$	ns
Output hold time	t_{OH}	$1.20 + 1.97 \times 10^{-3} \times B - 1.74 \times 10^{-5} \times W + 1.39 \times 10^{-6} \times B \times W$	ns
BE high-level time	t_{BEH}	$5.01 + 5.16 \times 10^{-2} \times B + 1.31 \times 10^{-3} \times W + 4.07 \times 10^{-7} \times B \times W$	ns
Precharge time	t_{PC}	$1.68 + 1.14 \times 10^{-2} \times B + 2.49 \times 10^{-3} \times W - 2.94 \times 10^{-6} \times B \times W$	ns
Address setup time	t_{AS}	$2.45 + 1.88 \times 10^{-2} \times B + 3.09 \times 10^{-5} \times W - 8.59 \times 10^{-6} \times B \times W$	ns
Address hold time	t_{AH}	0	ns
Write data setup time	t_{DIS}	$2.49 - 2.04 \times 10^{-3} \times B - 9.30 \times 10^{-6} \times W - 3.50 \times 10^{-7} \times B \times W$	ns
Write data hold time	t_{DIH}	0	ns
Write data through time	t_{DTH}	$4.36 + 9.61 \times 10^{-3} \times B + 2.79 \times 10^{-5} \times W + 5.83 \times 10^{-7} \times B \times W + 0.74 \times C_L$	ns
WEB setup time	t_{WS}	$1.52 + 1.84 \times 10^{-3} \times B - 1.43 \times 10^{-5} \times W - 1.10 \times 10^{-7} \times B \times W$	ns
WEB hold time	t_{WH}	0	ns
CSB setup time	t_{CS}	$1.78 - 4.65 \times 10^{-5} \times B - 8.00 \times 10^{-8} \times W$	ns
CSB hold time	t_{CH}	0	ns
Output floating time	t_{HZ}	$2.93 + 1.38 \times 10^{-2} \times B + 4.62 \times 10^{-7} \times W - 2.20 \times 10^{-8} \times B \times W$	ns
Output active time	t_{LZ}	$1.24 + 1.36 \times 10^{-2} \times B$	ns
DC output delay time	t_{DC}	$2.85 + 1.40 \times 10^{-2} \times B - 1.62 \times 10^{-6} \times W + 6.60 \times 10^{-8} \times B \times W + 2.64 \times C_L$	ns

In case of 2080 to 4096 words (T_A = –40 to +85°C)

Parameter	Symbol	Expression	Unit
Cycle time	t_{RC}	Where $t_{ACC} > t_{BEH} + t_{PC}$: t_{ACC} Where $t_{ACC} < t_{BEH} + t_{PC}$: $t_{BEH} + t_{PC}$	ns
Access time	t_{ACC}	$9.82 + 5.17 \times 10^{-2} \times B + 5.03 \times 10^{-4} \times W + 1.96 \times 10^{-6} \times B \times W + 0.74 \times C_L$	ns
Output hold time	t_{OH}	$1.09 + 3.52 \times 10^{-3} \times B - 9.72 \times 10^{-7} \times W + 1.71 \times 10^{-7} \times B \times W$	ns
BE high-level time	t_{BEH}	$7.83 + 4.08 \times 10^{-2} \times B + 4.93 \times 10^{-4} \times W + 2.19 \times 10^{-6} \times B \times W$	ns
Precharge time	t_{PC}	$1.41 + 3.45 \times 10^{-4} \times B + 1.26 \times 10^{-3} \times W + 3.14 \times 10^{-6} \times B \times W$	ns
Address setup time	t_{AS}	$2.72 + 4.18 \times 10^{-3} \times B + 7.14 \times 10^{-5} \times W - 9.90 \times 10^{-7} \times B \times W$	ns
Address hold time	t_{AH}	0	ns
Write data setup time	t_{DIS}	$2.92 - 7.18 \times 10^{-3} \times B + 1.18 \times 10^{-5} \times W - 4.50 \times 10^{-7} \times B \times W$	ns
Write data hold time	t_{DIH}	0	ns
Write data through time	t_{DTH}	$5.77 + 3.44 \times 10^{-2} \times B + 4.54 \times 10^{-5} \times W - 1.67 \times 10^{-6} \times B \times W + 0.74 \times C_L$	ns
WEB setup time	t_{WS}	$1.60 + 2.04 \times 10^{-5} \times B + 3.41 \times 10^{-6} \times W + 6.00 \times 10^{-8} \times B \times W$	ns
WEB hold time	t_{WH}	0	ns
CSB setup time	t_{CS}	$1.97 + 9.41 \times 10^{-4} \times B - 2.72 \times 10^{-6} \times W - 3.30 \times 10^{-7} \times B \times W$	ns
CSB hold time	t_{CH}	0	ns
Output floating time	t_{HZ}	$3.62 + 9.87 \times 10^{-3} \times B + 3.21 \times 10^{-6} \times W + 4.07 \times 10^{-7} \times B \times W$	ns
Output active time	t_{LZ}	$1.25 + 1.21 \times 10^{-2} \times B + 1.64 \times 10^{-5} \times W - 8.19 \times 10^{-7} \times B \times W$	ns
DC output delay time	t_{DC}	$3.54 + 9.90 \times 10^{-3} \times B + 1.65 \times 10^{-6} \times W + 4.84 \times 10^{-7} \times B \times W + 2.64 \times C_L$	ns

In case of 4160 to 8192 words (T_A = –40 to +85°C)

Parameter	Symbol	Expression	Unit
Cycle time	t_{RC}	Where $t_{ACC} > t_{BEH} + t_{PC}$: t_{ACC} Where $t_{ACC} < t_{BEH} + t_{PC}$: $t_{BEH} + t_{PC}$	ns
Access time	t_{ACC}	$9.95 + 9.40 \times 10^{-2} \times B + 2.63 \times 10^{-4} \times W + 1.38 \times 10^{-6} \times B \times W + 0.74 \times C_L$	ns
Output hold time	t_{OH}	$0.84 + 1.19 \times 10^{-2} \times B - 4.23 \times 10^{-7} \times W + 4.50 \times 10^{-8} \times B \times W$	ns
BE high-level time	t_{BEH}	$8.45 + 6.22 \times 10^{-2} \times B + 2.59 \times 10^{-4} \times W + 1.50 \times 10^{-6} \times B \times W$	ns
Precharge time	t_{PC}	$1.39 + 8.66 \times 10^{-3} \times B + 6.50 \times 10^{-4} \times W - 1.98 \times 10^{-7} \times B \times W$	ns
Address setup time	t_{AS}	$2.54 + 2.65 \times 10^{-2} \times B + 4.95 \times 10^{-5} \times W - 3.04 \times 10^{-6} \times B \times W$	ns
Address hold time	t_{AH}	0	ns
Write data setup time	t_{DIS}	$2.77 - 2.53 \times 10^{-2} \times B + 1.18 \times 10^{-6} \times W + 1.00 \times 10^{-8} \times B \times W$	ns
Write data hold time	t_{DIH}	0	ns
Write data through time	t_{DTH}	$6.14 + 4.48 \times 10^{-2} \times B - 1.12 \times 10^{-6} \times W + 1.54 \times 10^{-7} \times B \times W + 0.74 \times C_L$	ns
WEB setup time	t_{WS}	$1.39 - 1.24 \times 10^{-4} \times B + 1.44 \times 10^{-6} \times W - 4.00 \times 10^{-8} \times B \times W$	ns
WEB hold time	t_{WH}	0	ns
CSB setup time	t_{CS}	$1.81 - 1.28 \times 10^{-3} \times B$	ns
CSB hold time	t_{CH}	0	ns
Output floating time	t_{HZ}	$3.54 + 1.90 \times 10^{-2} \times B + 1.21 \times 10^{-7} \times W$	ns
Output active time	t_{LZ}	$1.36 + 1.14 \times 10^{-2} \times B$	ns
DC output delay time	t_{DC}	$3.47 + 1.75 \times 10^{-2} \times B + 3.08 \times 10^{-7} \times W - 1.10 \times 10^{-8} \times B \times W + 2.64 \times C_L$	ns

(2) V_{DD} = 2.0 ± 0.2 V

In case of 32 to 2048 words (T_A = –40 to +85°C)

Parameter	Symbol	Expression	Unit
Cycle time	t_{RC}	Where $t_{ACC} > t_{BEH} + t_{PC}$: t_{ACC} Where $t_{ACC} < t_{BEH} + t_{PC}$: $t_{BEH} + t_{PC}$	ns
Access time	t_{ACC}	$15.12 + 1.17 \times 10^{-1} \times B + 2.71 \times 10^{-3} \times W + 1.13 \times 10^{-5} \times B \times W + 1.39 \times C_L$	ns
Output hold time	t_{OH}	$2.13 + 6.65 \times 10^{-3} \times B + 7.79 \times 10^{-6} \times W – 1.62 \times 10^{-7} \times B \times W$	ns
BE high-level time	t_{BEH}	$11.52 + 1.17 \times 10^{-1} \times B + 2.58 \times 10^{-3} \times W + 1.51 \times 10^{-5} \times B \times W$	ns
Precharge time	t_{PC}	$3.01 + 7.87 \times 10^{-3} \times B + 4.44 \times 10^{-3} \times W + 6.23 \times 10^{-6} \times B \times W$	ns
Address setup time	t_{AS}	$5.55 + 1.80 \times 10^{-2} \times B – 2.48 \times 10^{-5} \times W – 9.48 \times 10^{-6} \times B \times W$	ns
Address hold time	t_{AH}	0	ns
Write data setup time	t_{DIS}	$5.64 – 1.33 \times 10^{-2} \times B – 7.34 \times 10^{-5} \times W + 2.81 \times 10^{-6} \times B \times W$	ns
Write data hold time	t_{DIH}	0	ns
Write data through time	t_{DTH}	$9.66 + 2.79 \times 10^{-2} \times B + 4.27 \times 10^{-5} \times W – 8.25 \times 10^{-7} \times B \times W + 1.39 \times C_L$	ns
WEB setup time	t_{WS}	$3.42 – 6.15 \times 10^{-3} \times B – 7.24 \times 10^{-5} \times W + 2.77 \times 10^{-6} \times B \times W$	ns
WEB hold time	t_{WH}	0	ns
CSB setup time	t_{CS}	$3.66 – 1.13 \times 10^{-3} \times B + 2.54 \times 10^{-6} \times W – 4.20 \times 10^{-7} \times B \times W$	ns
CSB hold time	t_{CH}	0	ns
Output floating time	t_{HZ}	$6.11 + 3.06 \times 10^{-2} \times B – 1.22 \times 10^{-6} \times W + 4.40 \times 10^{-8} \times B \times W$	ns
Output active time	t_{LZ}	$2.70 + 2.21 \times 10^{-2} \times B$	ns
DC output delay time	t_{DC}	$5.96 + 3.20 \times 10^{-2} \times B – 1.43 \times 10^{-5} \times W + 4.73 \times 10^{-7} \times B \times W + 4.58 \times C_L$	ns

In case of 2080 to 4096 words (T_A = –40 to +85°C)

Parameter	Symbol	Expression	Unit
Cycle time	t_{RC}	Where $t_{ACC} > t_{BEH} + t_{PC}$: t_{ACC} Where $t_{ACC} < t_{BEH} + t_{PC}$: $t_{BEH} + t_{PC}$	ns
Access time	t_{ACC}	$21.30 + 1.22 \times 10^{-1} \times B + 1.30 \times 10^{-3} \times W + 1.57 \times 10^{-6} \times B \times W + 1.39 \times C_L$	ns
Output hold time	t_{OH}	$2.05 - 8.46 \times 10^{-3} \times B - 6.93 \times 10^{-7} \times W + 4.50 \times 10^{-8} \times B \times W$	ns
BE high-level time	t_{BEH}	$17.18 + 9.61 \times 10^{-2} \times B + 1.30 \times 10^{-3} \times W + 1.70 \times 10^{-6} \times B \times W$	ns
Precharge time	t_{PC}	$1.84 + 2.09 \times 10^{-2} \times B + 2.45 \times 10^{-3} \times W + 2.31 \times 10^{-7} \times B \times W$	ns
Address setup time	t_{AS}	$5.73 + 6.94 \times 10^{-4} \times B + 1.38 \times 10^{-4} \times W - 6.70 \times 10^{-7} \times B \times W$	ns
Address hold time	t_{AH}	0	ns
Write data setup time	t_{DIS}	$6.12 - 1.42 \times 10^{-2} \times B + 6.18 \times 10^{-6} \times W - 1.80 \times 10^{-7} \times B \times W$	ns
Write data hold time	t_{DIH}	0	ns
Write data through time	t_{DTH}	$13.12 + 6.13 \times 10^{-2} \times B + 6.09 \times 10^{-5} \times W - 2.06 \times 10^{-6} \times B \times W + 1.39 \times C_L$	ns
WEB setup time	t_{WS}	$3.43 - 3.46 \times 10^{-4} \times B + 1.98 \times 10^{-5} \times W + 4.90 \times 10^{-7} \times B \times W$	ns
WEB hold time	t_{WH}	0	ns
CSB setup time	t_{CS}	$3.89 + 5.65 \times 10^{-3} \times B + 1.79 \times 10^{-5} \times W - 3.20 \times 10^{-7} \times B \times W$	ns
CSB hold time	t_{CH}	0	ns
Output floating time	t_{HZ}	$7.64 + 2.46 \times 10^{-2} \times B + 3.07 \times 10^{-6} \times W - 5.83 \times 10^{-7} \times B \times W$	ns
Output active time	t_{LZ}	$2.79 + 2.12 \times 10^{-2} \times B + 3.60 \times 10^{-8} \times W$	ns
DC output delay time	t_{DC}	$10.25 + 3.19 \times 10^{-2} \times B + 4.00 \times 10^{-5} \times W - 7.26 \times 10^{-7} \times B \times W + 4.58 \times C_L$	ns

In case of 4160 to 8192 words (T_A = –40 to +85°C)

Parameter	Symbol	Expression	Unit
Cycle time	t_{RC}	Where $t_{ACC} > t_{BEH} + t_{PC}$: t_{ACC} Where $t_{ACC} < t_{BEH} + t_{PC}$: $t_{BEH} + t_{PC}$	ns
Access time	t_{ACC}	$22.56 + 2.19 \times 10^{-1} \times B + 5.53 \times 10^{-4} \times W - 2.07 \times 10^{-6} \times B \times W + 1.39 \times C_L$	ns
Output hold time	t_{OH}	$1.61 + 7.26 \times 10^{-4} \times B - 2.17 \times 10^{-6} \times W + 5.31 \times 10^{-7} \times B \times W$	ns
BE high-level time	t_{BEH}	$19.33 + 1.48 \times 10^{-1} \times B + 5.59 \times 10^{-4} \times W - 2.48 \times 10^{-6} \times B \times W$	ns
Precharge time	t_{PC}	$2.33 + 1.54 \times 10^{-2} \times B + 1.20 \times 10^{-3} \times W - 2.31 \times 10^{-7} \times B \times W$	ns
Address setup time	t_{AS}	$5.31 + 3.30 \times 10^{-2} \times B + 8.47 \times 10^{-5} \times W - 3.83 \times 10^{-6} \times B \times W$	ns
Address hold time	t_{AH}	0	ns
Write data setup time	t_{DIS}	$5.67 - 4.48 \times 10^{-2} \times B + 4.00 \times 10^{-7} \times W + 6.00 \times 10^{-8} \times B \times W$	ns
Write data hold time	t_{DIH}	0	ns
Write data through time	t_{DTH}	$13.93 + 8.34 \times 10^{-2} \times B - 1.01 \times 10^{-5} \times W + 9.90 \times 10^{-7} \times B \times W + 1.39 \times C_L$	ns
WEB setup time	t_{WS}	$2.76 + 8.59 \times 10^{-5} \times B + 1.54 \times 10^{-6} \times W - 6.00 \times 10^{-8} \times B \times W$	ns
WEB hold time	t_{WH}	0	ns
CSB setup time	t_{CS}	$3.74 + 4.10 \times 10^{-3} \times B + 2.03 \times 10^{-6} \times W - 8.00 \times 10^{-8} \times B \times W$	ns
CSB hold time	t_{CH}	0	ns
Output floating time	t_{HZ}	$7.50 + 3.81 \times 10^{-2} \times B$	ns
Output active time	t_{LZ}	$2.81 + 2.52 \times 10^{-2} \times B$	ns
DC output delay time	t_{DC}	$7.35 + 3.95 \times 10^{-2} \times B + 4.58 \times C_L$	ns

4.7.2 Typical value (8 bits × 512 words)

(1) V_{DD} = 3.3 ± 0.3 V

Read/write operation (T_A = –40 to +85°C)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Cycle time	t_{RC}	9.14			ns
Access time	t_{ACC}			8.06	ns
Output hold time	t_{OH}	1.21			ns
BE high-level time	t_{BEH}	6.10			ns
Precharge time	t_{PC}	3.04			ns
Address setup time	t_{AS}	2.58			ns
Address hold time	t_{AH}	0			ns
Write data setup time	t_{DIS}	2.47			ns
Write data hold time	t_{DIH}	0			ns
Write data through time	t_{DTH}			4.61	ns
WEB setup time	t_{WS}	1.53			ns
WEB hold time	t_{WH}	0			ns
CSB setup time	t_{CS}	1.78			ns
CSB hold time	t_{CH}	0			ns
CSB, OEB control					
Output floating time	t_{HZ}	3.05			ns
Output active time	t_{LZ}	1.36			ns
DC output delay time	t_{DC}			3.50	ns

Remarks 1. The above data are calculated with an external load capacitance C_L of 0.2 pF.
2. The meanings of the symbols in the above table are as follows:
MIN. : minimum value necessary for operating macro under worst condition
MAX. : delay time of macro output under worst condition

(2) V_{DD} = 2.0 ± 0.2 V

Read/write operation (T_A = –40 to +85°C)

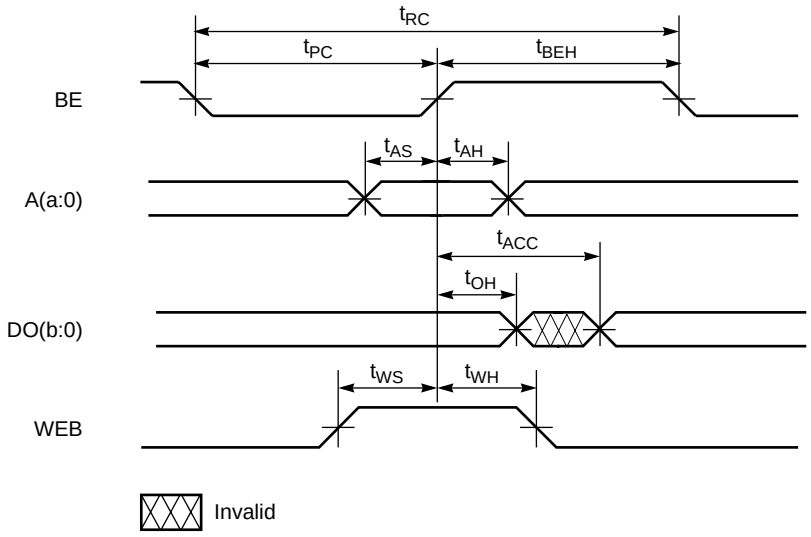
Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Cycle time	t_{RC}	19.22			ns
Access time	t_{ACC}			17.77	ns
Output hold time	t_{OH}	2.18			ns
BE high-level time	t_{BEH}	13.84			ns
Precharge time	t_{PC}	5.38			ns
Address setup time	t_{AS}	5.65			ns
Address hold time	t_{AH}	0			ns
Write data setup time	t_{DIS}	5.51			ns
Write data hold time	t_{DIH}	0			ns
Write data through time	t_{DTH}			10.18	ns
WEB setup time	t_{WS}	3.35			ns
WEB hold time	t_{WH}	0			ns
CSB setup time	t_{CS}	3.65			ns
CSB hold time	t_{CH}	0			ns
CSB, OEB control					
Output floating time	t_{HZ}	6.36			ns
Output active time	t_{LZ}	2.88			ns
DC output delay time	t_{DC}			7.14	ns

Remarks 1. The above data are calculated with an external load capacitance C_L of 0.2 pF.
2. The meanings of the symbols in the above table are as follows:
MIN.: minimum value necessary for operating macro under worst condition
MAX.: delay time of macro output under worst condition

4.8 Timing Chart

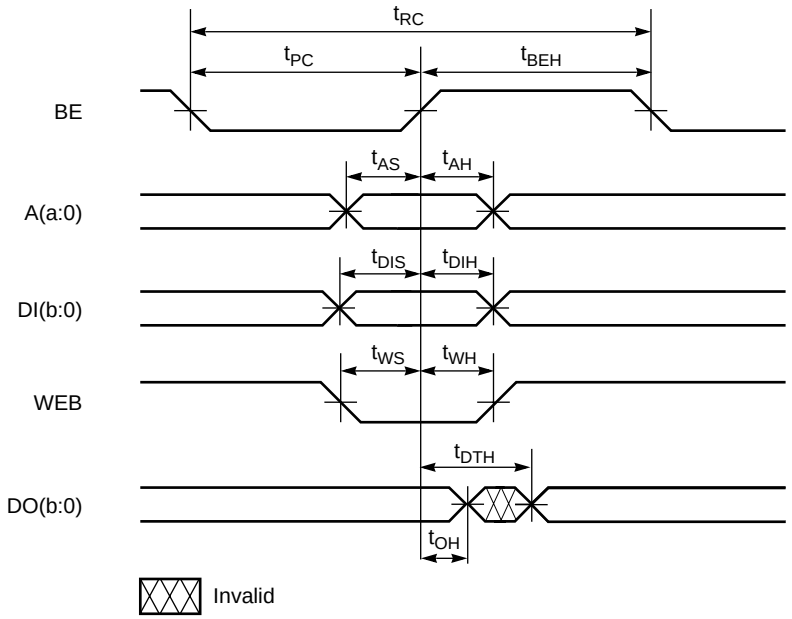
Read operation

Read cycle (CSB = low level, OEB = low level)



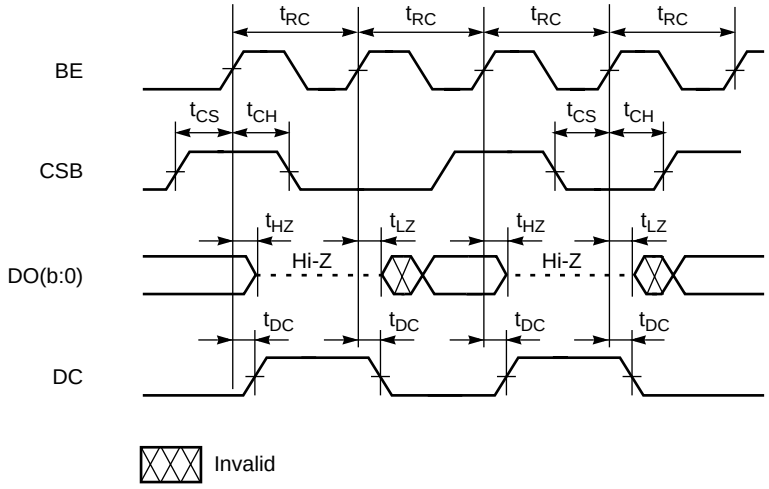
Write operation

Write cycle (CSB = low level, OEB = low level)

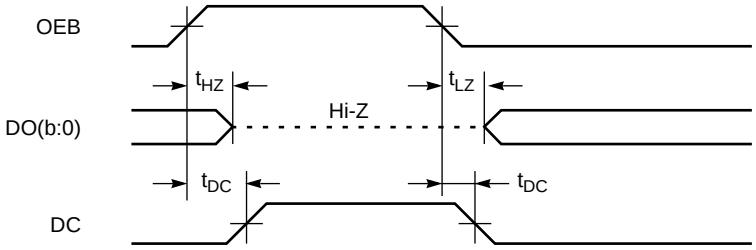


Read/write operation

(1) CSB control (OEB = low level)



(2) OEB control (CSB = low level)



4.9 Notes on Correct Use

(1) If spike is input to the clock input pin while CSB = L, the data of the RAM may be destroyed. In this case, the addresses other than that when the spike is input may be also destroyed.

(2) DO (b:0) is undefined during the period from power application to the rising edge of BE. Consequently bus fight may occur when these data outputs converge on a bus line.

(3) With the high-density single-port RAM (synchronous type), DO(b:0) and DC vary depending on the rising edge of BE if CSB is changed.
Refer to **4.8 (1) CSB control (OEB = low level)** for details.

★ (4) Current may continue to flow if the clock is stopped at a high level when power is applied, so be sure to either stop the clock while the clock pin is low, or input the clock first low then high (or high → low → high). If the clock is input at a low level even once, current will not flow no matter how the clock is subsequently stopped.

CHAPTER 5 HIGH-DENSITY DUAL-PORT (1R + 1W) RAM (SYNCHRONOUS TYPE)

5.1 General

- Dual-port RAM with read port + write port
- High-density integration
- Flexible memory size
  → High efficiency macro location by memory compiler.
  Block name: WBVxxxxx
  Bit width: 1 to 32 bits (variable in 1-bit units)
  Number of words: 32 to 1K words (variable in 8-word units)
- Operating voltage: 3.3 ± 0.3 V, 2.0 ± 0.2 V
- Operating ambient temperature: –40 to +85°C
- Storage temperature: –65 to +150°C
- 0.35 μm CMOS technology

5.1.1 Compiled range

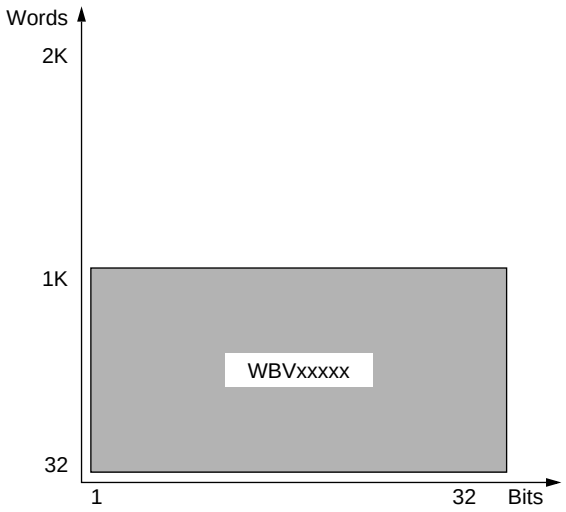
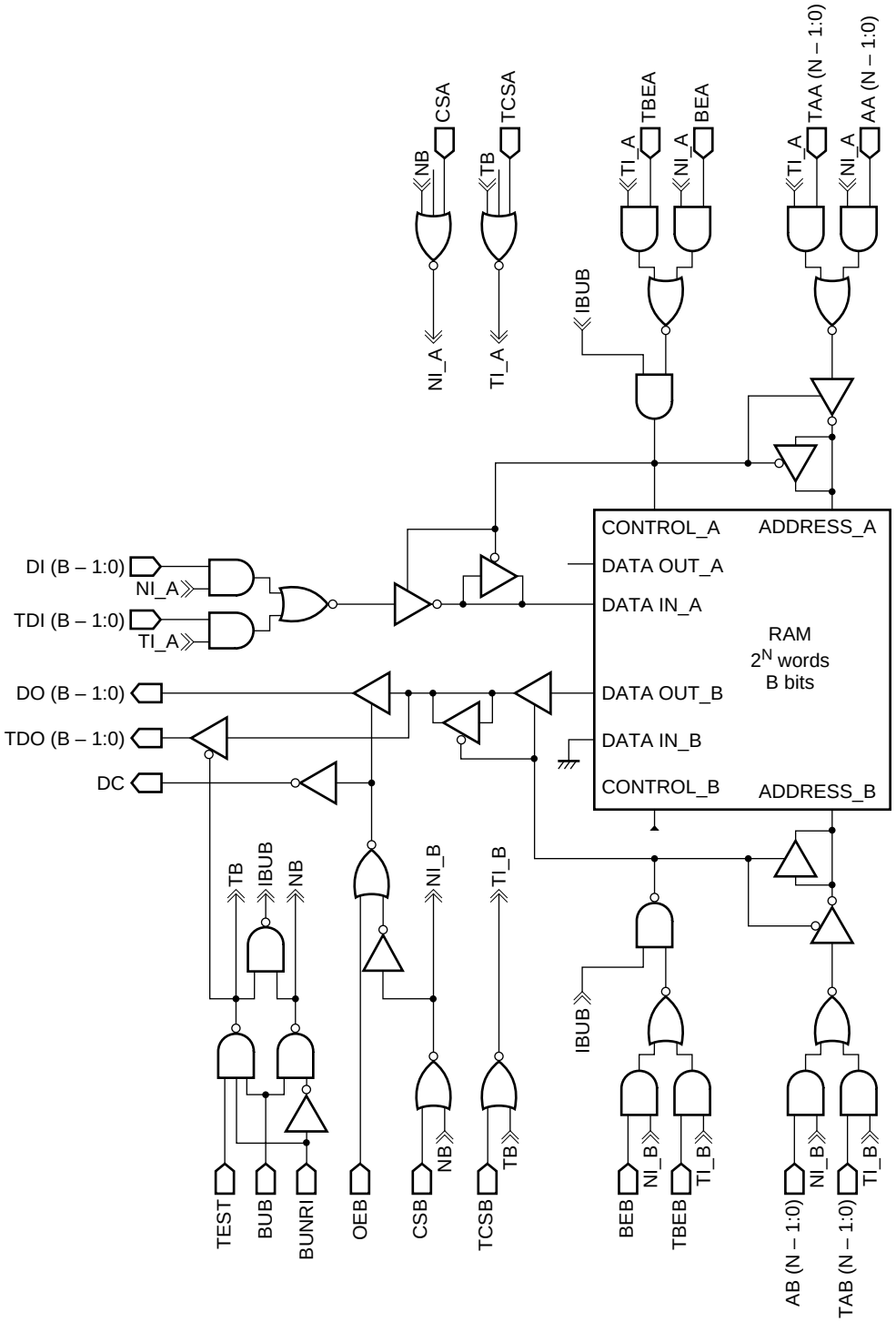


Figure 5-1 Compiled Range of High-Density Dual-Port (1R + 1W) RAM (Synchronous Type)

Table 5-1 Compiled Range of High-Density Dual-Port (1R + 1W) RAM (Synchronous Type)

Block Name	Minimum Size	Maximum Size	Step
WBVxxxxx	32 words × 1 bit	1K words × 32 bits	8 words/1 bit

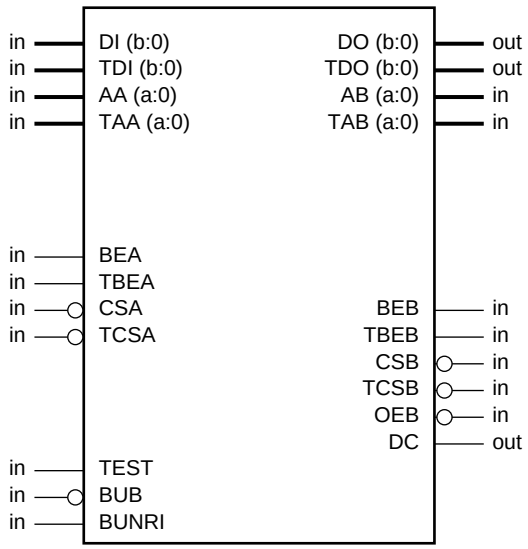
5.1.2 Equivalent circuit



Remark N: number of address lines, B: number of bits

Figure 5-2 Internal Equivalent Circuit

5.1.3 Symbol diagram



Remarks 1. A pin prefixed with "T" is a test pin.
2. "a" = (number of address lines) – 1, where $4 \leq a \leq 9$.
"b" = (number of bits) – 1, where $0 \leq b \leq 31$.

5.1.4 Pin capacitance

Pin Information GateDRC uses C_{IN} and C_{MAX} for fanin/fanout calculation.
Wiring capacitance = temporary wiring length × 0.18 (pF/mm)

Input		Output		
Pin Name/Symbol	**CIN (pF)**	**Pin Name/Symbol**	**CIN (pF)**	**CMAX (pF)**
DI(b:0)	0.026	DO(b:0)	0.087	6.00
TDI(b:0)	0.026	TDO(b:0)	0.087	6.00
AA(a:0)	0.026	DC	–	1.50
TAA(a:0)	0.026			
BEA	0.026			
TBEA	0.026			
CSA	0.020			
TCSA	0.020			
AB(a:0)	0.026			
TAB(a:0)	0.026			
BEB	0.026			
TBEB	0.026			
CSB	0.026			
TCSB	0.026			
OEB	0.020			
TEST	0.026			
BUB	0.039			
BUNRI	0.026			

Remark "a" = (number of address lines) – 1, where $4 \leq a \leq 9$
"b" = (number of bits) – 1, where $0 \leq b \leq 31$

5.2 Pin Function List

Pin Name/ Signal Name	Attribute	Mode	Port	Function
DI(b:0)	I	Normal	W	Data input b = number of bits – 1
DO(b:0)	OZ	Normal	R	Data output b = number of bits – 1
AA(a:0)	I	Normal	W	Address input a = number of address lines – 1 (determined by number of words)**Note**
BEA	I	Normal	W	Clock input
CSA	I	Normal	W	Chip select input
TDI(b:0)	I	Normal	W	Data input b = number of bits – 1
TDO(b:0)	OZ	Normal	R	Data output b = number of bits – 1
TAA(a:0)	I	Test	W	Address input a = number of address lines – 1 (determined by number of words)**Note**
TBEA	I	Test	W	Clock input
TCSA	I	Test	W	Chip select input
DC	O	Normal	R	Data control output DC = 0: DO(b:0) = 0, 1, undefined DC = 1: DO(b:0) = high impedance
AB(a:0)	I	Normal	R	Address input a = number of address lines – 1 (determined by number of words)**Note**
BEB	I	Normal	R	Clock input
CSB	I	Normal	R	Chip select input
OEB	I	Normal	R	Data output enable
TAB(a:0)	I	Test	R	Address input a = number of address lines – 1 (determined by number of words)**Note**
TBEB	I	Test	R	Clock input
TCSB	I	Test	R	Chip select input
BUNRI	I	Mode selection	–	Separation test input BUNRI = 0: Normal mode BUNRI = 1: Test mode
TEST	I	Mode selection	–	Test mode input BUNRI = 1, TEST = 0 Separated from test bus (tests other macros) BUNRI = 1, TEST = 1 Selected as subject to test
BUB	I	Mode selection	–	Backup mode input BUB = 0: Backup mode BUB = 1: Normal mode, test mode

Note Number of address lines = $\log_2$ (number of words) (rounded up at decimal place)

Remark The meanings of the symbols in the Attribute column are as follows:
I: input pin, OZ: 3-state output pin, O: output pin
The meanings of the symbols in the Port column are as follows:
W : write port, R: read port

5.3 Operation Truth Table

The operation timing between a read/write port and a read port is partially restricted. For details, refer to **5.8.2 Operation timing restrictions between read port and write port**.

The meanings of the symbols in the following operation truth tables are as follows:

Hi-Z : High impedance
X : Undefined state not including high impedance
XZ : Undefined state including high impedance
AAx, ABx : Any data
DIx : Input data
[ABx] : Data in memory

BUB	BUNRI	TEST	Mode	Normal Pin Status			Test Pin Status	
				Input	Output	DC	Input	Output
0	XZ	XZ	Backup	XZ	Hi-Z	1	XZ	Hi-Z
1	0	X	Normal	Valid	Valid	Valid	XZ	Hi-Z
1	1	0	Test (non-select)	XZ	Hi-Z	1	XZ	Hi-Z
1	1	1	Test (select)	XZ	Hi-Z	1	Valid	Valid

Normal mode access

Write port

CSA	BEA	AA(a:0)	DI(b:0)	Operation
0	↑	AAx	DIx	Write
0	0	X	X	Precharge
1	X	X	X	Macro off

Read port

CSB	BEB	OEB	AB(a:0)	DO(b:0)	DC	Operation
0	↑	0	ABx	[ABx]	0	Read
0	0	0	X	Hold	0	Precharge
0	X	1	X	Hi-Z	1	Output off
1	X	X	X	Hi-Z	1	Macro off

Test mode access

Write port

TCSA	TBEA	TAA(a:0)	TDI (b:0)	Operation
0	↗	AAx	DIx	Write
0	0	X	X	Precharge
1	X	X	X	Macro off

Read port

TCSB	TBEB	TAB(a:0)	TDO(b:0)	Operation
0	↗	ABx	DIx	Read
0	0	X	Hold	Precharge
1	X	X	Hold	Macro off

5.4 Macro Size

Use the following expressions to calculate the macro size.

Macro size = X × Y (grids)

W : number of words
B : number of bits
N : number of address lines (N = $\log_2$W (rounded up at decimal place))
α : Macro circumferential wiring area in X direction (73.53)
β : Macro circumferential wiring area in Y direction (7.353)

X = 50.36 × B + 11.71 × N + 160.61 + α (grids)
Y = 8.089 × 10^{-2} × W + 23.56 + β (grids)

Remarks 1. Round up the fraction below the decimal place.
2. Not necessary to add α and β when not taking the macro circumferential wiring area into consideration.

5.5 Electrical Characteristics

Absolute maximum ratings

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	–0.5 to +4.6	V
Operating ambient temperature	T_A	–40 to +85	°C
Storage temperature	T_{stg}	–65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended operating range (V_{DD} = 3.3 ± 0.3 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}	3.0	3.3	3.6	V
Operating ambient temperature	T_A	–40		+85	°C

Recommended operating range (V_{DD} = 2.0 ± 0.2 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}	1.8	2.0	2.2	V
Operating ambient temperature	T_A	–40		+85	°C

5.6 Operating Current Consumption

The operating current consumption (I_{DD}) changes depending on the number of bits, number of words, number of address lines, and operating frequency of the memory. The value of the operating current consumption can be calculated by the following expression.

I_{DD} (TYP.) = I_{DDR} (TYP.) + I_{DDW} (TYP.)
I_{DD} (MAX.) = I_{DDR} (MAX.) + I_{DDW} (MAX.)

I_{DDR} and I_{DDW} in the above expression can be worked out by the expressions in the table below.

The meanings of the symbols in the tables below are as follows:
B: number of bits, W: number of words, N: number of address lines (N = $\log_2$W (rounded up at decimal place)),
f_R: read operating frequency (MHz), f_W: write operating frequency (MHz), C_L: external load capacitance (pF),
A: operation rate [Note 1] (100% = 1)
DFa: MAX. data rate (MHz) of AA (a:0) or DI (b:0) pin
DFb: MAX. data rate (MHz) of AB (a:0) pin

(1) V_{DD} = 3.3V ± 0.3 V

TYP.
During read/write operation ($\alpha = 1.65 \times B \times C_L$)

Port	Condition	Expression	Unit
Read (I_{DDR})	W = 32	$\{(0.36 \times N + 6.6 \times B - 0.12) \times 10^{-3} \times W + 0.0254 \times B^2 + 0.737 \times N + 4.95 \times B + 4.97 + \alpha\} \times f_R$	μA
	W > 32	$\{(0.36 \times N + 6.6 \times B - 0.12) \times 10^{-3} \times W + 0.0254 \times B^2 + 0.737 \times N + 4.95 \times B + 5.42 + \alpha\} \times f_R$	μA
Write (I_{DDW})	W = 32	$\{(0.36 \times N + 2.16 \times B + 0.12) \times 10^{-3} \times W + 0.0229 \times B^2 + 0.725 \times N + 1.96 \times B + 4.88\} \times f_W$	μA
	W > 32	$\{(0.36 \times N + 2.16 \times B + 0.12) \times 10^{-3} \times W + 0.0229 \times B^2 + 0.725 \times N + 1.96 \times B + 5.34\} \times f_W$	μA

MAX.
During read/write operation ($\alpha = 1.8 \times B \times C_L$)

Port	Condition	Expression	Unit
Read (I_{DDR})	W = 32	$\{(0.6 \times N + 7.32 \times B - 0.48) \times 10^{-3} \times W + 0.0362 \times B^2 + 0.797 \times N + 6.18 \times B + 5.97 + \alpha\} \times f_R \times A$	μA
	W > 32	$\{(0.6 \times N + 7.32 \times B - 0.48) \times 10^{-3} \times W + 0.0362 \times B^2 + 0.797 \times N + 6.18 \times B + 6.48 + \alpha\} \times f_R \times A$	μA
Write (I_{DDW})	W = 32	$\{(0.36 \times N + 2.40 \times B + 0.36) \times 10^{-3} \times W + 0.0365 \times B^2 + 0.928 \times N + 2.27 \times B + 5.78\} \times f_W \times A$	μA
	W > 32	$\{(0.36 \times N + 2.40 \times B + 0.36) \times 10^{-3} \times W + 0.0365 \times B^2 + 0.928 \times N + 2.27 \times B + 6.33\} \times f_W \times A$	μA

In power-down mode[Note 2]

Condition	Port	Expression	Unit
TYP.	Read	$\{(0.72 \times N - 3.6) \times 10^{-3} \times W + 1.47 \times N + 0.120 \times B - 3.55\} \times DFb$	μA
	Write	$\{(0.72 \times N - 3.6) \times 10^{-3} \times W + 1.47 \times N + 0.556 \times B - 3.55\} \times DFa$	μA
MAX.	Read	$\{(0.72 \times N - 6.00) \times 10^{-3} \times W + 1.59 \times N + 0.131 \times B - 3.48\} \times DFb$	μA
	Write	$\{(0.72 \times N - 6.00) \times 10^{-3} \times W + 1.59 \times N + 0.662 \times B - 3.48\} \times DFa$	μA

(2) V_{DD} = 2.0 ± 0.2 V

TYP.
During read/write operation (α = 1.0 × B × C_L)

Port	Condition	Expression	Unit
Read (I_{DDR})	W = 32	$\{(0.2592 \times N + 3.92 \times B - 0.3744) \times 10^{-3} \times W - 3.136 \times 10^{-3} \times B^2 + 0.312 \times N + 2.512 \times B + 2.352 + \alpha\} \times f_R$	μA
	W > 32	$\{(0.2592 \times N + 3.92 \times B - 0.3456) \times 10^{-3} \times W - 3.136 \times 10^{-3} \times B^2 + 0.312 \times N + 2.512 \times B + 2.536 + \alpha\} \times f_R$	μA
Write (I_{DDW})	W = 32	$\{(0.216 \times N + 1.3 \times B + 0.036) \times 10^{-3} \times W + 1.44 \times 10^{-3} \times B^2 + 0.594 \times N + 1.10 \times B + 1.34\} \times f_W$	μA
	W > 32	$\{(0.216 \times N + 1.3 \times B + 0.144) \times 10^{-3} \times W + 1.44 \times 10^{-3} \times B^2 + 0.594 \times N + 1.10 \times B + 1.50\} \times f_W$	μA

MAX.
During read/write operation (α = 1.1 × B × C_L)

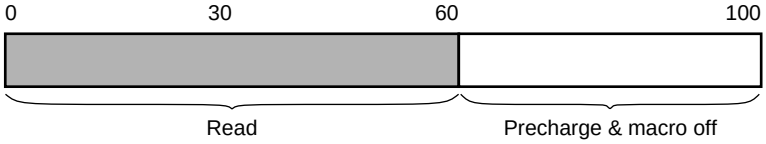
Port	Condition	Expression	Unit
Read (I_{DDR})	W = 32	$\{(0.324 \times N + 4.90 \times B - 0.468) \times 10^{-3} \times W - 0.00392 \times B^2 + 0.39 \times N + 3.14 \times B + 2.94 + \alpha\} \times f_R \times A$	μA
	W > 32	$\{(0.324 \times N + 4.90 \times B - 0.432) \times 10^{-3} \times W - 0.00392 \times B^2 + 0.39 \times N + 3.14 \times B + 3.17 + \alpha\} \times f_R \times A$	μA
Write (I_{DDW})	W = 32	$\{(0.216 \times N + 1.44 \times B + 0.0720) \times 10^{-3} \times W + 0.0032 \times B^2 + 0.439 \times N + 1.24 \times B + 2.69\} \times f_W \times A$	μA
	W > 32	$\{(0.216 \times N + 1.44 \times B + 0.216) \times 10^{-3} \times W + 0.0032 \times B^2 + 0.439 \times N + 1.24 \times B + 2.86\} \times f_W \times A$	μA

In power-down mode[Note 2]

Condition	Port	Expression	Unit
TYP.	Read	$\{(0.72 \times N - 3.6) \times 10^{-3} \times W + 0.613 \times N + 0.0683 \times B - 1.1\} \times DFb$	μA
	Write	$\{(0.72 \times N - 3.6) \times 10^{-3} \times W + 0.613 \times N + 0.308 \times B - 1.1\} \times DFa$	μA
MAX.	Read	$\{(0.324 \times N - 3.24) \times 10^{-3} \times W + 0.781 \times N + 0.0752 \times B - 1.56\} \times DFb$	μA
	Write	$\{(0.324 \times N - 3.24) \times 10^{-3} \times W + 0.781 \times N + 0.354 \times B - 1.56\} \times DFa$	μA

Notes 1. This operation rate is the ratio of the read and write operations to the total operation period (read, write, precharge, and macro off) of the RAM.

Example The operation rate is 60% (0.6) if read operations account for 60% of the total operation period of the read port.



2. Power-down mode indicates the precharge status or macro off status in **Normal mode access** in **5.3 Operation Truth Table**.

Remark If all the input signals of this RAM are fixed, the current consumption in the standby mode (I_{DD1}) = 0.

5.7 Timing

5.7.1 Expressions

The timing values can be calculated by the following expressions (rounded at the third place below the decimal place. However, the output hold time is truncated).

The meanings of the symbols in the table below are as follows:
W: number of words, B: number of bits, N: number of address lines ($N = \log_2 W$ (rounded up at decimal place)),
C_L: external load capacitance (pF)

(1) V_{DD} = 3.3 ± 0.3 V

Read/write operation (T_A = –40 to +85°C)

Parameter	Symbol	Expression	Unit
Cycle time	t_{RC}	Where $t_{BEH} > t_{PC}$: $t_{BEH} \times 2$ (clock duty: 50%) Where $t_{BEH} < t_{PC}$: $t_{PC} \times 2$ (clock duty: 50%)	ns
Access time	t_{ACC}	$4.74 + 3.71 \times 10^{-2} \times B + 4.62 \times 10^{-3} \times W + 2.00 \times 10^{-1} \times C_L$	ns
Output hold time	t_{OH}	$0.59 + 1.93 \times 10^{-2} \times B$	ns
BEA high-level time	t_{BEH_A}	$1.76 + 3.71 \times 10^{-2} \times B + 8.30 \times 10^{-4} \times W$	ns
BEB high-level time	t_{BEH_B}	$4.38 + 3.71 \times 10^{-2} \times B + 4.62 \times 10^{-3} \times W$	ns
Precharge time	t_{PC}	$4.38 + 3.71 \times 10^{-2} \times B + 4.62 \times 10^{-3} \times W$	ns
Address setup time	t_{AS}	(W = 32) 0.74 (W > 32) $1.48 + 4.30 \times 10^{-4} \times W$	ns
Address hold time	t_{AH}	$0.81 + 8.00 \times 10^{-3} \times N$	ns
Write data setup time	t_{DIS}	(B = 1) $0.05 – 3.00 \times 10^{-2} \times B$ (B > 1) 0	ns
Write data hold time	t_{DIH}	$1.18 + 2.96 \times 10^{-2} \times B$	ns
CSA, CSB setup time	t_{CS}	0.65	ns
CSA, CSB hold time	t_{CH}	0	ns
CSB control			
Output floating time	t_{HZ}	$1.53 + 1.89 \times 10^{-2} \times B$	ns
Output active time	t_{LZ}	$1.71 + 1.96 \times 10^{-2} \times B$	ns
DC output delay time	t_{DC}	$1.45 + 1.83 \times 10^{-2} \times B + 6.70 \times 10^{-1} \times C_L$	ns
OEB control			
Output floating time	t_{HZ}	$1.14 + 1.86 \times 10^{-2} \times B$	ns
Output active time	t_{LZ}	$1.30 + 2.00 \times 10^{-2} \times B$	ns
DC output delay time	t_{DC}	$1.05 + 1.88 \times 10^{-2} \times B + 6.70 \times 10^{-1} \times C_L$	ns

(2) V_{DD} = 2.0 ± 2.0 V

Read/write operation (T_A = –40 to +85°C)

Parameter	Symbol	Expression	Unit
Cycle time	t_{RC}	Where $t_{BEH} > t_{PC}$: $t_{BEH} \times 2$ (clock duty: 50%) Where $t_{BEH} < t_{PC}$: $t_{PC} \times 2$ (clock duty: 50%)	ns
Access time	t_{ACC}	$12.04 + 5.25 \times 10^{-2} \times B + 1.27 \times 10^{-2} \times W + 5.40 \times 10^{-1} \times C_L$	ns
Output hold time	t_{OH}	$1.00 + 2.43 \times 10^{-2} \times B$	ns
BEA high-level time	t_{BEH_A}	$4.36 + 6.14 \times 10^{-2} \times B + 1.25 \times 10^{-3} \times W$	ns
BEB high-level time	t_{BEH_B}	$11.17 + 5.25 \times 10^{-2} \times B + 1.27 \times 10^{-2} \times W$	ns
Precharge time	t_{PC}	$11.17 + 5.25 \times 10^{-2} \times B + 1.27 \times 10^{-2} \times W$	ns
Address setup time	t_{AS}	(W = 32) 1.96 (W > 32) $3.57 + 9.18 \times 10^{-4} \times W$	ns
Address hold time	t_{AH}	$1.85 + 1.00 \times 10^{-2} \times N$	ns
Write data setup time	t_{DIS}	(B ≤ 4) $0.24 – 4.96 \times 10^{-2} \times B$ (B > 4) 0	ns
Write data hold time	t_{DIH}	$2.62 + 5.00 \times 10^{-2} \times B$	ns
CSA, CSB setup time	t_{CS}	1.34	ns
CSA, CSB hold time	t_{CH}	0	ns
CSB control			
Output floating time	t_{HZ}	$3.11 + 3.21 \times 10^{-2} \times B$	ns
Output active time	t_{LZ}	$3.86 + 4.29 \times 10^{-2} \times B$	ns
DC output delay time	t_{DC}	$3.29 + 3.89 \times 10^{-2} \times B + 1.38 \times C_L$	ns
OEB control			
Output floating time	t_{HZ}	$2.31 + 3.14 \times 10^{-2} \times B$	ns
Output active time	t_{LZ}	$2.94 + 4.18 \times 10^{-2} \times B$	ns
DC output delay time	t_{DC}	$2.35 + 3.86 \times 10^{-2} \times B + 1.38 \times C_L$	ns

5.7.2 Typical value (8 bits × 512 words)

(1) V_{DD} = 3.3 ± 0.3 V

Read/write operation (T_A = –40 to +85°C)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Cycle time	t_{RC}	14.10			ns
Access time	t_{ACC}			7.45	ns
Output hold time	t_{OH}	0.75			ns
BEA high-level time	t_{BEH_A}	2.49			ns
BEB high-level time	t_{BEH_B}	7.05			ns
Precharge time	t_{PC}	7.05			ns
Address setup time	t_{AS}	1.71			ns
Address hold time	t_{AH}	0.89			ns
Write data setup time	t_{DIS}	0			ns
Write data hold time	t_{DIH}	1.42			ns
CSA, CSB setup time	t_{CS}	0.65			ns
CSA, CSB hold time	t_{CH}	0			ns
CSB control					
Output floating time	t_{HZ}	1.69			ns
Output active time	t_{LZ}	1.87			ns
DC output delay time	t_{DC}			1.74	ns
OEB control					
Output floating time	t_{HZ}	1.29			ns
Output active time	t_{LZ}	1.46			ns
DC output delay time	t_{DC}			1.34	ns

Remarks 1. The above values are calculated with an external load capacitance of 0.2 pF.

2. The meanings of the symbols in the above table are as follows:
MIN. : minimum value necessary for operating macro under worst condition
MAX. : delay time of macro output under worst condition

(2) V_{DD} = 2.0 ± 0.2 V

Read/write operation (T_A = –40 to +85°C)

Parameter		Symbol	MIN.	TYP.	MAX.	Unit
Cycle time		t_{RC}	36.20			ns
Access time		t_{ACC}			19.08	ns
Output hold time		t_{OH}	1.20			ns
BEA high-level time		t_{BEH_A}	5.50			ns
BEB high-level time		t_{BEH_B}	18.10			ns
Precharge time		t_{PC}	18.10			ns
Address setup time		t_{AS}	4.05			ns
Address hold time		t_{AH}	1.94			ns
Write data setup time		t_{DIS}	0			ns
Write data hold time		t_{DIH}	3.02			ns
CSA, CSB setup time		t_{CS}	1.34			ns
CSA, CSB hold time		t_{CH}	0			ns
CSB control						
	Output floating time	t_{HZ}	3.37			ns
	Output active time	t_{LZ}	4.21			ns
	DC output delay time	t_{DC}			3.88	ns
OEB control						
	Output floating time	t_{HZ}	2.57			ns
	Output active time	t_{LZ}	3.28			ns
	DC output delay time	t_{DC}			2.94	ns

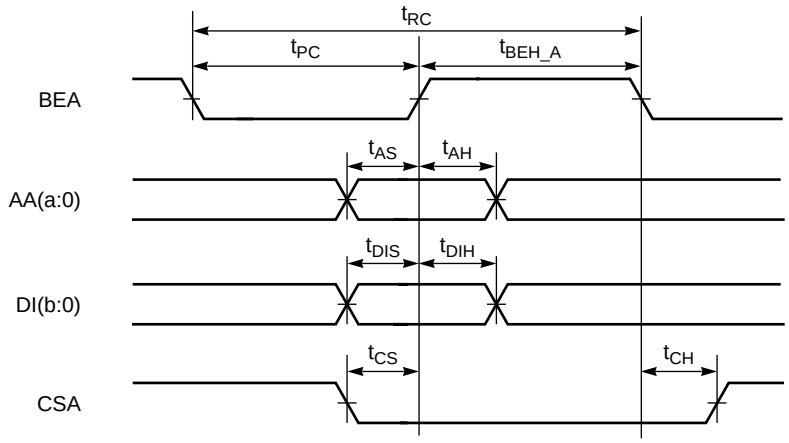
Remarks 1. The above values are calculated with an external load capacitance of 0.2 pF.

2. The meanings of the symbols in the above table are as follows:
MIN. : minimum value necessary for operating macro under worst condition
MAX. : delay time of macro output under worst condition

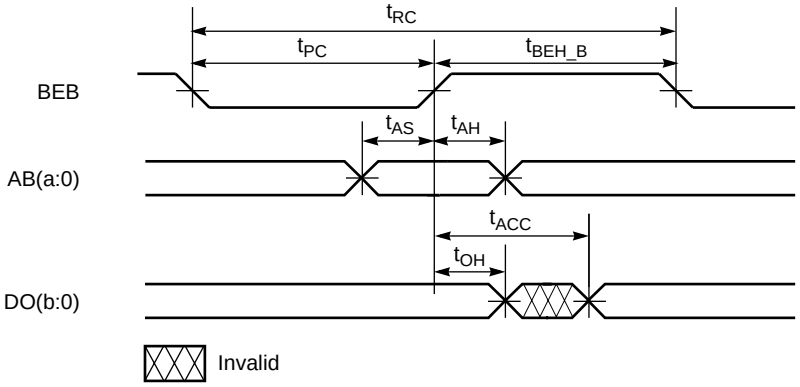
5.8 Timing Chart

5.8.1 Read port and write port

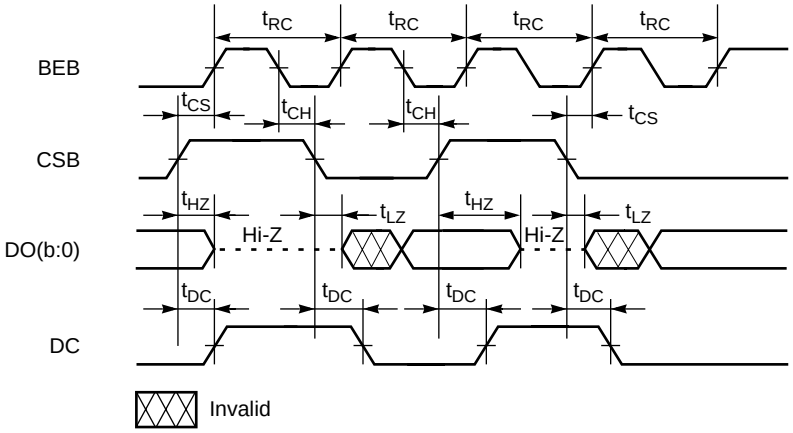
(1) Write operation
Write cycle (write port)



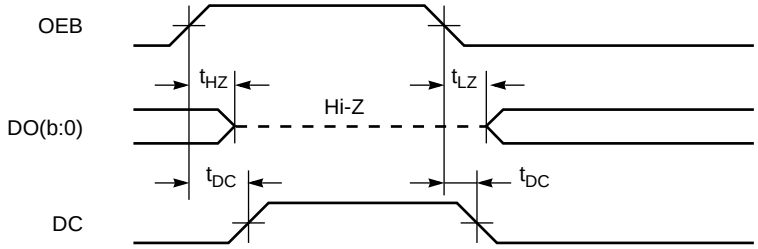
(2) Read operation
Read cycle (read port) (CSB = low level, OEB = low level)



(3) CSB control (OEB = low level)



(4) OEB control (CSB = low level)



5.8.2 Operation timing restrictions between read port and write port

(1) When read port and write port access different addresses

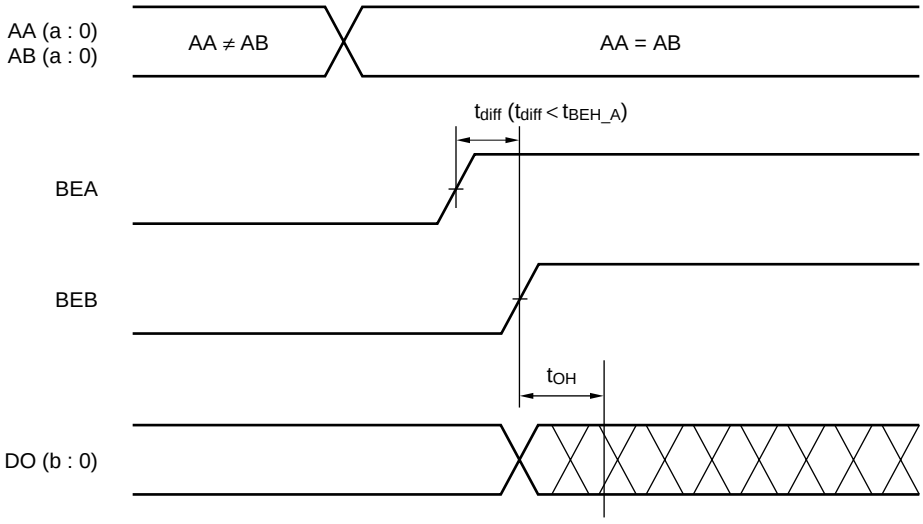
There is no operation timing restriction between the read port and write port.
For the operation of each port, refer to the operation timing of **5.8.1 Read port and write port**.

(2) When the read port and the write port access the same address

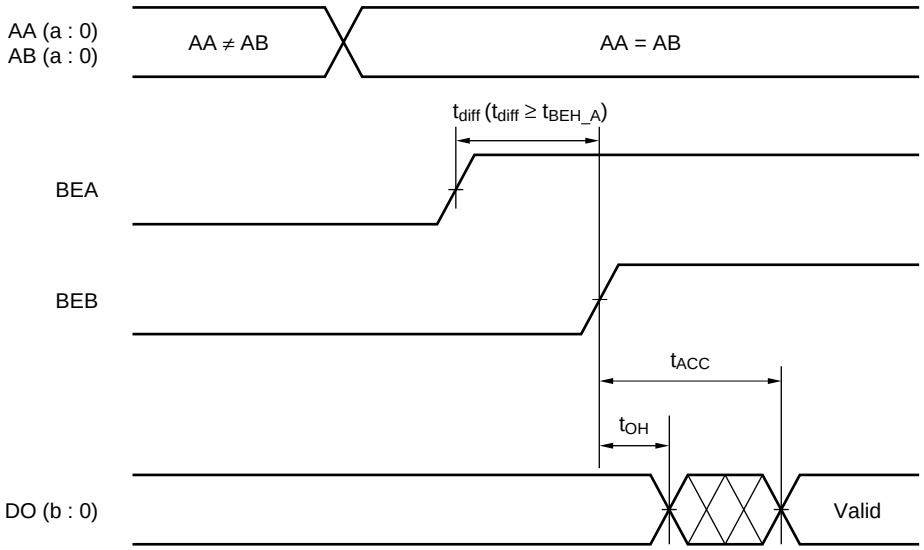
Write operation is performed normally. Read operation varies depending on the timings shown below.

(a) If BEA (write port clock) rises before BEB (read port clock)

- If $t_{diff} < t_{BEH\_A}$
  Output of the read port is undefined. t_{OH} is not guaranteed.

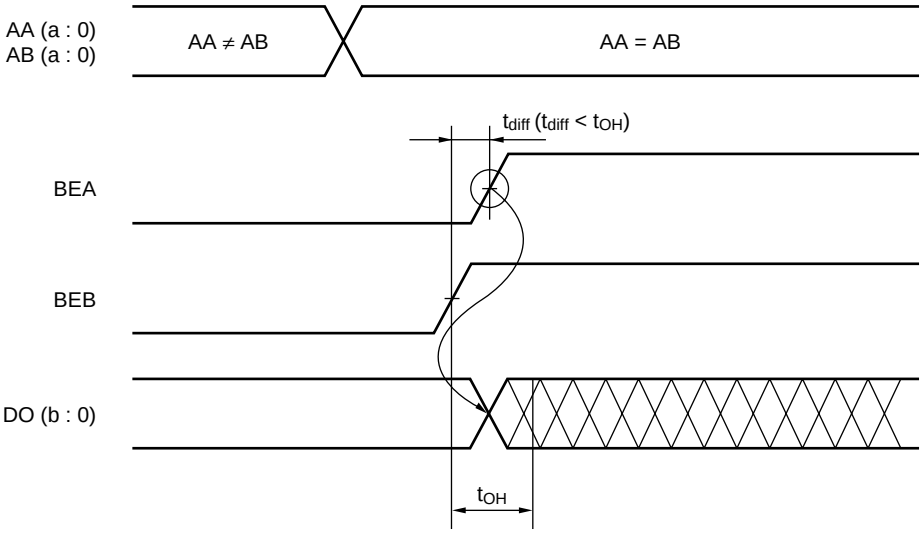


- If $t_{diff} \geq t_{BEH\_A}$
  Output of the read port is performed normally.

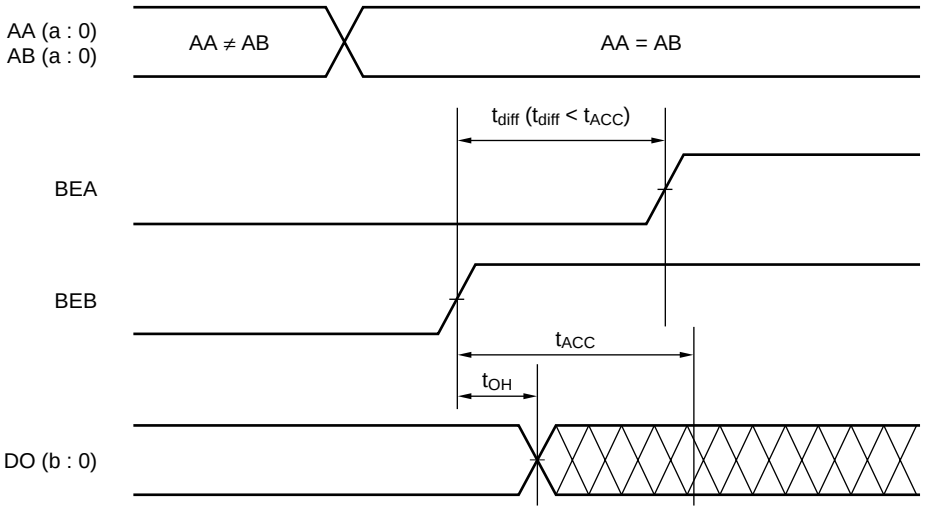


(b) If BEA (write port clock) rises after BEB (read port clock)

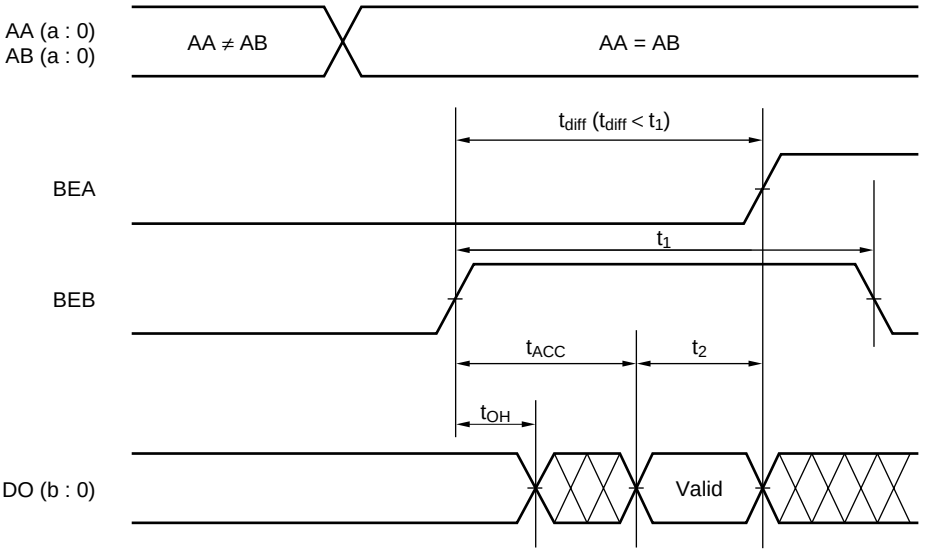
- If $t_{diff} < t_{OH}$
  Output of the read port is undefined. t_{OH} is not guaranteed.



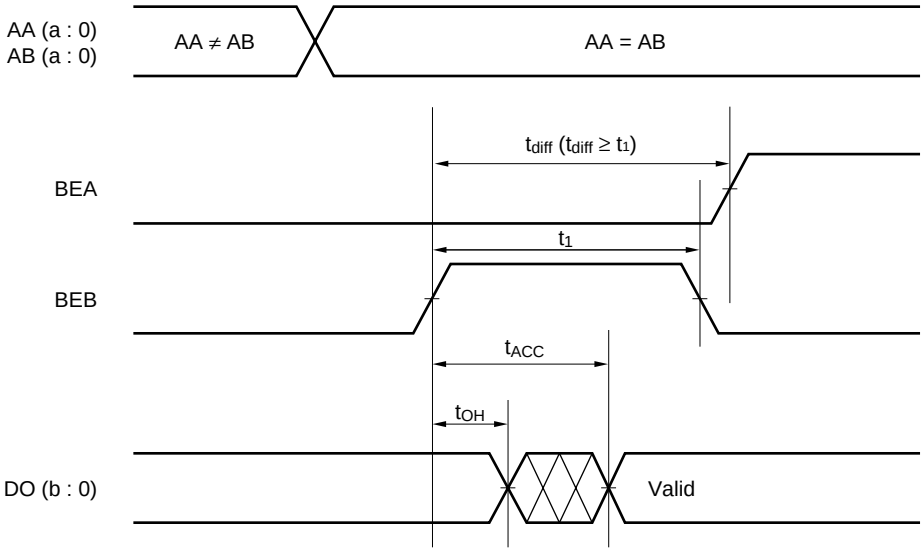
- If $t_{diff} < t_{ACC}$ and $t_{diff} \geq t_{OH}$
  Output of the read port is undefined. t_{OH} is guaranteed.



- If $t_{diff} < t_1$ and $t_{diff} \geq t_{ACC}$
  The read port outputs the previous write data during period t_2.
  The output becomes undefined when BEA rises.



- If $t_{diff} \geq t_1$ and $t_1 \geq t_{BEH\_B}$, and $t_{ACC} < t_{diff}$
  The read port correctly outputs the previous write data.



5.9 Notes on Correct Use

(1) If spike is input to the clock input pin while CSA, CSB = L, the data of the RAM may be destroyed. In this case, the addresses other than that when the spike is input may be also destroyed.

★ (2) Current may continue to flow if the clock is stopped at a high level when power is applied, so be sure to either stop the clock while the clock pin is low, or input the clock first low then high (or high → low → high). If the clock is input at a low level even once, current will not flow no matter how the clock is subsequently stopped.

CHAPTER 6 SUPER HIGH-SPEED SINGLE-PORT RAM (SYNCHRONOUS TYPE)

6.1 General

- Single-port SRAM (I/O separation type)
- Super high-speed operation
- Flexible memory size
  → High efficiency macro location by memory compiler.
  Block name: WHVxxxxx
  Bit width: 1 to 16 bits (variable in 1-bit units)
  Number of words: 64 to 1K words (variable in 64-word units)
- Operating voltage: 3.3 ± 0.3 V
- Operating temperature: –40 to +85°C
- Storage ambient temperature: –65 to +150°C
- 0.35 μm CMOS technology

6.1.1 Compiled range

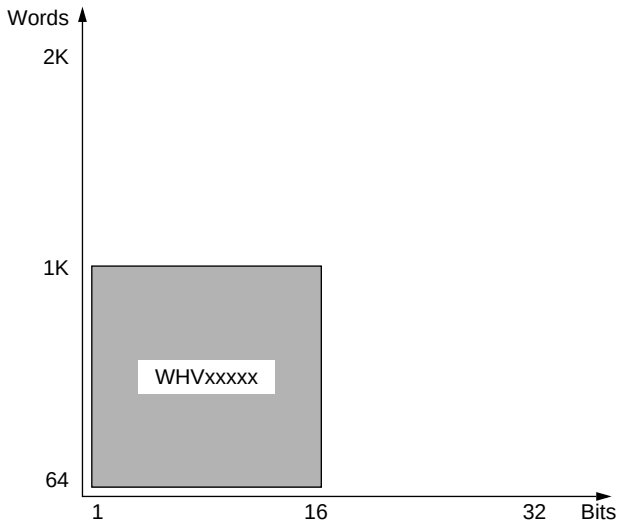
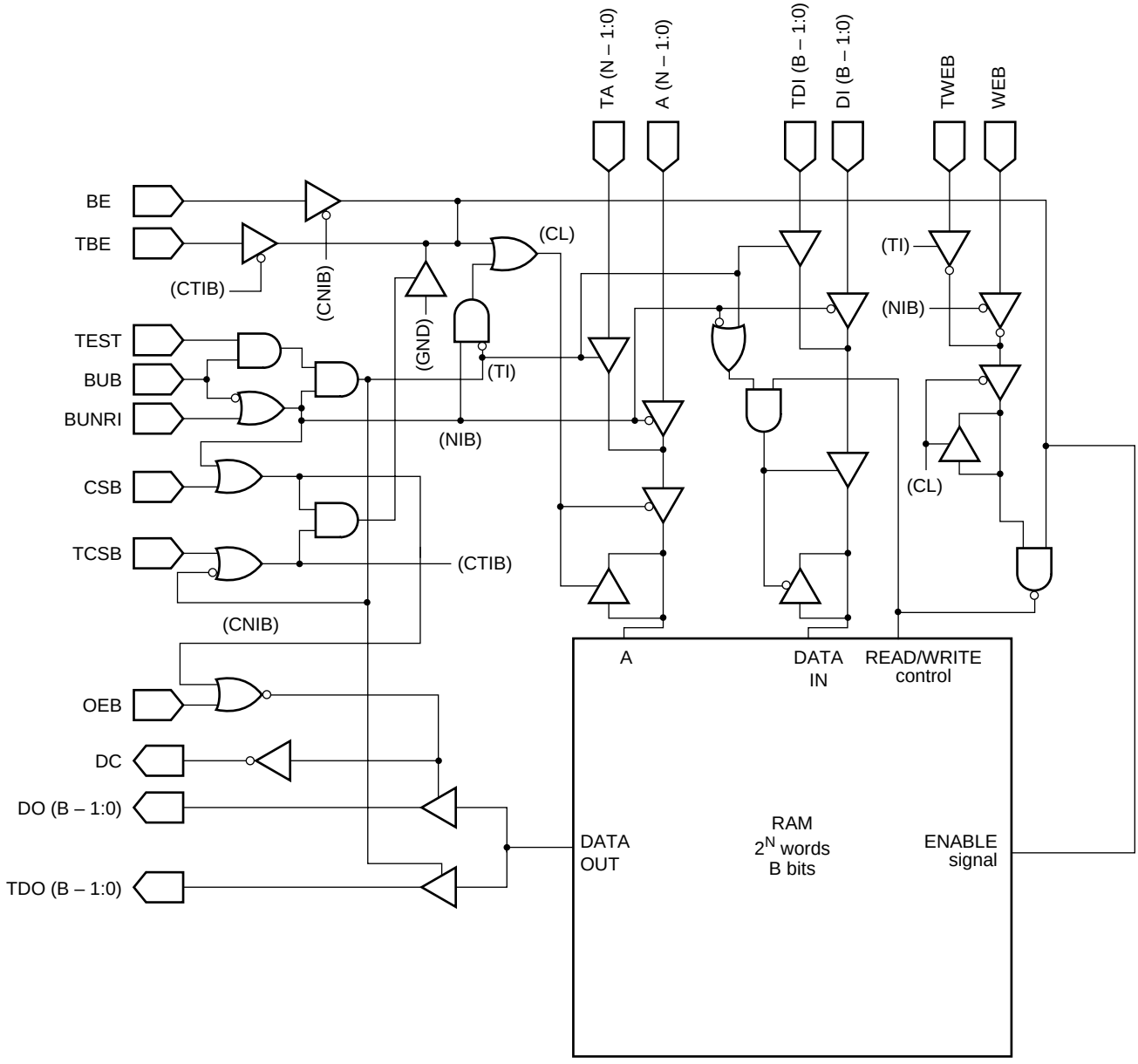


Figure 6-1 Compiled Range of Super High-Speed Single-Port RAM (Synchronous Type)

Table 6-1 Compiled Range of Super High-Speed Single-Port RAM (Synchronous Type)

Block Name	Minimum Size	Maximum Size	Step
WHVxxxxx	64 words × 1 bit	1K words × 16 bits	64 words/1 bit

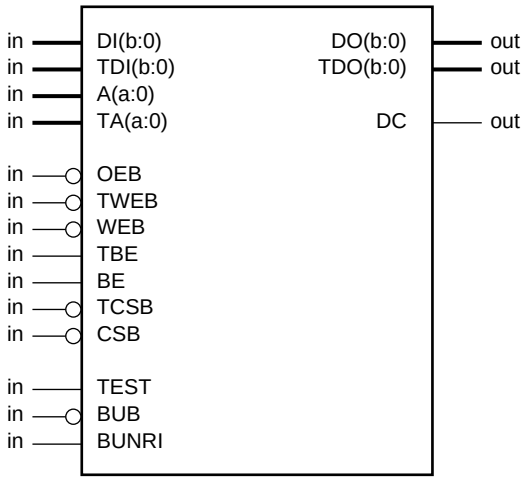
6.1.2 Equivalent circuit



Remark N: number of address lines, B: number of bits

Figure 6-2 Internal Equivalent Circuit

6.1.3 Symbol diagram



Remarks 1. A pin prefixed with “T” is a test pin.
2. “a” = (number of address lines) – 1, where $5 \leq a \leq 9$.
“b” = (number of bits) – 1, where $0 \leq b \leq 15$.

6.1.4 Pin capacitance

Pin Information GateDRC uses C_{IN} and C_{MAX} for fanin/fanout calculation.
Wiring capacitance = Temporary wiring length × 0.18 (pF/mm)

Input		Output		
Pin Name/Symbol	**CIN (pF)**	**Pin Name/Symbol**	**CIN (pF)**	**CMAX (pF)**
DI(b:0)	0.015	DO(b:0)	0.05	6.0
TDI(b:0)	0.015	TDO(b:0)	0.05	6.0
A(a:0)	0.025	DC	–	1.5
TA(a:0)	0.025			
BE	0.15			
TBE	0.15			
CSB	0.01			
TCSB	0.01			
WEB	0.015			
TWEB	0.015			
OEB	0.001			
TEST	0.001			
BUB	0.015			
BUNRI	0.01			

Remark “a” = (number of address lines) – 1, where $5 \leq a \leq 9$
“b” = (number of bits) – 1, where $0 \leq b \leq 15$

6.2 Pin Function List

Pin Name/Signal Name	Attribute	Mode	Function
DI(b:0)	I	Normal	Data input b = number of bits – 1
DO(b:0)	OZ	Normal	Data output b = number of bits – 1
A(a:0)	I	Normal	Address input a = number of address lines – 1 (determined by number of words)**Note**
BE	I	Normal	Clock input
CSB	I	Normal	Chip select input
WEB	I	Normal	Write enable input
OEB	I	Normal	Data output enable input
TDI(b:0)	I	Test	Data input b = number of bits – 1
TDO(b:0)	OZ	Test	Data output b = number of bits – 1
TA(a:0)	I	Test	Address input a = number of address lines – 1 (determined by number of words)**Note**
TBE	I	Test	Clock input
TCSB	I	Test	Chip select input
TWEB	I	Test	Write enable input
BUNRI	I	Mode selection	Separation test input (normal mode: low level, test mode: high level) BUNRI = 0: Normal mode BUNRI = 1: Test mode
TEST	I	Mode selection	Test mode input BUNRI = 1, TEST = 0 Separated from test bus (tests other macros) BUNRI = 1, TEST = 1 Selected as subject to test
BUB	I	Mode selection	Backup mode input BUB = 0: Backup mode BUB = 1: Normal mode, test mode
DC	O	Normal	Data control output DC = 0: DO(b:0) = 0, 1, undefined DC = 1: DO(b:0) = high impedance

Note Number of address lines = $\log_2$ (number of words) (rounded up at decimal place)

Remark The meanings of the symbols in the Attribute column are as follows:
I: input pin, OZ: 3-state output pin, O: output pin

6.3 Operation Truth Table

The meanings of the symbols in the following operation truth tables are as follows:

Hi-Z : High impedance
X : Undefined state not including high impedance
XZ : Undefined state including high impedance
Ax : Any data
DIx : Input data
[Ax] : Data in memory

BUB	BUNRI	TEST	Mode	Normal Pin Status			Test Pin Status	
				Input	Output	DC	Input	Output
0	XZ	XZ	Backup	XZ	Hi-Z	1	XZ	Hi-Z
1	0	X	Normal	Valid	Valid	Valid	XZ	Hi-Z
1	1	0	Test (non-select)	XZ	Hi-Z	1	XZ	Hi-Z
1	1	1	Test (select)	XZ	Hi-Z	1	Valid	Valid

Normal mode access

CSB	BE	WEB	OEB	A(a:0)	DI(b:0)	DO(b:0)	DC	Operation
0	↑	0	1	Ax	DIx	Hi-Z	1	Write (output off)
0	↑	0	0	Ax	DIx	[Ax] = DIx**Note**	0	Write (output on)
0	↑	1	0	Ax	X	[Ax]	0	Read
0	0	X	0	X	X	Hold	0	Precharge
0	X	X	1	X	X	Hi-Z	1	Output off
1	X	X	X	X	X	Hi-Z	1	Macro off

Note The data input from the DI(b:0) pin is output through.

Test mode access

TCSB	TBE	TWEB	TA(a:0)	TDI(b:0)	TDO(b:0)	Operation
0	↑	0	Ax	DIx	[Ax] = DIx**Note**	Write
0	↑	1	Ax	X	[Ax]	Read
0	0	X	X	X	Hold	Precharge
1	X	X	X	X	Hold	Macro off

Note The data input from the TDI(b:0) pin is output through.

6.4 Macro Size

Use the following expressions to calculate the macro size.

Macro size = X × Y (grids)

W : number of words
B : number of bits
N : number of address lines (N = $\log_2$ W (rounded up at decimal place))
α : Macro circumferential wiring area in X direction (73.53)
β : Macro circumferential wiring area in Y direction (7.353)

$X = 37.89 \times B + 4.59 \times N + 153.00 + \alpha$ (grids)
$Y = 7.464 \times 10^{-2} \times W + 18.51 + \beta$ (grids)

Remarks 1. Round up the fraction below the decimal place.
2. Not necessary to add α and β when not taking the macro circumferential wiring area into consideration.

6.5 Electrical Characteristics

Absolute maximum ratings

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	–0.5 to +4.6	V
Operating ambient temperature	T_A	–40 to +85	°C
Storage temperature	T_{stg}	–65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended operating range

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}	3.0	3.3	3.6	V
Operating ambient temperature	T_A	–40		+85	°C

6.6 Operating Current Consumption

The operating current consumption (I_{DD}) changes depending on the number of bits, number of words, number of address lines, and operating frequency of the memory. The value of the operating current consumption can be calculated by the following expression.

I_{DD} (TYP.) = I_{DDR} (TYP.) + I_{DDW} (TYP.)
I_{DD} (MAX.) = I_{DDR} (MAX.) + I_{DDW} (MAX.)

I_{DDR} and I_{DDW} in the above expression can be worked out by the expressions in the table below.

The meanings of the symbols in the tables below are as follows:
B: number of bits, W: number of words, N: number of address lines ($N = \log_2 W$ (rounded up at decimal place)),
f_R: read operating frequency (MHz), f_W: write operating frequency (MHz), C_L: external load capacitance (pF),
A: Operation rate **Note 1** (100% = 1)
DF: MAX. data rate (MHz) of A (a:0), WEB, or DI (b:0) pin

(1) V_{DD} = 3.3 V ± 0.3 V

TYP.
During read/write operation ($\alpha = 1.65 \times B \times C_L$)

Operation	Expression	Unit
Read (I_{DDR})	$\{(1.19 \times N + 4.06 \times B - 4.28) \times 10^{-3} \times W + 0.669 \times N + 2.95 \times B + 10.7 + 2 \times \alpha\} \times f_R \times A + 722 \times B + 0.288 \times W$	μA
Write (I_{DDW})	$\{(1.19 \times N + 4.31 \times B - 4.28) \times 10^{-3} \times W + 0.669 \times N + 4.33 \times B + 10.7 + 2 \times \alpha\} \times f_W \times A$	μA

MAX.
During read/write operation ($\alpha = 1.8 \times B \times C_L$)

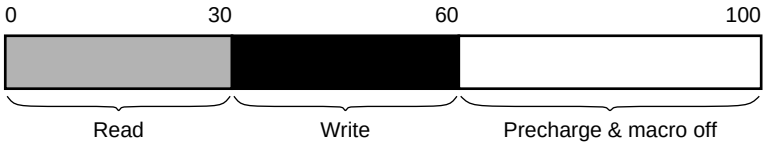
Operation	Expression	Unit
Read (I_{DDR})	$\{(1.70 \times N + 5.80 \times B - 6.11) \times 10^{-3} \times W + 0.955 \times N + 4.22 \times B + 15.3 + 2 \times \alpha\} \times f_R \times A + 1032 \times B + 0.411 \times W$	μA
Write (I_{DDW})	$\{(1.70 \times N + 6.15 \times B - 6.11) \times 10^{-3} \times W + 0.955 \times N + 6.18 \times B + 15.3 + 2 \times \alpha\} \times f_W \times A$	μA

In power-down mode Note2

Condition	Expression	Unit
TYP.	$\{5.78 \times 10^{-3} \times (N - 5) \times W + 0.493 \times N + 0.331 \times B + 0.495\} \times DF$	μA
MAX.	$\{8.25 \times 10^{-3} \times (N - 5) \times W + 0.704 \times N + 0.473 \times B + 0.71\} \times DF$	μA

Notes 1. This operation rate is the ratio of the read and write operations to the total operation period (read, write, precharge, and macro off) of the RAM.

Example The operation rate is 60% (0.6) if read operations account for 30% of the total operation period of RAM and write operations account for 30%.



2. Power-down mode indicates the precharge status or macro off status in **Normal mode access** in **6.3 Operation Truth Table**.

Remarks 1. Calculate the read/write operating frequency (MHz) based on the following concept (read 50%, write 50% during read/write operation).

Example To read and write alternately every 1 clock at 50 MHz
Calculate I_{DDR} and I_{DDW} assuming the following.
Read frequency: f_R = 25 MHz
Write frequency: f_W = 25 MHz

2. If OEB is fixed to H during write operation, α of I_{DDW} is 0 (in the write (output off) status for the normal mode access in the operation truth table).

6.7 Timing

6.7.1 Expressions

The timing values of the RAM can be calculated by the following expressions (rounded at the third place below the decimal place. However, the output hold time is truncated).

The meanings of the symbols in the table below are as follows:
W: number of words, B: number of bits, N: number of address lines ($N = \log_2 W$ (rounded up at decimal place)), C_L: external load capacitance (pF)

(1) V_{DD} = 3.3 ± 0.3 V

Read/write operation (T_A = –40 to +85°C)

Parameter		Symbol	Expression	Unit
Cycle time		t_{RC}	Where $t_{BEH} > t_{PC}$: $t_{BEH} \times 2$ (clock duty: 50%) Where $t_{BEH} < t_{PC}$: $t_{PC} \times 2$ (clock duty: 50%)	ns
Access time		t_{ACC}	$2.30 + 1.60 \times 10^{-2} \times B + 9.40 \times 10^{-4} \times W + 3.21 \times 10^{-1} \times C_L$	ns
Output hold time		t_{OH}	$0.24 + 1.55 \times 10^{-2} \times B$	ns
BE high-level time		t_{BEH}	$1.40 + 1.60 \times 10^{-2} \times B + 8.94 \times 10^{-4} \times W$	ns
Precharge time		t_{PC}	$1.09 + 1.30 \times 10^{-2} \times B + 5.83 \times 10^{-4} \times W$	ns
Address setup time		t_{AS}	$0.87 + 2.54 \times 10^{-4} \times W$	ns
Address hold time		t_{AH}	$0.72 + 1.25 \times 10^{-2} \times N$	ns
Write data setup time		t_{DIS}	0	ns
Write data hold time		t_{DIH}	$1.05 + 1.88 \times 10^{-2} \times B$	ns
Write data through time		t_{DTH}	$2.21 + 1.77 \times 10^{-2} \times B + 3.21 \times 10^{-1} \times C_L$	ns
WEB setup time		t_{WS}	0.60	ns
WEB hold time		t_{WH}	$0.72 + 1.25 \times 10^{-2} \times N$	ns
CSB setup time		t_{CS}	1.00	ns
CSB hold time		t_{CH}	0	ns
CSB, OEB control				
	Output floating time	t_{HZ}	$1.60 + 2.66 \times 10^{-2} \times B$	ns
	Output active time	t_{LZ}	$1.75 + 2.20 \times 10^{-2} \times B$	ns
	DC output delay time	t_{DC}	$1.80 + 2.00 \times 10^{-2} \times B + 1.46 \times C_L$	ns

6.7.2 Typical value (8 bits × 512 words)

(1) V_{DD} = 3.3 ± 0.3 V

Read/write operation (T_A = –40 to +85°C)

Parameter		Symbol	MIN.	TYP.	MAX.	Unit
Cycle time		t_{RC}	3.98			ns
Access time		t_{ACC}			2.98	ns
Output hold time		t_{OH}	0.36			ns
BE high-level time		t_{BEH}	1.99			ns
Precharge time		t_{PC}	1.50			ns
Address setup time		t_{AS}	1.01			ns
Address hold time		t_{AH}	0.84			ns
Write data setup time		t_{DIS}	0			ns
Write data hold time		t_{DIH}	1.21			ns
Write data through time		t_{DTH}			2.42	ns
WEB setup time		t_{WS}	0.60			ns
WEB hold time		t_{WH}	0.84			ns
CSB setup time		t_{CS}	1.00			ns
CSB hold time		t_{CH}	0			ns
CSB, OEB control						
	Output floating time	t_{HZ}	1.82			ns
	Output active time	t_{LZ}	1.93			ns
	DC output delay time	t_{DC}			2.26	ns

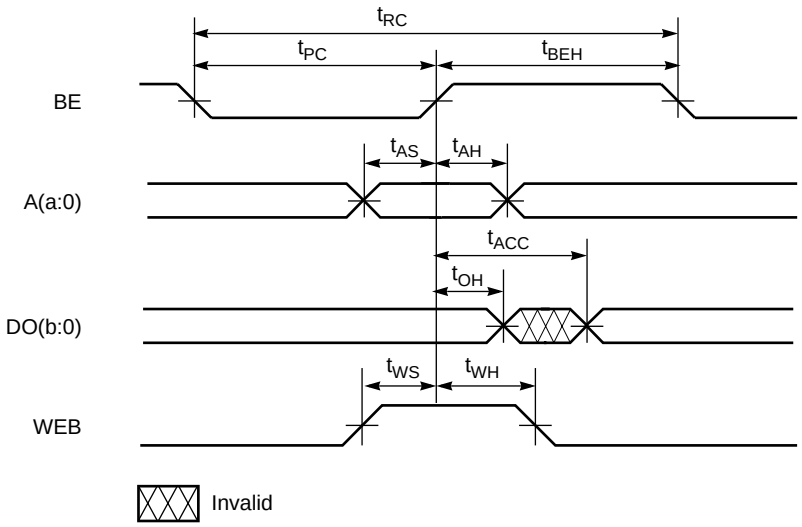
Remarks 1. The above data are calculated with an external load capacitance of 0.2 pF.

2. The meanings of the symbols in the above table are as follows:
MIN. : minimum value necessary for operating macro under worst condition
MAX. : delay time of macro output under worst condition

6.8 Timing Chart

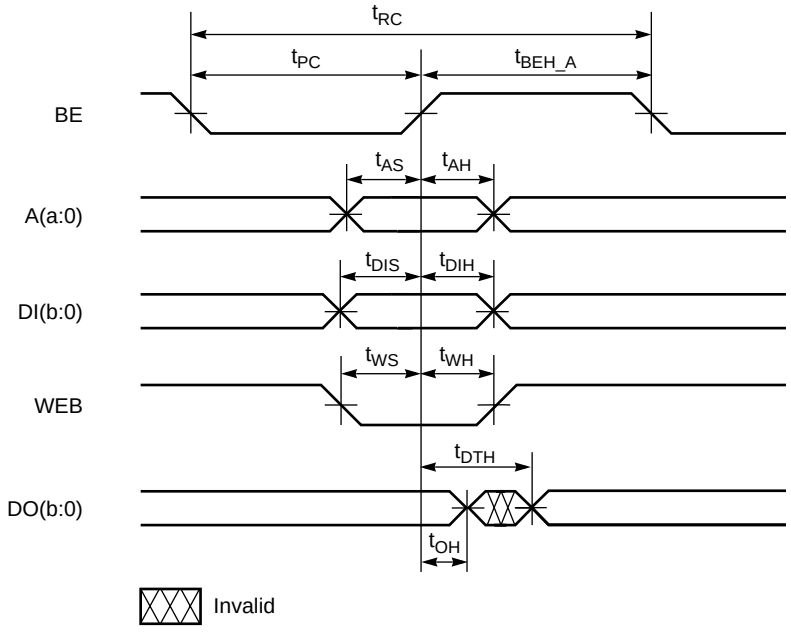
Read operation

Read cycle (CSB = low level, OEB = low level)



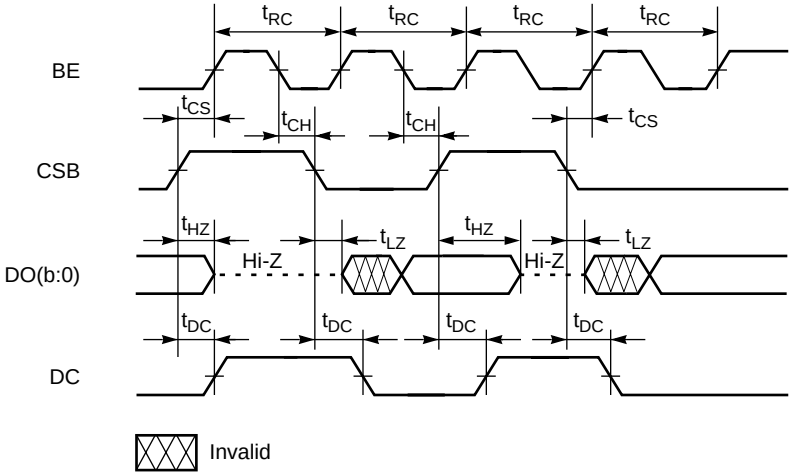
Write operation

Write cycle (CSB = low level, OEB = low level)

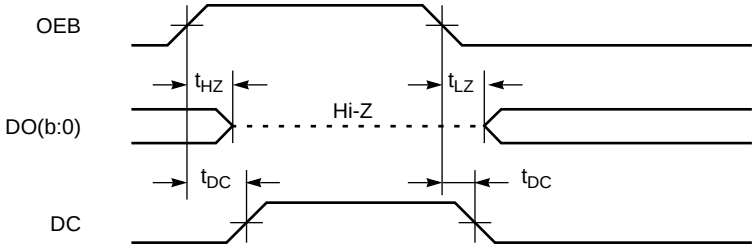


Read/write operation

(1) CSB control (OEB = low level)



(2) OEB control (CSB = low level)



6.9 Notes on Correct Use

(1) If a spike is input to the clock input pin while CSB = L, the data in the RAM may be destroyed. In this case, the addresses other than that when the spike was input may be also destroyed.

(2) Static current is consumed by the super high-speed synchronous single-port RAM in the following case. To prevent static current consumption from occurring, configure the circuit so that "H" can be input to CSB (chip select).

Normal mode

CSB = L, WEB = H, BE = H period: Read operation

Test mode

TCSB = L, TWEB = H, TBE = H period: Read operation

Static current consumption calculation expression

I_{DDS} (MAX) = $1.032 \times B + 4.11 \times 10^{-4} \times W$ [mA]

CHAPTER 7 REGISTER FILE (DUAL-PORT)

7.1 General

- Dedicated to VX/VM type
- Compiled type
  Bit width: 4 to 64 bits (variable in 1-bit units)
  Number of words: 8 to 512 words (variable in 4-word units)
- Read access time (64 bits × 512 words, C_L = 0.2 pF)
  At V_{DD} = 3.3 ± 0.3 V: t_{RA} = 19.76 (ns)
  At V_{DD} = 2.0 ± 0.2 V: t_{RA} = 44.77 (ns)
- Operating voltage: 3.3 ± 0.3 V, 2.0 ± 0.2 V
- Operating temperature: –40 to +85°C
- 0.35 μm CMOS technology

7.1.1 Compiled range

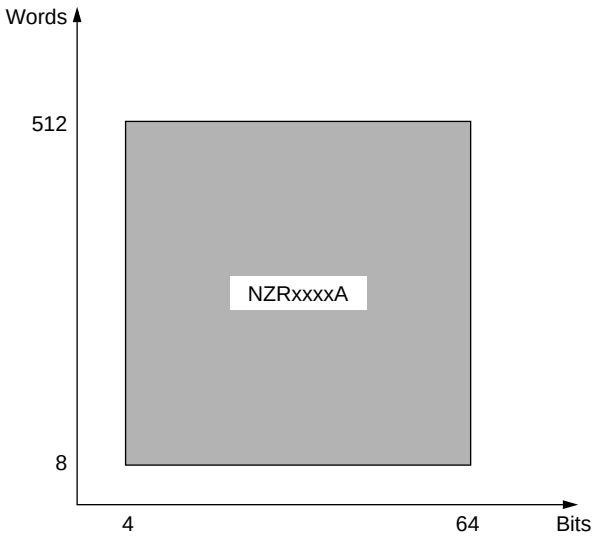
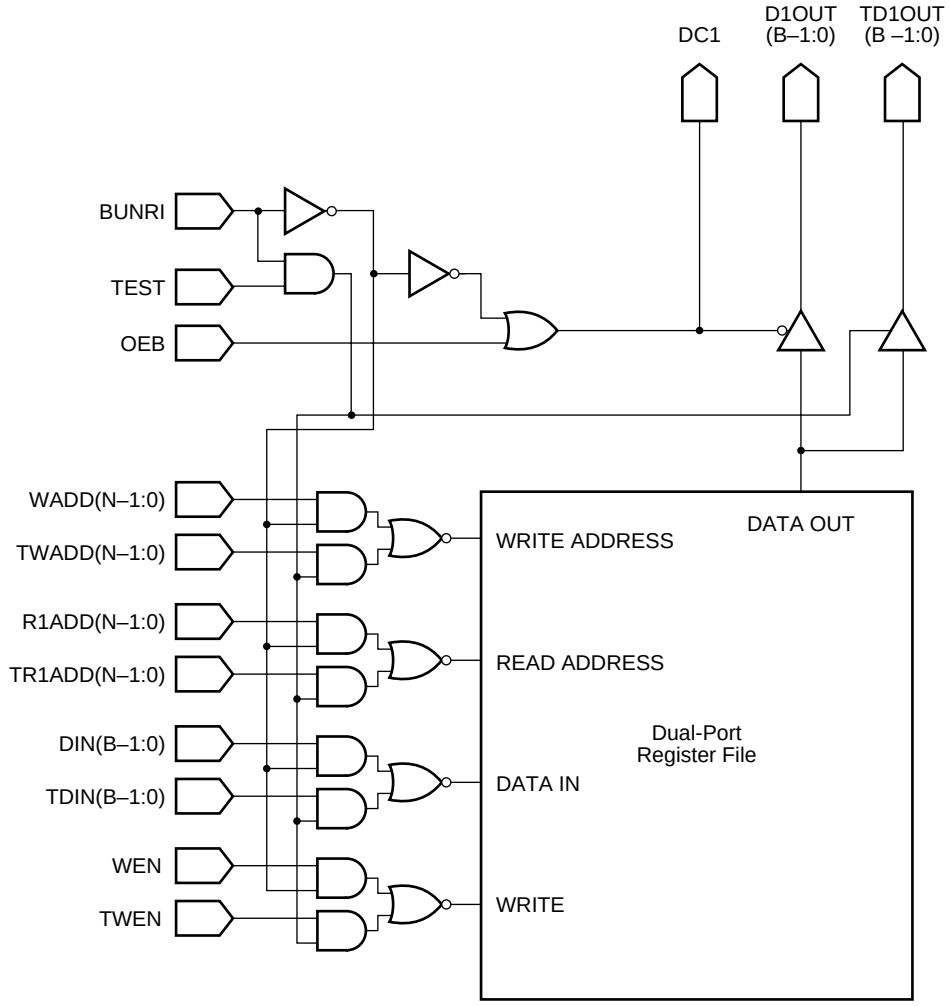


Figure 7-1 Compiled Range of Register File

Table 7-1 Compiled Range of Register File

Block Name	Minimum Size	Maximum Size	Step
NZRxxxxA	8 words × 4 bits	512K words × 64 bits	4 words/1 bit

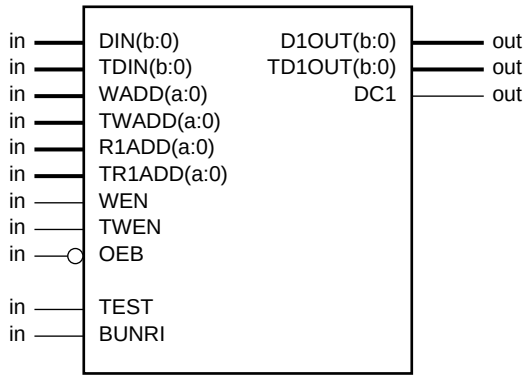
7.1.2 Equivalent circuit



Remark N: number of address lines, B: number of bits

Figure 7-2 Internal Equivalent Circuit

7.1.3 Symbol diagram



Remarks 1. A pin prefixed with “T” is a test pin.
2. “a” = (number of address lines) – 1, where $2 \leq a \leq 8$.
“b” = (number of bits) – 1, where $3 \leq b \leq 63$.

7.1.4 Pin capacitance

Pin Information GateDRC uses C_{IN} and C_{MAX} for fanin/fanout calculation.
Wiring capacitance = Temporary wiring length × 0.18 (pF/mm)

Input		Output		
Pin Name/Symbol	**CIN (pF)**	**Pin Name/Symbol**	**CIN (pF)**	**CMAX (pF)**
DIN(b:0)	0.005	D1OUT(b:0)	0.011	3.42
TDIN(b:0)	0.005			(2.82)
WADD(a:0)	0.007	TD1OUT(b:0)	0.007	3.42
TWADD(a:0)	0.007			(2.82)
RA1ADD(a:0)	0.007	DC1	–	3.42
TR1ADD(a:0)	0.007			(2.82)
WEN	0.005			
TWEN	0.005			
OEB	0.007			
TEST	0.007			
BUNRI	0.007			

Remarks 1. “a” = (number of address lines) – 1, where $2 \leq a \leq 8$
“b” = (number of bits) – 1, where $3 \leq b \leq 63$
2. ( ): $V_{DD} = 2.0 \pm 0.2$ V

7.2 Pin Function List

Pin Name/Signal Name	Attribute	Mode	Function
DIN(b:0)	I	Normal	Data input b = number of bits – 1
D1OUT(b:0)	OZ	Normal	Data output b = number of bits – 1
WADD(a:0)	I	Normal	Write address input a = number of address lines – 1 (determined by number of words)
R1ADD(a:0)	I	Normal	Read address input a = number of address lines – 1 (determined by number of words)
WEN	I	Normal	Write enable input
OEB	I	Normal	Data output enable input
TDIN(b:0)	I	Test	Data input b = number of bits – 1
TD1OUT(b:0)	OZ	Test	Data output b = number of bits – 1
TWADD(a:0)	I	Test	Write address input a = number of address lines – 1 (determined by number of words)
TR1ADD(a:0)	I	Test	Read address input a = number of address lines – 1 (determined by number of words)
TWEN	I	Test	Write enable input
BUNRI	I	Mode selection	Separation test input BUNRI = 0: Normal mode BUNRI = 1: Test mode
TEST	I	Mode selection	Test mode input BUNRI = 1, TEST = 0 Separated from test bus (tests other macros) BUNRI = 1, TEST = 1 Selected as subject to test
DC1	O	Normal	Data control output DC1 = 0: D1OUT(b:0) = 0, 1, undefined DC1 = 1: D1OUT(b:0) = high impedance

Remark The meanings of the symbols in the Attribute column are as follows:
I: input pin, OZ: 3-state output pin, O: output pin

7.3 Operation Truth Table

The meanings of the symbols in the following operation truth tables are as follows:

Hi-Z : High impedance
X : Undefined state not including high impedance
XZ : Undefined state including high impedance
Ad, AdA, AdB : Any data
D : Input data
[Ad], [AdA], [AdB] : Data in memory

BUNRI	TEST	Mode	Normal Pin Status			Test Pin Status	
			Input	Output	DC1	Input	Output
0	X	Normal	Valid	Valid	Valid	XZ	Hi-Z
1	0	Test (non-select)	XZ	Hi-Z	1	XZ	Hi-Z
1	1	Test (select)	XZ	Hi-Z	1	Valid	Valid

Normal mode access

R1ADD (a:0)	WADD (a:0)	WEN	DIN (b:0)	OEB	D1OUT (b:0)	DC1	Latch	Operation
Ad	X	0	X	0	[Ad]	0	Hold	Read
X	Ad	1	D	1	Hi-Z	1	[Ad] = D	Write
AdA	AdB	1	D	0	[AdA]	0	[AdB] = D	Read/write
X	X	0	X	1	Hi-Z	1	Hold	Output off

Test mode access

TR1ADD (a:0)	TWADD (a:0)	TWEN	TDIN (b:0)	TD1OUT (b:0)	Latch	Operation
Ad	X	0	X	[Ad]	Hold	Read
X	Ad	1	D	X	[Ad] = D	Write

7.4 Macro Size

Use the following expressions to calculate the macro size.

Macro size = X × Y (grids)

W : number of words
B : number of bits
N : number of address lines ($N = \log_2 W$ (rounded up at decimal place))
Rx : X-direction power supply ring width
Ry : Y-direction power supply ring width
α : Macro circumferential wiring area in X direction (73.53)
β : Macro circumferential wiring area in Y direction (7.353)

$X = 47.43 + Rx \times 4 + 9.12 \times (N - 2) + 20.48 \times B + \alpha$ (grids)
$Y = 6.02 + Ry \times 4 + 0.29 \times W + \beta$ (grids)

Rx, Ry

Number of Bits	Rx	Ry
4 to 8	5.15	0.52
9 to16	8.09	0.81
17 to 32	11.77	1.18
33 to 64	15.45	1.55

Remarks 1. Round up the fraction below the decimal place.
2. Not necessary to add α and β when not to take the macro circumferential wiring area into consideration.

7.5 Electrical Characteristics

Absolute maximum ratings

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	–0.5 to +4.6	V
Operating ambient temperature	T_A	–40 to +85	°C
Storage temperature	T_{stg}	–65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended operating range

V_{DD} = 3.3 ± 0.3 V

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}	3.0	3.3	3.6	V
Operating ambient temperature	T_A	–40		+85	°C

V_{DD} = 2.0 ± 0.2 V

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}	1.8	2.0	2.2	V
Operating ambient temperature	T_A	–40		+85	°C

7.6 Operating Current Consumption

The operating current consumption (I_{DD}) changes depending on the number of bits, number of words, and operating frequency of the memory. The value of the operating current consumption can be calculated by the following expression.

I_{DD} (TYP.) = I_{DDR} (TYP.) + I_{DDW} (TYP.)
I_{DD} (MAX.) = I_{DDR} (MAX.) + I_{DDW} (MAX.)

I_{DDR} and I_{DDW} in the above expression can be worked out by the expressions in the table below.

The meanings of the symbols in the tables below are as follows:
B: number of bits, W: number of words, f_R: read operating frequency (MHz)
f_W: write operating frequency (MHz), C_L: external load capacitance (pF)
A: Operation rate[Note] (100% = 1)

(1) V_{DD} = 3.3 ± 0.3 V

TYP.
During read/write operation ($\alpha = 1.65 \times C_L \times B$)

Operation	Expression	Unit
Read (I_{DDR})	$(0.367 \times W + 3.286 \times B - 0.849 + \alpha) \times f_R$	μA
Write (I_{DDW})	$(0.249 \times W + 2.685 \times B - 0.610) \times f_W$	μA

MAX.
During read/write operation ($\alpha = 1.8 \times C_L \times B$)

Operation	Expression	Unit
Read (I_{DDR})	$(0.409 \times W + 3.603 \times B - 0.944 + \alpha) \times f_R$	μA
Write (I_{DDW})	$(0.259 \times W + 2.970 \times B - 0.575) \times f_W$	μA

(2) V_{DD} = 2.0 ± 0.2 V

TYP.
During read/write operation ($\alpha = 1.0 \times C_L \times B$)

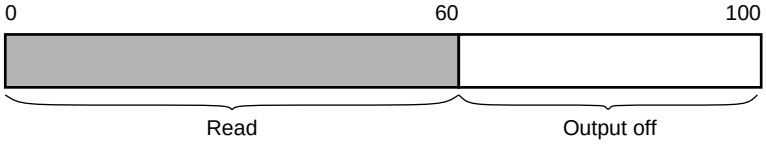
Operation	Expression	Unit
Read (I_{DDR})	$(0.233 \times W + 3.759 \times B - 0.981 + \alpha) \times f_R$	μA
Write (I_{DDW})	$(-0.027 \times W + 1.113 \times B - 2.234) \times f_W$	μA

MAX.
During read/write operation ($\alpha = 1.1 \times C_L \times B$)

Operation	Expression	Unit
Read (I_{DDR})	$(0.252 \times W + 4.229 \times B - 1.029 + \alpha) \times f_R$	μA
Write (I_{DDW})	$(0.165 \times W + 0.415 \times B - 0.598) \times f_W$	μA

Note This operation rate is the ratio of the read and write operations to the total operation period (read, write, and output off).

Example The operation rate is 60% (0.6) if read operations account for 60% of the total operation period.



Remark If all the input signals are fixed, the current consumption in the standby mode (I_{DD1}) = 0.

7.7 Timing

7.7.1 Expressions

The timing values of the RAM can be calculated by the following expressions (rounded at the third place below the decimal place.)

The meanings of the symbols in the table below are as follows:
W: number of words, B: number of bits, C_L: external load capacitance (pF)

(1) V_{DD} = 3.3 ± 0.3 V

Read/write operation (T_A = –40 to +85°C)

Parameter	Symbol	Expression	Unit
Read access time	t_{RA}	$3.899 + 2.021 \times 10^{-2} \times B + 2.831 \times 10^{-2} \times W + 3.54 \times 10^{-1} \times C_L$	ns
Read cycle time	t_{RC}	$3.899 + 2.021 \times 10^{-2} \times B + 2.831 \times 10^{-2} \times W$	ns
Write cycle time	t_{WC}	$4.446 + 2.010 \times 10^{-2} \times B + 1.270 \times 10^{-3} \times W$	ns
Output hold time	t_{OH}	0.580	ns
Write enable access time	t_{WO}	$5.176 + 1.960 \times 10^{-2} \times B + 2.486 \times 10^{-2} \times W + 3.54 \times 10^{-1} \times C_L$	ns
Data input to data output	t_{IO}	$8.232 + 3.210 \times 10^{-4} \times B + 2.373 \times 10^{-2} \times W + 3.54 \times 10^{-1} \times C_L$	ns
Output active time	t_{OEA}	$1.804 + 1.656 \times 10^{-2} \times B – 9.200 \times 10^{-5} \times W + 3.54 \times 10^{-1} \times C_L$	ns
Output floating time	t_{OEZ}	$3.540 + 1.995 \times 10^{-2} \times B + 1.530 \times 10^{-4} \times W + 3.54 \times 10^{-1} \times C_L$	ns
Write address setup time	t_{WAS}	$2.996 + 1.508 \times 10^{-2} \times B – 1.120 \times 10^{-3} \times W$	ns
Write address hold time	t_{WAH}	0	ns
Data setup time	t_{DS}	$4.514 – 8.290 \times 10^{-3} \times B – 1.350 \times 10^{-3} \times W + 3.54 \times 10^{-1} \times C_L$	ns
Data hold time	t_{DH}	0	ns
Write pulse width	t_{WP}	$1.450 + 5.011 \times 10^{-3} \times B + 2.391 \times 10^{-3} \times W$	ns
DC1 output delay time	t_{DC}	$2.700 + 3.54 \times 10^{-1} \times C_L$	ns

(2) V_{DD} = 2.0 ± 0.2 V

Read/write operation (T_A = –40 to +85°C)

Parameter	Symbol	Expression	Unit
Read access time	t_{RA}	$8.528 + 5.821 \times 10^{-2} \times B + 6.322 \times 10^{-2} \times W + 7.31 \times 10^{-1} \times C_L$	ns
Read cycle time	t_{RC}	$8.528 + 5.821 \times 10^{-2} \times B + 6.322 \times 10^{-2} \times W$	ns
Write cycle time	t_{WC}	$8.163 + 6.527 \times 10^{-2} \times B + 7.828 \times 10^{-3} \times W$	ns
Output hold time	t_{OH}	0.9	ns
Write enable access time	t_{WO}	$9.665 + 5.300 \times 10^{-2} \times B + 6.667 \times 10^{-2} \times W + 7.31 \times 10^{-1} \times C_L$	ns
Data input to data output	t_{IO}	$18.013 + 7.756 \times 10^{-2} \times B + 5.858 \times 10^{-2} \times W + 7.31 \times 10^{-1} \times C_L$	ns
Output active time	t_{OEA}	$3.496 + 3.494 \times 10^{-2} \times B – 7.600 \times 10^{-5} \times W + 7.31 \times 10^{-1} \times C_L$	ns
Output floating time	t_{OEZ}	$6.423 + 3.988 \times 10^{-2} \times B – 1.100 \times 10^{-4} \times W + 7.31 \times 10^{-1} \times C_L$	ns
Write address setup time	t_{WAS}	$5.463 + 5.352 \times 10^{-2} \times B – 1.800 \times 10^{-3} \times W$	ns
Write address hold time	t_{WAH}	0	ns
Data setup time	t_{DS}	$9.429 – 1.327 \times 10^{-2} \times B – 2.330 \times 10^{-3} \times W + 7.31 \times 10^{-1} \times C_L$	ns
Data hold time	t_{DH}	0	ns
Write pulse width	t_{WP}	$2.700 + 1.175 \times 10^{-2} \times B + 6.028 \times 10^{-3} \times W$	ns
DC1 output delay time	t_{DC}	$5.2 + 7.31 \times 10^{-1} \times C_L$	ns

7.7.2 Typical value (8 bits × 512 words)

(1) V_{DD} = 3.3 ± 0.3 V

Read/write operation (T_A = –40 to +85°C)

Parameter	Symbol	MIN	TYP	MAX	Unit
Read access time	t_{RA}			18.63	ns
Read cycle time	t_{RC}	18.56			ns
Write cycle time	t_{WC}	5.26			ns
Output hold time	t_{OH}	0.58			ns
Write enable access time	t_{WO}			18.14	ns
Data input to data output	t_{IO}			20.46	ns
Output active time	t_{OEA}			1.97	ns
Output floating time	t_{OEZ}			3.85	ns
Write address setup time	t_{WAS}	2.55			ns
Write address hold time	t_{WAH}	0			ns
Data setup time	t_{DS}	3.83			ns
Data hold time	t_{DH}	0			ns
Write pulse width	t_{WP}	2.72			ns
DC1 output delay time	t_{DC}			2.78	ns

(2) V_{DD} = 2.0 ± 0.2 V

Read/write operation (T_A = –40 to +85°C)

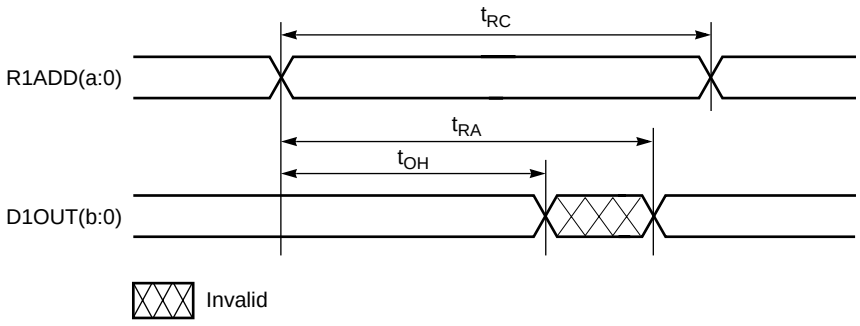
Parameter	Symbol	MIN	TYP	MAX	Unit
Read access time	t_{RA}			41.51	ns
Read cycle time	t_{RC}	41.37			ns
Write cycle time	t_{WC}	12.7			ns
Output hold time	t_{OH}	0.9			ns
Write enable access time	t_{WO}			44.38	ns
Data input to data output	t_{IO}			48.78	ns
Output active time	t_{OEA}			3.89	ns
Output floating time	t_{OEZ}			6.84	ns
Write address setup time	t_{WAS}	4.97			ns
Write address hold time	t_{WAH}	0			ns
Data setup time	t_{DS}	9.6			ns
Data hold time	t_{DH}	0			ns
Write pulse width	t_{WP}	5.89			ns
DC1 output delay time	t_{DC}			5.35	ns

Remarks 1. The above data are calculated with an external load capacitance of 0.2 pF.
2. The meanings of the symbols in the above table are as follows:
MIN. : minimum value necessary for operating macro under worst condition
MAX. : delay time of macro output under worst condition

7.8 Timing Chart

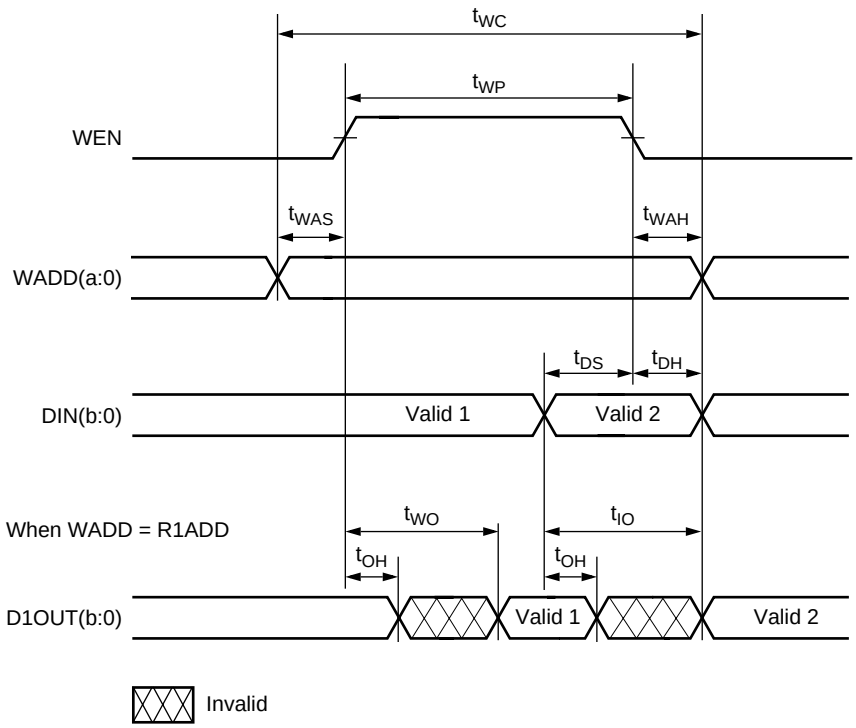
Read operation

Read cycle (OEB = 0)



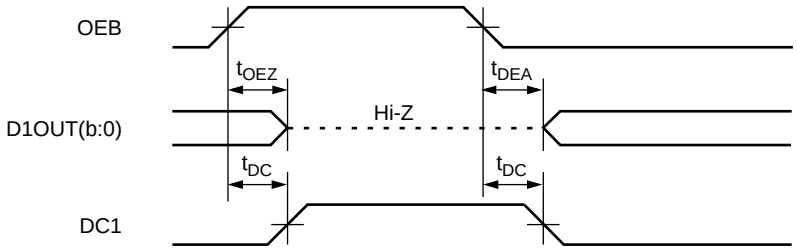
Write operation

Write cycle (OEB = 0)



Read/write operation

OEB control



CHAPTER 8 HIGH-SPEED ROM (SYNCHRONOUS TYPE)

8.1 General

- Synchronous ROM
- Flexible memory size
  → High efficiency macro location by memory compiler
  Block name : ZTYxxxxx
  Bit width : 1 to 32 bits (variable in 1-bit units)
  Number of words : 64 to 8K words (variable in 32-word units)
  Block name : ZTTxxxxx
  Bit width : 33 to 64 bits (variable in 1-bit units)
  Number of words : 64 to 8K words (variable in 32-word units)
- Operating voltage: 3.3 ± 0.3 V, 2.0 ± 0.2 V
- Operating ambient temperature: –40 to +85°C
- Storage temperature: –65 to +150°C
- 0.35 μm CMOS technology

8.1.1 Compiled range

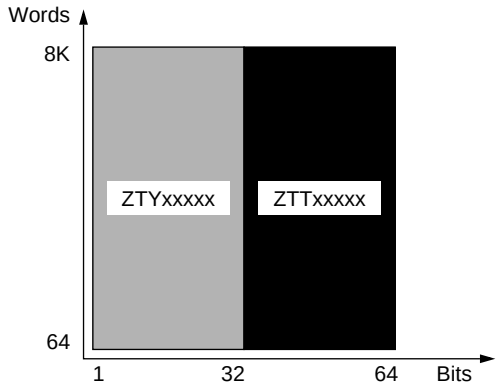
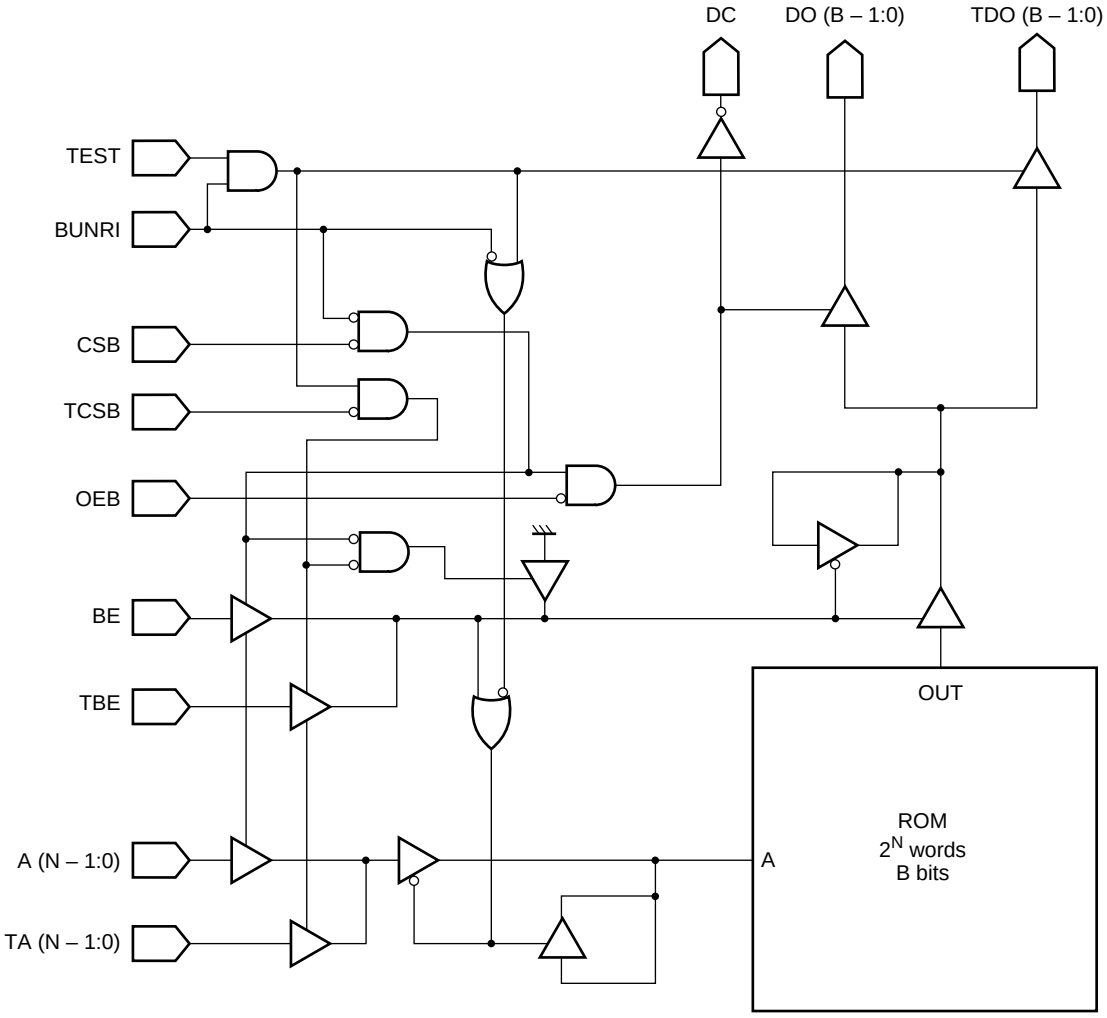


Figure 8-1 Compiled Range of High-Speed ROM (Synchronous Type)

Table 8-1 Compiled Range of High-Speed ROM (Synchronous Type)

Block Name	Minimum Size	Maximum Size	Step
ZTYxxxxx	64 words × 1 bit	8K words × 32 bits	32 words/1 bit
ZTTxxxxx	64 words × 33 bits	8K words × 64 bits	32 words/1 bit

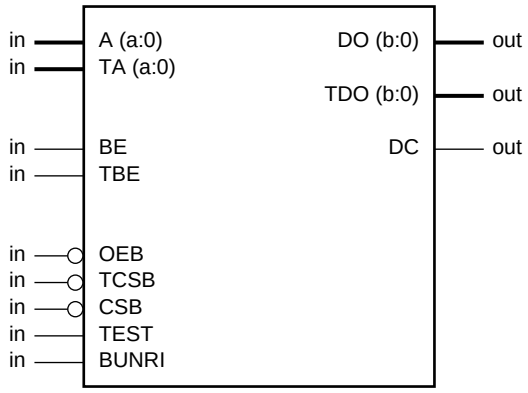
8.1.2 Equivalent circuit



Remark N: number of address lines, B: number of bits

Figure 8-2 Internal Equivalent Circuit

8.1.3 Symbol diagram



Remarks 1. A pin prefixed with “T” is a test pin.
2. “a” = (number of address lines) – 1, where $5 \leq a \leq 12$ (64 words MIN., 8K words MAX.)
“b” = (number of bits) – 1, where $0 \leq b \leq 63$ (1 bit MIN., 64 bits MAX.)

8.1.4 Pin capacitance

Pin Information GateDRC uses C_{IN} and C_{MAX} for fan-in/fan-out calculation.
Wiring capacitance = Temporary wiring length $\times$ 0.18 (pF/mm)

Input		Output		
Pin Name/Symbol	**CIN (pF)**	**Pin Name/Symbol**	**CIN (pF)**	**CMAX (pF)**
A(a:0)	0.055	DO(b:0)	0.058	8.849
TA(a:0)	0.055			(2.278)
BE	0.047	TDO(b:0)	0.047	8.849
TBE	0.047			(2.278)
OEB	0.020	DC	–	3.191
CSB	0.020			(1.343)
TCSB	0.020			
TEST	0.015			
BUNRI	0.023			

Remarks 1. ( ): Value at $V_{DD} = 2.0 \pm 0.2$ V
2. “a” = (number of address lines) – 1, where $5 \leq a \leq 12$ (64 words MIN., 8K words MAX.)
“b” = (number of bits) – 1, where $0 \leq b \leq 63$ (1 bit MIN., 64 bits MAX.)

8.2 Pin Function List

Pin Name/Signal Name	Attribute	Mode	Function
DO(b:0)	OZ	Normal	Data output b = number of bits – 1
A(a:0)	I	Normal	Address input a = number of address lines – 1 (determined by number of words)
BE	I	Normal	Clock input
CSB	I	Normal	Chip select input
OEB	I	Normal	Data output enable input
TDO(b:0)	OZ	Test	Data output b = number of bits – 1
TA(a:0)	I	Test	Address input a = number of address lines – 1 (determined by number of words)
TBE	I	Test	Clock input
TCSB	I	Test	Chip select input
BUNRI	I	Mode selection	Separation test input (normal mode: low level, test mode: high level) BUNRI = 0: Normal mode BUNRI = 1: Test mode
TEST	I	Mode selection	Test mode input BUNRI = 1, TEST = 0 Separated from test bus (tests other macros) BUNRI = 1, TEST = 1 Selected to be tested
DC	O	Normal	Data control output DC = 0: DO(b:0) = 0, 1, undefined DC = 1: DO(b:0) = high impedance

Remark The meanings of the symbols in the Attribute column are as follows:
I: Input pin, OZ: 3-state output pin, O: Output pin

8.3 Operation Truth Table

The meanings of the symbols in the following operation truth tables are as follows:

Hi-Z : High impedance
X : Undefined state not including high impedance
XZ : Undefined state including high impedance
Ax : Any data
[Ax] : Data in memory

BUNRI	TEST	Mode	Normal Pin Status			Test Pin Status	
			Input	Output	DC	Input	Output
0	XZ	Normal	Valid	Valid	Valid	XZ	Hi-Z
1	0	Test (non-select)	XZ	Hi-Z	1	XZ	Hi-Z
1	1	Test (select)	XZ	Hi-Z	1	Valid	Valid

Normal mode access

CSB	BE	OEB	A(a:0)	DO(b:0)	DC	Operation
0	↑	0	Ax	[Ax]	0	Read
0	0	0	X	Hold	0	Precharge
0	X	1	X	Hi-Z	1	Output off
1	X	X	X	Hi-Z	1	Macro off

Test mode access

TCSB	TBE	TA(a:0)	TDO(b:0)	Operation
0	↑	Ax	[Ax]	Read
0	0	X	Hold	Precharge
1	X	X	X	Macro off

★ 8.4 Macro Size

Use the following expressions to calculate the macro size.

Macro size = X × Y (grids)
W : Number of words
B : Number of bits
N : Number of address lines N = $\log_2$ W (rounded at decimal place)
α : Macro circumferential wiring area in X direction (73.53)
β : Macro circumferential wiring area in Y direction (7.353)

B ≤ 32	X = 10.691 × B + 7.530 × (N–5) + 185.68 + α	(grids)
	Y = 2.647 × 10^{-2} × W + 20.913 + β	(grids)
B > 32	X = 10.691 × B + 7.530 × (N–5) + 197.44 + α	(grids)
	Y = 2.647 × 10^{-2} × W + 20.913 + β	(grids)

Remarks 1. Round up the fraction below the decimal place.
2. Not necessary to add α and β when not to take the macro circumferential wiring area into consideration.

8.5 Electrical Characteristics

Absolute maximum ratings

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	–0.5 to +4.6	V
Operating ambient temperature	T_A	–40 to +85	°C
Storage temperature	T_{stg}	–65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended operating range (V_{DD} = 3.3 ± 0.3 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}	3.0	3.3	3.6	V
Operating ambient temperature	T_A	–40		+85	°C

Recommended operating range (V_{DD} = 2.0 ± 0.2 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}	1.8	2.0	2.2	V
Operating ambient temperature	T_A	–40		+85	°C

8.6 Operating Current Consumption

The operating current consumption (I_{DD}) changes depending on the number of bits, number of words, and operating frequency of the memory. The value of the operating current consumption can be calculated by the following expression. The meanings of the symbols in the tables below are as follows:

B: Number of bits, W: Number of words, f: Operating frequency (MHz), A: Operation rate **Note** (100% = 1)

(1) V_{DD} = 3.3 ± 0.3 V

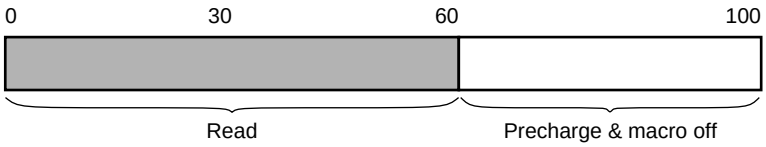
Condition	Expression (MAX.)	Unit
TYP.	$(0.0191 \times W + 6.70 \times B + 18 + 1.65 \times B \times C_L) \times f \times A$	μA
MAX.	$(0.0235 \times W + 8.29 \times B + 21 + 1.8 \times B \times C_L) \times f \times A$	μA

(2) V_{DD} = 2.0 ± 0.2 V

Condition	Expression (MAX.)	Unit
TYP.	$(0.0101 \times W + 3.65 \times B + 8 + 1.0 \times B \times C_L) \times f \times A$	μA
MAX.	$(0.0123 \times W + 4.38 \times B + 9 + 1.1 \times B \times C_L) \times f \times A$	μA

Note This operation rate is the ratio of the read operation to the total operation period (read, precharge, and macro off) of the ROM.

Example The operation rate is 60% (0.6) if read operations account for 60% of the total operation period of ROM.



Remark If all the input signals of this ROM are fixed, the current consumption in the standby mode (I_{DD1}) = 0.

8.7 Timing

8.7.1 Expressions

The timing values can be calculated by the following expressions (rounded at the third place below the decimal place).

The meanings of the symbols in the table below are as follows:
B: number of bits, W: number of words, C_L: external load capacitance (pF)

(1) V_{DD} = 3.3 ± 0.3 V

Read operation (T_A = –40 to +85°C)

Parameter	Symbol	Expression	Unit
Cycle time	t_{RC}	$t_{BEH} + t_{PC}$	ns
Access time	t_{ACC}	$5.09 + 5.66 \times 10^{-4} \times W + 9.85 \times 10^{-3} \times B + 3.39 \times 10^{-1} \times C_L$	ns
Output hold time	t_{OH}	0.65	ns
BE high-level time	t_{BEH}	$5.09 + 5.66 \times 10^{-4} \times W + 9.85 \times 10^{-3} \times B$	ns
Precharge time	t_{PC}	$3.17 + 3.41 \times 10^{-4} \times W + 6.13 \times 10^{-3} \times B$	ns
Address setup time	t_{AS}	1.40	ns
Address hold time	t_{AH}	0.60	ns
CSB setup time	t_{CS}	2.49	ns
CSB hold time	t_{CH}	1.50	ns
Output floating time	t_{HZ}	3.68	ns
Output active time	t_{LZ}	3.90	ns
DC output delay time	t_{DC}	$3.67 + 9.40 \times 10^{-1} \times C_L$	ns

(2) V_{DD} = 2.0 ± 0.2 V

Read operation (T_A = –40 to +85°C)

Parameter	Symbol	Expression	Unit
Cycle time	t_{RC}	$t_{BEH} + t_{PC}$	ns
Access time	t_{ACC}	$12.06 + 7.99 \times 10^{-4} \times W + 1.33 \times 10^{-2} \times B + 7.90 \times 10^{-1} \times C_L$	ns
Output hold time	t_{OH}	1.15	ns
BE high-level time	t_{BEH}	$12.06 + 7.99 \times 10^{-4} \times W + 1.33 \times 10^{-2} \times B$	ns
Precharge time	t_{PC}	$4.29 + 7.15 \times 10^{-4} \times W + 1.45 \times 10^{-2} \times B$	ns
Address setup time	t_{AS}	2.80	ns
Address hold time	t_{AH}	0.90	ns
CSB setup time	t_{CS}	4.21	ns
CSB hold time	t_{CH}	3.10	ns
Output floating time	t_{HZ}	7.36	ns
Output active time	t_{LZ}	8.11	ns
DC output delay time	t_{DC}	$7.68 + 1.34 \times C_L$	ns

8.7.2 Typical value (8 bits × 512 words)

(1) V_{DD} = 3.3 ± 0.3 V

Read operation (T_A = –40 to +85°C)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Cycle time	t_{RC}	8..86			ns
Access time	t_{ACC}			5.53	ns
Output hold time	t_{OH}	0.65			ns
BE high-level time	t_{BEH}	5.46			ns
Precharge time	t_{PC}	3.40			ns
Address setup time	t_{AS}	1.40			ns
Address hold time	t_{AH}	0.60			ns
CSB setup time	t_{CS}	2.49			ns
CSB hold time	t_{CH}	1.50			ns
Output floating time	t_{HZ}	3.68			ns
Output active time	t_{LZ}	3.90			ns
DC output delay time	t_{DC}			3.86	ns

(2) V_{DD} = 2.0 ± 0.2 V

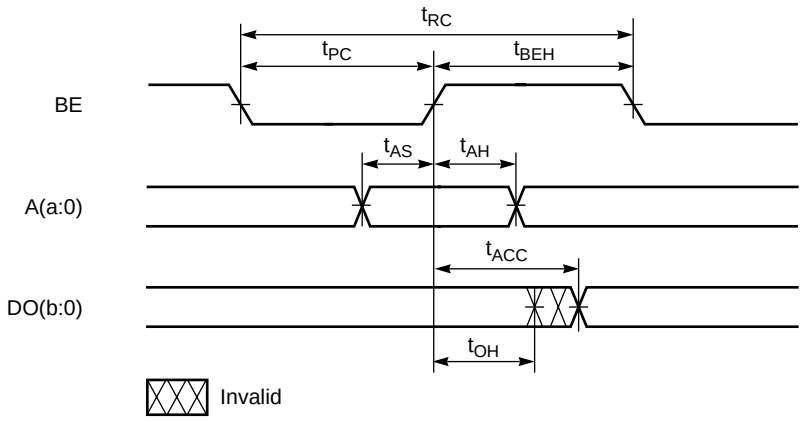
Read operation (T_A = –40 to +85°C)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Cycle time	t_{RC}	17.36			ns
Access time	t_{ACC}			12.74	ns
Output hold time	t_{OH}	1.15			ns
BE high-level time	t_{BEH}	12.58			ns
Precharge time	t_{PC}	4.78			ns
Address setup time	t_{AS}	2.80			ns
Address hold time	t_{AH}	0.90			ns
CSB setup time	t_{CS}	4.21			ns
CSB hold time	t_{CH}	3.10			ns
Output floating time	t_{HZ}	7.36			ns
Output active time	t_{LZ}	8.11			ns
DC output delay time	t_{DC}			7.95	ns

Remarks 1. The above values are calculated with an external load capacitance of 0.2 pF.
2. The meanings of the symbols in the above table are as follows:
MIN. : minimum value necessary for operating macro under worst condition
MAX. : delay time of macro output under worst condition

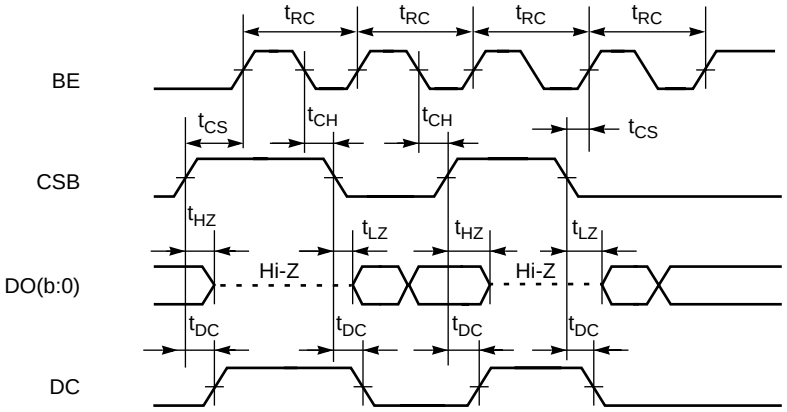
8.8 Timing Chart

(1) BE access (CSB = low level, OEB = low level)

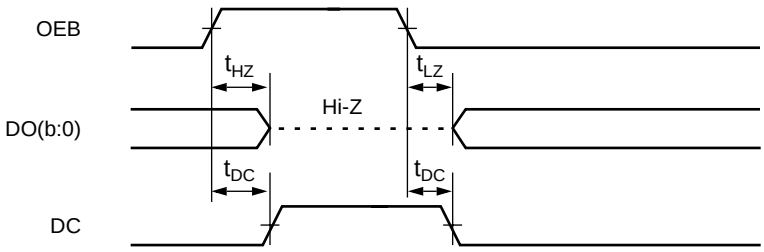


Remark When t_{RC} is MIN., operation at duty of 50 % is impossible.

(2) CSB control (OEB = low level)



(3) OEB control (CSB = low level)



CHAPTER 9 BIST

9.1 Overview

With the CB-9 family VX/VM type RAM, a macro test by connecting to a gate-array method BIST (Built-in Self Test) circuit can be performed.
BIST is a method of testing by which a test pattern is automatically generated inside a circuit. An external source can test the circuit simply by applying a test mode signal and test clock to the circuit. This method is effective for testing circuits with a regular structure, such as RAM circuits.
The BIST method has the following advantages over the conventional test bus method.

- Fewer test pins connected to external pins (only three pins: TIN, TEB, and TOUT). Therefore, the increase in delay caused by inserting a circuit, such as a selector, in the test output can be eliminated.
- Because a RAM test pattern is not necessary, the limit on the number of user patterns can be relaxed.
- Because a RAM test pattern is not necessary, the user can check RAM more easily.

For details of BIST, refer to **Design For Test User's Manual (A14357E)**.

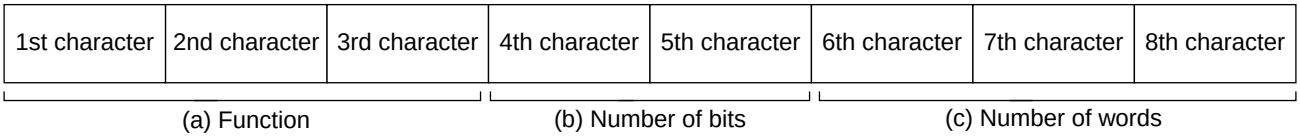
9.2 Type of BIST

The following BIST circuits are available for cell-based ICs:

- For single-port RAM (synchronous type)
- For dual-port (1R/W+1R) RAM (synchronous type)
- For dual-port (1R+1R) RAM (synchronous type)

9.2.1 Block name of BIST

The blocks of the BIST are named in compliance with a convention. Each character of the name has the following meaning:



(1) Function

The first through third characters indicate the variation of the BIST.

Characters	Function
D8U	For single-port RAM
DUU	For dual-port RAM (1R/W + 1R)
DBU	For dual-port RAM (1R + 1W)

(2) Number of bits

The fourth and fifth characters indicate the number of bits in base-32 number format. Therefore, the number of bits indicated by these characters ranges from 0 to 1023. For the correspondence between a base-32 number and the number of bits, refer to **(4) Correspondence with base-32 numbers**.

Number of bits = 4th character × 32 + 5th character

4	5	Number of bits	4	5	Number of bits
0	0	Missing number	0	G	16
0	1	1	0	H	17
0	2	2	0	I	Missing number
0	3	3	0	J	18
0	4	4	:	:	:
0	5	5	0	X	30
0	6	6	0	Y	31
0	7	7	0	Z	Missing number
0	8	8	1	0	32
0	9	9	1	1	33
0	A	10	1	2	34
0	B	11	:	:	:
0	C	12	Y	Y	1023
0	D	13	Y	Z	Missing number
0	E	14	Z	–	Missing number
0	F	15			

(3) Number of words

The sixth through eighth characters indicate the number of words in base-32 number format. Therefore, the number of words indicated by three characters ranges from 0 to 32767. For the correspondence between a base-32 number and the number of words, refer to **(4) Correspondence with base-32 numbers**.

Number of words = 6th character × 1024 + 7th character × 32 + 8th character

6	7	8	Number of Words	6	7	8	Number of Words
0	0	0	Missing number	0	0	J	18
0	0	1	1	:	:	:	:
0	0	2	2	0	0	X	30
0	0	3	3	0	0	Y	31
0	0	4	4	0	0	Z	Missing number
0	0	5	5	0	1	0	32
0	0	6	6	0	1	1	33
0	0	7	7	0	1	2	34
0	0	8	8	:	:	:	:
0	0	9	9	0	Y	Y	1023
0	0	A	10	0	Y	Z	Missing number
0	0	B	11	0	Z	–	Missing number
0	0	C	12	1	0	0	1024
0	0	D	13	:	:	:	
0	0	E	14	Y	Y	Y	32767
0	0	F	15	Y	Y	Z	Missing number
0	0	G	16	Y	Z	–	Missing number
0	0	H	17	Z	–	–	Missing number
0	0	I	Missing number				

(4) Correspondence with base-32 numbers

This table indicates the correspondence between base-32 numbers and the number of bits or words. The base-32 numbering system is an extension of the hexadecimal numbering system and uses 0 through 9 and alphabetic characters to indicate numbers 0 through 31. Note, however, that I, O, Q, and Z are not used in this numbering system.

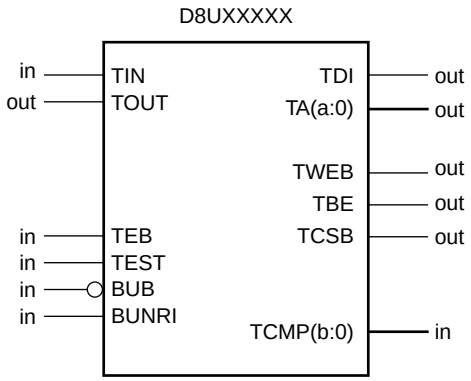
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F

16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
G	H	J	K	L	M	N	P	R	S	T	U	V	W	X	Y

9.3 BIST Circuit Specifications

9.3.1 Single-port RAM (synchronous type)

(1) Symbol diagram



(2) Pin function list

Pin Name/ Signal Name	Attribute	Function
TIN	I	Test input
TOUT	O	Test output
TEB	I	Test mode input
TEST	I	Test mode input
BUB	I	Backup mode input
BUNRI	I	Separation mode input
TDI	O	Test write data output
TA(a:0)	O	Test address output
TWEB	O	Test write enable output
TBE	O	Test clock output
TCSB	O	Test chip select output
TCMP(b:0)	I	Test comparator input

Remark The meanings of the symbols in the above table are as follows:
I: Input pin, O: Output pin
a = number of address lines – 1 (number of address lines = $\log_2$ number of words) rounded up at decimal point)
b = number of bits – 1

(3) Operation truth table

The meanings of the symbols in the following operation truth tables are as follows:

X : Undefined state not including high impedance
XZ : Undefined state including high impedance

BUB	BUNRI	TEST	TEB	TIN	TOUT	Output[Note 1]	Mode
0	XZ	XZ	XZ	XZ	X	X	Backup
1	0	X	X	X	X	X	Normal
1	1	0	X	X	X	X	Test (non-select)
1	1	1	1	X	X	X	Test (non-select)
1	1	1	0	0 or 1	0	X	Test (select, stop)
1	1	1	0	↗	OUT[Note 2]	Valid	Test (operation)

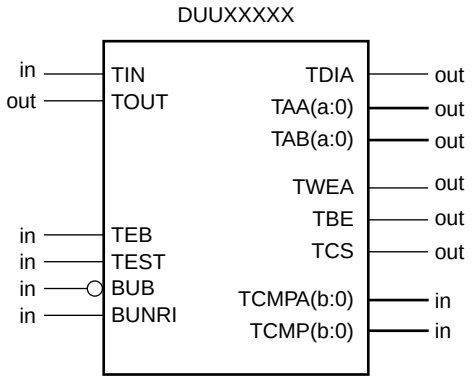
Notes 1. TDI, TA (a:0), TWEB, TBE, TCSB
2. If clock is input to TIN in the order of 1-0-1-0, TOUT is output in the order of 1-0-0-0.

(4) Macro size

2789 [grids]

9.3.2 Dual-port (1R/W + 1R) RAM (synchronous type)

(1) Symbol diagram



(2) Pin function list

Pin Name/ Signal Name	Attribute	Function
TIN	I	Test input
TOUT	O	Test output
TEB	I	Test mode input
TEST	I	Test mode input
BUB	I	Backup mode input
BUNRI	I	Separate mode input
TDIA	O	Test write data output (for A port)
TAA(a:0)	O	Test address output (for A port)
TAB(a:0)	O	Test address output (for B port)
TWEA	O	Test write enable output (for A port)
TBE	O	Test clock output (for both A and B ports)
TCS	O	Test chip select output (for both A and B ports)
TCMPA(b:0)	I	Test comparator input (for A port)
TCMPB(b:0)	I	Test comparator input (for B port)

Remark The meanings of the symbols in the above table are as follows:
I: Input pin, O: Output pin
a = number of address lines – 1 (number of address lines = $\log_2$ number of words) rounded up at decimal point)
b = number of bits – 1

(3) Operation truth table

The meanings of the symbols in the following operation truth tables are as follows:

X : Undefined state not including high impedance
XZ : Undefined state including high impedance

BUB	BUNRI	TEST	TEB	TIN	TOUT	Output[Note 1]	Mode
0	XZ	XZ	XZ	XZ	X	X	Backup
1	0	X	X	X	X	X	Normal
1	1	0	X	X	X	X	Test (non-select)
1	1	1	1	X	X	X	Test (non-select)
1	1	1	0	0 or 1	0	X	Test (select, stop)
1	1	1	0		OUT[Note 2]	Valid	Test (operation)

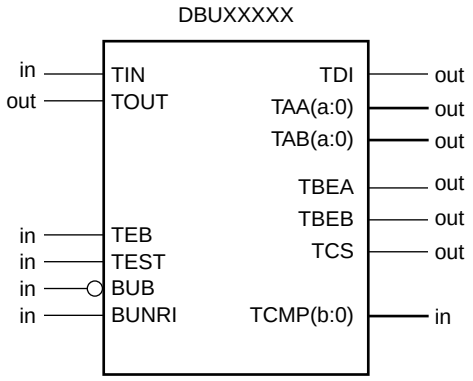
Notes 1. TDIA, TAA (a:0), TAB (a:0), TWEA, TBE, TCS
2. If clock is input to TIN in the order of 1-0-1-0, TOUT is output in the order of 1-0-0-0.

(4) Macro size

4286 [grids]

9.3.3 Dual-port (1R + 1W) RAM (synchronous type)

(1) Symbol diagram



(2) Pin function list

Pin Name/ Signal Name	Attribute	Function
TIN	I	Test input
TOUT	O	Test output
TEB	I	Test mode input
TEST	I	Test mode input
BUB	I	Backup mode input
BUNRI	I	Separate mode input
TDI	O	Test write data output (for A port)
TAA(a:0)	O	Test address output (for A port)
TAB(a:0)	O	Test address output (for B port)
TBEA	O	Test clock output (for A port)
TBEB	O	Test clock output (for B port)
TCS	O	Test chip select output (for both A and B ports)
TCMP(b:0)	I	Test comparator input (for B port)

Remark The meanings of the symbols in the above table are as follows:
I: Input pin, O: Output pin
a = number of address lines – 1 (number of address lines = $\log_2$ number of words) rounded up at decimal point)
b = number of bits – 1

(3) Operation truth table

The meanings of the symbols in the following operation truth tables are as follows:

X : Undefined state not including high impedance
XZ : Undefined state including high impedance

BUB	BUNRI	TEST	TEB	TIN	TOUT	Output[Note 1]	Mode
0	XZ	XZ	XZ	XZ	X	X	Backup
1	0	X	X	X	X	X	Normal
1	1	0	X	X	X	X	Test (non-select)
1	1	1	1	X	X	X	Test (non-select)
1	1	1	0	0 or 1	0	X	Test (select, stop)
1	1	1	0	↗	OUT[Note 2]	Valid	Test (operation)

Notes 1. TDI, TAA (a:0), TAB (a:0), TBEA, TBEB, TCS
2. If clock is input to TIN in the order of 1-0-1-0, TOUT is output in the order of 1-0-0-0.

(4) Macro size

2869 [grids]

APPENDIX A NUMBER OF GRIDS

Table A-1 High-Speed Single-Port RAM (Synchronous Type)

Unit: Grids

Number of Bits	Number of Grids	Number of Words (number of address lines)						
		32 (5)	**64 (6)**	**128 (7)**	**256 (8)**	**512 (9)**	**1024 (10)**	**2048 (11)**
1	X	275	280	286	292	298	305	311
	Y	33	38	43	52	72	110	186
	X × Y	9075	10640	12298	15184	21456	33550	57846
2	X	307	311	318	324	330	336	343
	Y	33	38	43	52	72	110	186
	X × Y	10131	11818	13674	16848	23760	36960	63798
4	X	370	375	381	387	394	400	406
	Y	33	38	43	52	72	110	186
	X × Y	12210	14250	16383	20124	28368	44000	75516
8	X	497	502	508	514	520	527	533
	Y	33	38	43	52	72	110	186
	X × Y	16401	19076	21844	26728	37440	57970	99138
16	X	751	756	762	768	774	781	787
	Y	33	38	43	52	72	110	186
	X × Y	24783	28728	32766	39936	55728	85910	146382
32	X	1286	1291	1297	1304	1310	1316	1322
	Y	33	38	43	52	72	110	186
	X × Y	42438	49058	55771	67808	94320	144760	245892

Remark Including macro circumferential wiring area

Table A-2 High-Speed Dual-Port (1R/W + 1R) RAM (Synchronous Type)

Unit: Grids

Number of Bits	Number of Grids	Number of Words (number of address lines)						
		32 (5)	**64 (6)**	**128 (7)**	**256 (8)**	**512 (9)**	**1024 (10)**	**2048 (11)**
1	X	304	332	388	501	726	1177	2078
	Y	35	36	36	37	38	38	39
	X × Y	10640	11952	13968	18537	27588	44726	81042
2	X	309	338	394	507	732	1182	2084
	Y	40	41	42	43	43	44	45
	X × Y	12360	13858	16548	21801	31476	52008	93780
4	X	330	358	415	527	753	1203	2104
	Y	52	52	53	54	54	55	56
	X × Y	17160	18616	21995	28458	40662	66165	117824
8	X	353	381	437	550	775	1225	2127
	Y	74	75	75	76	77	77	78
	X × Y	26122	28575	32775	41800	59675	94325	165906
16	X	416	444	501	613	839	1289	2190
	Y	119	119	120	121	121	122	123
	X × Y	49504	52836	60120	74173	101519	157258	269370
32	X	534	562	619	731	956	1407	2308
	Y	211	212	212	213	214	214	215
	X × Y	112674	119144	131228	155703	204584	301098	496220

Remark Including macro circumferential wiring area

Table A-3 High-Density Single-Port RAM (Synchronous Type)

Unit: Grids

Number of Bits	Number of Grids	Number of Words (number of address lines)								
		32 (5)	**64 (6)**	**128 (7)**	**256 (8)**	**512 (9)**	**1024 (10)**	**2048 (11)**	**4096 (12)**	**8192 (13)**
1	X	225	233	238	245	253	260	265	351	430
	Y	31	33	37	44	60	90	150	150	150
	X × Y	6975	7689	8806	10780	15180	23400	39750	52650	64500
2	X	252	260	264	272	280	287	292	405	537
	Y	31	33	37	44	60	90	150	151	150
	X × Y	7812	8580	9768	11968	16800	25830	43800	61155	80550
4	X	306	313	318	326	333	341	346	512	751
	Y	31	33	37	44	60	90	150	151	151
	X × Y	9486	10329	11766	14344	19980	30690	51900	77312	113401
8	X	416	423	428	436	441	448	453	726	1180
	Y	32	34	37	45	60	90	150	152	152
	X × Y	13312	14382	15836	19620	26460	40320	67950	110352	179360
16	X	633	641	646	653	658	665	670	1155	2038
	Y	32	34	38	45	60	91	151	154	153
	X × Y	20256	21794	24548	29385	39480	60515	101170	177870	311814
32	X	1062	1070	1075	1082	1087	1094	1099	2013	3754
	Y	32	34	38	45	60	91	151	157	156
	X × Y	33984	36380	40850	48690	65220	99554	165949	316041	585624

Remark Including macro circumferential wiring area

Table A-4 High-Density Dual-Port (1R + 1W) RAM (Synchronous Type)

Unit: Grids

Number of Bits	Number of Grids	Number of Words (number of address lines)					
		32 (5)	**64 (6)**	**128 (7)**	**256 (8)**	**512 (9)**	**1024 (10)**
1	X	344	355	367	379	390	402
	Y	34	37	42	52	73	114
	X × Y	11696	13135	15414	19708	28470	45828
2	X	394	406	417	429	441	452
	Y	34	37	42	52	73	114
	X × Y	13396	15022	17514	22308	32193	51528
4	X	495	506	518	530	541	553
	Y	34	37	42	52	73	114
	X × Y	16830	18722	21756	27560	39493	63042
8	X	696	708	719	731	743	775
	Y	34	37	42	52	73	114
	X × Y	23664	26196	30198	38012	54239	86070
16	X	1099	1111	1122	1134	1146	1157
	Y	34	37	42	52	73	114
	X × Y	37366	41107	47124	58968	83658	131898
32	X	1905	1916	1928	1940	1952	1963
	Y	34	37	42	52	73	114
	X × Y	64770	70892	80976	100880	142496	223782

Remark Including macro circumferential wiring area

Table A-5 Super High-Speed Single-Port RAM (Synchronous Type)

Unit: Grids

Number of Bits	Number of Grids	Number of Words (number of address lines)				
		64 (6)	**128 (7)**	**256 (8)**	**512 (9)**	**1024 (10)**
1	X	292	297	302	306	311
	Y	31	36	45	65	103
	X × Y	9052	10692	13590	19890	32033
2	X	330	335	340	344	349
	Y	31	36	45	65	103
	X × Y	10230	12060	15300	22360	35947
4	X	406	411	415	420	424
	Y	31	36	45	65	103
	X × Y	12586	14796	18675	27300	43672
8	X	558	562	567	571	576
	Y	31	36	45	65	103
	X × Y	17298	20232	25515	37115	59328
16	X	861	865	870	875	879
	Y	31	36	45	65	103
	X × Y	26691	31140	39150	56875	90537

Remark Including macro circumferential wiring area

Table A-6 Register File (Dual-Port)

Unit: Grids

Number of Bits	Number of Grids	Number of Words (number of address lines)						
		8 (3)	**16 (4)**	**32 (5)**	**64 (6)**	**128 (7)**	**256 (8)**	**512 (9)**
4	X	233	243	252	261	270	279	288
	Y	18	21	25	35	53	90	164
	X × Y	4194	5103	6300	9135	14310	25110	47232
8	X	315	324	334	343	352	361	370
	Y	18	21	25	35	53	90	164
	X × Y	5670	6804	8350	12005	18656	32490	60680
16	X	491	500	509	518	527	537	546
	Y	19	22	26	36	54	91	166
	X × Y	9329	11000	13234	18648	28458	48867	90636
32	X	833	842	852	861	870	879	888
	Y	21	23	28	37	56	93	167
	X × Y	17493	19366	23856	31857	48720	81747	148296
64	X	1503	1513	1522	1531	1540	1549	1558
	Y	22	25	29	39	57	94	169
	X × Y	33066	37825	44138	59709	87780	145606	263302

Remark Including macro circumferential wiring area

★ **Table A-7 High-Speed ROM (Synchronous Type)**

Unit: Grids

Number of Bits	Number of Grids	Number of Words (number of address lines)							
		64 (6)	128 (7)	256 (8)	512 (9)	1024 (10)	2048 (11)	4096 (12)	8192 (13)
1	X	279	287	294	302	309	317	324	332
	Y	30	32	36	42	56	83	137	246
	X × Y	8370	9184	10584	12684	17304	26311	44388	81672
2	X	290	298	305	313	320	328	335	343
	Y	30	32	36	42	56	83	137	246
	X × Y	8700	9536	10980	13146	17920	27224	45895	83378
4	X	311	319	326	334	341	349	357	364
	Y	30	32	36	42	56	83	137	246
	X × Y	9330	10208	11736	14028	19096	28967	48909	89544
8	X	354	362	369	375	384	392	399	407
	Y	30	32	36	42	56	83	137	246
	X × Y	10620	11584	13284	15834	21504	32536	54663	100122
16	X	439	447	455	462	470	477	485	492
	Y	30	32	36	42	56	83	137	246
	X × Y	13170	14304	16380	19404	26320	39591	66445	121032
32	X	610	618	625	633	640	648	655	663
	Y	30	32	36	42	56	83	137	246
	X × Y	18300	19776	22500	26586	35840	53784	89735	163098
64	X	964	971	979	986	994	1001	1009	1016
	Y	32	33	37	44	57	84	138	247
	X × Y	30848	32043	36223	43384	56658	84084	139242	250952

Remark Including macro circumferential wiring area

APPENDIX B OPERATING CURRENT CONSUMPTION LIST

The conditions are as follows:
External load capacitance (C_L): 0.2 pF MAX.
Operation rate: 100%

(1) V_{DD} = 3.3 ± 0.3 V (read/write operation)

Table B-1 High-Speed Single-Port RAM (Synchronous Type)

Unit: μA

Number of Bits	Number of Words (number of address lines)						
	32 (5)	64 (6)	128 (7)	256 (8)	512 (9)	1024 (10)	2048 (11)
1	654	690	735	797	898	1085	1452
2	1104	1160	1229	1327	1488	1787	2378
4	1385	1428	1488	1579	1738	2039	2638
8	2359	2412	2491	2620	2857	3312	4220
16	4308	4381	4498	4704	5095	5859	7384
32	8206	8317	8511	8872	9571	10952	13711

Remark Operating frequency: 20 MHz (read operating frequency: 10 MHz, write operating frequency: 10 MHz)

Table B-2 High-Speed Dual-Port (1R/W + 1R) RAM (Synchronous Type)

Unit: μA

Number of Bits	Number of Words (number of address lines)						
	32 (5)	64 (6)	128 (7)	256 (8)	512 (9)	1024 (10)	2048 (11)
1	1330	1407	1491	1585	1708	1891	2203
2	1842	1920	2009	2112	2251	2464	2841
4	2867	2949	3044	3166	3335	3613	4120
8	4916	5008	5118	5271	5505	5912	6678
16	9015	9121	9266	9483	9847	10513	11790
32	17211	17352	17558	17905	18527	19708	22014

Remark Operating frequency: 20 MHz
(read/write port ..... read operating frequency: 10 MHz, write operating frequency: 10 MHz,
read port ..... read operating frequency: 20 MHz)

Table B-3 High-Density Single-Port RAM (Synchronous Type)

Unit: μA

Number of Bits	Number of Words (number of address lines)								
	32 (5)	64 (6)	128 (7)	256 (8)	512 (9)	1024 (10)	2048 (11)	4096 (12)	8192 (13)
1	1279	1297	1334	1408	1545	1820	2370	3329	2990
2	1443	1452	1491	1568	1721	2018	2632	3753	3670
4	1732	1753	1794	1887	2073	2434	3168	4609	5030
8	2329	2353	2420	2535	2776	3257	4228	6323	7749
16	3513	3563	3653	3832	4192	4911	6359	9750	13198
32	5901	5973	6118	6416	7024	8220	10611	16604	24096

Remark Operating frequency: 20 MHz (read operating frequency: 10 MHz, write operating frequency: 10 MHz)

Table B-4 High-Density Dual-Port (1R + 1W) RAM (Synchronous Type)

Unit: μA

Number of Bits	Number of Words (number of address lines)					
	32 (5)	64 (6)	128 (7)	256 (8)	512 (9)	1024 (10)
1	595	662	718	800	932	1173
2	782	855	923	1029	1212	1553
4	1165	1249	1343	1499	1782	2321
8	1963	2073	2217	2472	2954	3892
16	3702	3862	4105	4560	5438	7173
32	7738	7997	8439	9292	10968	14294

Remark Operating frequency: 20 MHz
(read port..... read operating frequency: 20 MHz,
write port..... write operating frequency: 20 MHz)

Table B-5 Super High-Speed Single-Port RAM (Synchronous Type)

Unit: μA

Number of Bits	Number of Words (number of address lines)				
	64 (6)	128 (7)	256 (8)	512 (9)	1024 (10)
1	2650	2738	2902	3216	3844
2	4820	4916	5094	5438	6126
4	9160	9272	9478	9882	10690
8	17842	17982	18248	18772	19816
16	35204	35404	35788	36548	38068

Remark Operating frequency: 20 MHz (read operating frequency: 10 MHz, write operating frequency: 10 MHz)

Table B-6 Register File (Dual-Port)

Unit: μA

Number of Bits	Number of Words (number of address lines)						
	8 (3)	16 (4)	32 (5)	64 (6)	128 (7)	256 (8)	512 (9)
4	316	370	476	690	1118	1974	3684
8	594	648	754	968	1396	2250	3960
16	1149	1202	1309	1523	1950	2805	4515
32	2258	2312	2418	2632	3060	3914	5624
64	4476	4530	4636	4850	5278	6133	7843

Remark Operating frequency: 10 MHz

Table B-7 High-Speed ROM (Synchronous Type)

Unit: μA

Number of Bits	Number of Words (number of address lines)							
	64 (6)	128 (7)	256 (8)	512 (9)	1024 (10)	2048 (11)	4096 (12)	8192 (13)
1	624	654	714	834	1075	1556	2519	4444
2	797	827	887	1007	1248	1729	2692	4617
4	1143	1173	1233	1353	1594	2075	3038	4963
8	1835	1865	1925	2045	2286	2767	3730	5655
16	3219	3249	3309	3429	3670	4151	5114	7039
32	5987	6017	6077	6197	6438	6919	7882	9807
64	11523	11553	11613	11733	11974	12455	13418	15343

Remark Operating frequency: 20 MHz

(2) V_{DD} = 2.0 ± 0.2 V (read/write operation)

Table B-8 High-Speed Single-Port RAM (Synchronous Type)

Unit: μA

Number of Bits	Number of Words (number of address lines)						
	32 (5)	64 (6)	128 (7)	256 (8)	512 (9)	1024 (10)	2048 (11)
1	379	401	427	462	521	628	842
2	521	543	572	613	683	812	1070
4	802	828	862	915	1007	1181	1528
8	1367	1397	1443	1518	1655	1919	2443
16	2494	2537	2604	2723	2950	3392	4275
32	4750	4814	4927	5136	5541	6340	7937

Remark Operating frequency: 20 MHz (read operating frequency: 10 MHz, write operating frequency: 10 MHz)

Table B-9 High-Density Single-Port RAM (Synchronous Type)

Unit: μA

Number of Bits	Number of Words (number of address lines)								
	32 (5)	64 (6)	128 (7)	256 (8)	512 (9)	1024 (10)	2048 (11)	4096 (12)	8192 (13)
1	739	754	773	801	878	1021	1306	1258	1674
2	953	958	978	1018	1098	1249	1560	1610	2085
4	1360	1376	1398	1442	1530	1705	2067	2322	2886
8	2194	2202	2238	2289	2402	2628	3070	3757	4507
16	3843	3865	3908	3985	4148	4464	5098	6606	7730
32	7160	7189	7248	7375	7629	8137	9142	12315	14186

Remark Operating frequency: 20 MHz (read operating frequency: 10 MHz, write operating frequency: 10 MHz)

Table B-10 High-Density Dual-Port (1R + 1W) RAM (Synchronous Type)

Unit: μA

Number of Bits	Number of Words (number of address lines)					
	32 (5)	64 (6)	128 (7)	256 (8)	512 (9)	1024 (10)
1	294	325	355	400	475	616
2	390	425	463	524	632	837
4	582	625	680	773	946	1280
8	966	1025	1112	1270	1573	2168
16	1731	1823	1975	2263	2825	3939
32	3258	3413	3696	4243	5325	7478

Remark Operating frequency: 20 MHz

Table B-11 Register File (Dual-Port)

Unit: μA

Number of Bits	Number of Words (number of address lines)						
	8 (3)	16 (4)	32 (5)	64 (6)	128 (7)	256 (8)	512 (9)
4	212	246	313	446	713	1247	2314
8	407	440	508	640	908	1441	2509
16	796	829	897	1030	1297	1830	2898
32	1575	1608	1675	1808	2075	2609	3676
64	3131	3165	3231	3365	3631	4166	5233

Remark Operating frequency: 10 MHz

Table B-12 High-Speed ROM (Synchronous Type)

Unit: μA

Number of Bits	Number of Words (number of address lines)							
	64 (6)	128 (7)	256 (8)	512 (9)	1024 (10)	2048 (11)	4096 (12)	8192 (13)
1	288	304	335	398	524	776	1280	2288
2	380	396	427	490	616	868	1372	2380
4	564	580	611	674	800	1052	1556	2564
8	932	948	979	1042	1168	1420	1924	2932
16	1668	1684	1715	1778	1904	2156	2660	3668
32	3140	3156	3187	3250	3376	3628	4132	5140
64	6084	6100	6131	6194	6320	6572	7076	8084

Remark Operating frequency: 20 MHz

APPENDIX C ACCESS TIME (t_{ACC}) LIST

The conditions are as follows:
External load capacitance (C_L): 0.2 pF

(1) V_{DD} = 3.3 ± 0.3 V (T_A = –40 to +85°C)

Table C-1 High-Speed Single-Port RAM (Synchronous Type)

Unit: ns

Number of Bits	Number of Words (number of address lines)						
	32 (5)	64 (6)	128 (7)	256 (8)	512 (9)	1024 (10)	2048 (11)
1	3.22	3.24	3.27	3.33	3.46	3.71	4.22
2	3.25	3.27	3.30	3.36	3.49	3.74	4.25
4	3.32	3.33	3.36	3.43	3.55	3.81	4.31
8	3.45	3.46	3.49	3.56	3.68	3.94	4.44
16	3.70	3.72	3.75	3.81	3.94	4.19	4.70
32	4.22	4.23	4.26	4.33	4.45	4.71	5.21

Table C-2 High-Speed Dual-Port (1R/W + 1R) RAM (Synchronous Type)

Unit: ns

Number of Bits	Number of Words (number of address lines)						
	32 (5)	64 (6)	128 (7)	256 (8)	512 (9)	1024 (10)	2048 (11)
1	3.26	3.29	3.34	3.44	3.65	3.98	4.64
2	3.27	3.30	3.36	3.46	3.67	4.01	4.69
4	3.31	3.33	3.39	3.50	3.71	4.07	4.78
8	3.37	3.40	3.46	3.58	3.80	4.19	4.97
16	3.49	3.53	3.59	3.73	3.96	4.42	5.33
32	3.74	3.78	3.87	4.04	4.30	4.89	6.07

Table C-3 High-Density Single-Port RAM (Synchronous Type)

Unit: ns

Number of Bits	Number of Words (number of address lines)								
	32 (5)	64 (6)	128 (7)	256 (8)	512 (9)	1024 (10)	2048 (11)	4096 (12)	8192 (13)
1	7.07	7.12	7.20	7.37	7.71	8.40	9.76	12.09	12.36
2	7.12	7.17	7.25	7.42	7.76	8.45	9.81	12.15	12.47
4	7.22	7.26	7.35	7.52	7.86	8.55	9.92	12.27	12.68
8	7.41	7.46	7.54	7.72	8.06	8.75	10.12	12.51	13.10
16	7.80	7.85	7.93	8.11	8.46	9.15	10.54	12.99	13.94
32	8.58	8.63	8.72	8.89	9.25	9.96	11.37	13.94	15.63

Table C-4 High-Density Dual-Port (1R + 1W) RAM (Synchronous Type)

Unit: ns

Number of Bits	Number of Words (number of address lines)					
	32 (5)	64 (6)	128 (7)	256 (8)	512 (9)	1024 (10)
1	4.97	5.12	5.41	6.00	7.19	9.55
2	5.01	5.15	5.45	6.04	7.22	9.59
4	5.08	5.23	5.52	6.12	7.30	9.66
8	5.23	5.38	5.67	6.26	7.45	9.81
16	5.53	5.67	5.97	6.56	7.74	10.11
32	6.12	6.27	6.56	7.15	8.34	10.70

Table C-5 Super High-Speed Single-Port RAM (Synchronous Type)

Unit: ns

Number of Bits	Number of Words (number of address lines)				
	64 (6)	128 (7)	256 (8)	512 (9)	1024 (10)
1	2.45	2.51	2.63	2.87	3.35
2	2.46	2.52	2.64	2.88	3.36
4	2.49	2.55	2.67	2.91	3.40
8	2.56	2.62	2.74	2.98	3.46
16	2.69	2.75	2.87	3.11	3.59

Table C-6 Register File (Dual-Port)

Unit: ns

Number of Bits	Number of Words (number of address lines)						
	8 (3)	16 (4)	32 (5)	64 (6)	128 (7)	256 (8)	512 (9)
4	4.28	4.51	4.96	5.87	7.68	11.30	18.55
8	4.36	4.59	5.04	5.95	7.76	11.38	18.63
16	4.52	4.75	5.20	6.11	7.92	11.55	18.79
32	4.85	5.07	5.53	6.43	8.25	11.87	19.12
64	5.49	5.72	6.17	7.08	8.89	12.52	19.76

Table C-7 High-Speed ROM (Synchronous Type)

Unit: ns

Number of Bits	Number of Words (number of address lines)							
	64 (6)	128 (7)	256 (8)	512 (9)	1024 (10)	2048 (11)	4096 (12)	8192 (13)
1	5.21	5.25	5.32	5.46	5.75	6.33	7.49	9.81
2	5.22	5.25	5.33	5.47	5.76	6.34	7.50	9.82
4	5.24	5.27	5.35	5.49	5.78	6.36	7.52	9.84
8	5.28	5.31	5.39	5.53	5.82	6.40	7.56	9.88
16	5.36	5.39	5.47	5.61	5.90	6.48	7.64	9.96
32	5.51	5.55	5.62	5.77	6.06	6.64	7.80	10.11
64	5.83	5.87	5.94	6.08	6.37	6.95	8.11	10.43

(2) V_{DD} = 2.0 ± 0.2 V (T_A = –40 to +85°C)

Table C-8 High-Speed Single-Port RAM (Synchronous Type)

Unit: ns

Number of Bits	Number of Words (number of address lines)						
	32 (5)	64 (6)	128 (7)	256 (8)	512 (9)	1024 (10)	2048 (11)
1	7.08	7.13	7.23	7.45	7.87	8.72	10.42
2	7.13	7.18	7.29	7.50	7.92	8.77	10.47
4	7.23	7.29	7.39	7.60	8.03	8.88	10.58
8	7.44	7.49	7.60	7.81	8.24	9.09	10.79
16	7.86	7.91	8.02	8.23	8.66	9.51	11.21
32	8.70	8.75	8.86	9.07	9.49	10.34	12.04

Table C-9 High-Density Single-Port RAM (Synchronous Type)

Unit: ns

Number of Bits	Number of Words (number of address lines)								
	32 (5)	64 (6)	128 (7)	256 (8)	512 (9)	1024 (10)	2048 (11)	4096 (12)	8192 (13)
1	15.61	15.69	15.87	16.22	16.91	18.31	21.09	27.04	27.58
2	15.72	15.81	15.99	16.34	17.04	18.44	21.23	27.16	27.78
4	15.96	16.05	16.22	16.58	17.28	18.69	21.51	27.42	28.18
8	16.43	16.52	16.70	17.06	17.77	19.21	22.07	27.94	28.99
16	17.37	17.46	17.65	18.02	18.76	20.24	23.20	28.96	30.61
32	19.25	19.34	19.54	19.93	20.72	22.29	25.44	31.02	33.84

Table C-10 High-Density Dual-Port (1R + 1W) RAM (Synchronous Type)

Unit: ns

Number of Bits	Number of Words (number of address lines)					
	32 (5)	64 (6)	128 (7)	256 (8)	512 (9)	1024 (10)
1	12.61	13.02	13.83	15.46	18.71	25.21
2	12.66	13.07	13.88	15.51	18.76	25.26
4	12.77	13.18	13.99	15.61	18.87	25.37
8	12.98	13.39	14.20	15.82	19.08	25.58
16	13.40	13.81	14.62	16.24	19.50	26.00
32	14.24	14.65	15.46	17.08	20.34	26.84

Table C-11 Register File (Dual-Port)

Unit: ns

Number of Bits	Number of Words (number of address lines)						
	8 (3)	16 (4)	32 (5)	64 (6)	128 (7)	256 (8)	512 (9)
4	9.42	9.92	10.94	12.96	17.00	25.10	41.28
8	9.65	10.16	11.17	13.19	17.24	25.33	41.51
16	10.12	10.62	11.63	13.66	17.70	25.79	41.98
32	11.05	11.55	12.56	14.59	18.63	26.73	42.91
64	12.91	13.42	14.43	16.45	20.50	28.59	44.77

Table C-12 High-Speed ROM (Synchronous Type)

Unit: ns

Number of Bits	Number of Words (number of address lines)							
	64 (6)	128 (7)	256 (8)	512 (9)	1024 (10)	2048 (11)	4096 (12)	8192 (13)
1	12.29	12.34	12.44	12.65	13.05	13.87	15.51	18.78
2	12.30	12.35	12.45	12.66	13.07	13.89	15.52	18.80
4	12.33	12.38	12.48	12.69	13.09	13.91	15.55	18.82
8	12.38	12.43	12.53	12.74	13.15	13.97	15.60	18.87
16	12.49	12.54	12.64	12.84	13.25	14.07	15.71	18.98
32	12.70	12.75	12.85	13.06	13.47	14.28	15.92	19.19
64	13.13	13.18	13.28	13.48	13.89	14.71	16.35	19.62

APPENDIX D CYCLE TIME (t_{RC}) LIST

The conditions are as follows:
External load capacitance (C_L): 0.2 pF

(1) V_{DD} = 3.3 ± 0.3 V (T_A = –40 to +85°C)

Table D-1 High-Speed Single-Port RAM (Synchronous Type)

Unit: ns

Number of Bits	Number of Words (number of address lines)						
	32 (5)	64 (6)	128 (7)	256 (8)	512 (9)	1024 (10)	2048 (11)
1	5.44	5.46	5.52	5.62	5.80	6.20	7.20
2	5.50	5.52	5.58	5.68	5.88	6.26	7.30
4	5.64	5.66	5.70	5.80	6.00	6.44	7.50
8	5.88	5.92	5.96	6.06	6.32	6.84	7.90
16	6.62	6.64	6.72	6.84	7.10	7.64	8.68
32	8.20	8.24	8.30	8.44	8.70	9.22	10.28

Table D-2 High-Speed Dual-Port (1R/W + 1R) RAM (Synchronous Type)

Unit: ns

Number of Bits	Number of Words (number of address lines)						
	32 (5)	64 (6)	128 (7)	256 (8)	512 (9)	1024 (10)	2048 (11)
1	6.40	6.44	6.54	6.76	7.18	7.84	9.16
2	6.42	6.48	6.58	6.80	7.22	7.90	9.26
4	6.48	6.54	6.66	6.88	7.30	8.02	9.44
8	6.60	6.66	6.78	7.02	7.46	8.24	9.80
16	6.86	6.92	7.06	7.34	7.80	8.72	10.54
32	7.36	7.44	7.60	7.94	8.46	9.64	12.00

Table D-3 High-Density Single-Port RAM (Synchronous Type)

Unit: ns

Number of Bits	Number of Words (number of address lines)								
	32 (5)	64 (6)	128 (7)	256 (8)	512 (9)	1024 (10)	2048 (11)	4096 (12)	8192 (13)
1	7.07	7.12	7.25	7.74	8.70	10.65	14.54	16.49	17.38
2	7.12	7.17	7.31	7.80	8.77	10.72	14.60	16.55	17.47
4	7.22	7.26	7.44	7.92	8.89	10.83	14.71	16.68	17.62
8	7.41	7.46	7.69	8.17	9.14	11.08	14.94	16.93	17.95
16	7.83	7.95	8.19	8.67	9.63	11.55	15.40	17.44	18.61
32	8.83	8.96	9.19	9.67	10.62	12.53	16.33	18.44	19.91

Table D-4 High-Density Dual-Port (1R + 1W) RAM (Synchronous Type)

Unit: ns

Number of Bits	Number of Words (number of address lines)					
	32 (5)	64 (6)	128 (7)	256 (8)	512 (9)	1024 (10)
1	9.14	9.44	10.02	11.20	13.58	18.30
2	9.22	9.50	10.10	11.28	13.64	18.38
4	9.36	9.66	10.24	11.44	13.80	18.52
8	9.66	9.96	10.54	11.72	14.10	18.82
16	10.26	10.54	11.14	12.32	14.68	19.42
32	11.44	11.74	12.32	13.50	15.88	20.60

Table D-5 Super High-Speed Single-Port RAM (Synchronous Type)

Unit: ns

Number of Bits	Number of Words (number of address lines)				
	64 (6)	128 (7)	256 (8)	512 (9)	1024 (10)
1	2.96	3.08	3.30	3.76	4.68
2	2.98	3.10	3.34	3.78	4.70
4	3.06	3.16	3.40	3.86	4.76
8	3.18	3.30	3.52	3.98	4.90
16	3.44	3.56	3.78	4.24	5.16

Table D-6 Register File (Dual-Port)

Unit: ns

Number of Bits	Number of Words (number of address lines)						
	8 (3)	16 (4)	32 (5)	64 (6)	128 (7)	256 (8)	512 (9)
4	4.21	4.44	4.89	5.80	7.61	11.23	18.48
8	4.29	4.52	4.97	5.88	7.69	11.31	18.56
16	4.45	4.68	5.13	6.04	7.85	11.47	18.72
32	4.78	5.00	5.46	6.36	8.17	11.80	19.05
64	5.42	5.65	6.10	7.01	8.82	12.44	19.69

Table D-7 High-Speed ROM (Synchronous Type)

Unit: ns

Number of Bits	Number of Words (number of address lines)							
	64 (6)	128 (7)	256 (8)	512 (9)	1024 (10)	2048 (11)	4096 (12)	8192 (13)
1	8.34	8.40	8.52	8.75	9.21	10.14	12.00	15.71
2	8.36	8.42	8.53	8.76	9.23	10.16	12.01	15.73
4	8.39	8.45	8.57	8.79	9.26	10.19	12.05	15.76
8	8.46	8.52	8.63	8.86	9.32	10.25	12.11	15.83
16	8.58	8.65	8.76	8.99	9.45	10.38	12.24	15.96
32	8.84	8.89	9.02	9.25	9.71	10.64	12.50	16.21
64	9.35	9.41	9.52	9.76	10.22	11.15	13.00	16.72

(2) V_{DD} = 2.0 ± 0.2 V (T_A = –40 to +85°C)

Table D-8 High-Speed Single-Port RAM (Synchronous Type)

Unit: ns

Number of Bits	Number of Words (number of address lines)						
	32 (5)	64 (6)	128 (7)	256 (8)	512 (9)	1024 (10)	2048 (11)
1	12.16	12.26	12.46	12.86	13.66	15.26	18.48
2	12.26	12.36	12.56	12.96	13.76	15.38	18.58
4	12.46	12.56	12.78	13.18	13.98	15.58	18.80
8	12.88	12.98	13.18	13.60	14.40	16.00	19.22
16	13.72	13.82	14.02	14.42	15.24	16.84	20.06
32	15.70	15.76	15.88	16.10	16.90	18.52	21.72

Table D-9 High-Density Single-Port RAM (Synchronous Type)

Unit: ns

Number of Bits	Number of Words (number of address lines)								
	32 (5)	64 (6)	128 (7)	256 (8)	512 (9)	1024 (10)	2048 (11)	4096 (12)	8192 (13)
1	15.61	15.69	15.87	16.47	18.27	21.87	29.09	34.51	36.22
2	15.72	15.81	15.99	16.60	18.41	22.02	29.26	34.64	36.36
4	15.96	16.05	16.22	16.86	18.68	22.32	29.59	34.88	36.64
8	16.43	16.52	16.70	17.38	19.22	22.90	30.26	35.39	37.21
16	17.37	17.46	17.65	18.42	20.30	24.08	31.62	36.39	38.34
32	19.25	19.34	19.54	20.50	22.48	26.43	34.31	38.39	40.60

Table D-10 High-Density Dual-Port (1R + 1W) RAM (Synchronous Type)

Unit: ns

Number of Bits	Number of Words (number of address lines)					
	32 (5)	64 (6)	128 (7)	256 (8)	512 (9)	1024 (10)
1	23.26	24.08	25.70	28.96	35.46	48.46
2	23.38	24.18	25.82	29.06	35.56	48.56
4	23.58	24.40	26.02	29.28	35.78	48.78
8	24.00	24.82	26.44	29.70	36.20	49.20
16	24.84	25.66	27.28	30.54	37.04	50.04
32	26.52	27.34	28.96	32.22	38.72	51.72

Table D-11 Register File (Dual-Port)

Unit: ns

Number of Bits	Number of Words (number of address lines)						
	8 (3)	16 (4)	32 (5)	64 (6)	128 (7)	256 (8)	512 (9)
4	9.27	9.78	10.79	12.81	16.86	24.95	41.13
8	9.50	10.01	11.02	13.04	17.09	25.18	41.37
16	9.97	10.48	11.49	13.51	17.56	25.65	41.83
32	10.90	11.41	12.42	14.44	18.49	26.58	42.76
64	12.76	13.27	14.28	16.30	20.35	28.44	44.63

Table D-12 High-Speed ROM (Synchronous Type)

Unit: ns

Number of Bits	Number of Words (number of address lines)							
	64 (6)	128 (7)	256 (8)	512 (9)	1024 (10)	2048 (11)	4096 (12)	8192 (13)
1	16.49	16.58	16.77	17.17	17.94	19.48	22.59	28.79
2	16.51	16.61	16.81	17.19	17.97	19.52	22.61	28.82
4	16.57	16.66	16.86	17.25	18.03	19.57	22.67	28.87
8	16.68	16.77	16.97	17.36	18.13	19.69	22.78	28.99
16	16.90	17.00	17.19	17.58	18.36	19.90	23.01	29.20
32	17.34	17.44	17.64	18.03	18.80	20.35	23.45	29.66
64	18.24	18.33	18.53	18.92	19.69	21.24	24.34	30.54

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