NEC
NEC Electronics Inc.

μPD9305
MEMORY ACCESS AND GENERAL BUS INTERFACE FOR THE μPD7281

Description

The NEC μPD9305 memory access and general bus interface chip (MAGIC) is a peripheral LSI support device for the μPD7281 image pipelined processor (ImPP). The μPD7281 is a data flow architecture processor that supports high speed image and signal processing applications. The μPD9305 chip can support from one to eight μPD7281s and also interfaces to both 8-bit and 16-bit host processors.

The μPD9305's powerful interface capabilities allow it to support basic interface operations, object program load, read/write/modify operations on image memory, and multiple μPD7281 image memory accesses.

Since the μPD7281 ImPP does not use direct addressing, the memories in a μPD7281 processor system can be seen as processing modules with unique module numbers. These separate modules must output memory access tokens containing their own unique address, data, and control signals. The modules must perform the necessary processing, and then output the result of the access as another memory access token. To do this, the multiple μPD7281 modules require external circuitry to process the memory access tokens that they output. In addition, this same circuitry is required to organize the data output from the memory into token format.

Circuitry is also needed between the host processor and the μPD7281s to organize the data from the host into token format and to return the data output from the μPD7281s into the form required by the host processor. Finally, tokens may have to be returned to other μPD7281s in token form for further processing.

The μPD9305 simplifies the above operations by keeping the data in the most convenient form. The μPD9305 replaces approximately 80 medium/small scale integrated devices with a single integrated circuit.

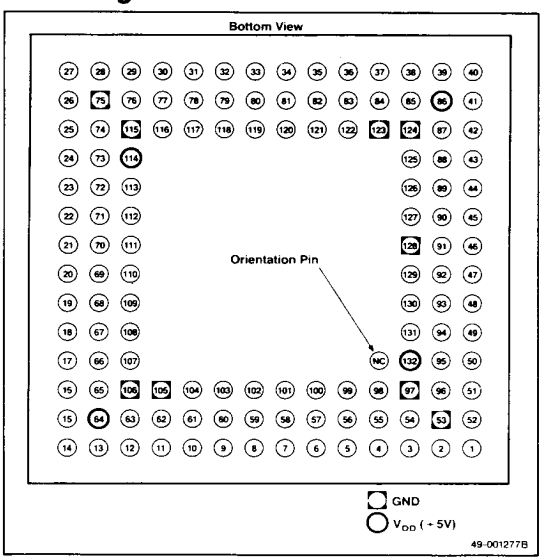
Features

- ☐ High performance image memory interface
- ☐ Reduces external circuits required for ImPP system
- ☐ Simplifies host interface
- ☐ Up to 24-bit image memory addressing
- ☐ Up to 18-bit image memory data
- ☐ Register file for memory access
- ☐ Refresh control of image memory
- ☐ Functions with separate DMA controller
- ☐ Single +5 V power supply
- ☐ CMOS technology for lower power consumption

Ordering Information

Part Number	Package Type
μPD9305R	132-pin ceramic grid array

Pin Configuration



Pin Identification

No.	Symbol	Function
1	CLK	Clock input
2-4	D_{10},D_{12}, D_{15}	Bidirectional data bus bits
5	$\overline{OACK}$	Output acknowledge input
6	$\overline{OREQ}$	Output request output
7	IDB_{14}	Input data bus bit
8	ODB_{14}	Output data bus bit
9	IDB_{11}	Input data bus bit
10, 11	ODB_{11}, ODB_8	Output data bus bits
12	IDB_9	Input data bus bit
13	ODB_5	Output data bus bit
14	IDB_8	Input data bus bit
15	ODB_4	Output data bus bit
16	IDB_7	Input data bus bit
17	ODB_2	Output data bus bit

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Pin Identification (Cont)

No.	Symbol	Function
18	IDB_6	Input data bus bit
19	MN_2	Module number output
20	IDB_4	Input data bus bit
21	IMA_{22}	Image memory address output bit
22	IDB_2	Input data bus bit
23, 24	IMA_{18}, IMA_{15}	Image memory address output bits
25	IDB_0	Input data bus bit
26-28	IMA_{12}-IMA_{10}	Image memory address output bits
29	SOLBSY	Self object load busy output
30	CPURQ	CPU request output
31	DMAAEN	DMA address enable input
32-34	IMA_5,IMA_2, IMA_0	Image memory address output bits
35	$\overline{DMAAK1}$	DMA / 1 acknowledge input
36	$\overline{DMARQ1}$	DMA / 1 request output
37	IMD_{13}	Bidirectional image memory data bus bit
38	$\overline{IMAK}$	Image memory acknowledge input
39-42	IMD_{10}-IMD_7	Bidirectional image memory data bus bits
43	A_0	Address select input
44,45	IMD_3,IMD_1	Bidirectional image memory data bus bits
46	IMWR	Image memory write output
47	$\overline{WR}$	Write input
48,49	D_2,D_5	Bidirectional data bus bits
50	$\overline{CS}$	Chip select input
51,52	D_8,D_9	Bidirectional data bus bits
53	GND	Ground
54,55	D_{11},D_{14}	Bidirectional data bus bits
56	$\overline{IREQ}$	Input request input
57	$\overline{IACK}$	Input acknowledge output
58	IDB_{13}	Input data bus bit
59	ODB_{13}	Output data bus bit
60	IDB_{10}	Input data bus bit
61-63	ODB_{10},ODB_7, ODB_6	Output data bus bits
64	V_{DD}	+5 V power supply
65,66	ODB_3,ODB_1	Output data bus bits
67	IDB_5	Input data bus bit
68	MN_1	Module number output bit

Pin Indentification (Cont)

No.	Symbol	Function
69,70	IMA_{23},IMA_{21}	Image memory address output bits
71	IDB_1	Input data bus bit
72-74	IMA_{17},IMA_{14}, IMA_{13}	Image memory address output bits
75	GND	Ground
76,77	IMA_9,IMA_8	Image memory address output bits
78	INBUSY	Input to ImPP busy output
79, 80	IMA_4,IMA_1	Image memory address output bits
81	IMD_{17}	Bidirectional image memory data bus bit
82	$\overline{DMAAK2}$	DMA / 2 acknowledge input
83	$\overline{DMARQ2}$	DMA / 2 request output
84, 85	IMD_{12},IMD_{11}	Bidirectional image memory data bus bits
86	V_{DD}	+5 V power supply
87,88	IMD_6,IMD_5	Bidirectional image memory data bus bits
89	A_1	Address select input
90	IMD_0	Bidirectional image memory data bus bit
91	IMRF	Image memory refresh output
92	D_0	Bidirectional data bus bit
93	$\overline{RD}$	Read input
94-96	D_4,D_6,D_7	Bidirectional data bus bits
97	GND	Ground
98	D_{13}	Bidirectional data bus bit
99	$\overline{IPPRST}$	Image pipelined processor reset output
100	IDB_{15}	Input data bus bit
101	ODB_{15}	Output data bus bit
102	IDB_{12}	Input data bus bit
103,104	ODB_{12},ODB_9	Output data bus bits
105,106	GND	Ground
107	ODB_0	Output data bus bit
108,109	MN_3,MN_0	Module number output bits
110	IDB_3	Input data bus bit
111-113	IMA_{20},IMA_{19}, IMA_{16}	Image memory address outputs
114	V_{DD}	+5 V power supply
115	GND	Ground
116-118	IMA_7,IMA_6, IMA_3	Image memory address outputs

Pin Identification (Cont)

No.	Symbol	Function
119	$\overline{RESET}$	Reset input
120-122	IMD_{16}-IMD_{14}	Bidirectional image memory data bus bits
123,124	GND	Ground
125,126	IMD_4,IMD_2	Bidirectional image memory data bus bits
127	IMRD	Image memory read output
128	GND	Ground
129	ERR	Error output
130,131	D_1,D_3	Bidirectional data bus bits
132	V_{DD}	+5 V power supply

Pin Functions

Table 1 shows the μPD9305 pins in their particular functional groups. The paragraphs that follow table 1 describe the operation of the pins in each group.

All unused input or output pins should be pulled up to V_{DD} or down to GND through a 2K-3K ohm resistor.

Table 1. μPD9305 Pins by Function

I/O	Signal	No.
I	CLK	1
	$\overline{RESET}$	119
	Status	
O	ERR	129
	$\overline{SOLBSY}$	29
	$\overline{CPURQ}$	30
	$\overline{INBUSY}$	78
	Host Interface	
I	$\overline{WR}$	47
	$\overline{RD}$	93
	$\overline{CS}$	50
	A_0	43
	A_1	89
I/O	D_0	92
	D_1	130
	D_2	48
	D_3	131
	D_4	94
	D_5	49
	D_6	95
	D_7	96
	D_8	51
	D_9	52
	D_{10}	2
	D_{11}	54
	D_{12}	3
	D_{13}	98
	D_{14}	55
	D_{15}	4
	DMA	
O	$\overline{DMARQ1}$	36
	$\overline{DMARQ2}$	83
I	$\overline{DMAAK1}$	35
	$\overline{DMAAK2}$	82
	DMAAEN	31

Table 1. μPD9305 Pins by Function (Cont)

I/O	Signal	No.
	μPD7281 Interface	
0	$\overline{MN_0}$	109
	$\overline{MN_1}$	68
	$\overline{MN_2}$	19
	$\overline{MN_3}$	108
0	$\overline{OREQ}$	6
I	$\overline{OACK}$	5
	$\overline{IREQ}$	56
0	$\overline{IACK}$	57
	$\overline{IPPRST}$	99
0	$\overline{ODB_0}$	107
	$\overline{ODB_1}$	66
	$\overline{ODB_2}$	17
	$\overline{ODB_3}$	65
	$\overline{ODB_4}$	15
	$\overline{ODB_5}$	13
	$\overline{ODB_6}$	63
	$\overline{ODB_7}$	62
	$\overline{ODB_8}$	11
	$\overline{ODB_9}$	104
	$\overline{ODB_{10}}$	61
	$\overline{ODB_{11}}$	10
	$\overline{ODB_{12}}$	103
	$\overline{ODB_{13}}$	59
	$\overline{ODB_{14}}$	8
	$\overline{ODB_{15}}$	101
I	$\overline{IDB_0}$	25
	$\overline{IDB_1}$	71
	$\overline{IDB_2}$	22
	$\overline{IDB_3}$	110
	$\overline{IDB_4}$	20
	$\overline{IDB_5}$	67
	$\overline{IDB_6}$	18
	$\overline{IDB_7}$	16
	$\overline{IDB_8}$	11
	$\overline{IDB_9}$	12
	$\overline{IDB_{10}}$	60
	$\overline{IDB_{11}}$	9
	$\overline{IDB_{12}}$	102
	$\overline{IDB_{14}}$	7
	$\overline{IDB_{15}}$	100

Table 1. μPD9305 Pins by Function (Cont)

I/O	Signal	No.
	Image Memory Interface	
I	$\overline{IMAK}$	38
0	$\overline{IMRD}$	127
	$\overline{IMWR}$	46
	$\overline{IMRF}$	91
I/O	IMD_0	90
	IMD_1	45
	IMD_2	126
	IMD_3	44
	IMD_4	125
	IMD_5	88
	IMD_6	87
	IMD_7	42
	IMD_8	41
	IMD_9	40
	IMD_{10}	39
	IMD_{11}	85
	IMD_{12}	84
	IMD_{13}	37
	IMD_{14}	122
	IMD_{15}	121
	IMD_{16}	120
	IMD_{17}	81

Table 1. μPD9305 Pins by Function (Cont)

I/O	Signal	No.
	Image Memory Interface	
	IMA_0	34
	IMA_1	80
	IMA_2	33
	IMA_3	118
	IMA_4	79
	IMA_5	32
	IMA_6	117
	IMA_7	116
	IMA_8	77
	IMA_9	76
	IMA_{10}	28
0	IMA_{11}	27
	IMA_{12}	26
	IMA_{13}	74
	IMA_{14}	73
	IMA_{15}	24
	IMA_{16}	113
	IMA_{17}	72
	IMA_{18}	23
	IMA_{19}	112
	IMA_{20}	111
	IMA_{21}	70
	IMA_{22}	21
	IMA_{23}	69

CLK (Clock)

CLK is the single phase master clock input. The μPD9305 clock frequency can be independent of ImPP clock frequency.

$\overline{\text{RESET}}$ (Reset)

$\overline{\text{RESET}}$ initializes the μPD9305. A reset places $\overline{\text{OREQ}}$, $\overline{\text{IACK}}$, the token I/O flip-flop, and IM access request signals at an inactive level. $\overline{\text{RESET}}$ resets the refresh address counter, refresh timer counter, and mode register to 0. $\overline{\text{RESET}}$ must be held low for a minimum of four μPD9305 or μPD7281 clock cycles, whichever is slower.

V_{DD} (Power)

V_{DD} is the single +5 volt power supply.

GND (Ground)

GND is the ground signal.

Status Signal Pin Functions

CPURQ (CPU Request)

CPURQ indicates to the host processor that the μPD9305 is ready to transfer a token to the host.

INBUSY (Input Busy)

INBUSY indicates that tokens are being input to the first ImPP from the μPD9305.

SOLBSY (Self Object Load Busy)

SOLBSY indicates that a self object load is being executed.

ERR (Error)

ERROR indicates that an error was output from the ImPPs, the host has read an invalid output token, or that the host has input a token while INBUSY was active.

Host Interface Signal Pin Functions

$\overline{\text{RD}}$ (Read)

RD reads the contents of the internal registers specified by A_1 and A_0.

$\overline{\text{WR}}$ (Write)

$\overline{\text{WR}}$ writes an input from the data bus to the internal register specified by A_1 and A_0.

$\overline{\text{CS}}$ (Chip Select)

$\overline{\text{CS}}$ enables the $\overline{\text{RD}}$ or $\overline{\text{WR}}$ control signals.

A_0, A_1 (Address)

A_0 and A_1 select the internal register for a read or write operation.

D_0-D_{15} (Data Bus)

The contents of the internal registers are read from or written to via data bus bits D_0-D_{15}.

DMA Signal Pin Functions

DMAAEN (Direct Memory Access Address Enable)

DMAAEN is used to indicate to the μPD9305 that an external DMA controller is putting DMA addresses on the address bus. During a DMA operation, DMA addresses (system memory addresses) are input to A_0 and A_1. However, these addresses have no meaning for the μPD9305 and might alter register contents. For this reason, the μPD9305 operates as if A_0 and A_1 are both reset to 0 when DMAAEN is active (high).

$\overline{\text{DMARQ1}}$ (Direct Memory Access Request 1)

$\overline{\text{DMARQ1}}$ issues a request to an external DMA controller to transfer data from the host system memory to the μPD9305.

$\overline{\text{DMARQ2}}$ (Direct Memory Access Request 2)

DMARQ2 issues a request to an external DMA controller to transfer data from the μPD9305 to the host system memory.

$\overline{\text{DMAAK1}}$ (Direct Memory Access Acknowledge 1)

$\overline{\text{DMAAK1}}$ is issued by the external DMA controller to indicate to the μPD9305 that $\overline{\text{DMARQ1}}$ has been received.

$\overline{\text{DMAAK2}}$ (Direct Memory Access Acknowledge 2)

$\overline{\text{DMAAK2}}$ is issued by the external DMA controller to indicate to the μPD9305 that $\overline{\text{DMARQ2}}$ has been received.

μPD7281 Interface Signal Pin Functions

MN_0-MN_3 (Module Number)

MN_0-MN_3 specify the module number of one ImPP. During a reset, one module number is output via MN_0-MN_3, the other via IDB_{12}-IDB_{15}. MN_0-MN_3 are three-state pins.

$\overline{\text{OREQ}}$ (Output Request)

$\overline{\text{OREQ}}$ signals to the first ImPP that the μPD9305 is ready to transfer half a token.

$\overline{\text{OACK}}$ (Output Acknowledge)

$\overline{\text{OACK}}$ signals to the μPD9305 that a half token has been accepted by the first ImPP.

$\overline{\text{IREQ}}$ (Input Request)

$\overline{\text{IREQ}}$ signals from the last ImPP that a half token is ready to be transferred from the ImPP to the μPD9305.

$\overline{\text{IACK}}$ (Input Acknowledge)

$\overline{\text{IACK}}$ indicates to the last ImPP that the μPD9305 has accepted the half token.

$\overline{\text{IPPRST}}$ (Image Pipelined Processor Reset)

IPPRST resets the ImPPs during RESET or a command reset.

ODB_0-ODB_{15} (Output Data Bus)

ODB_0-ODB_{15} transfer tokens from the μPD9305 to the first ImPP.

IDB_0-IDB_{15} (Input Data Bus)

IDB_0-IDB_{15} transfer tokens between the output of the last ImPP and the μPD9305.

Image Memory Interface Signal Pin Functions

IMRD (Image Memory Read)

IMRD requests a read of the contents of the image memory addressed by IMA_0-IMA_{23}.

IMWR (Image Memory Write)

IMWR requests a write to the image memory location addressed by IMA_0-IMA_{23}.

IMRF (Image Memory Refresh)

IMRF indicates an image memory refresh cycle.

$\overline{\text{IMAK}}$ (Image Memory Acknowledge)

$\overline{\text{IMAK}}$ indicates to the μPD9305 that an image memory read, write or refresh has been completed.

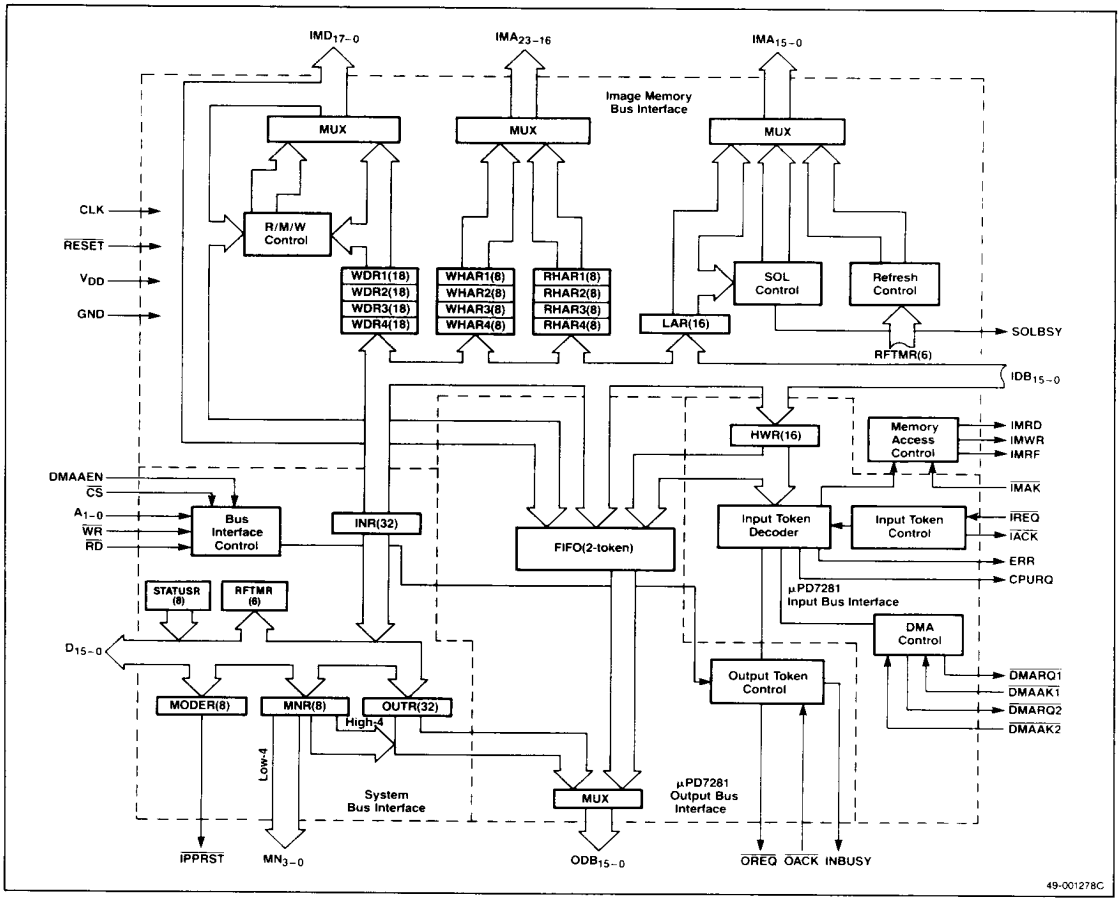
IMA_0-IMA_{23} (Image Memory Address)

IMA_0-IMA_{23} supplies the image memory address for a read or write operation or for DRAM refresh (IMA_0-IMA_9 only).

IMD_0-IMD_{17} (Image Memory Data)

IMD_0-IMD_{17} is the bidirectional data bus for transferring data to and from the image memory.

μPD9305 Block Diagram



Functional Description

The μPD9305 has the following functional units:

- μPD7281 input bus interface
- μPD7281 output bus interface
- System bus interface
- Image memory bus interface
  - —Register file
  - —R/M/W control
  - —Self object load control
  - —Image memory refresh control

μPD7281 Input Bus Interface

After the last ImPP outputs a token, the input bus interface determines whether the token should be an output token to the host CPU, to the image memory, or to the output bus interface block. The high order 16 bits of the token output from the last ImPP are latched into in the high word register (HWR) and then decoded by the input token decoder to determine the token type.

μPD7281 Output Bus Interface

The output bus interface logic transmits tokens through the multiplexer (MUX) to the first ImPP. The transmitted tokens come from the system bus interface, the μPD7281 input bus interface, or the image memory bus interface. The output bus interface uses a priority control mechanism to prevent collisions between the tokens coming from the different blocks.

System Bus Interface

The system bus interface receives a token from the host CPU for the ImPPs, sends it to the output register (OUTR), and signals the output bus interface. Conversely, it sends a token, which is output from the last ImPP, through the input register (INR) to the host CPU according to instructions from the host CPU. The host CPU can set input or output modes (MODER register), read the status register (STATUSR), set image memory refresh timing (RFTMR register), and set module numbers (MNR) for two μPD7281s.

Image Memory Bus Interface

The image memory bus interface accepts the following five types of tokens:

Token	Description
WHA	Write high address
WLA	Write low address
WD	Write data
RHA	Read high address
RLA	Read low address

Tokens have a 16-bit data value, so the address is transferred in two tokens to form the 24-bit image memory address. The lower 16-bits of the image memory address are latched in the lower address register.

The image memory bus interface also performs read/modify/write functions with the R/M/W control logic and provides a register file.

Register File. The register file is used for storing write high addresses (WHAR/four 8-bit registers), write data (WDR/four 18-bit registers), and read high addresses (RHAR/four 8-bit registers).

Read/Modify/Write (R/M/W) Control. The R/M/W control reads a word from the image memory, performs a logical operation (AND, OR, or XOR) between it and the contents of a write data register (WDR), and then writes it back to a location referenced by the WHAR (the same lower 16-bit address, but a different upper eight bits).

Self Object Load (SOL). The self object load control loads ImPP object programs stored in image memory into the ImPPs. When the SOL is given a starting address, the SOL control automatically generates the appropriate addresses to read the image memory.

Image Memory Refresh Control. The μPD9305 generates a 10-bit address and the timing for refreshing dynamic image memories. The timing is set by the RFTMR register.

Figure 1 shows the input/output token format and table 2 shows how the image memory access tokens function.

Figure 1. Input/output Token Format

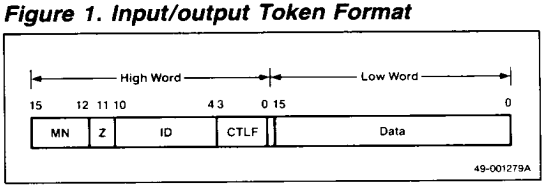


Table 2. Image Memory Access Tokens[1]

MN	Z	ID		CTLF	Data	Function	Operation
0001	–	MN′	ID′	----	Image memory read low address	Image memory read (RHAR1 reference)	R
		111	----	----	------ Image memory read high address	Read high address register (RHAR1) set (Note 2)	S
0010	–	MN′	ID′	----	Image memory read low address	Image memory read (RHAR2 reference)	R
		111	----	----	------ Image memory read high address	Read high address register (RHAR2) set (Note 2)	S
0011	–	MN′	ID′	----	Image memory read low address	Image memory read (RHAR3 reference)	R
		111	----	----	------ Image memory read high address	Read high address register (RHAR3) set (Note 2)	S
0100	–	MN′	ID′	----	Image memory read low address	Image memory read (RHAR4 reference)	R
		111	----	----	------ Image memory read high address	Read high address register (RHAR4) set (Note 2)	S
		00000	DIR	----	Image memory write low address	Image memory write (referencing WHAR and WDR selected by DIR)	W
		001--	DIR	----	------ Image memory write high address	Set write high address register (WHAR) selected by DIR	S
0101	–	010--	DIR	--C,S	Image memory write data register	Set write data register (WDR) selected by DIR	S
		011--	DIR	----	------ Image memory read high address	Set read high address register (RHAR) selected by DIR	S
		100 MASK	DIR	----	Read/write low address	Read/modify/write	RW
		101--	DIR	----	Read/write low address	Read / modify / write (write CS bits selects mask)	RW
		00---	DIR	----	Load starting low address	Self object load	R
0110	–	01---	DIR	----	Load starting low address	Self object load MN of output token is SOLMN)	R
		1----	--	----	---------- SOLMN	Set SOLMN for self object load	S

Notes:

(1) The following definitions refer to the above table:
MN: Module number
Z: Always 0
ID: Identifier
CTLF: Control field
ID′: ID used for next circulation
MN′: MN used for next circulation (MN ≠ 111)
DIR: Specifies registers for memory image access
MASK: Specifies the modify mode
–: Do not care
S: Set
R: Read
W: Write

(2) When RHASEL of the mode register is 1, the tokens become image memory read (request) tokens

Table 3 shows module number (MN) values and the five token types (refer to figure 12).

The five token types are:
(1) Output request data to the host
(2) Image memory access data
(3) DMA request data
(4) Pass data
(5) Delete data

Table 3. MN Values and Token Types

Token Type	MN	ID	Function	Abbreviation
(1)	0 0 0 0	x x x x x x x x	μPD7281 output data to host	CPU
(2)	0 0 0 1	MN′ ID′ x x x x x x x	Image memory read1 (RHAR1 select)	IMR
		1 1 1 x x x x	RHAR1 set (Note 2)	
	0 0 1 0	MN′ ID′ x x x x x x x	Image memory read2 (RHAR2 select)	
		1 1 1 x x x x	RHAR2 set (Note 2)	
	0 0 1 1	MN′ ID′ ↔ ↔	Image memory read3 (RHAR3 select)	
		1 1 1 x x x x	RHAR3 set (Note 2)	
	0 1 0 0	MN′ ID′ ↔ ↔	Image memory read4 (RHAR4 select)	
		1 1 1 x x x x	RHAR4 set (Note 2)	
	0 1 0 1	0 0 0 0 0 DIR ↔	Image memory write	IMW
		0 0 1 x x DIR ↔	High address set for write (selected register file is DIR +1)	IMWHA
		0 1 0 x x DIR ↔	Write data set (selected register file is DIR +1)	IMWD
		0 1 1 x x DIR ↔	High address set for read (selected register file is DIR +1)	IMREA
		1 0 0 Mask DIR ↔ ↔	Read/modify/write1	RMW1
		1 0 1 x x DIR ↔	Read / modify / write2 (mask selected by CS bits of image memory write data)	RMW2
(3)	0 1 0 1	1 1 0 x x x x	DMA1 (host → μPD7281)	DMA1
		1 1 1 x x x x	DMA2 (μPD7281 → host)	DMA2
(2)	0 1 1 0	0 0 x x x DIR ↔	Self object load1	SOL1
		0 1 x x x DIR ↔	Self object load2 (rewrite MN)	SOL2
		1 x x x x x x	MN set for self object load	SOLMN
(4)	0 1 1 1		μPD7281 module number (when RHASEL=1)	PASS
	1 0 0 0 1 0 0 1 1 0 1 0 1 1 0 0 1 1 0 1 1 1 1 0		μPD7281 module numbers	
(5)	1 1 1 1		Deleted	VANISH

Notes:

(1) The following definitions refer to the above table:
MN: Module number
ID: Identifier
MN′: MN used for next circulation (MN ≠ 111)
ID′: ID used for next circulation

(2) When RHASEL of the mode register is 1, the tokens become image memory read tokens.

Absolute Maximum Ratings

T_A = 25°C

Power supply voltage, V_{DD}	−0.5 V to 7.0 V
Input voltage, V_I	−0.5 V to 7.0 V
Output current, I_O	10 mA
Operating temperature, T_{OPT}	0°C to 70°C
Storage temperature, T_{STG}	−65°C to 150°C

***Comment:** Exposing the device to stresses above those listed in absolute maximum ratings could cause permanent damage. Do not operate the device under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_A = 25°C

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
Input capacitance	C_I		10	pF	f_c = 1 MHz Unmeasured pins are at 0 V.
Output capacitance	C_O		15	pF	
Input/output capacitance	C_{IO}		15	pF	

DC Characteristics

T_A = 0°C to +70°C, V_{DD} = 5 V ± 10%

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Input low voltage	V_{IL}	−0.5		0.8	V	
Input high voltage	V_{IH}	2.0		V_{DD}+0.5	V	
Output low voltage	V_{OL}			0.4	V	I_{OL} = 2 mA
Output high voltage	V_{OH}	V_{DD} −0.4			V	I_{OL} = −400 μA
Input leakage current	I_{LI}			±10	μA	$0 \le V_I \le V_{DD}$
Output leakage current	I_{LO}			±10	μA	$0 \le V_I \le V_{DD}$
Supply current	I_{DD}		10	100	mA	10 MHz

AC Characteristics

T_A = 0°C to +70°C, V_{DD} = 5 V ± 10%

Clock Timing

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
CLK cycle time	t_{CYK}	80		ns	
Clock pulse width high	t_{WKH}	30		ns	
Clock pulse width low	t_{WKL}	30		ns	
Clock rise time	t_{KR}		10	ns	
Clock fall time	t_{KF}		10	ns	

Input Timing

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
Input rise time	t_{IR}	0	10	μs	
Input fall time	t_{IF}	0	10	μs	

RESET Timing

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
$\overline{\text{RESET}}$ pulse width	t_{RST}	t_{CYK}		ns	μPD9305 only
$\overline{\text{RESET}}$ setup time to $\overline{\text{IPPRST}}$	t_{DRSPRL}		40	ns	
$\overline{\text{IPPRST}}$ hold time after $\overline{\text{RESET}}$ ↑	t_{DRSPRH}		50	ns	
$\overline{\text{IPPRST}}$ setup to MN_0-MN_3	t_{DMN}		60	ns	
MN_0-MN_3 float time after $\overline{\text{IPPRST}}$ ↑	t_{FMN}		50	ns	
$\overline{\text{IPPRST}}$ low until OBD_{15}-OBD_{12} active	t_{DPROD}		60	ns	
OBD_{15}-OBD_{12} float time after $\overline{\text{IPPRST}}$ ↑	t_{FPROD}		50	ns	

3h

Host CPU ↔ μPD9305 Read/Write Timing

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
Address setup to $\overline{WR}$ ↓, $\overline{RD}$ ↓	t_{SARW}	20		ns	
Address hold time after $\overline{WR}$ ↑, $\overline{RD}$ ↑	t_{HRWA}	20		ns	
$\overline{CS}$ setup to $\overline{WR}$ ↓ $\overline{RD}$ ↓	t_{SCRW}	0		ns	
$\overline{CS}$ hold time after $\overline{WR}$ ↑, $\overline{RD}$ ↑	t_{HRWC}	0		ns	
$\overline{WR}$, $\overline{RD}$ pulse width	t_{WRWL}	100		ns	
$\overline{RD}$ setup to data	t_{DRD}		80	ns	
Data float time after $\overline{RD}$ ↑	t_{FRD}		30	ns	
Data setup to $\overline{WR}$ ↑	t_{SDW}	20		ns	
Data hold after $\overline{WR}$ ↑	t_{HWD}	20		ns	

DMA Request Timing(1)

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
$\overline{DMARQ}$ ↓ setup time to $\overline{DMAAK}$ ↓	t_{DDQDA}	20		ns	
$\overline{DMARQ}$ ↑ time from $\overline{DMAAK}$ ↓	t_{DDADQ}		50	ns	
$\overline{DMARQ}$ ↓ time from $\overline{DMAAK}$ ↑	t_{RVDQ}	50		ns	
DMAAEN ↑ setup time to ($\overline{RD}$,$\overline{WR}$) ↓	t_{SDERW}	30		ns	
DMAAEN hold time after ($\overline{RD}$,$\overline{WR}$) ↑	t_{HRWDE}	30		ns	
$\overline{DMAAK}$ low setup time to ($\overline{RD}$,$\overline{WR}$) ↓	t_{SDARW}	0		ns	
$\overline{DMAAK}$ hold time after ($\overline{RD}$,$\overline{WR}$) ↑	t_{HRWDA}	0		ns	
$\overline{DMAAK}$ pulse width	t_{WDAL}	t_{CYK}		ns	

Note:
(1) $\overline{DMAAK}$ = $\overline{DMAAK1}$ or $\overline{DMAAK2}$
$\overline{DMARQ}$ = $\overline{DMARQ1}$ or $\overline{DMARQ2}$

I/O Request/Acknowledge Timing

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
$\overline{IREQ}$ ↓ setup time to $\overline{IACK}$ ↓	$t_{DIQIAL1}$	15	60	ns	
$\overline{IACK}$ ↓ setup time to $\overline{IREQ}$ ↑	$t_{DIAIQH1}$	10		ns	
$\overline{IREQ}$ ↑ setup time to $\overline{IACK}$ ↑	$t_{DIQIAH1}$	20	70	ns	
$\overline{IACK}$ ↑ setup to $\overline{IREQ}$ ↓	t_{DIAIQL}	10		ns	
ID bus setup time to $\overline{IREQ}$ ↑	t_{SIDIQ}	20		ns	
ID bus hold time from $\overline{IREQ}$ ↑	t_{HIQID}	10		ns	
$\overline{OREQ}$ ↓ setup time to $\overline{OACK}$ ↓	t_{DOQOAL}	10		ns	
$\overline{OACK}$ ↓ setup time to $\overline{OREQ}$ ↑	t_{DOAOQH}	20	70	ns	
$\overline{OREQ}$ ↑ setup time to $\overline{OACK}$ ↑	t_{DOQOAH}	10		ns	
$\overline{OACK}$ ↑ setup time to $\overline{OREQ}$ ↓	t_{DOAOQL}	15	60	ns	
$\overline{OREQ}$ ↓ setup time to $\overline{ODB}$ valid	t_{DOQOD}		10	ns	
$\overline{ODB}$ float time after $\overline{OREQ}$ ↑	t_{FOQOD}	10		ns	

Note:
Pull-up resistors required on μPD9305 IDB_{15}-IDB_0 to meet t_{HIQID} timing.

Image Memory Read, Write, Refresh Timing

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
IMA(1) ↑ active time from CLK ↓	t_{DKMARF}		100	ns	IM refresh
IMA active time from CLK ↓	t_{DKMAMC}		60	ns	IM read or IM write
IMA float time from IMC ↓	t_{FMCMA}	10		ns	
IMC recovery time	t_{RVMC}	$1.5t_{CYK}$		ns	
IMC ↑ delay time from CLK ↓	t_{DKMCH}		35	ns	
IMC ↓ delay time from CLK ↓	t_{DKMCL}		40	ns	
$\overline{IMAK}$ recovery time	t_{RVMK}	$1.5t_{CYK}$		ns	
$\overline{IMAK}$ setup time to CLK ↓	t_{SMKK}	10		ns	
$\overline{IMAK}$ hold time from IMC ↓	t_{HMCMK}	0		ns	
IMD setup time to CLK ↑	t_{SMDK}	20		ns	Image memory read timing
IMD hold time from IMRD ↓	t_{HMRMD}	0		ns	Image memory read timing
IMD delay time from CLK ↓	t_{DKMD}		30	ns	Image memory write timing
IMD float time from IMWR ↓	t_{FMWMD}	20		ns	Image memory write timing

Note:
(1) IMA = IMA_{23}-IMA_0
(2) IMC + IMRD, IMWR or IMRF
(3) To maximize IM access time use $\overline{IMAK}$ = $\overline{IMC}$. Then IM cycle time will be $3.k_{CYK}$

SOLBSY Timing

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
SOLBSY delay time from $\overline{IACK}$ ↑	t_{DIASB}		30	ns	
SOLBSY delay time from CLK ↓	t_{DKSB}		60	ns	

CPURQ Timing

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
CPURQ delay time from $\overline{IACK}$ ↑	t_{DIAPQ}		30	ns	
CPURQ delay time from $\overline{RD}$ ↑	t_{DPRQ}		60	ns	

INBUSY Timing

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
INBUSY ↑ delay time from $\overline{WR}$ ↑	t_{DWIB}		70	ns	
INBUSY ↓ delay time from $\overline{OREQ}$ ↑	t_{DOQIB}		40	ns	

ERR Timing

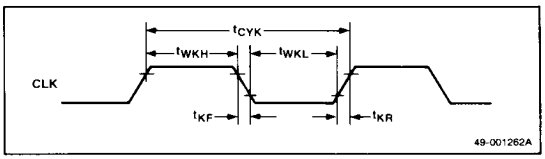
Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
ERR ↑ delay time from $\overline{IACK}$ ↑	t_{DIAE}		30	ns	Error token output
ERR ↑ delay time from $\overline{WR}$ ↓	t_{DWE}		60	ns	INBUSY = 1
ERR ↑ delay time from $\overline{RD}$	t_{DRE}		60	ns	CPURQ = 0
INBUSY hold time from $\overline{WR}$ ↓	t_{HWIB}		10	ns	
CPURQ setup time to $\overline{RD}$ ↓	t_{SPQR}		10	ns	

Note:

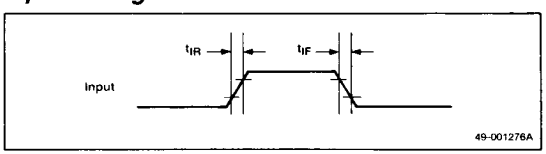
All unused input or output pins should be pulled up to V_{DD} or down to GND through a 2K-3K ohm resistor.

Timing Waveforms

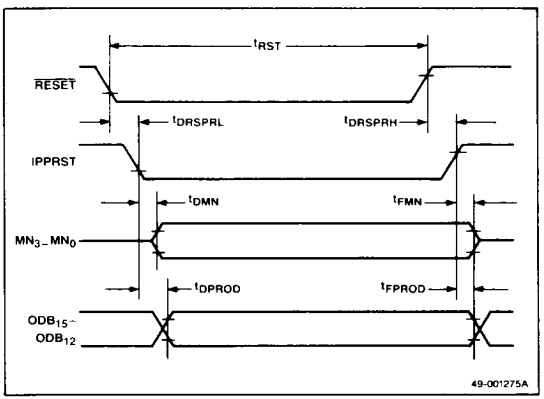
Clock Timing



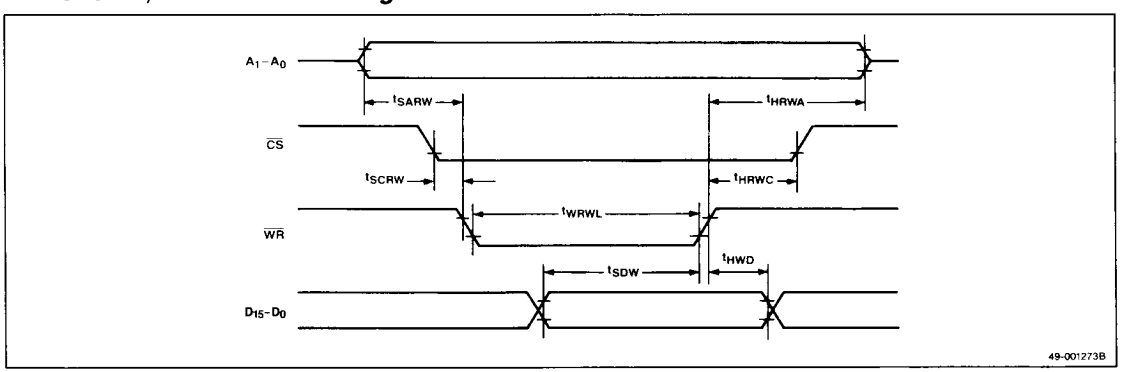
Input Timing



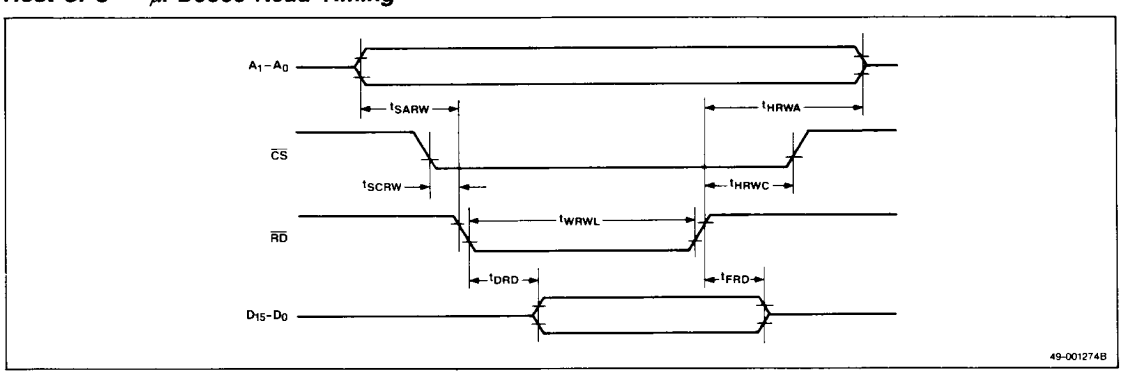
RESET Timing



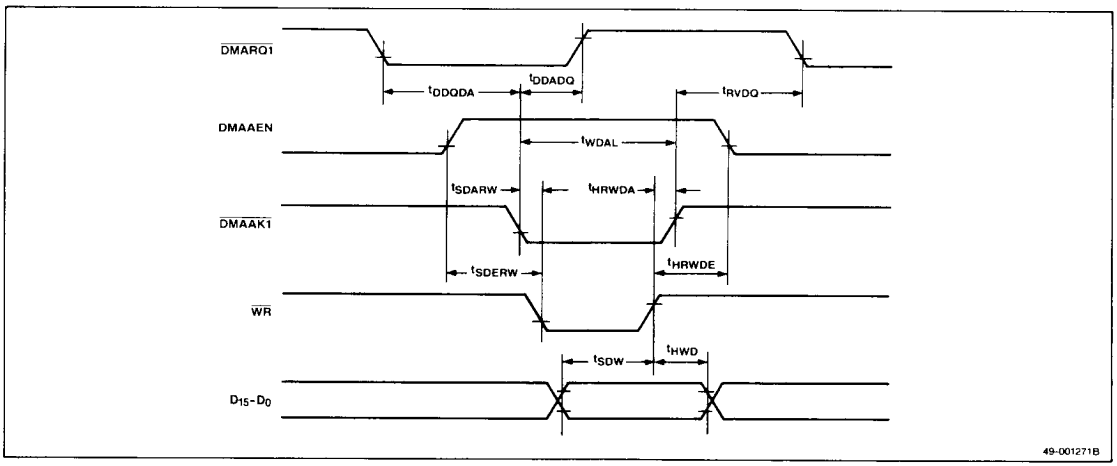
Host CPU ↔ μPD9305 Write Timing



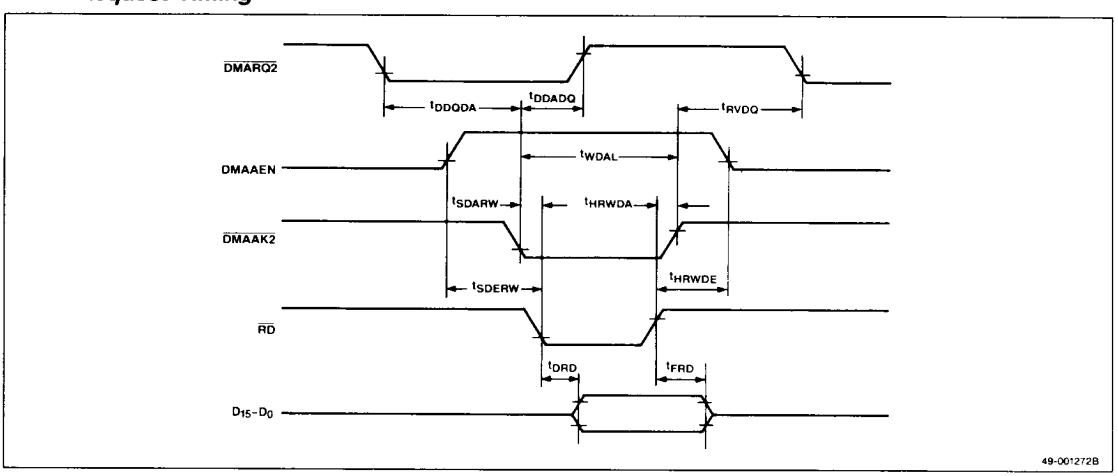
Host CPU ↔ μPD9305 Read Timing



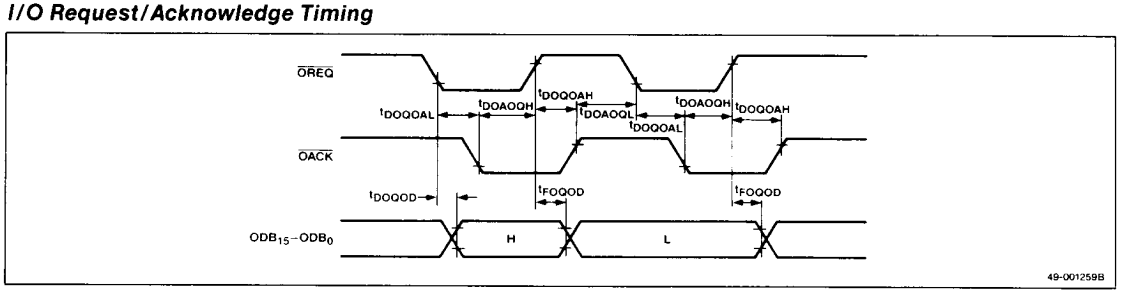
DMA1 Request Timing



DMA2 Request Timing



I/O Request/Acknowledge Timing



3h

I/O Data Bus Handshake Timing

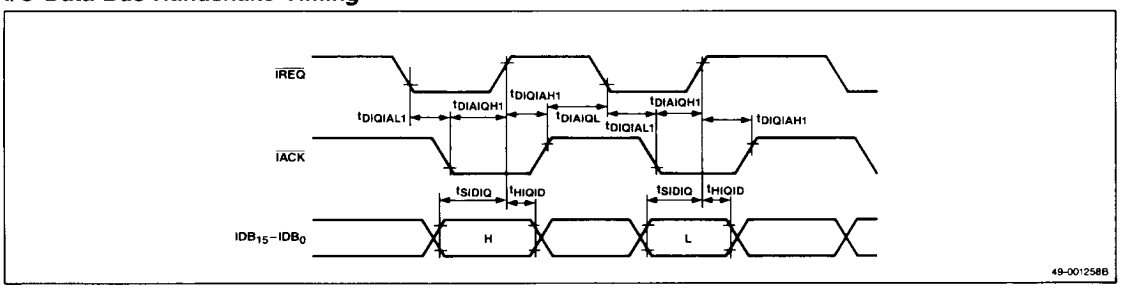


Image Memory Read Timing

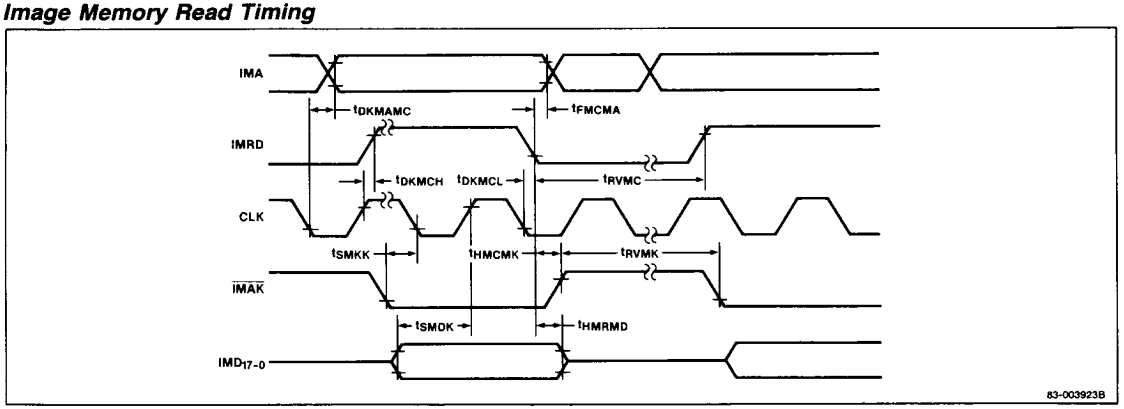


Image Memory Write Timing

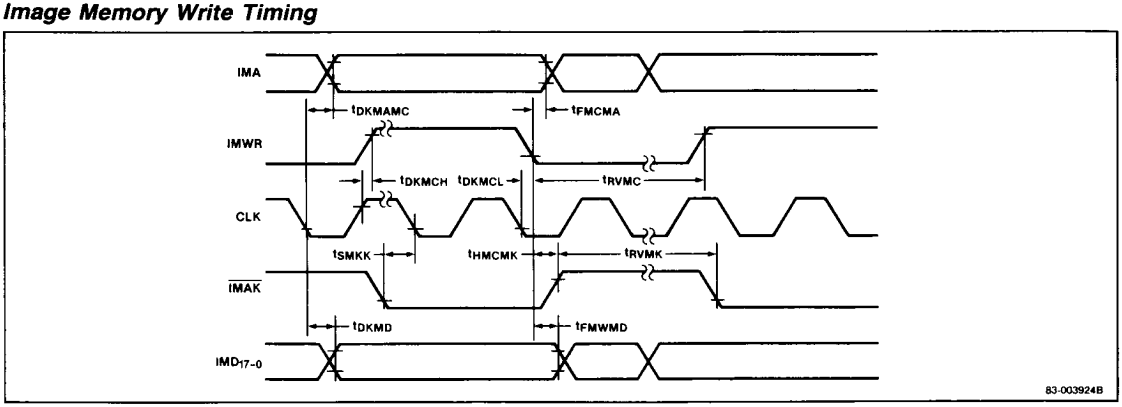
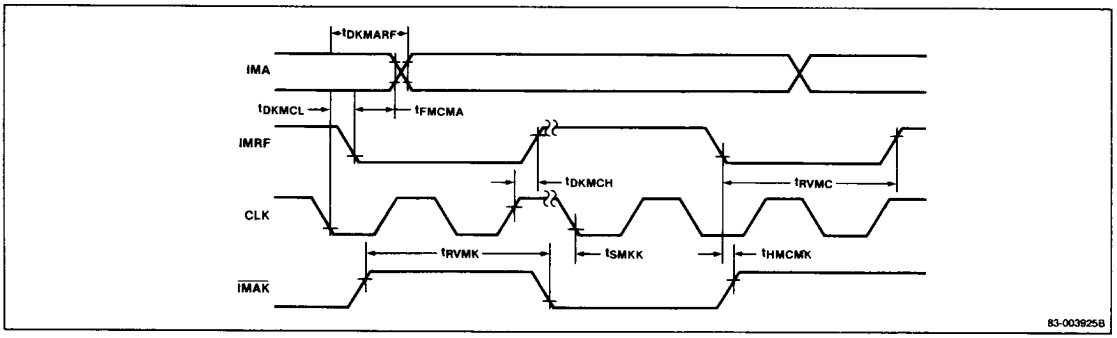
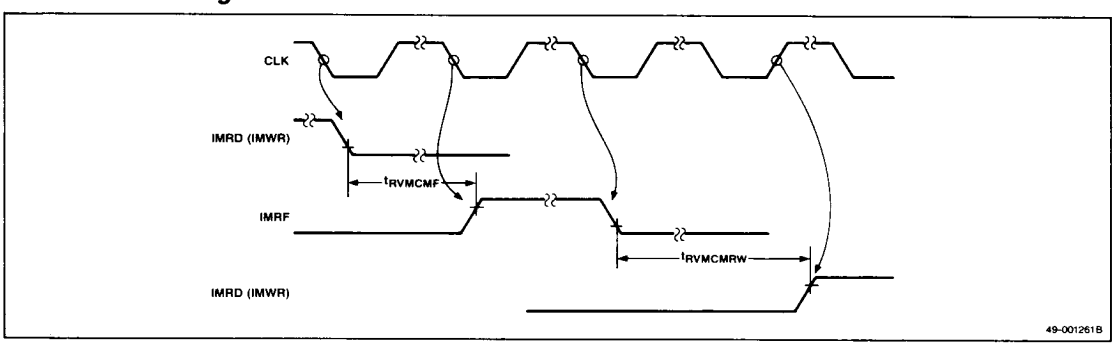


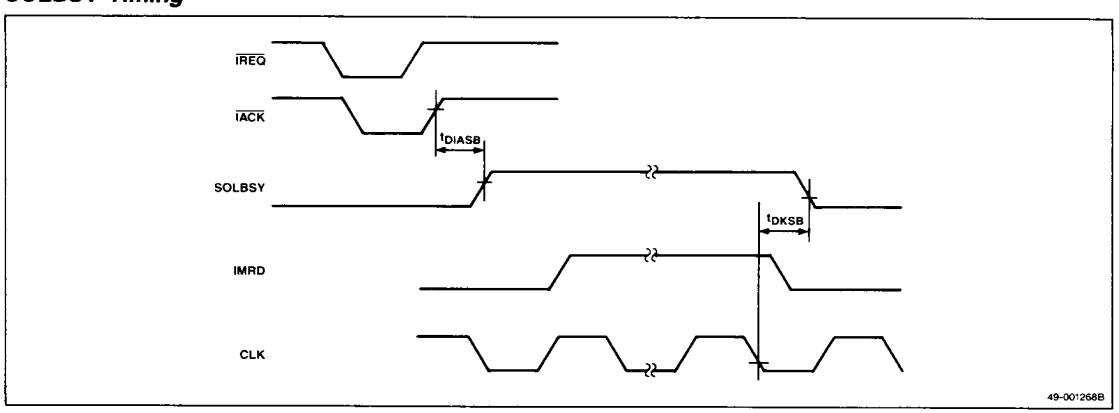
Image Memory Refresh Timing



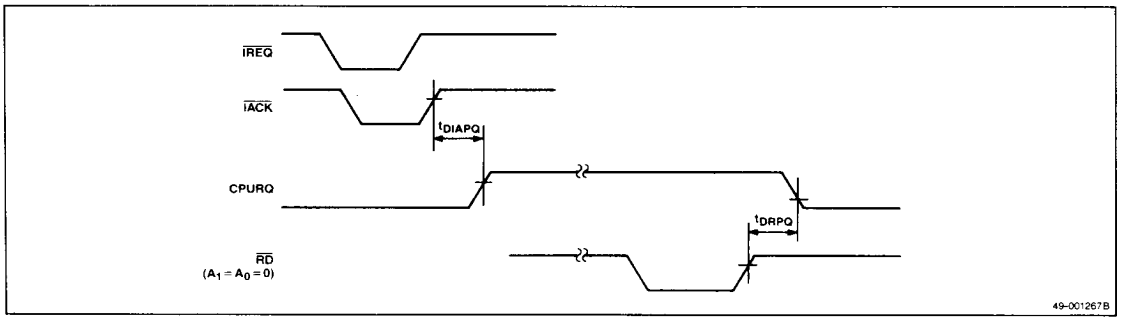
IM Command Timing



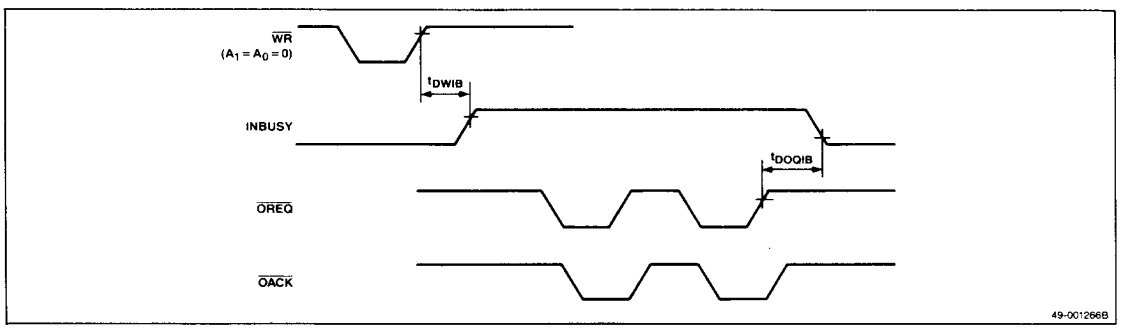
SOLBSY Timing



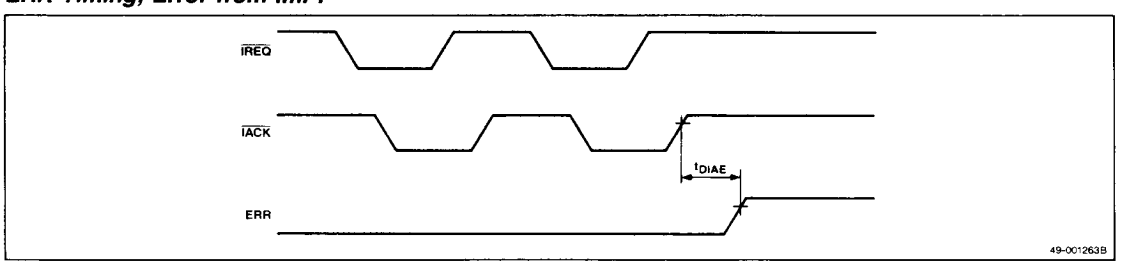
CPURQ Timing



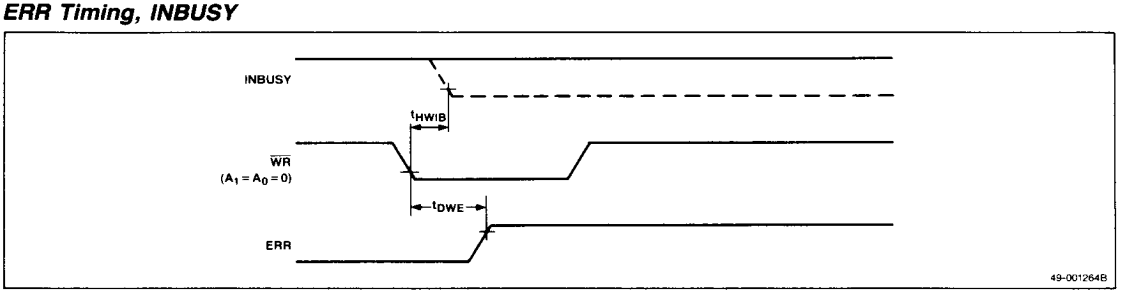
INBUSY Timing



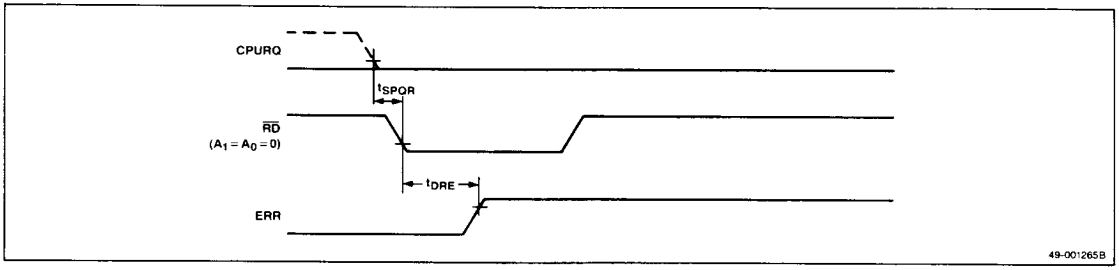
ERR Timing, Error from ImPP



ERR Timing, INBUSY



ERR Timing, CPU Request



μPD9305 Operation

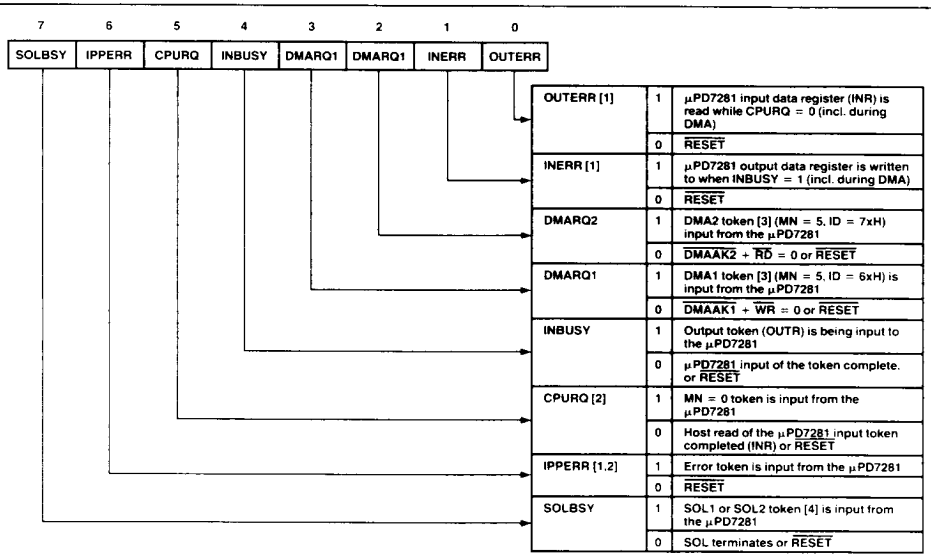
Table 4 shows how the μPD9305 uses signals $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, and A_1, A_0 to read or write to I/O ports.

Table 4. I/O Ports

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_1	A_0	Internal I/O Ports
0	0	1	0	0	Read ImPP input data register (from ImPP)
0	0	1	0	1	Read status register
0	0	1	1	0	Command $\overline{RESET}$, data read has no meaning
0	0	1	1	1	Not used
0	1	0	0	0	Write ImPP output data register (to ImPP)
0	1	0	0	1	Write mode register
0	1	0	1	0	Write module number register
0	1	0	1	1	Write refresh timing register

Figure 2 shows the status register format.

Figure 2. Status Register Format

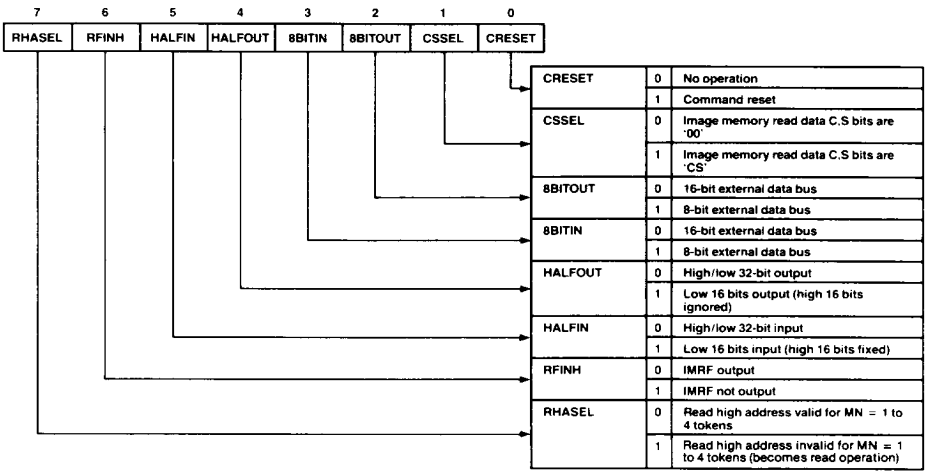


Notes: [1] IPPERR, INERR and OUTERR are ORed and output to the ERR pin.
[2] When IPPERR becomes '1', CPURQ also becomes '1' at the same time.
[3] Refer to μPD9305 User's Manual, Section 6, DMA Request Function
[4] Refer to μPD9305 User's Manual, Section 5, Image Memory/μPD7281 Interfacing

49-001280B

Figure 3 shows the mode register format.

Figure 3. Mode Register Format

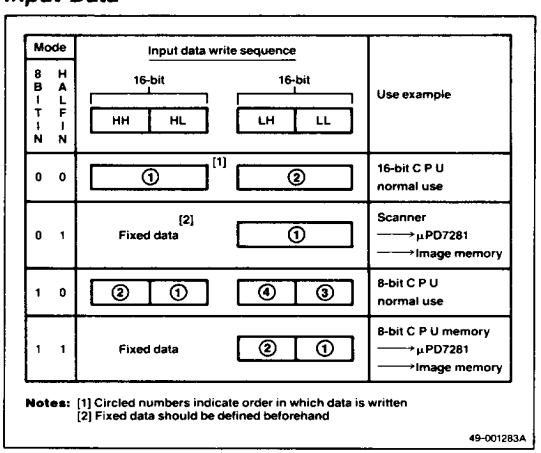


Note: All bits of the mode register default to 0 when an external reset is applied.

49-001281A

Figures 4-20 graphically show μPD9305 operation. For a detailed description of μPD9305 operation, refer to the *μPD9305 User's Manual.*

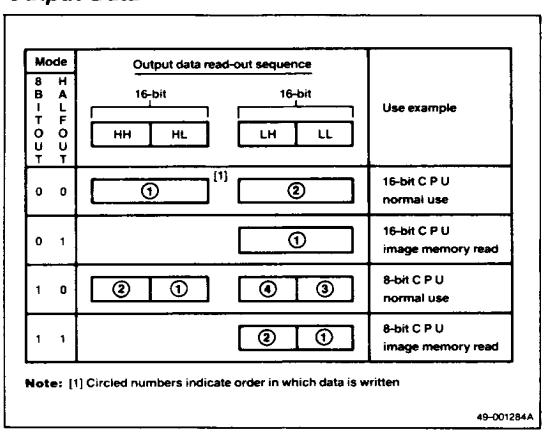
Figure 4. Setting Write Method for Input Data



Notes: [1] Circled numbers indicate order in which data is written
[2] Fixed data should be defined beforehand

49-001283A

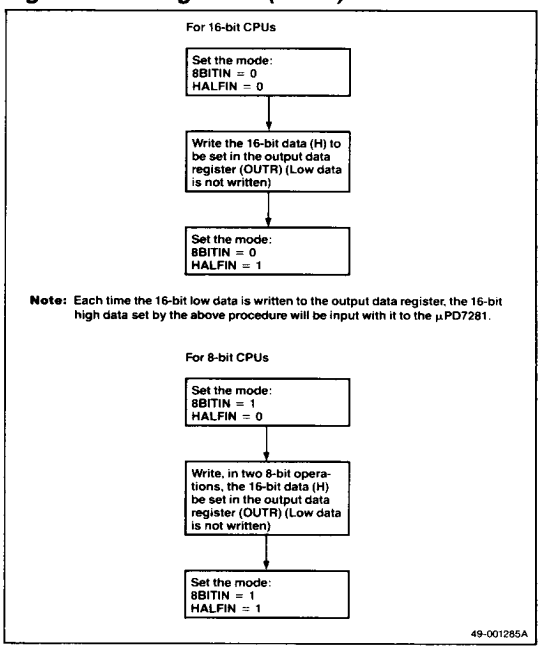
Figure 5. Setting Read Method for Output Data



Note: [1] Circled numbers indicate order in which data is written

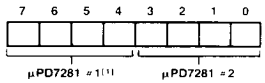
49-001284A

Figure 6. Setting Fixed (16-Bit) Data



Note: Each time the 16-bit low data is written to the output data register, the 16-bit high data set by the above procedure will be input with it to the μPD7281.

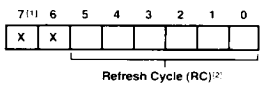
Figure 7. MN Register



Note: [1] Bits 7–4 are output on the output data bus

49-001287A

Figure 8. Refresh Timing Register



Notes: [1] X = don't care
[2] The actual refresh cycle is (RC + 1) x 8 CLK. RC = 0 to 63

49-001288A

3h

Figure 9. Input Timing (Host to μPD9305 to μPD7281)

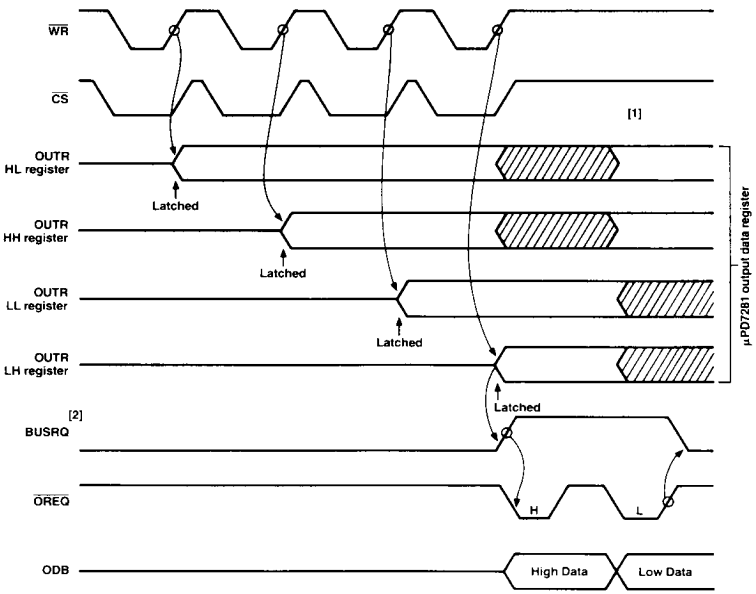


Figure 10. Output Timing (μPD7281 to μPD9305 to Host)

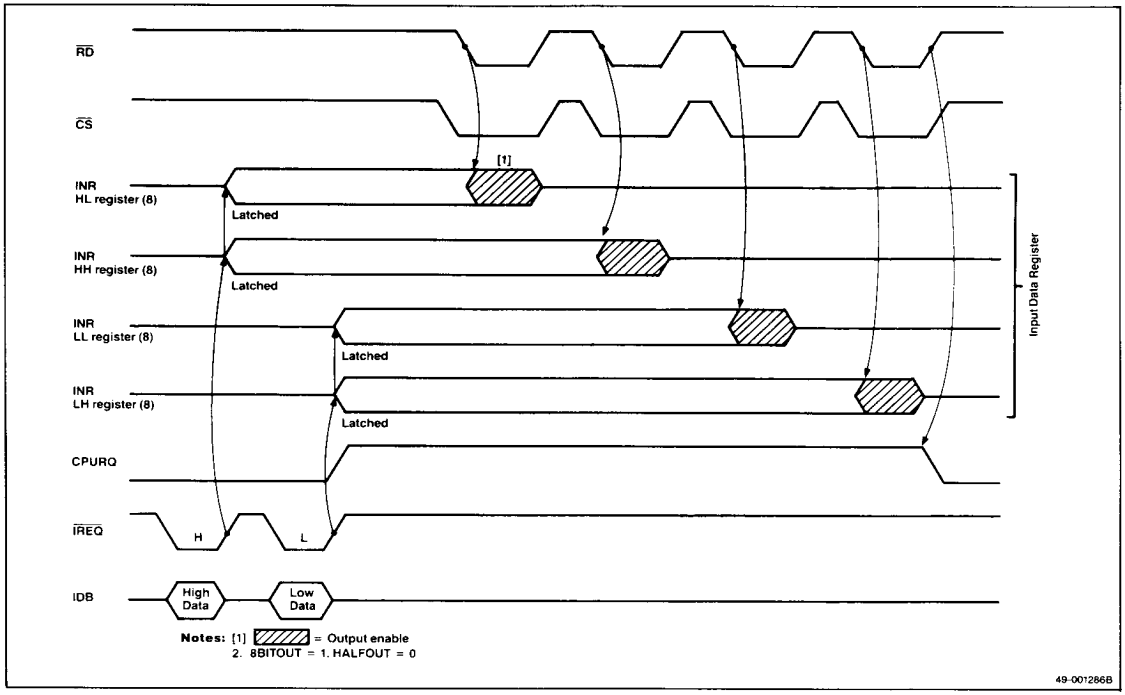


Figure 11. Output to μPD7281, Control Data Paths

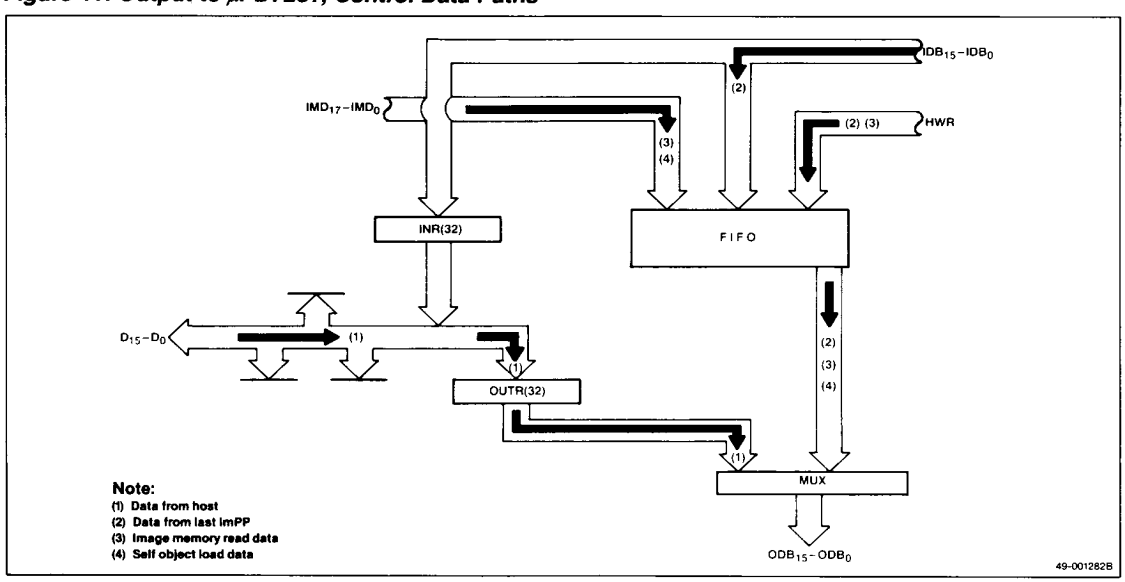


Figure 12. μPD7281, Input Control Data Flow

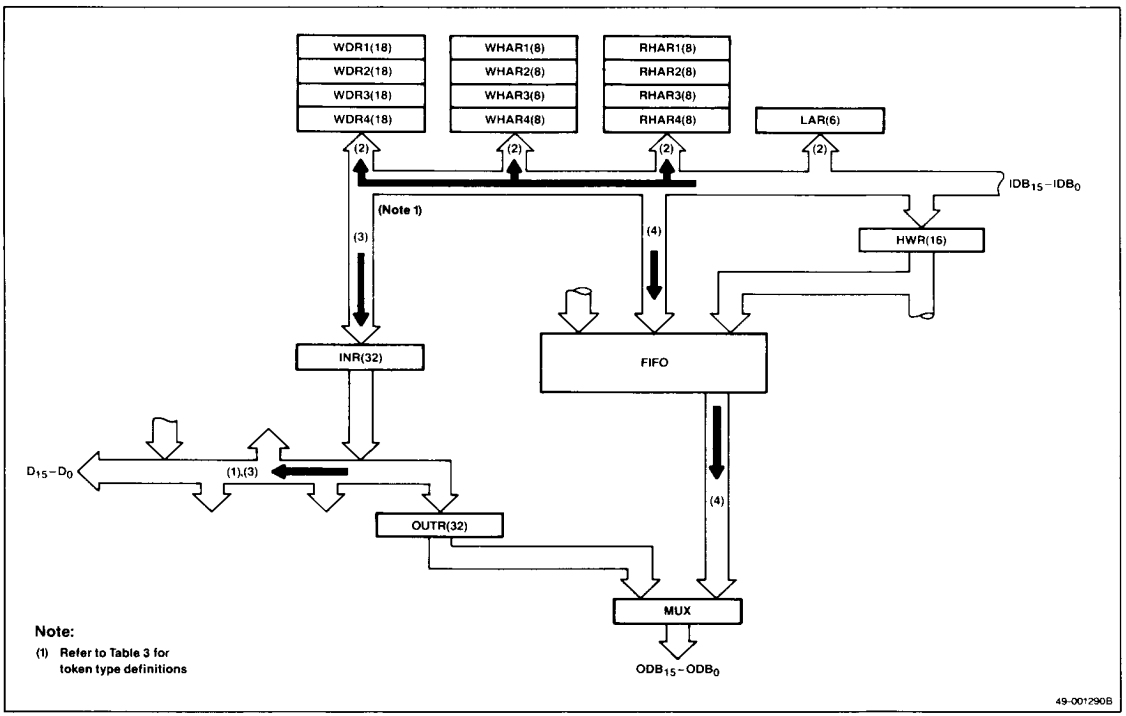


Figure 13. Image Memory Read Timing (Without Refresh Request)

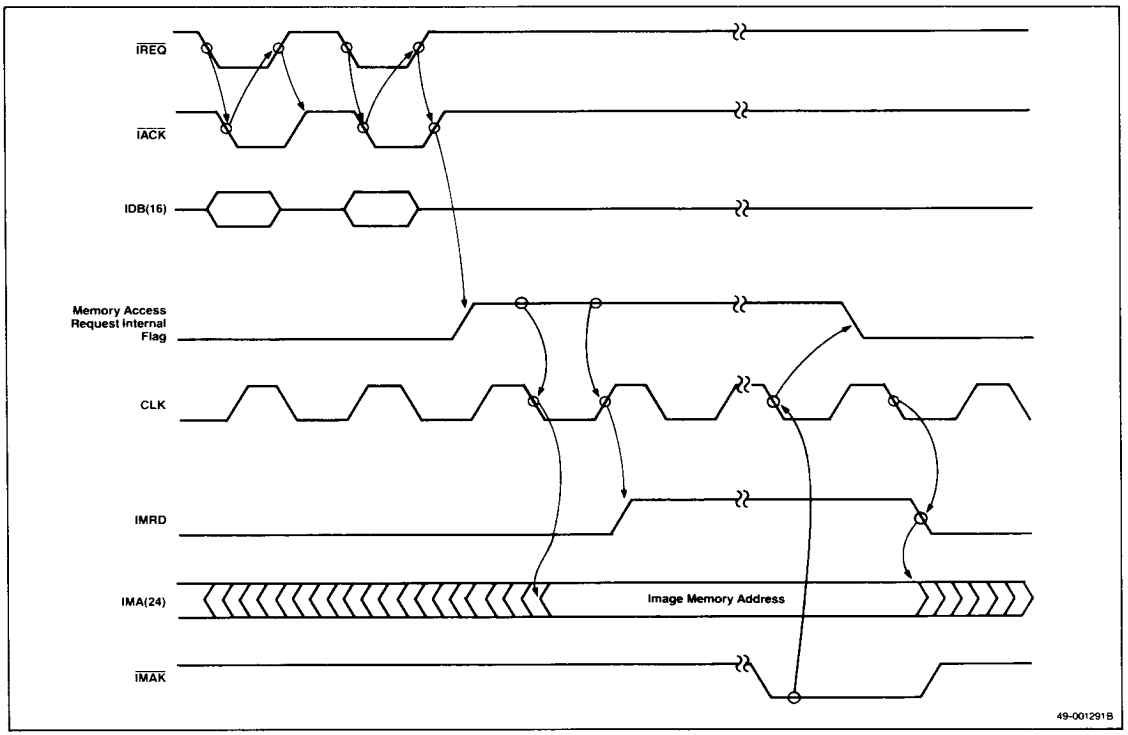


Figure 14. Image Memory Write Timing (Without Refresh Request)

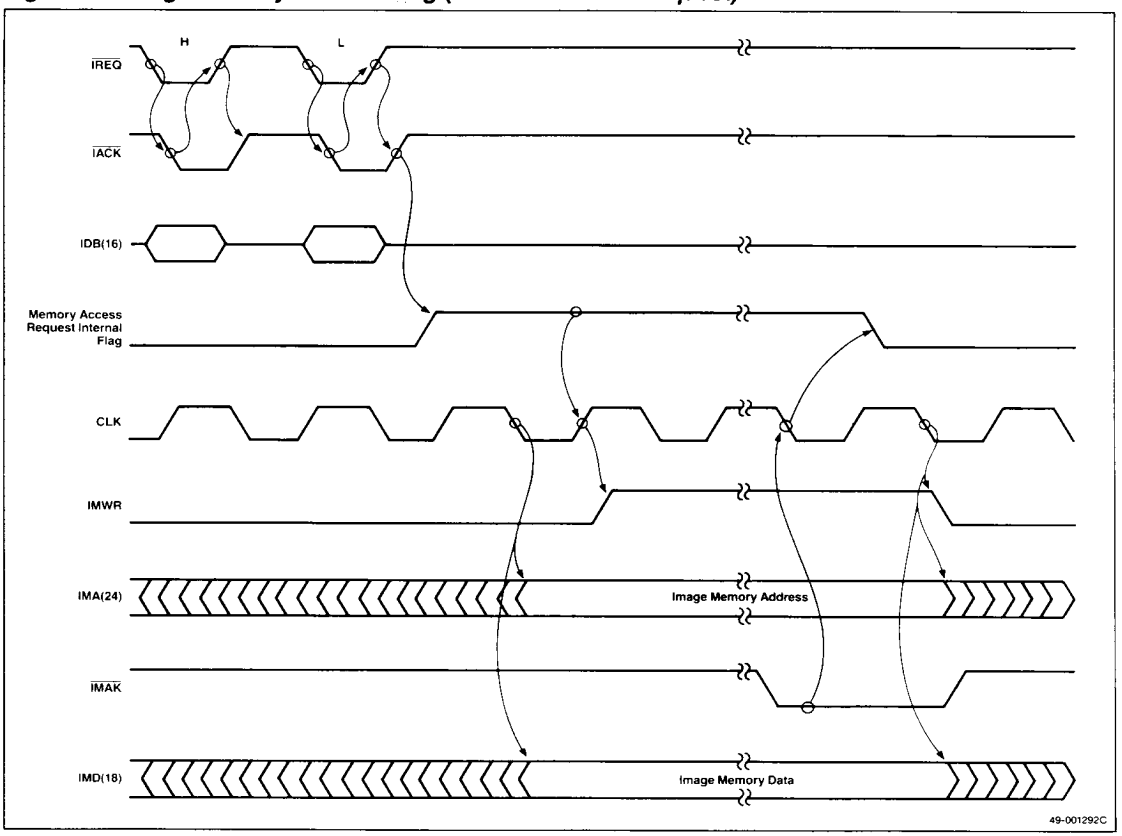


Figure 15. Image Memory Access Request Priority Control

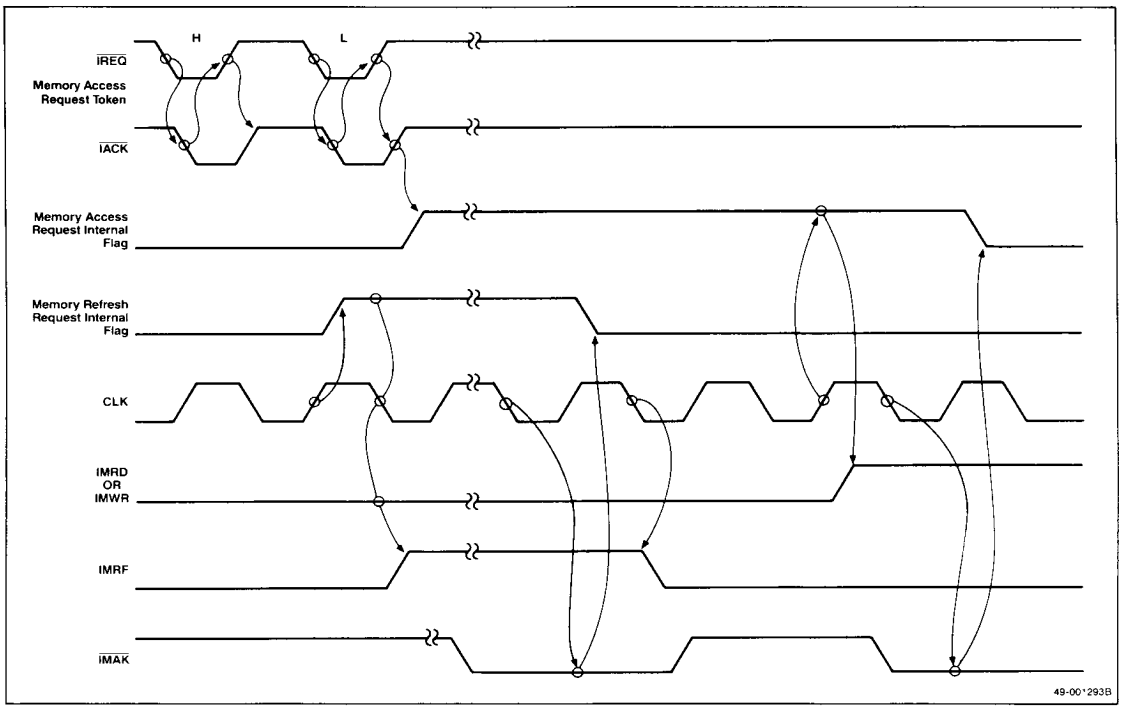


Figure 16. Read Data → μPD7281 Output Timing (Single Output)

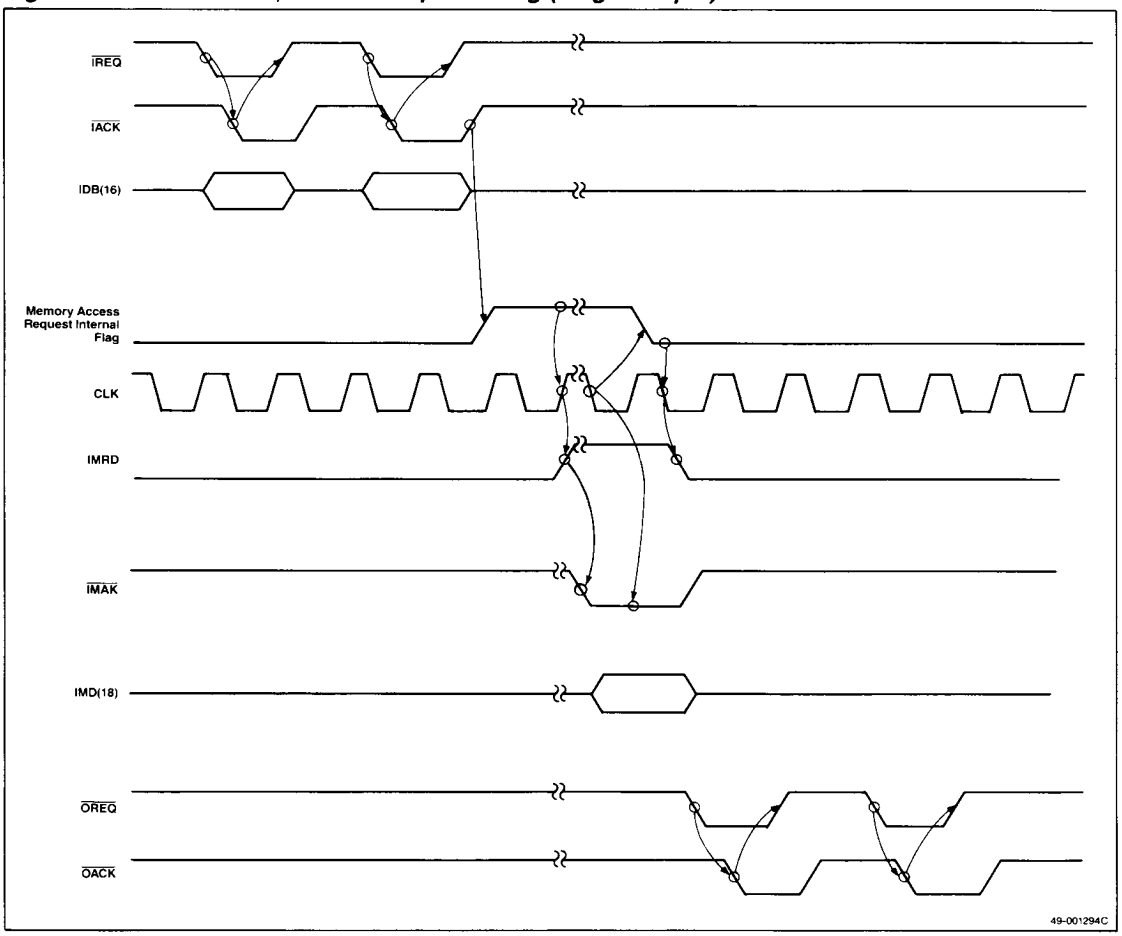


Figure 17. Read Data → μPD7281 Output Timing (Continuous Output)

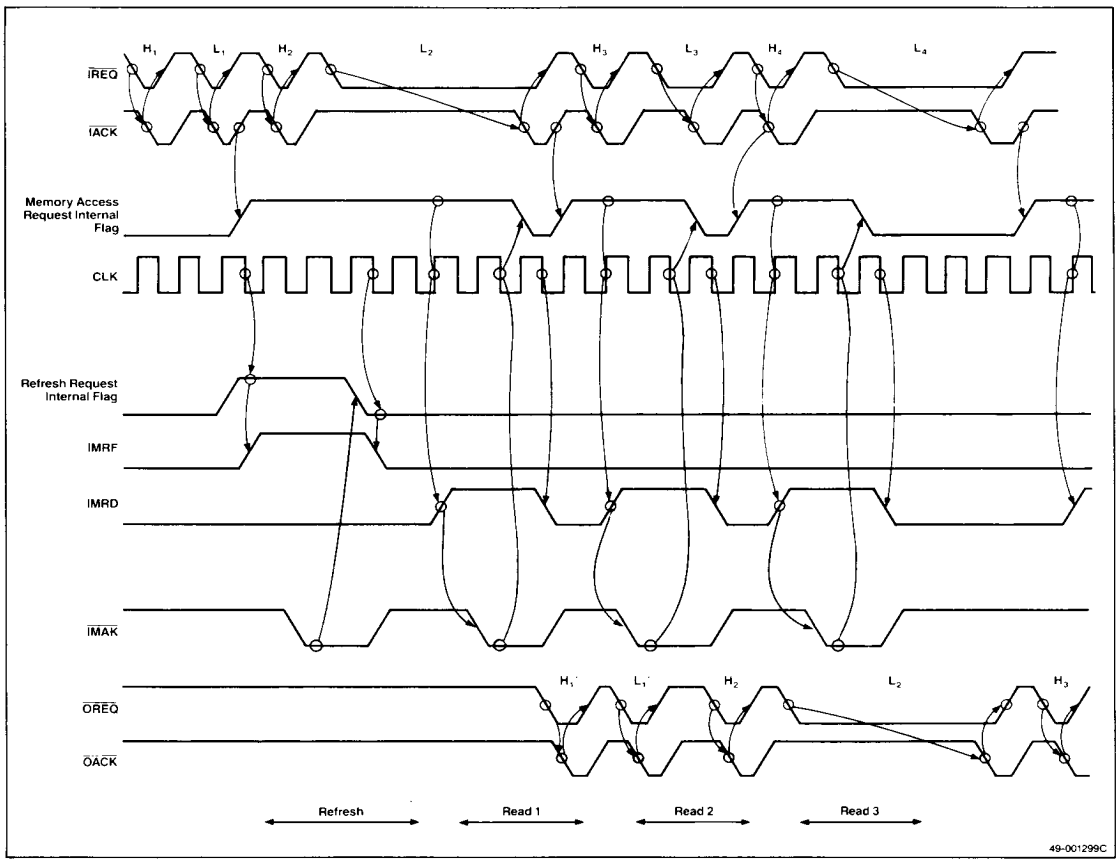
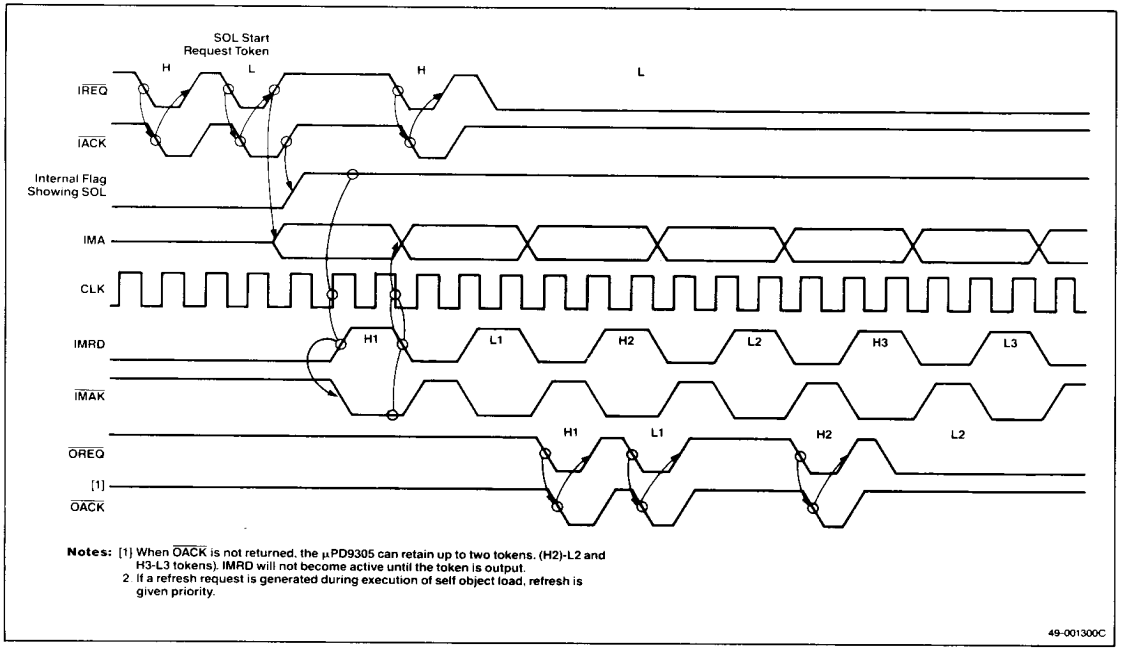


Figure 18. Self Object Load Timing



Notes: [1] When $\overline{OACK}$ is not returned, the μPD9305 can retain up to two tokens. (H2)-L2 and H3-L3 tokens). IMRD will not become active until the token is output.
2 If a refresh request is generated during execution of self object load, refresh is given priority.

Figure 19. Refresh Timing

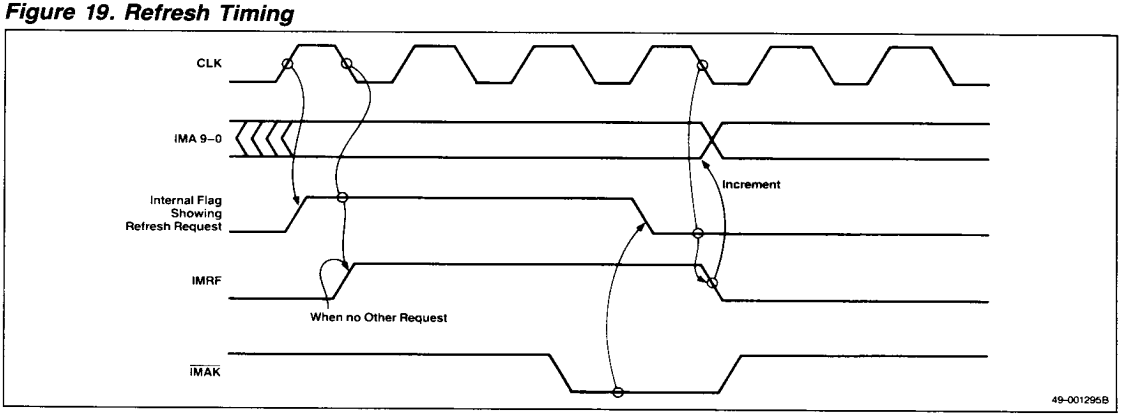


Figure 20. Read/Modify/Write Timing

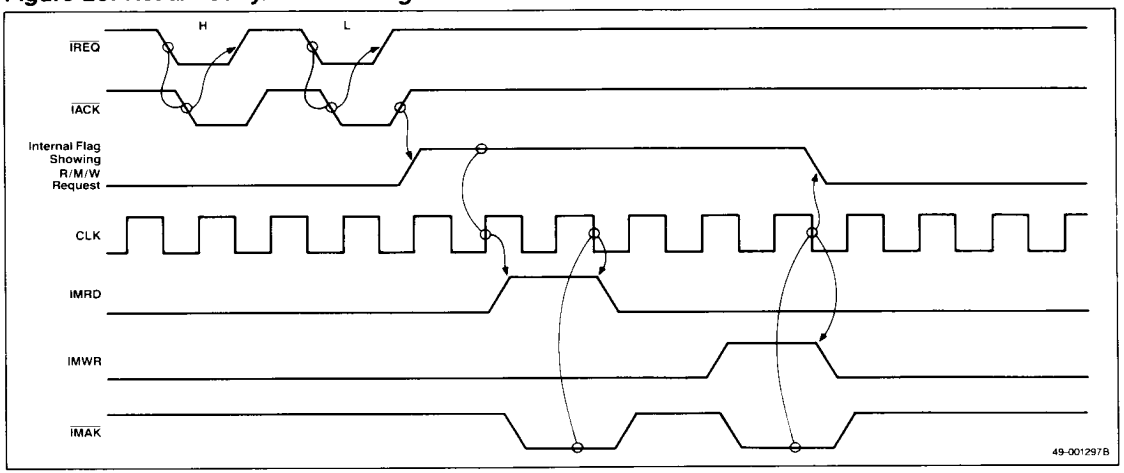


Table 5 shows the differences between command and external resets.

Figure 21 shows a typical system configuration using the μPD9305 with several ImPPs.

Table 5. Command and External Reset Differences

Item	RESET	Commmand Reset
I/O data counter; Tokens in the μPD9305; image memory access requests (except refresh); OREQ, IACK; DMA request	Cleared	Cleared
Refresh timer; refresh request; refresh address; mode register	Default values	No change
IPPRST pin	0 (active)	0 (active)

Figure 21. Typical System Configuration