

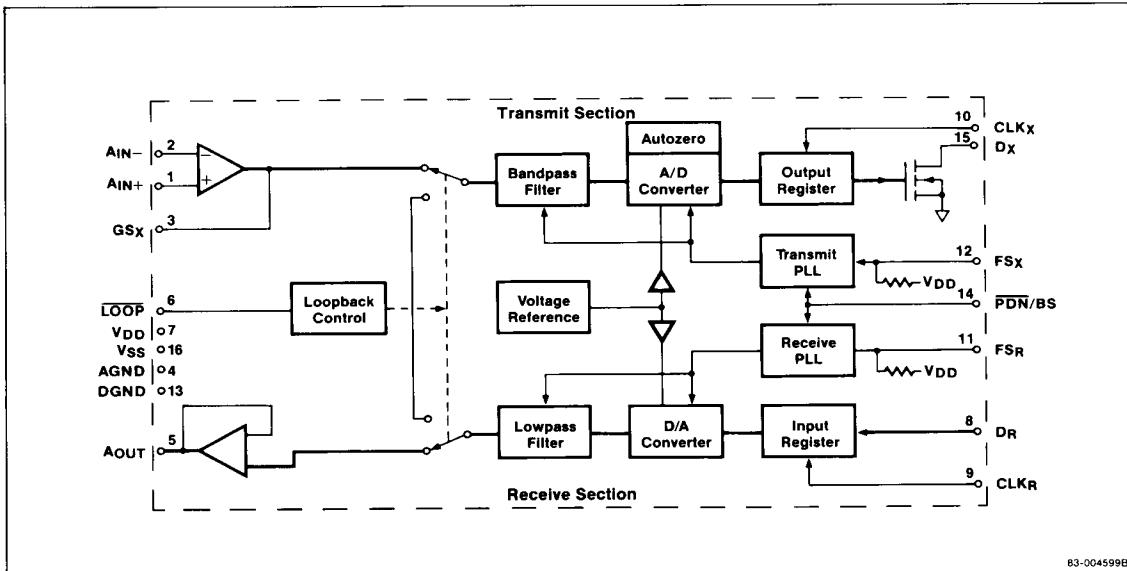
### Description

The  $\mu$ PD9601AD and  $\mu$ PD9602AD are PCM codec-filter combo chips, A-law and  $\mu$ -law compatible, respectively. These monolithic CMOS LSIs include phase-locked loops (PLL) that derive internal signal processing clocks from the transmit and receive frame sync clock inputs.

### Features

- Transmit input operational amplifier
- Transmit active lowpass filter and switched-capacitor bandpass filter
- Autozero circuit
- Receive unbalanced 600- $\Omega$  output power amplifier
- Receive switched-capacitor lowpass filter

### Block Diagram



- Digital serial I/O interface circuit
- A-law (9601AD) and  $\mu$ -law (9602AD) companding
- Precision reference voltage circuit
- Synchronous or asynchronous operation
- Data rate, 64 kb/s to 2.048 Mb/s
- Low power dissipation
  - 50 mW normal mode
  - 5 mW power-down or standby mode
- 16-pin ceramic DIP

### Ordering Information

Part No.	Companding	Package Type
$\mu$ PD9601AD	A-law	16-pin ceramic DIP (300 mil)
$\mu$ PD9602AD	$\mu$ -law	