DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD98402A

LOCAL ATM SONET FRAMER

The μPD98402A is one of the ATM-LAN LSIs and incorporates the TC sublayer function in the SONET/SDH-based physical layer of the ATM protocol. The main functions of the μPD98402A include a transmit function for mapping ATM cells received from the ATM layer onto the payload block of the SONET STS-3c/SDH STM-1 frame and sending them to PMD (Physical Media Dependent) in the physical layer, and a receive function for separating the overhead block and ATM cells from the data string received from the PMD sublayer and sending the ATM cells to the ATM layer.

Futhermore, the μPD98402A is compliant with the ATM Forum UNI Recommendations.

FEATURES

- Provision of TC sublayer function of ATM protocol physical layer
- Support of SONET STS-3c frame/SDH STM-1 frame format
- Provision of stop mode for cell scramble/descramble and frame scramble/descramble
- Disposal/transitory selection of unassigned cells is possible.
- Compliant with UTOPIA interface
- Incorporation of internal loopback function at PMD and ATM layer turns
- PMD interface
  - 155.52 Mbps serial interface
  - 19.44 MHz parallel interface
- Provided with registers for writing/reading overhead information
  - SOH (section overhead): C1 (1st to 3rd) bytes, F1 byte
  - LOH (line overhead): K2 byte
  - POH (pass overhead): F2 byte, C2 byte
- CMOS process
- +5 V single power supply

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- Incorporation of OAM (Operation And Maintenance) function

Transmitting side

Transmission of various alarms

- Transmission by generation of sources
  - Line RDI (FERF), Path RDI (FERF)
  - Line FEBE, Path FEBE
- Transmission by command instruction
  - Line AIS, Path AIS
  - Line FEBE, Path FEBE

Receiving side

- Detection of alarms and error signals
  - LOS (Loss Of Signal)
  - OOF (Out Of Frame)
  - LOF (Loss Of Frame)
  - LOP (Loss Of Pointer)
  - LOC (Loss Of Cell delineation)
  - Line RDI (FERF), Path RDI (FERF)
  - Line AIS, Path AIS
- Detection and display of quality deterioration sources
  - B1 error, B2 error, B3 error, Line FEBE, Path FEBE
- Incorporation of counter for counting number of performance monitoring errors
  - B1 byte error counter
  - B2 byte error counter
  - B3 byte error counter
  - Line FEBE error counter
  - Path FEBE error counter

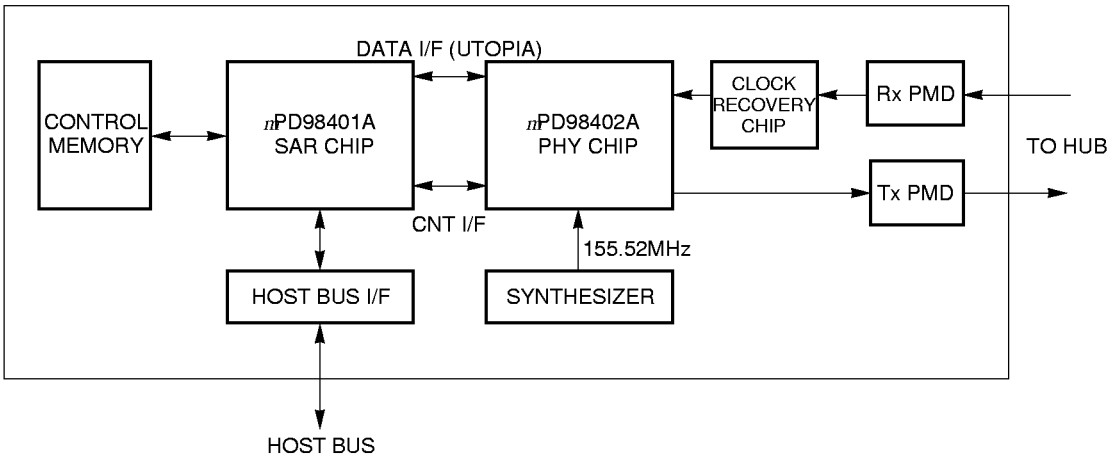
ORDERING INFORMATION

Part Number	Package
μPD98402AGM-KED	160-pin plastic QFP (FINE PITCH) (24 × 24 mm)

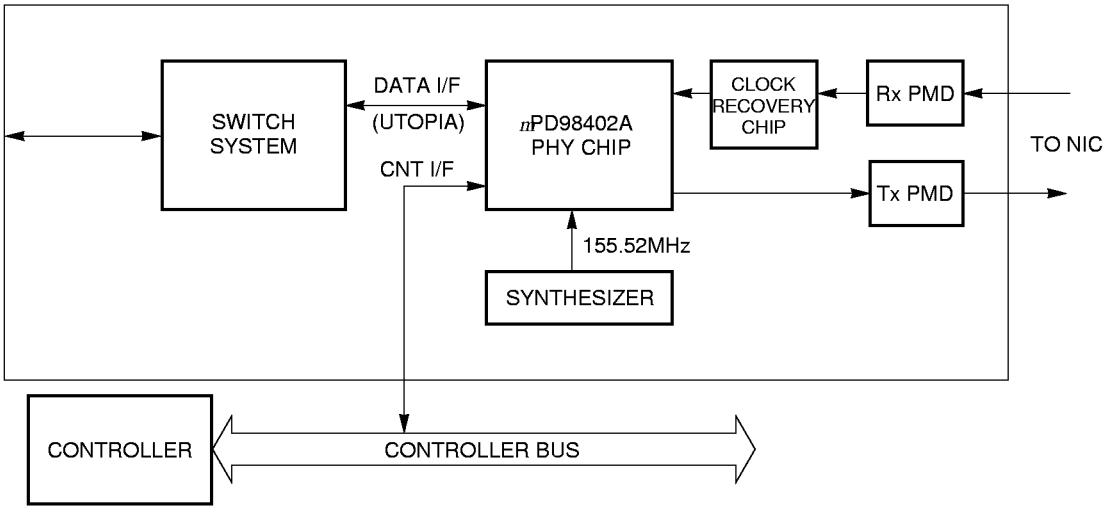
APPLICATION EXAMPLES

The followings are examples of the terminal equipment and the ATM Hub application using the μPD98402A.

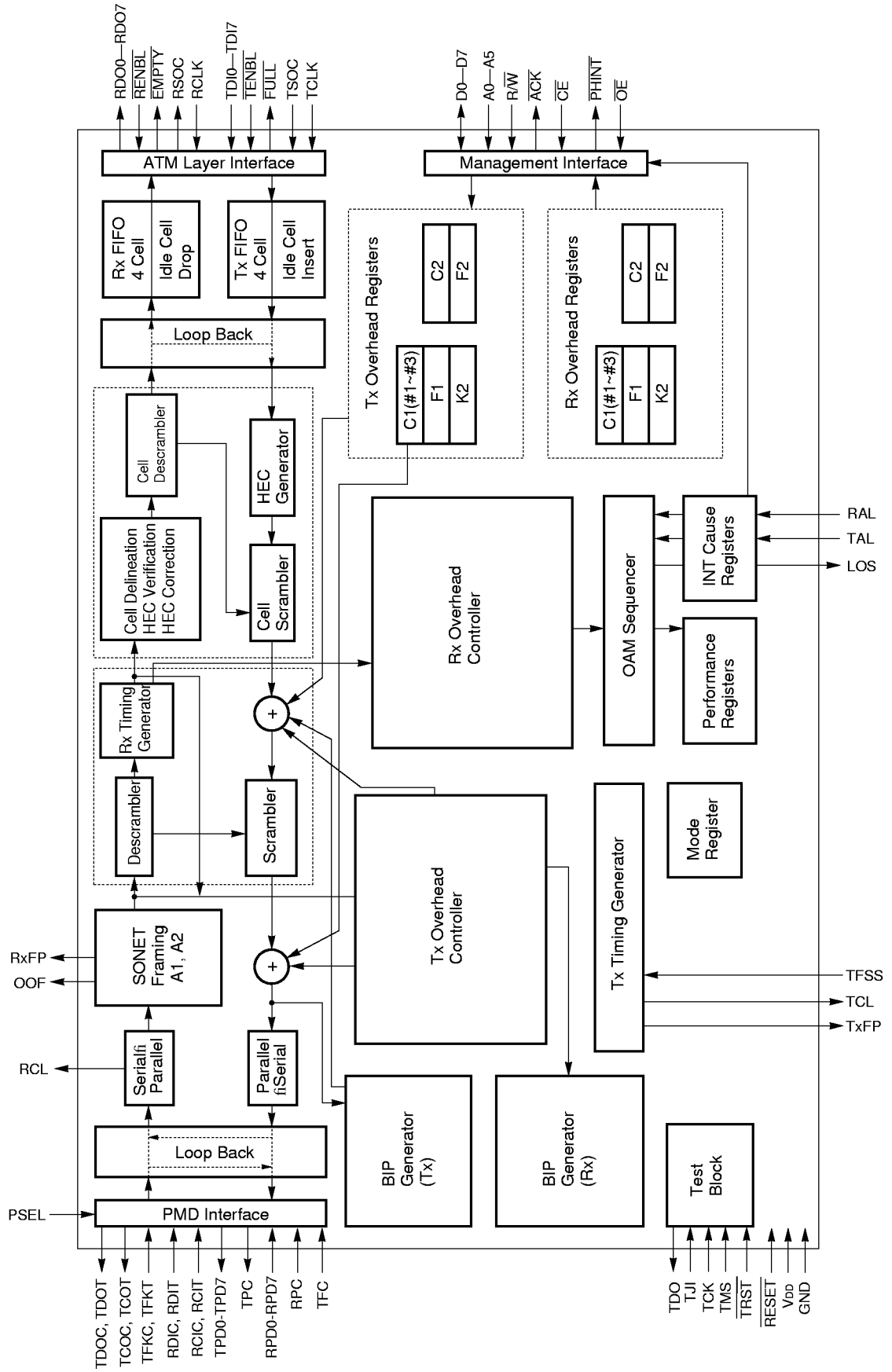
NIC APPLICATION



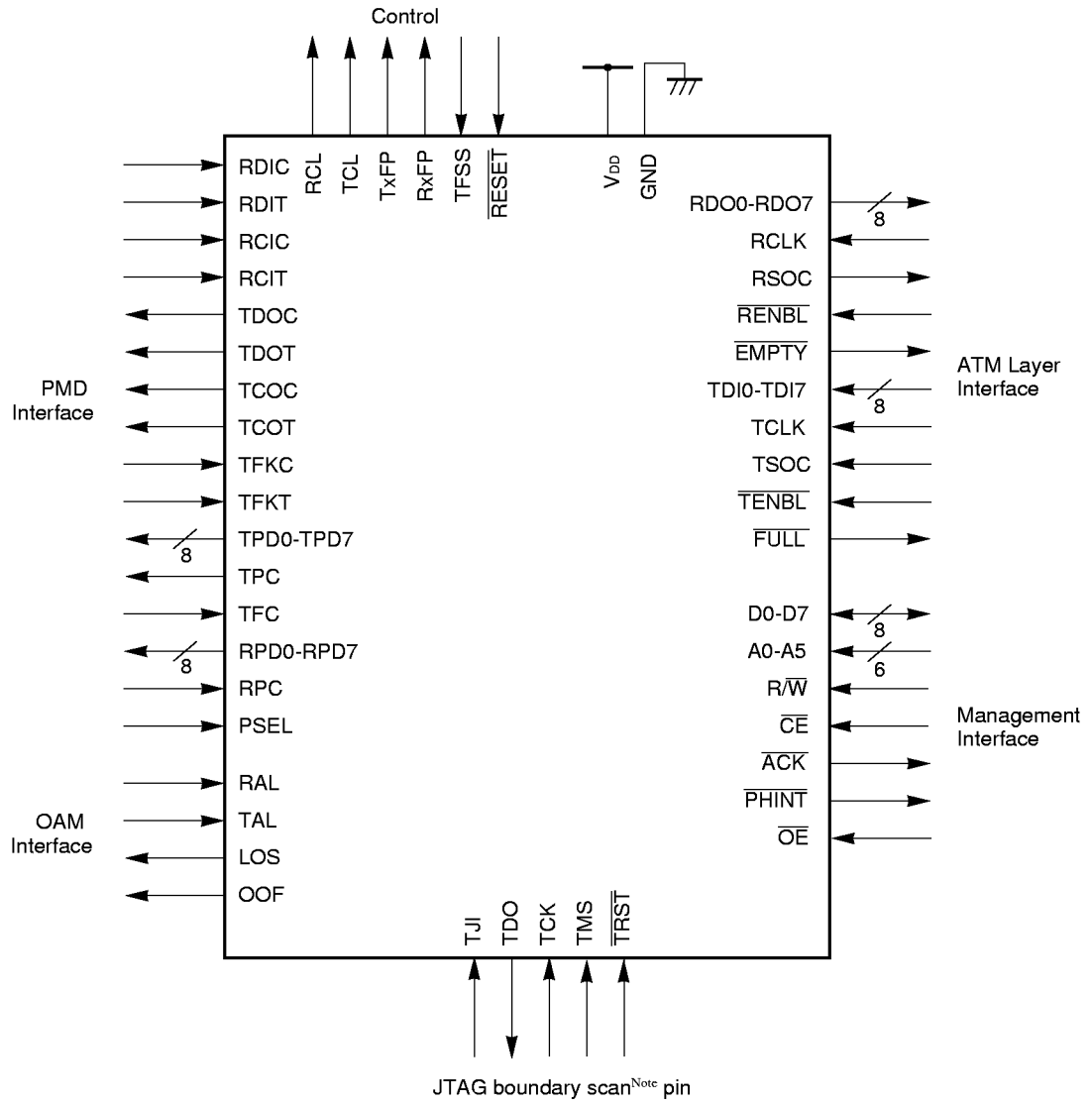
HUB APPLICATION (NIC SIDE)



BLOCK DIAGRAM



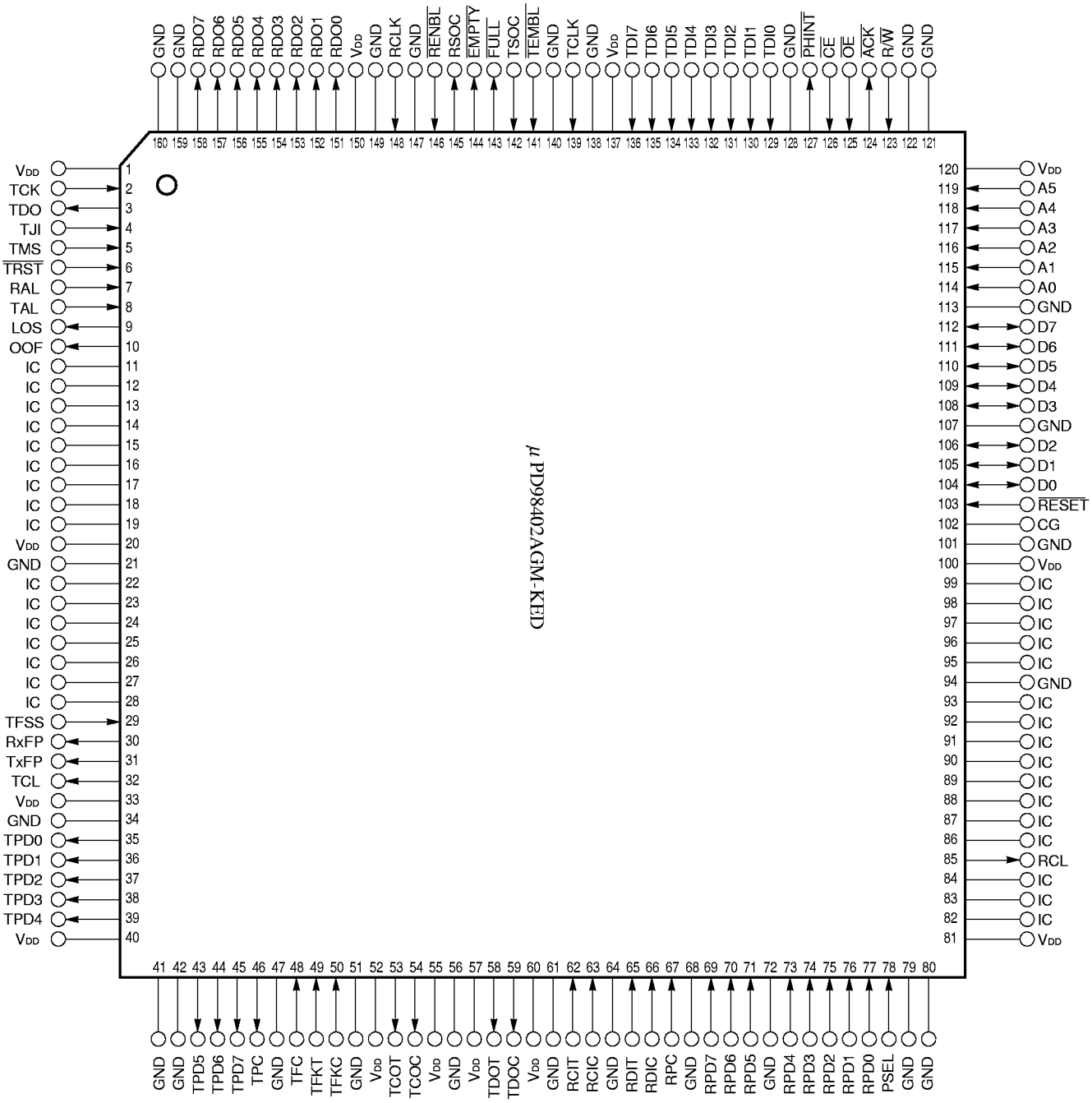
FUNCTIONAL PIN GROUPS



Note This function can be supported at the customer's request.

PIN CONFIGURATION

160-pin plastic QFP (FINE PITCH) (24 × 24 mm) (Top View)



Remarks 1. IC : Internally Connected. Leave open.

2. CG : Connect to GND.

A0-A5	: Address Bus
$\overline{ACK}$	: Read/write Cycle Receive Acknowledge
$\overline{CE}$	: Chip Enable
D0–D7	: Data Bus
$\overline{EMPTY}$	: Output Buffer Empty
$\overline{FULL}$	: Buffer Full
GND	: Ground
LOS	: Loss of Signal
$\overline{OE}$	: Output Enable
OOF	: Out of Frame
$\overline{PHINT}$	: Physical Interrupt
PSEL	: PMD I/F Select
RAL	: Receive Alarm
RCIC	: Receive Clock Input Complement
RCIT	: Receive Clock Input True
RCL	: Internal Receive System Clock
RCLK	: Receive Data Transferring Clock from the ATM Layer Device
RDIC	: Receive Data Input Complement
RDIT	: Receive Data Input True
RDO0-RDO7	: Receive Data Output
$\overline{RENBL}$	: Receive Data Enable
$\overline{RESET}$	: System Reset
RPC	: Receive Parallel Data Clock
RPD0-RPD7	: Receive Parallel Data
RSOC	: Receive Start Address of ATM Cell
R/$\overline{W}$	: Read/write Control
RxFP	: Receive Frame Pulse
TAL	: Transmit Alarm
TCK	: Test Clock
TCL	: Internal Transmit System Clock
TCLK	: Transmit Data Transferring Clock from the ATM Layer Device
TCOC	: Transmit Clock Output Complement
TCOT	: Transmit Clock Output True
TDI0-TDI7	: Transmit Data Input from the ATM Layer
TDO	: Test Data Output
TDOC	: Transmit Data Output Complement
TDOT	: Transmit Data Output True
$\overline{TENBL}$	: Transmit Data Enable
TFC	: Transmit Reference Clock
TFKC	: Transmit Reference Clock Complement
TFKT	: Transmit Reference Clock True
TFSS	: Transmit Frame Set Signal
TJI	: Test JTAG Data Input
TPC	: Transmit Parallel Data Clock
TPD0-TPD7	: Transmit Parallel Data
TMS	: Test Mode Select
$\overline{TRST}$	: Test Reset
TSOC	: Transmit Start Address of ATM Cell
TxFP	: Transmit Frame Pulse
V_{DD}	: Supply Voltage

1. PIN FUNCTIONS

- **PMD Interface**

Symbol	Pin No.	I/O	I/O Level	Function
RDIC	66	I	Pseudo ECL Complement (–)	These pins are used to input receive serial data when serial interface mode is used (PSEL pin input = low level). Ground them when Parallel interface mode is used.
RDIT	65	I	Pseudo ECL True (+)	
RCIC	63	I	Pseudo ECL Complement (–)	These pins are used to input the receive system clock when serial interface mode is used (PSEL pin input = low level). Clocks are input in synchronization with receive data. Ground them when parallel interface mode is used.
RCIT	62	I	Pseudo ECL True (+)	
TDOC	59	O	Pseudo ECL Complement (–)	These pins are used to output transmit serial data when serial interface mode is used (PSEL pin input = low level). They are open-drain pins. Terminate them with V_{DD} –2 V via a 50 Ω resistor. To be undefined after reset.
TDOT	58	O	Pseudo ECL True (+)	
TCOC	54	O	Pseudo ECL Complement (–)	These pins are used to output transmit clocks when serial interface mode is used (PSEL pin input = low level). Transmit clocks to be input to the TFKC/TFKT pins are output passing through internal gates. They are open-drain pins. Terminate them with V_{DD} –2 via a 50 Ω resistor. To be undefined after reset.
TCOT	53	O	Pseudo ECL True (+)	
TFKC	50	I	Pseudo ECL Complement (–)	These pins are used to input transmit system clocks when serial interface mode is used (PSEL pin input = low level). Transmit data output from the TDOC/TDOT pins is output in synchronization with clocks that are input to these pins. Ground them when parallel interface mode is used.
TFKT	49	I	Pseudo ECL True (+)	
RPD0-RPD7	77-73, 71-69	I	TTL	These pins are used to input receive parallel data when parallel interface mode is used (PSEL pin input = high level). Leave them open when serial interface mode is used.
RPC	67	I	TTL	This pin is used to input the receive system clock when parallel interface mode is used (PSEL pin input = high level). Input clocks synchronous with the receive data. Leave it open when serial interface mode is used.
TPD0-TPD7	35-39, 43-45	O	CMOS	These pins are used to output transmit parallel data when parallel interface mode is used (PSEL pin input = high level). Leave them open when serial interface mode is used.
TPC	46	O	CMOS	This pin is used to output transmit clocks when parallel interface mode is used (PSEL pin input = high level). Transmit clocks to be input to the TFC pin are output passing through internal gates. Leave it open when serial interface mode is used.
TFC	48	I	TTL	This pins is used to input transmit system clocks when parallel interface mode is used (PSEL pin input = high level). Transmit data output from pins TPD0 to TPD7 are output in synchronization with the clocks input to this pin. Leave it open when serial interface mode is used.
PSEL	78	I	CMOS	This pin is used to select the mode for PMD interface serial/ parallel interface. Low level: Serial interface mode High level: Parallel interface mode

- **Power supply**

Symbol	Pin No.	I/O	Function
V_{DD}	1, 20, 33, 40, 52, 55, 57, 60, 81, 100, 120, 137, 150	–	Supply voltage, 5 V ±5 %
GND	21, 34, 41, 42, 47, 51, 56, 61, 64, 68, 72, 79, 80, 94, 101, 107, 113, 121, 122, 128, 138, 140, 147, 149, 159, 160	–	Ground

- **ATM Layer Interface**

Symbol	Pin No.	I/O	I/O Level	Function
RDO0-RDO7	151-158	O	CMOS	Connected to 8-bit data bus to output the receive data to the ATM Layer device. Output is synchronized with the RCLK rising up. To be undefined after reset.
RCLK	148	I	TTL	Input pin of the receive data transferring clock from the ATM Layer device.
RSOC	145	O	CMOS	Receive cell start address signal. To the ATM Layer device, this signal indicates the start address byte of the receive ATM cell. To be undefined after reset.
$\overline{\text{RENBL}}$	146	I	TTL	Receive enable signal. Input pin of the signal indicating that the ATM layer device can receive data.
$\overline{\text{EMPTY}}$	144	O	CMOS	Output buffer empty signal. This signal indicates that there is no data to be transferred to the receive FIFO of the μPD98402A. To be inactive after reset.
TDI0-TDI7	129-136	I	TTL	8-bit data bus to input the transmit data from the ATM Layer device. Reading a data on the bus is synchronized with the TCLK rising-up.
TCLK	139	I	TTL	Input pin of the transmit data transferring clock from the ATM layer device.
TSOC	142	I	TTL	Transmit cell start address signal. Input pin of the signal indicating the start byte of the transmit ATM cell input from the ATM Layer device to the μPD98402A.
$\overline{\text{TENBL}}$	141	I	TTL	Transmit enable signal. This signal indicates that the ATM Layer device is transmitting the valid data to the TDI0-TDI7.
$\overline{\text{FULL}}$	143	O	CMOS	Input buffer full signal. When 4 bytes remain as the acceptable bytes of transmit FIFO at last, this signal changes to active. To be inactive after reset.

- **Management Interface**

Symbol	Pin No.	I/O	I/O Level	Function
D0-D7	104-106 108-112	I/O	CMOS	8-bit data bus for data transfer between the control processor and the internal register of the μPD98402A.
A0-A5	114-119	I	TTL	Address bus. Used for setting the internal register address of the μPD98402A.
R/$\overline{W}$	123	I	TTL	Read/write control signal. Low level: Write cycle High level: Read cycle
$\overline{CE}$	126	I	TTL	Chip enable signal. At low level, internal register access is to be enable.
$\overline{ACK}$	124	O	CMOS	Read/write cycle receive acknowledge or ready signal. After reset, this signal indicates inactive level.
$\overline{PHINT}$	127	O	CMOS	Signal which indicates the interrupt cause occurrence to the processor. After reset, this signal indicates inactive level.
$\overline{OE}$	125	I	TTL	Output enable. When this signal is set to low level, the μPD98402A outputs data to the control bus. Even if the $\overline{CE}$ signal is inactive, when this signal is at low level, the μPD98402A drives the control bus.

- **OAM Interface**

Symbol	Pin No.	I/O	I/O Level	Function
LOS	9	O	CMOS	Loss of signal detection. Output high level when receive serial data input is "0" for 50 μs continuously or optical input stop signal (RAL) is input. When 2 consecutive frames of valid synchronous pattern is detected, or when input of the optical input stop signal is released, low level is output. To be inactive after reset.
OOF	10	O	CMOS	Out of frame detection. When 4 consecutive frames of wrong synchronous pattern are detected, high level is output. When 2 consecutive frames of normal synchronous pattern are detected, low level is output. To be inactive after reset.
RAL	7	I	TTL	Receive alarm. Inputs receiver-side optical input stop signal by the optical module. Low level: Normal High level: Optical input stopped.
TAL	8	I	TTL	Transmit alarm. Inputs transmit-side optical output stop signal output by the optical module. Low level: Normal High level: Optical output stopped.

- **Control**

Symbol	Pin No.	I/O	I/O Level	Function
TFSS	29	I	TTL	This is the transmit frame setting signal input pin. It allows synchronization timing of transmit frame output to be set. The μPD98402A samples this input signal by the internal transmit system clock (TCL). Initial output of the transmit frame is restarted 9 clocks into TCL clock cycle after a high level is latched at TCL rise.
$\overline{\text{RESET}}$	103	I	TTL	This is the system reset signal input pin. It initializes the μPD98402A. It is necessary to input a reset signal with a pulse width of 2 cycles or more of the clock that has the longest cycle among the following clocks input to the μPD98402A. ATM layer : TCLK, RCLK clock cycles PMD layer : 1/8 cycle of TFKT/TFKC, RCIC/RCIT clocks, TFC, RPC clock cycles Immediately after a reset, no read/write is possible to registers during 5 clocks of the TCL clock (19.44 MHz).
TCL	32	O	CMOS	This pin is used to output an internal transmit system clock. The μPD98402A outputs as the internal transmit system clock, the TFKT/TFKC input clock (155.52 MHz) scaled by 8 in serial interface mode, and the TFC input clock (19.44 MHz) in parallel interface mode.
RCL	85	O	CMOS	This pin is used to output an internal receive system clock. The μPD98402A outputs as the internal receive system clock, the RCIC/RCIT input clock (155.52 MHz) scaled by 8 in serial interface mode, and the RFC input clock (19.44 MHz) in parallel interface mode.
TxFP	31	O	CMOS	This is a frame pulse signal on the transmitting side. It outputs pulses synchronous with the transmit frame start. To be inactive after reset.
RxFP	30	O	CMOS	This is a frame pulse signal on the receiving side. It outputs pulses synchronous with the receive frame start. To be inactive after reset.

- **JTAG boundary scan pins (This function can be supported at the customer's request.)**

Symbol	Pin No.	I/O	I/O Level	Function
TJI	4	I	TTL	This is a pin for JTAG boundary scan. Pull it up or ground it in normal operation.
TDO	3	O	CMOS	This is a pin for JTAG boundary scan. Leave it open in normal operation.
TCK	2	I	TTL	This is a pin for JTAG boundary scan. Pull it up or ground it in normal operation.
TMS	5	I	TTL	This is a pin for JTAG boundary scan. Pull it up or ground it in normal operation.
$\overline{\text{TRST}}$	6	I	TTL	This is a pin for JTAG boundary scan. Ground it in normal operation.

- **Recommended Connection for Unused Pins**

Pin	Recommended connection
TDOC, TDOT, TCOC, TCOT, $\overline{\text{ACK}}$, LOS, OOF, TCL, TxFP, RxFP	leave open
RAL, TAL, TFSS	connect to GND

2. ELECTRICAL SPECIFICATION

Absolute maximum ratings

Parameters	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		–0.5 to +6.5	V
Input/output voltage	V_I/V_O		–0.5 to V_{DD} +0.5	V
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		–65 to +150	°C

Caution Exposure to absolute maximum ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The parameters apply independently. The device should be operated within the limits specified under DC and AC characteristics.

Capacitance

Parameters	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f = 1 MHz		10	20	pF
Output capacitance	C_O			10	20	pF
Input/output capacitance	C_{IO}			10	20	pF

Recommended operating conditions

Parameters	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}		4.75		5.25	V
Operating ambient temperature	T_A		0		+70	°C
Low level input voltage	V_{IL1}	**Note1**	0		+0.8	V
	V_{IL2}	**Note2**	V_{DD}–2		V_{DD}–1.5	
	V_{IL3}	**Note3**	0		0.3 V_{DD}	
High level input voltage	V_{IH1}	**Note1**	2.2		V_{DD}	V
	V_{IH2}	**Note2**	V_{DD}–1.1		V_{DD}	
	V_{IH3}	**Note3**	0.7 V_{DD}		V_{DD}	

Notes 1. TTL input pin
2. Pseudo ECL input pin
3. CMOS input pin

DC Characteristics (V_{DD} = 5 V ±0.25 V, T_A = 0 to +70 °C)

Parameters	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Off-state output current	I_{OZ}	$V_I = V_{DD}$ or GND Note1	—		10	μA
Input leak current	I_{LI1}	$V_I = V_{DD}$ or GND Note2	—		10	μA
	I_{LI2}	**Note 3**	—		10	
High level output voltage	V_{OH1}	I_{OH} = –0.5 mA Note4	0.7 V_{DD}		—	V
	V_{OH2}	**Note 5**	V_{DD}–0.9		V_{DD}–0.4	
Low level output voltage	V_{OL1}	I_{OL} = 6.0 mA Note4	—		0.4	V
	V_{OL2}	**Note 5**	V_{DD}–2.0		V_{DD}–1.7	
Supply current	I_{DD}	Normal operation	—		300	mA

Notes 1. 3-state data bus
2. TTL input pin
3. Pseudo ECL input pin
4. CMOS output pin
5. Pseudo ECL output pin

AC Characteristics

(1) Management Interface

Internal Register Read/Write

Parameters	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
A0-A5 setup time (to $\overline{CE}\downarrow$)	t_{SCC1}		5			ns
R/$\overline{W}$ setup time (to $\overline{CE}\downarrow$)	t_{SCC2}		5			
A0-A5 hold time (to $\overline{CE}\downarrow$)	t_{HCC1}		3			ns
R/$\overline{W}$ hold time (to $\overline{CE}\downarrow$)	t_{HCC2}		3			
$\overline{CE}\downarrow\rightarrow\overline{ACK}\downarrow$ delay time (read)	t_{DCNAR}	Load capacitor 15 pF At parallel data input	3 × t_{CYPPR}		4.5 × t_{CYPPR}	ns
		Load capacitor 15 pF At serial data input	3 × (t_{CYPSR} × 8)		4.5 × (t_{CYPSR} × 8)	
$\overline{CE}\downarrow\rightarrow\overline{ACK}\downarrow$ delay time (write)	t_{DCNAW}	Load capacitor 15 pF At parallel data input	2 × t_{CYPPR}		3.5 × t_{CYPPR}	ns
		Load capacitor 15 pF At serial data input	2 × (t_{CYPSR} × 8)		3.5 × (t_{CYPSR} × 8)	
$\overline{CE}\uparrow\rightarrow\overline{ACK}\uparrow$ delay time	t_{DCPA}	Load capacitor 15 pF At parallel data input	1 × t_{CYPPR}		2.5 × t_{CYPPR}	ns
		Load capacitor 15 pF At serial data input	1 × (t_{CYPSR} × 8)		2.5 × (t_{CYPSR} × 8)	
$\overline{CE}\downarrow\rightarrow$ data output delay time	t_{DCD}	Load capacitor 15 pF At parallel data input	2 × t_{CYPPR}		3.5 × t_{CYPPR}	ns
		Load capacitor 15 pF At serial data input	2 × (t_{CYPSR} × 8)		3.5 × (t_{CYPSR} × 8)	
$\overline{OE}\downarrow\rightarrow$ data output delay time	t_{DOD}	Load capacitor 15 pF	—		9.4	ns
$\overline{OE}\uparrow\rightarrow$ data floating output delay time	t_{FOD}	Load capacitor 15 pF	—		10	ns
D0-D7 setup time (to $\overline{CE}\downarrow$)	t_{SDC}		5		—	ns
D0-D7 hold time (to $\overline{CE}\downarrow$)	t_{HCD}		3		—	ns
$\overline{CE}$ low-level width	t_{CEBW}	At parallel data input	3.5 × t_{CYPPR}		—	ns
		At serial data input	3.5 × (t_{CYPSR} × 8)		—	
$\overline{OE}$ low-level width	t_{OEBW}	At parallel data input	2.5 × t_{CYPPR}		—	ns
		At serial data input	2.5 × (t_{CYPSR} × 8)		—	

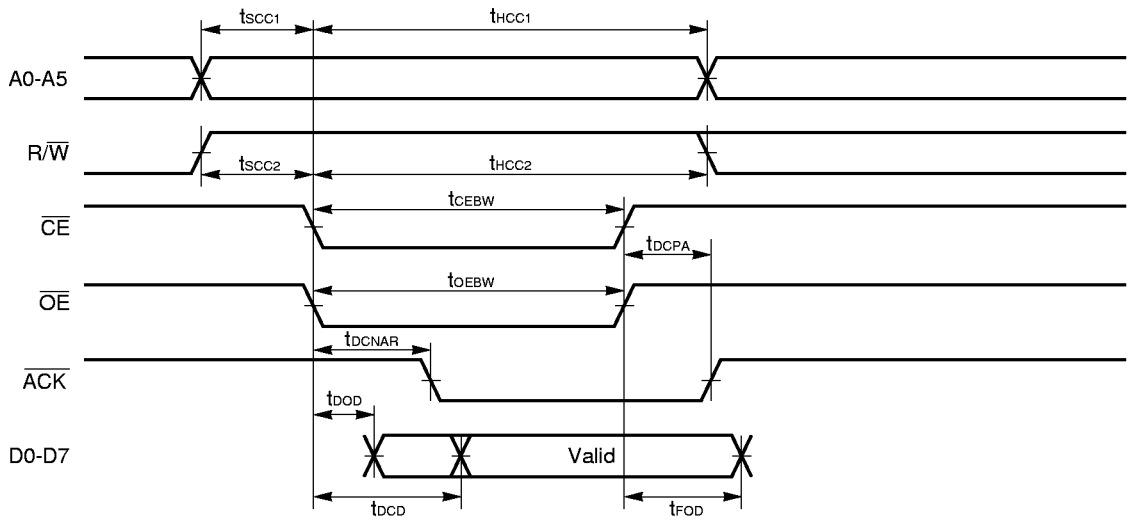
Remarks 1. For t_{CYPPR}, refer to **(6) PMD parallel interface timing**.

2. For t_{CYPSR}, refer to **(7) PMD serial interface timing**.

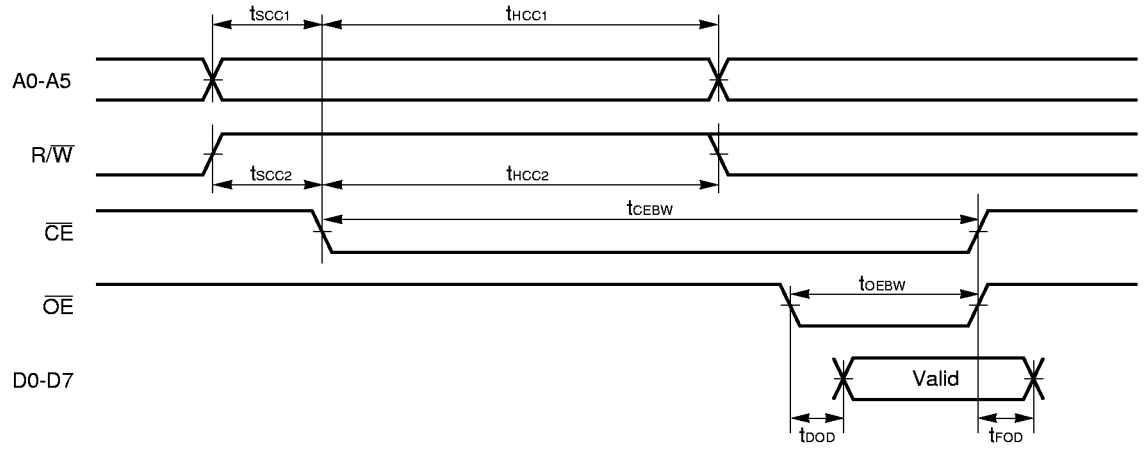
Management Interface

Internal Register Read

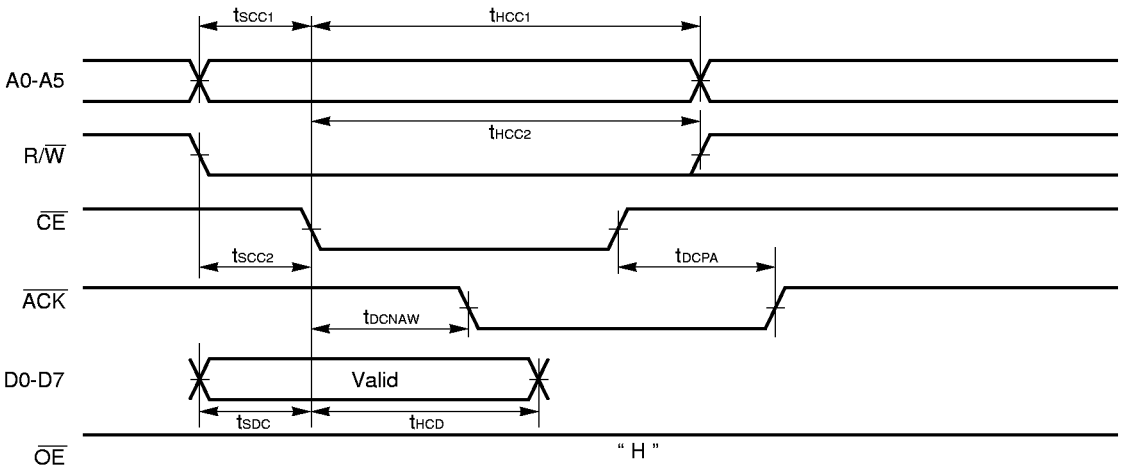
(a) Case 1 When the host uses $\overline{ACK}$ signal



(b) Case 2 When the host does not use $\overline{ACK}$ signal



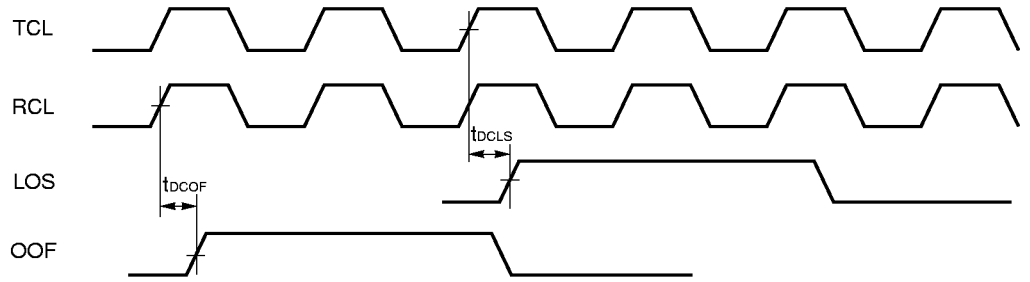
Internal Register Write



(2) OAM Interface

Parameters	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
TCL↑→LOS delay time	t_{DCLS}	load capacitor = 15 pF	5		30	ns
RCL↑→OOF delay time	t_{DCOF}	load capacitor = 15 pF	–5		+7	ns

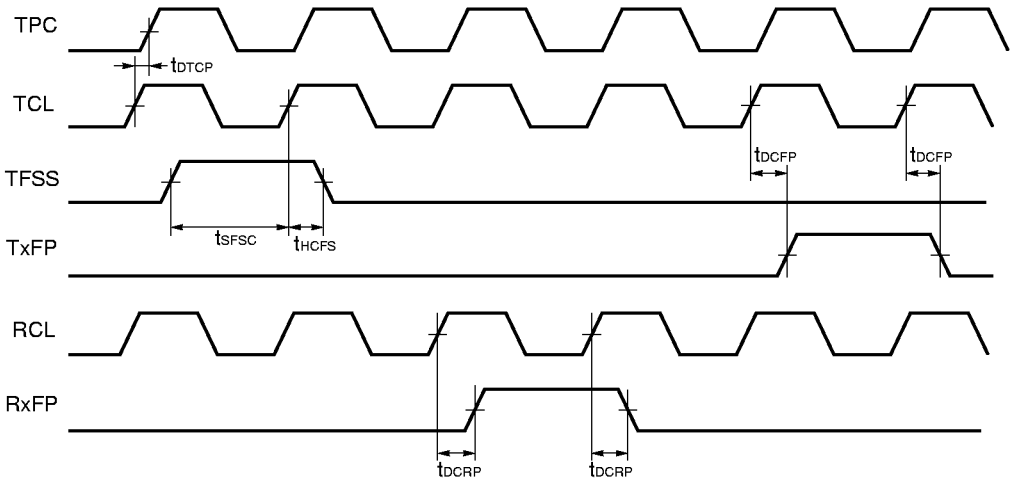
OAM Interface



(3) Control Signal Interface

Parameters	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
TCL↑→TPC delay time	t_{DTCP}	load capacitor = 15 pF	0		+5	ns
TFSS setup time (to TCL↑)	t_{SFSC}		10		—	ns
TFSS hold time (to TCL↑)	t_{HCFS}		5		—	ns
TCL↑→TxFP delay time	t_{DCFP}	load capacitor = 15 pF	0		+20	ns
RCL↑→RxFP delay time	t_{DCRP}	load capacitor = 15 pF	–5		+20	ns

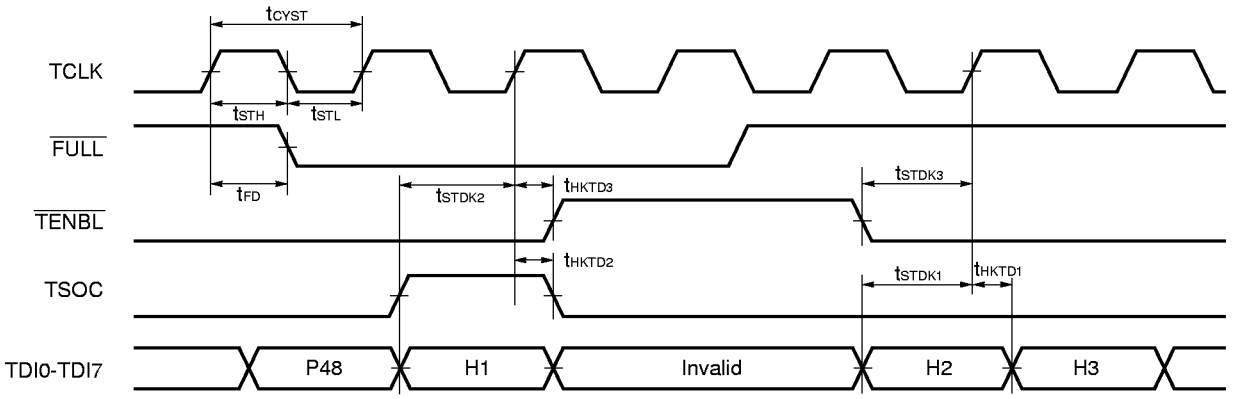
Control Signal Interface



(4) SAR Interface (Transmitter Side)

Parameters	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
TCLK cycle time	t_{CYST}		30		125	ns
TCLK high level width	t_{STH}		12		110	ns
TCLK low level width	t_{STL}		12		110	ns
TCLK↑→$\overline{\text{FULL}}$↓ delay time	t_{FD}	load capacitor = 15 pF	5		17	ns
TDI0-TDI7 setup time (to TCLK↑)	t_{STDK1}		5		—	ns
TSOC setup time (to TCLK↑)	t_{STDK2}		12		—	ns
$\overline{\text{TENBL}}$ setup time (to TCLK↑)	t_{STDK3}		5		—	ns
TDI0-TDI7 hold time (to TCLK↑)	t_{HKTD1}		3		—	ns
TSOC hold time (to TCLK↑)	t_{HKTD2}		3		—	ns
$\overline{\text{TENBL}}$ hold time (to TCLK↑)	t_{HKTD2}		3		—	ns

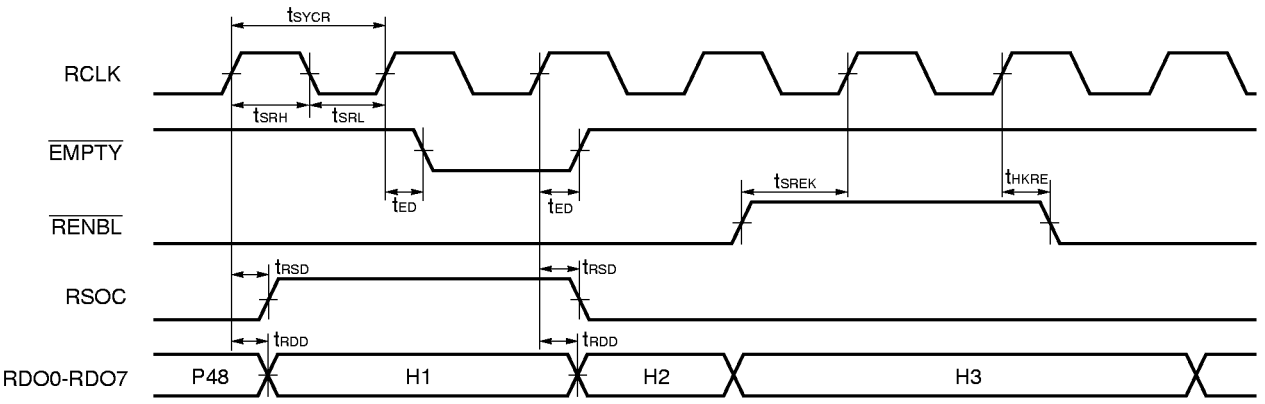
SAR Interface (Transmitter Side)



(5) SAR Interface (Receiver Side)

Parameters	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
RCLK cycle time	t_{SYCR}		30		125	ns
RCLK high level width	t_{SRH}		12		110	ns
RCLK low level width	t_{SRL}		12		110	ns
RCLK↑→$\overline{\text{EMPTY}}$↑↓delay time	t_{ED}	load capacitor = 15 pF	5		17	ns
$\overline{\text{RENBL}}$ setup time (to RCLK↑)	t_{SREK}		12		—	ns
$\overline{\text{RENBL}}$ hold time (to RCLK↑)	t_{HKRE}		3		—	ns
RCLK↑→RSOC↑↓ delay time	t_{RSD}	load capacitor = 15 pF	0		17	ns
RCLK↑→RDO0-RDO7 delay time	t_{RDD}	load capacitor = 15 pF	0		17	ns

SAR Interface (Receiver Side)

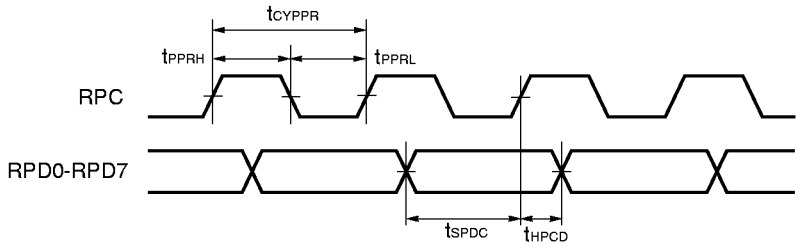


(6) PMD Parallel Interface

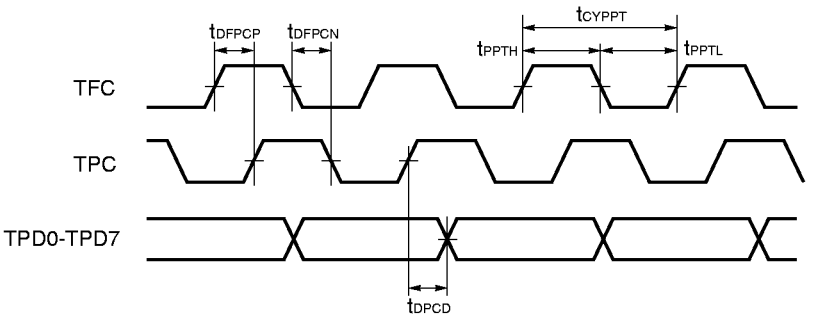
Parameters	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
RPC cycle time	t_{CYPPR}		50		—	ns
RPC high level width	t_{PPRH}		20		—	ns
RPC low level width	t_{PPRL}		20		—	ns
TFC cycle time	t_{CYPPT}		50		—	ns
TFC high level width	t_{PPTH}		20		—	ns
TFC low level width	t_{PPTL}		20		—	ns
RPD0-RPD7 setup time (to RPC↑)	t_{SPDC}		5		—	ns
RPD0-RPD7 hold time (to RPC↑)	t_{HPCD}		3		—	ns
TFC↑→TPC↑ delay time	t_{DFPCP}	load capacitor = 15 pF	3		25	ns
TFC↓→TPC↓ delay time	t_{DFPCN}	load capacitor = 15 pF	3		25	ns
TPC↑→TPD0-TPD7 delay time	t_{DPCD}	load capacitor = 15 pF	–3.0		+1.0	ns

PMD Parallel Interface

Receive Side



Transmit Side

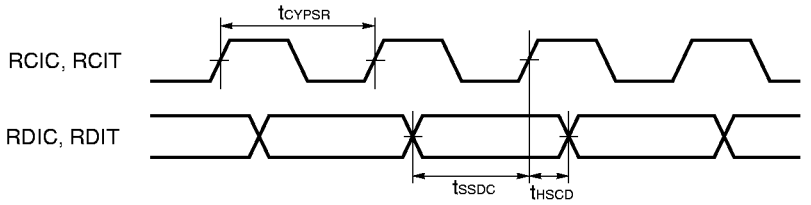


(7) PMD Serial Interface

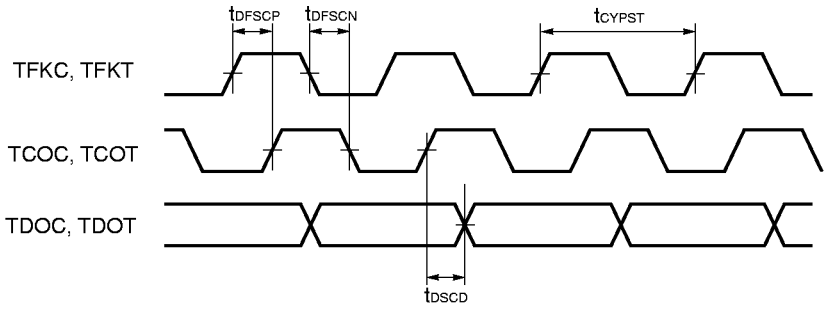
Parameters	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
RCIT (RCIC) cycle time	t_{CYPSR}		6.4		—	ns
TFKT (TFKC) cycle time	t_{CYPST}		6.4		—	ns
Serial data setup time	t_{SSDC}		1.0		—	ns
Serial data hold time	t_{HSCD}		1.0		—	ns
Serial clock delay time (rising)	t_{DFSCP}	Load capacitor 15 pF	—		8	ns
Serial clock delay time (falling)	t_{DFSCN}	Load capacitor 15 pF	—		8	ns
Transmit serial data delay time	t_{DSCD}	Load capacitor 15 pF	—		3	ns

PMD Serial Interface

Receive Side

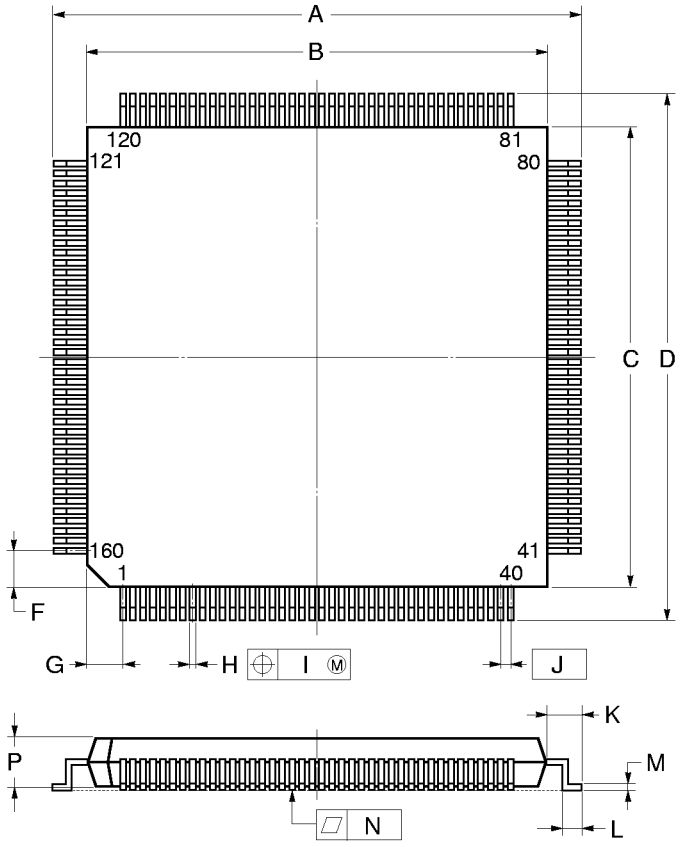


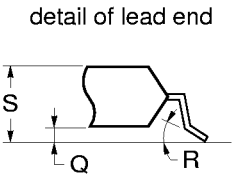
Transmit Side



3. PACKAGE DRAWING

160 PIN PLASTIC QFP (FINE PITCH) (□24)





NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	26.0±0.2	$1.024^{+0.008}_{-0.009}$
B	24.0±0.2	0.945±0.008
C	24.0±0.2	0.945±0.008
D	26.0±0.2	$1.024^{+0.008}_{-0.009}$
F	2.25	0.089
G	2.25	0.089
H	$0.22^{+0.05}_{-0.04}$	0.009±0.002
I	0.10	0.004
J	0.5 (T.P.)	0.020 (T.P.)
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
L	0.5±0.2	$0.020^{+0.008}_{-0.009}$
M	$0.17^{+0.03}_{-0.07}$	$0.007^{+0.001}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.125±0.075	0.005±0.003
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

S160GM-50-3ED, JED, KED-2

4. RECOMMENDED SOLDERING CONDITIONS

For the μPD98402A, soldering must be performed under the following conditions.

For details of recommended conditions for surface mounting, refer to information document **"Semiconductor Device Mounting Technology Manual" (IEI-1207)**.

For other soldering methods, please consult with NEC sales personnel.

- **μPD98402AGM-KED: 160-pin plastic QFP (FINE PITCH) (24 × 24 mm)**

Soldering Method	Soldering Conditions	Symbol
Infrared reflow	Package peak temperature: 235 °C, time: 30 sec. max. (over 210 °C), count: twice or less, restriction days: 3[Note] (after that, 125 °C pre-baking for 20 hours is necessary) Precautions: (1) Reflow a second time should be started when the device temperature has returned to its normal state after the first reflow. (2) Avoid flux cleaning with water after the first reflow.	IR35-203-2
Pin partial heating	Pin temperature: 300 °C max., time: 3 seconds max. (per side)	—

Note This means the number of days after unpacking the dry pack. Storage conditions are 25 °C and 65 % RM max.