NEC®

MASTER/SLAVE D FLIP-FLOP

UPG700B
UPG700P

FEATURES

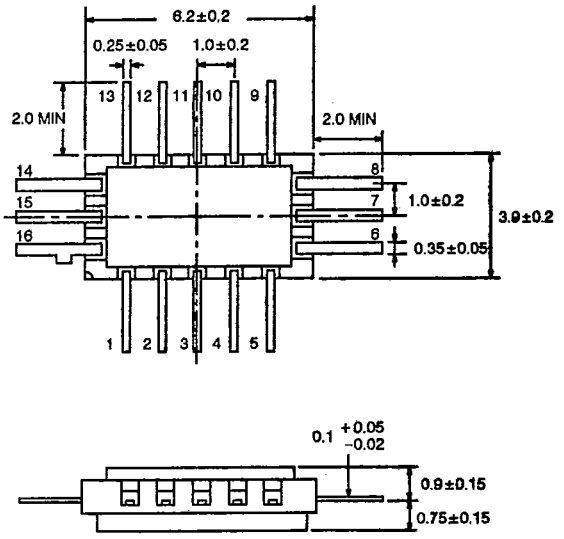
- **LOGIC LEVELS AND SUPPLY VOLTAGES ARE ECL COMPATIBLE**
- **ULTRA HIGH SPEED**
  (Typ. Operating Clock Frequency-3.2 GHz)
- **HERMETICALLY SEALED PACKAGE ASSURES HIGH RELIABILITY**

DESCRIPTION AND APPLICATIONS

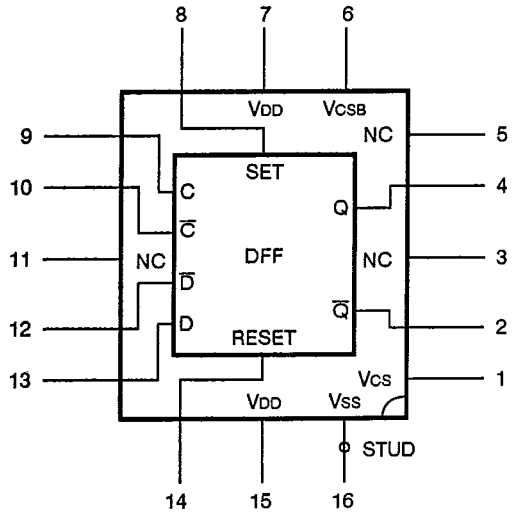
The UPG700B is an ultra high speed GaAs digital integrated circuit. It is a Master Slave D-type Flip Flop with Set, Reset functions. Data input applied to the "D" terminal is transferred to the output on the positive transition of the clock pulse. When clock input is low, the data input controls only the "Master" portion of the Flip Flop. When clock input changes from a low to a high level, the data present in the "Master" is transferred to the "Slave" and the output. A high level voltage applied to S(R) terminal makes the output HIGH (low), regardless of the clock or data inputs. It is fully ECL compatible both in I/O levels and supply voltages. The 16 pin ceramic package is low loss and hermetically sealed. Devices are highly reliable because of the stability of WSi refractory gate metallization. This device is compatible with other NEC, MSI, and SSI GaAs logic products, and can be tested using a MD16EVAL 16-pin evaluation kit.

OUTLINE DIMENSIONS (Units in mm)

OUTLINE H16



CONNECTION DIAGRAM



TRUTH TABLES

INPUT				OUTPUT	
CLOCK	DATA	SET	PRESET	Qn + 1	$\overline{Qn}$ + 1
H↓	L	L	L	L	H
H↓	H	L	L	H	L
L↓	X	L	L	Qn	$\overline{Qn}$
X	X	L	H	L	H
X	X	H	L	H	L
X	X	H	H	–	–

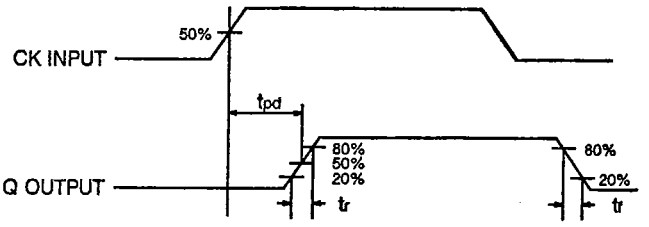
H: High Level
L: Low Level
X: High or Low
Qn: The output before the clock pulse
Qn + 1: The output after the clock pulse

Positive Clock edge triggered.

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

SYMBOLS	PARAMETERS	UNITS	RATINGS
V_{DD}	Supply Voltage	V	+4
V_{SS}	Supply Voltage	V	-8
V_{TT}	Terminating Voltage	V	V_{DD}-4
V_{IN}	Input Voltage	V	V_{DD} - V_{SS}
T_{STG}	Storage Temperature	°C	-65 to +175
T_{OP}	Operating Temperature	°C	-65 to +125
P_T	Total Power Dissipation	mW	500

OPERATIONAL WAVEFORMS



Notes:
The Vcs and Vcss are normally open. They can be used as a bias adjustment to optimize operating frequency or output waveform. The Vcs and Vcss are bias terminals which are used to adjust the Flip Flop circuit current and output level, respectively.

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

PART NUMBER PACKAGE OUTLINE				UPG700B, UPG700P H16, CHIP		
SYMBOLS	PARAMETERS	TEST CONDITIONS	UNITS	MIN.	TYP.	MAX.
I_{DD}	Supply Current		mA		90	145
I_{SS}	Supply Current	V_{DD} = 0 V	mA		70	105
V_{OH}	High Level Output Voltage	V_{TT} = -2 V (50 Ω termination)	V	-1.0	-0.8	-0.6
V_{OL}	Low Level Output Voltage		V	-2.0	-1.8	-1.6
V_{TH}	Threshold Voltage	V_{SS} = -5.2 V	V		-1.3	
I_{OH}	High Level Output Current**		mA		25	
I_{OL}	Low Level Output Current**		mA		4	
I_{IH}	High Level Input Current		mA		.7	
I_{IL}	Low Level Input Current		mA		.02	
$f_{\phi MAX}$	Maximum Clock Frequency		GHz	2.5	3.2	
f_{MAX}	Maximum Data Input Rate		GHz	2.2		
t_{pd}	Switching Time		ps		300	400
t_r	Output Rise Time*		ps		130	200
t_{f1}	Output Fall Time*		ps		120	200
t_{s1}	Set Up Time		ps		100	150
t_h	Hold Time		ps		100	150

Note:

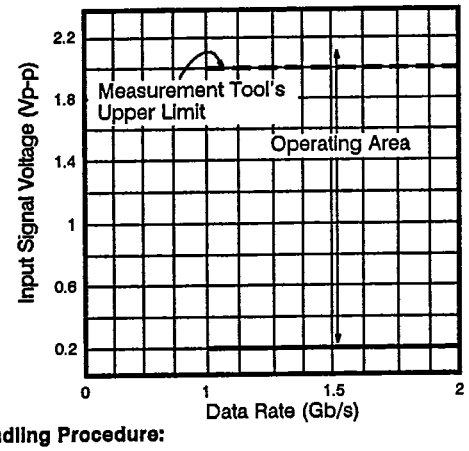
*The time from 20% to 80% of output voltage.

**The value in case 50 Ω load resistance is connected between output and V_{TT} terminal; (-2 Volts) V_{TT} is the terminating voltage of the external 50 Ω load resistance.

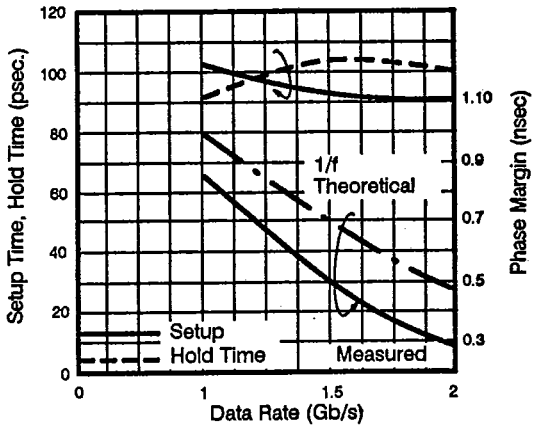
5

TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C)

UPG700B
INPUT SIGNAL SENSITIVITY
vs. DATA RATE



UPG700B
SETUP TIME, HOLD TIME
vs. DATA RATE

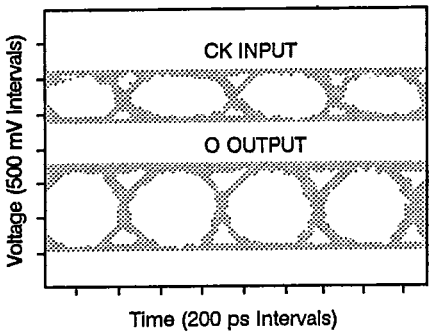


Handling Procedure:

1. When handling the device a ground strap should be used to prevent Electric Static Discharge (ESD) that can damage the GaAs MES FETs in the IC.

WAVEFORM

UPG700B

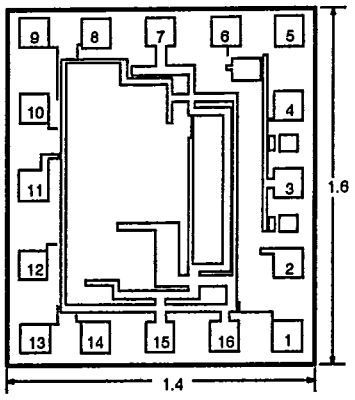


Attention:

The metallized section on the back surface of the package is used as a heat sink and it is shared with the Vss terminal (Vss = -5.2 V normally). Do not ground the metallized section to GND (0 V). This is to prevent a short circuit with V_{DD} (V_{DD} = 0 V normally) or some other terminals.

OUTLINE DIMENSIONS (Units in µm)

UPG700P (CHIP)



1. Vcs	9. CK
2. $\overline{Q}$	10. $\overline{CK}$
3. NC	11. NC
4. Q	12. $\overline{D}$
5. NC	13. D
6. V_{CSB}	14. Reset
7. V_{DD}	15. V_{DD}
8. Set	16. Vss

RECOMMENDED CHIP ASSEMBLY CONDITIONS

Die Attachment

Atmosphere:	N_2 gas	
Temperature:	320 ± 3°C	
AuSn Preform:	UPG700P	0.7 x 0.7 x 0.05t (mm), 2 piece

The use of hard solder (AuSi or AuGe) is not recommended. Don't use a solder which has a melting point higher than AuSn.

Base material: CuW, Cu, KV

Epoxy Die Attach is not recommended.

Bonding:

Machine:	TCB
Wire:	30 µm diameter Au wire
Temperature:	260 ± 10°C
Bonding Force:	44 ± 5g
Atmosphere:	N_2 gas