NEC®

3-INPUT OR/NOR GATE

UPG702B
UPG702P

FEATURES

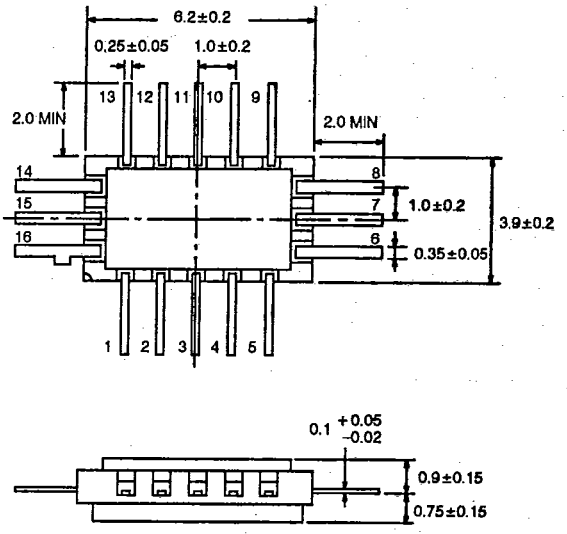
- **LOGIC LEVELS AND SUPPLY VOLTAGES ECL COMPATIBLE**
- **HIGH SPEED**
  (Operating Clock Frequency beyond 2 GHz)
- **HERMETICALLY SEALED PACKAGE ASSURES HIGH RELIABILITY**

DESCRIPTION AND APPLICATIONS

The UPG702B is a high speed GaAs digital integrated circuit that is configured as a 3-input OR/NOR gate with typical rise and fall times of 160 and 130 psec. respectively. It is ECL compatible both in I/O levels and supply voltages. The 16-pin ceramic package is low loss and hermetically sealed. Devices are highly reliable because of the stability of WSi refractory gate metallization. This device is compatible with other NEC MSI and SSI GaAs logic products, and can be tested using a MD16EVAL-1 16-pin evaluation kit or a MD12BRD universal prototyping board.

OUTLINE DIMENSIONS (Units in mm)

OUTLINE H16



ELECTRICAL CHARACTERISTICS[1] (T_A = 25°C)

PART NUMBER / PACKAGE OUTLINE				UPG702B H16		
SYMBOLS	PARAMETERS	TEST CONDITIONS	UNITS	MIN	TYP	MAX
I_{DD}	Supply Current		mA		70	115
I_{SS}	Supply Current	V_{DD} = 0 V	mA		50	75
V_{OH}	High Level Output Voltage	V_{TT} = −2 V (50 Ω termination)	V	−1.0	−0.8	−0.6
V_{OL}	Low Level Output Voltage		V	−2.0	−1.8	−1.6
V_{TH}	Threshold Voltage	V_{SS} = −5.2 V	V		−1.3	
I_{OH}	High Level Output Current[4]		mA		25	
I_{OL}	Low Level Output Current[4]		mA		4	
I_{IH}	High Level Input Current		mA		.8	
I_{IL}	Low Level Input Current		mA		0	
t_{PD}	Switching Time[3]		ps		300	400
t_R[2]	Output Rise Time[3]		ps		160	250
t_F[2]	Output Fall Time[3]		ps		130	200

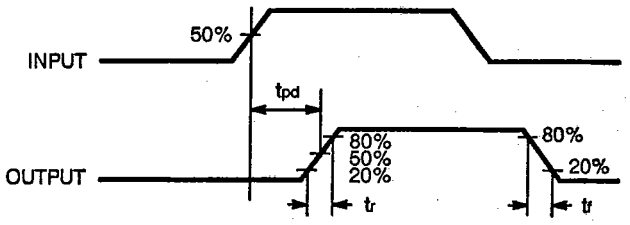
Notes:

1. When handling the device a ground strap should be used to prevent Electric Static Discharge (ESD) that can damage the GaAs MES FETs in the IC.
2. The time from 20% to 80% of output voltage.
3. See Operational Waveforms; t_{pd}, t_r, t_f.
4. The valve of the output whereby a 50 ohm load is connected between output and V_{TT} terminal (−2 V). Note V_{TT} is the terminating voltage of the 50 ohm load resistance.

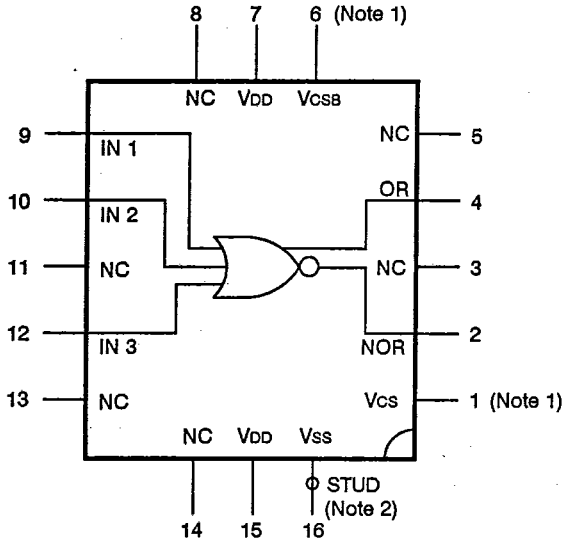
ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

SYMBOLS	PARAMETERS	UNITS	RATINGS
V_{DD}	Supply Voltage	V	+4
V_{SS}	Supply Voltage	V	-12
V_{TT}	Terminating Voltage	V	V_{DD} - 4
V_{IN}	Input Voltage	V	V_{DD} - V_{SS}
T_{STG}	Storage Temperature	°C	-65 to +175
T_{OP}	Operating Temperature	°C	-65 to +125
P_T	Total Power Dissipation	mW	450

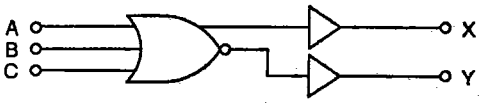
OPERATIONAL WAVEFORMS



CONNECTION DIAGRAM



LOGIC DIAGRAM

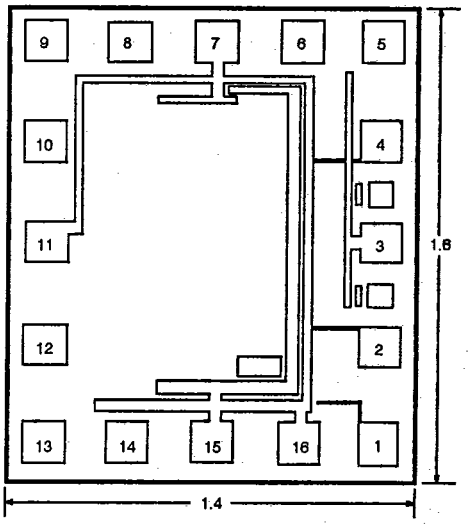


OR (X) = A+B+C

NOR (Y) = $\overline{A+B+C}$

CHIP DIMENSIONS (Units in µm)

UPG702P (CHIP)



1. V_{CS}
2. NOR
3. NC
4. OR
5. NC
6. V_{CSB}
7. V_{DD}
8. NC
9. IN1
10. IN2
11. NC
12. IN3
13. Ref.
14. NC
15. V_{DD}
16. V_{SS}

RECOMMENDED CHIP ASSEMBLY CONDITIONS

Die Attachment

Atmosphere: N_2 gas
Temperature: 320 ± 3°C
AuSn Preform: UPG702P 0.7 x 0.7 x 0.05 (mm), 2 piece

The use of hard solder (AuSi or AuGe) is not recommended. Don't use a solder which has a melting point higher than AuSn.

Base material: CuW, Cu, KV

Epoxy Die Attach is not recommended.

Bonding:

Machine: TCB
Wire: 30 µm diameter Au wire
Temperature: 260 ± 10°C
Bonding Force: 44 ± 5g
Atmosphere: N_2 gas

Notes:

1. V_{CS} and V_{CSB}, which are normally open, can also be used as bias during adjusting terminals to optimize operating frequency or output waveform.
2. The metallized section on the back surface of the package, which is used as a heat sink and is shared with the V_{SS2} terminal (V_{SS} = -5.2 V normally).
   Do not ground the metallized section to GND (0 V). This is to prevent a short circuit with V_{DD} (V_{DD} = 0 V normally) or some other terminals.