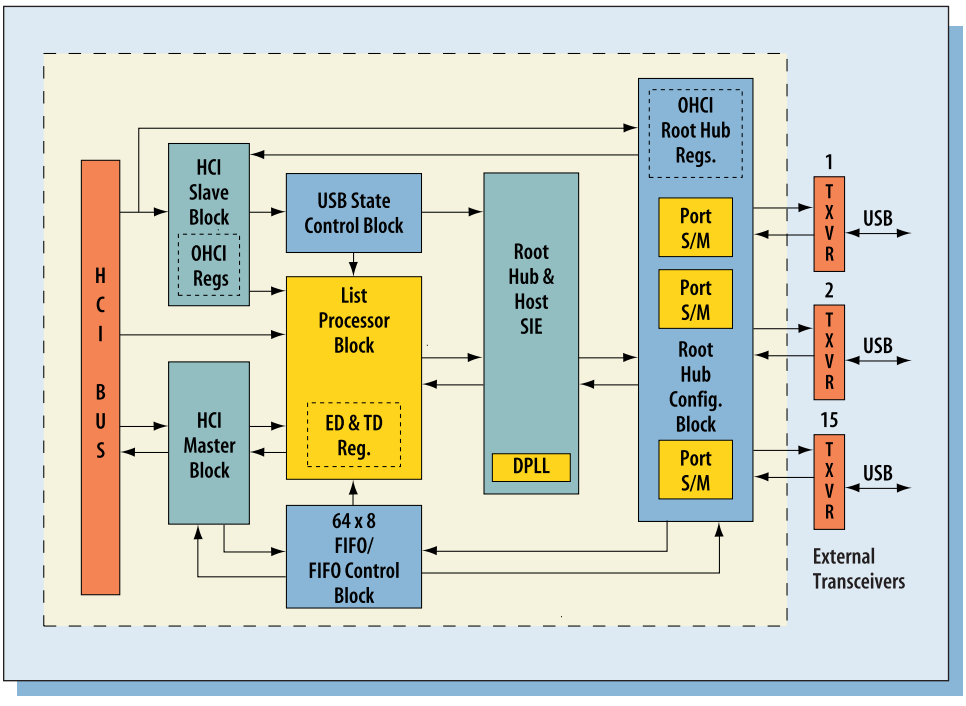
USB Host Core

Host Core for Universal Serial Bus Solutions

Overview

The USB Host Core, a component of LSI Logic's comprehensive USB solution set, is a flexible and configurable core that manages and generates the Universal Serial Bus, providing support of USB peripherals in highly integrated embedded systems.

Enabling USB in applications such as handheld and palm-size PCs, direct-print digital cameras, set-top boxes, and industrial control, the USB Host Core manages the USB system and establishes communications between software applications and the corresponding USB peripherals. The Open HCI-compliant Host Core implements the USB protocol and OHCI register set and provides a generic FIFO-based interface to the system ASIC application logic.



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The USB Host Core is part of a complete suite of USB cores spanning the entire USB topology, including peripherals and hub applications.

As an element of LSI Logic's proven CoreWare® library, the USB Host Core is fully supported by industry-leading design methodology and complements other cores in the family.

USB UNIVERSAL SERIAL BUS

LSI LOGIC

USB Host Core

Features

- Open HCI Rev 1.0-complaint and USB specification Rev 1.1-compliant
- Firm implementation; fixed netlist with flexible layout guidelines
- Configurable Root Hub for number of ports and power switching options
- Simple FIFO-based application interface
- Integrated Digital PLL
- Supports low- and full-speed data rates
- SCAN-inserted netlist
- Gated clock option
- Interfaces with LSI Logic's USB transceiver I/Os
- Verified functionality and timing in LSI Logic's ASIC technologies

Simplified Design and Integration

To simplify design integration, the cores are provided in both encrypted RTL and unencrypted SCAN-inserted netlist forms. RTL speeds the development of the system ASIC architecture at the behavioral simulation level.

The netlist accelerates the structural implementation, and, with an optimized, proven, fixed netlist in LSI Logic's ASIC technology, frees the designer to concentrate on other value-added aspects of the system ASIC.

Cost-Effective and Differentiated USB-Embedded Products

In addition, by combining the USB Host Core and LSI Logic's USB transceiver I/Os with other CoreWare components and customer-defined logic, designers can quickly create cost-effective and differentiated single-chip USB system solutions.

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USB Host Core Description

The USB Host Core controls mode operation, frame management and list processing tasks, operating in conjunction with Host Controller Driver (HCD) software in the Operating System. The number and power option support of Root Hub ports can be easily configured to customize the implementation based on the application requirements. Together with separate USB transceivers from LSI Logic's I/O library, the USB Host Core provides a complete solution to create USB-enabled applications.

USB Host Core Components

The USB Host Core is composed of the following blocks:

HCI Slave Block

The HCI Slave Block is the slave on the HCI Bus, interfacing the internal OHCI registers and the application. It processes all writes to and reads from the OHCI registers implemented within the block.

USB State Control Block

The USB State Control Block generates the Host Controller states as defined in the OHCI Specification. It also generates control signals to transmit Start of Frame (SOF) tokens, initiates reset/resume signaling and triggers the List Processor Block when it is set in the operational state.

Root Hub and Host SIE Block

The Root Hub manages connect/disconnect events through port enable/disable, device recognition and status reporting mechanisms. The Serial Interface Engine (SIE) performs parallel-to-serial and serial-to-parallel data conversion, clock embedding and recovery, data encoding/decoding and error checking functions between the Root Hub and the USB.

Root Hub Configuration Block

The Root Hub Configuration Block is a configurable element of the USB Host Core providing flexibility to set port number and power switching attributes. From 1-15 Root Hub ports, supporting various power options on a global and per-port basis, can be implemented.

HCI Master Block

The HCI Master Block is the master on the HCI Bus, managing all reads and writes from and to system memory initiated by the List Processor Block.

Benefits

- Ensures Hot *Plug and Play* interoperability
- More flexible layout interface vs. fixed layout and placement
- Performance and gate count optimized for each application
- Eases system-on-a-chip integration
- No external components required
- Interoperates with all low- and full-speed peripherals
- Reduces power consumption
- Simplifies test verification
- External transceiver chip not required
- Fast time to market with Right-First-Time™ methodology designs

USB Host Core

USB Host Core Components (continued)

List Processor Block

The List Processor Block processes the data transfer lists scheduled by the HCD according to the priority programmed in the operational registers.

FIFO/FIFO Control Block

The FIFO provides a data buffer between the HCI Master and Root Hub and Host SIE Blocks with the FIFO/FIFO Controller Block steering data in the proper direction.

CoreWare Design Program

The CoreWare Design Program enables system-on-a-chip design integration, delivering unmatched market advantages. It is a proven and complete methodology, offering the technology and application know-how to put an entire system on a single chip. Industry-standard functions, or cores, are combined with on-chip memory and user-defined logic to create market-leading, one-of-a-kind designs efficiently and rapidly.

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