Semicustom Products

UTE/UTE-R Gate Array Family

Data Sheet

UNITED TECHNOLOGIES MICROELECTRONICS CENTER

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FEATURES

- Up to 125,000 usable equivalent gates
- QML Q and V compliant
- Designed specifically for high reliability applications
- Advanced sub-micron (0.9 l_{eff}) silicon gate CMOS process
- JTAG (IEEE 1149.1) boundary-scan registers built into I/O cells
- Low noise package technology for high-speed circuits
- Latchup-immune over specified use conditions
- Radiation-hardened to 1.0E6 rads(Si) total dose (functional) and SEU-immune cells to less than 1.0E-10 errors/bit-day (UTE-R process)
- Design support using Mentor Graphics®, Synopsys and VHDL tools on HP and Sun workstations
- Ability to translate/alternate source FPGAs and third-party ASIC designs
- Approved by NASA for listing in MIL-STD-975
- Available against Standard Microcircuit Drawing 5962-96B02

PRODUCT DESCRIPTION

Introduction

The high-performance UTE/UTE-R gate array family features densities of up to 125,000 equivalent gates and is available in MIL-PRF-38535 QML Q and V quality levels and radiation-hardened (UTE-R).

Advanced Silicon-Gate CMOS Process

The UTE/UTE-R processes feature submicron channel lengths (0.9 l_{eff}) in a twin-tub, epitaxial bulk CMOS technology. These processes have options for two or three levels of metal interconnect which allow efficient layouts for designs requiring high functional density.

For those designs requiring stringent radiation hardness, special processing techniques are used to enhance the total dose radiation hardness of the field and gate oxides while maintaining circuit density and reliability. In addition, for both greater transient radiation hardness and latchup immunity, the radiation-hardened processes are built on epitaxial substrate wafers.

Patented High Density Array Architecture

Developed from UTMC's patented architectures, the UTE/UTE-R array family uses a highly efficient continuous-transistor architecture for the internal cell constructions. This arrangement minimizes the number of otherwise unusable transistors common in conventional block-structured arrays. Combined with placement and routing tools, the utilization of available transistors is maximized using two or three levels of metal interconnect, enabling the designer to achieve very high functional density in a single ASIC.

Gate Array Family

Arrays fabricated in both UTE and UTE-R (radiation-hardened option) processes are available with usable gate densities of up to 125,000 equivalent gates and 342 total pads (see table 1).

Table 1. Gate Densities

DEVICE PART NUMBERS[1]	EQUIVALENT USABLE GATES[2]	SIGNAL I/O[3]	POWER & GROUND PADS[4]
UT25E/-R	5,000 - 25,000	175	40
UT35E/-R	35,000	175	40
UT75E/-R	75,000	256	80
UT100E/-R	125,000	256	80

Notes:
1. The -R denotes the radiation-hardened option.
2. Based on NAND2 equivalents. Actual usable gate count is design-dependent. Estimates reflect a mix of functions including RAM.
3. Includes five pins that may or may not be reserved for JTAG boundary-scan, depending on user requirements.
4. Reserved for dedicated V_{DD}/V_{SS} and V_{DDQ}/V_{SSQ}.

Low-noise Device and Package Solutions

UTE/UTE-R output drivers feature programmable slew rate control for minimizing noise and switching transients. This feature allows the user to optimize edge characteristics to match system requirements. Separate on-chip power and ground buses are provided for internal cells and output drivers which further isolate internal design circuitry from switching noise.

In addition, UTMC offers advanced low-noise package technology with multi-layer, co-fired ceramic construction featuring built-in isolated power and ground planes. These planes provide lower overall resistance/inductance through power and ground paths which minimize voltage drops during periods of heavy switching. These isolated planes also help sustain supply voltage during dose rate events, thus preventing rail span collapse.

Flatpacks are available with up to 304 leads; PGAs are available with up to 280 leads. UTMC's flatpacks feature a non-conductive tie bar that helps maintain lead integrity through test and handling operations. In addition to the packages listed in table 2, UTMC offers custom package development and package tooling modification services for individual requirements.

Table 2. Packages

PACKAGE TYPE/LEADCOUNT[1]	UT25E/-R	UT35E/-R	UT75E/-R	UT100E/-R
Flatpack				
84	X	X		
132	X	X		
172	X	X	X	X
196	X	X	X	X
224			X	X
256			X	X
304			X	X
PGA[2]				
84	X	X		
120			X	X
144	X	X		
208	X	X	X	X
280			X	X

Notes:
1. The number of device I/O pads available may be restricted by the selected package.
2. PGA packages have one additional non-connected index pin (i.e., 144 + 1 index pin = 145 total package pins for the 144 PGA). Contact UTMC for specific package drawings.

Extensive Cell Library

The UTE/UTE-R family of gate arrays is supported by an extensive cell library that includes SSI, MSI, and 54XX-equivalent functions, as well as RAM and other megafunctions. User-selectable options for cell configurations include scan for all register elements, as well as output drive strength. UTMC's megacell library includes the following functions:

- Intel® 80C31 equivalent
- MIL-STD-1553 functions (BCRTM, RTI, RTMP)
- MIL-STD-1750 microprocessor
- Standard microprocessor peripheral functions
- Configurable RAM

Refer to UTMC's UTE/UTE-R Design Manual for complete cell listing and details.

I/O Buffers

The UTE/UTE-R gate array family offers up to 342 device pad locations (note: device pad availability is affected by package selection and pinout.) The I/O cells can be configured by the user to serve as input, output, bidirectional, three-state, or additional power and ground pads. Output drive options range from 2 to 8mA. To drive larger off-chip loads, output drivers can be combined in parallel to provide additional drive up to 12mA.

Other I/O buffer features and options include:

- Slew rate control
- Pull-up and pull-down resistors
- TTL, CMOS, and Schmitt levels
- Built-in boundary-scan

JTAG Boundary-Scan

UTE/UTE-R arrays include a test access port and boundary-scan architecture that conforms to the IEEE Standard 1149.1 (JTAG). Some of the benefits this capability offers include the following:

- Allows easy test of complex assembled printed circuit boards
- Can be used to gain access to and control internal scan paths
- Can be used to initiate Built-In Self Test

Clock Driver Distribution

UTMC design tools provide methods for balanced clock distribution that maximize drive capability and minimize relative clock skew between clocked devices.

Speed and Performance

UTMC specializes in high-performance circuits designed to operate in harsh military and radiation environments. Table 3 presents a sampling of typical cell delays.

Note that the propagation delay for a CMOS device is a function of its fanout loading, supply voltage, operating temperature, and processing tolerance. In a radiation environment, additional performance variances must be considered. The UTE/UTE-R simulation models account for all of these effects to accurately determine circuit performance for its particular set of use conditions.

Power Dissipation

Each internal gate or I/O driver has an average power consumption based on its switching frequency and capacitive loading. The radiation-hardened processes exhibit power dissipation that is typical of CMOS processes. For a rigorous power estimating methodology, refer to the UTMC UTE/UTE-R Design Manual or consult with a UTMC Applications Engineer.

Table 3. Typical Cell Delays

CELL	OUTPUT TRANSITION	PROPAGATION DELAY [1]
Internal Gates		
INV1, Inverter	HL	0.29
	LH	0.38
INV4, Inverter 4X	HL	0.17
	LH	0.22
NAND2, 2-Input NAND	HL	0.41
	LH	0.38
NOR2, 2-Input NOR	HL	0.30
	LH	0.62
DFF	CLK to Q	1.58
Latch	Enable to Q	1.36
Output Buffers		
OCN10, CMOS Scan	HL	4.83
	LH	5.27
O4N10, TTL Scan, 4mA	HL	5.92
	LH	4.01
OTN10, TTL Scan, 12mA	HL	3.76
	LH	3.14
Input Buffers		
ICN10, CMOS Scan	HL	1.91
	LH	1.58
ITN10, TTL Scan	HL	2.47
	LH	1.42

Note:
1. All specifications in ns (typical). Output load capacitance is 50pF. Fanout loading for input buffers and gates is the equivalent of two gate input loads.

ASIC DESIGN SOFTWARE

Using a combination of state-of-the-art third-party and proprietary design tools, UTMC delivers the CAE support and capability to handle complex, high-performance ASIC designs from design concept through design verification and test.

DESIGN CREATION

UTMC's flexible design creation methodology supports high level designs by providing UTE-R cell libraries for synthesis. Using Mentor Graphics and Synopsys synthesis tools, a structural design can be created for verification in VITAL-compliant VHDL or the Mentor Graphics environment. UTMC's cell libraries also support Automatic Test Program Generation to improve design testing.

DESIGN ANALYSIS

UTMC's design analysis tools check the integrity of the design and ensures that it can be manufactured in UTMC processes. Design analysis tools include:

DESIGN ANALYSIS TOOL	FUNCTION
Logical Rule Checker	Makes sure the design meets connectivity rules
Tester Rule Checker	Makes sure the design can be tested on UTMC testers
Design Transfer Tool	Allows accurate transfer of design data to UTMC

TOOLS SUPPORTED BY UTMC

MENTOR GRAPHICS	SYNOPSYS	VHDL
AutoLogicII®	Design Compiler™	Synopsys VSS™
QuickSimII®	VHDL Compiler™	Mentor Graphics Quick-VHDL®
QuickFault III®	TestSim™	Cadence Leapfrog®
QuickGradeII®	Verilog HDL Compiler™	Viewlogic Vantage™
FastScan ®/ FlexTest® / DFT Advisor®	Test Compiler Plus™	Any VITAL-compliant VHDL tool

XDT℠ (eXTERNAL DESIGN TRANSLATION)

Through UTMC's XDT services, customers can convert an existing non-UTMC design to UTMC's processes. The XDT is particularly useful for converting an FPGA to a UTMC radiation-hardened gate array. The XDT translation tools convert industry standard netlist formats and vendor libraries to UTMC formats and libraries. Industry standard netlist formats supported by UTMC include:

- VHDL
- Verilog HDL™
- FPGA source files (Actel, Altera, Xilinx)
- EDIF
- Third-party netlists supported by Synopsys

PHYSICAL DESIGN

Using two or three layers of metal interconnect, UTMC achieves optimized layouts that maximize speed of critical nets, overall chip performance, and design density up to 125,000+ equivalent gates.

Test Capability

UTMC supports all phases of test development from test stimulus generation through high-speed production test. This support includes ATPG, fault simulation, and fault grading. Scan design options are available on all UTE/UTE-R storage elements. In addition, all UTE/UTE-R arrays feature JTAG boundary-scan (per IEEE Standard 1149.1). Automatic test program development capabilities handle large vector sets for use with UTMC's LTX/Trillium MicroMasters, supporting high-speed testing (up to 80MHz with pin multiplexing).

Unparalleled Quality and Reliability

UTMC is dedicated to satisfying the demanding quality and reliability requirements of aerospace and defense systems suppliers. Quality assurance and reliability programs are integrated into the entire manufacturing process with Statistical Process Control (SPC) fully implemented for all manufacturing operations. These high quality standards have enabled UTMC to offer product in accordance with:

- MIL-PRF-38535, QML Q and V
- MIL-PRF-38535 Appendix A
- Other enhanced reliability flows

Because of numerous product variations permitted with customer specific designs, much of the reliability testing is performed using a Standard Evaluation Circuit (SEC) and Technology Characterization Vehicle (TCV). Thus, UTMC can assure high reliability prior to delivery of product to the customer.

Radiation Hardened

UTMC incorporates radiation-hardening techniques in process design, design rules, array design, power distribution, and library element design. All key radiation-hardening process parameters are controlled and monitored using statistical methods and in-line testing.

PARAMETER	RADIATION HARD	NOTES
Total dose	1.0E6 rads(Si) functional	1
Dose rate upset	5.0E9 rads(Si)/sec UT24E/-R, UT35E/-R 1.0E9 rads(Si)/sec UT75E/-R, UT100E/-R	2
Dose rate survivability	1.0E13 rads(Si)/sec UT25E/-R, UT35E/-R 1.0E12 rads(Si)/sec UT75E/-R, UT100E/-R	3
SEU	<1.0E-10 errors per cell-day	3,4
Projected neutron fluence	1.0E14 n/sq cm	
Latchup	Latchup-immune over specified use conditions	

Notes:

1. Total dose Co-60 testing is in accordance with MIL-STD-883, Method 1019. Data sheet electrical characteristics guaranteed to 1.0E6 rads(Si). All post-radiation values measured at 25°C; I_{DDQ} post-rad limit = 4mA.
2. Short pulse 20ns FWHM (full width, half maximum).
3. May be design dependent.
4. SEU-hard flip-flop cell. Non-hard flip-flop typical is 5E-8.

ABSOLUTE MAXIMUM RATINGS [1]

(Referenced to V_{SS})

SYMBOL	PARAMETER	LIMITS
V_{DD}	DC supply voltage	-0.3 to 7.0V
$V_{I/O}$	Voltage on any pin	-0.3V to V_{DD} + 0.3
T_{STG}	Storage temperature	-65 to +150°C
T_J	Maximum junction temperature	+175°C
I_{LU}	Latchup immunity	±150mA
I_I	DC input current	±10mA
T_{LS}	Lead temperature (soldering 5 sec)	+300°C

Note:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS
V_{DD}	Positive supply voltage	4.5 to 5.5V
T_C	Case temperature range	-55 to +125C
V_{IN}	DC input voltage	0V to V_{DD}

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 5.0V ±10%; -55°C < T_C < +125°C)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage [1] TTL inputs CMOS, OSC inputs				 0.8 $.3V_{DD}$	V
V_{IH}	High-level input voltage [1] TTL inputs CMOS, OSC inputs		 2.2 $.7V_{DD}$			V
V_{T+}	Schmitt Trigger, positive going [1] threshold				4.0	V
V_{T-}	Schmitt Trigger, negative going [1] threshold		1.0			V
V_H	Schmitt Trigger, typical range of hysteresis [2]		1.5		2.0	V
I_{IN}	Input leakage current TTL, CMOS, and Schmitt inputs Inputs with pull-down resistors Inputs with pull-down resistors, OSC Inputs with pull-up resistors Inputs with pull-up resistors, OSC	 $V_{IN} = V_{DD}$ or V_{SS} $V_{IN} = V_{DD}$ $V_{IN} = V_{SS}$ $V_{IN} = V_{SS}$ $V_{IN} = V_{DD}$	 -1 +150 -10 -900 -10		 1 +900 +10 -150 +10	µA
V_{OL}	Low-level output voltage [3] TTL half-drive buffer TTL single-drive buffer TTL double-drive buffer TTL triple-drive buffer * CMOS outputs CMOS outputs (optional) OSC outputs	 I_{OL} = 2.0mA I_{OL} = 4.0mA I_{OL} = 8.0mA I_{OL} = 12.0mA I_{OL} = 1.0µA I_{OL} = 100µA I_{OL} = 100µA			 0.4 0.4 0.4 0.4 0.05 0.25 1.0	V
V_{OH}	High-level output voltage [3] TTL half-drive buffer TTL single-drive buffer TTL double-drive buffer TTL triple-drive buffer * CMOS outputs CMOS outputs (optional) OSC outputs	 I_{OH} = -2.0mA I_{OH} = -4.0mA I_{OH} = -8.0mA I_{OH} = -12.0mA I_{OH} = -1.0µA I_{OH} = -100µA I_{OH} = -100µA	 2.4 2.4 2.4 2.4 V_{DD}-0.05 V_{DD}-0.25 3.5			V

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
I_{OZ}	Three-state output leakage current TTL half-drive buffer TTL single-drive, CMOS, OSC buffers TTL double-drive buffer TTL triple-drive buffer *	$V_O = V_{DD}$ and V_{SS}	 -5 -10 -20 -30		 5 10 20 30	µA
I_{OS}	Short-circuit output current [2,4] TTL half-drive buffer TTL single-drive, CMOS, OSC buffers TTL double-drive buffer TTL triple-drive buffer *	$V_O = V_{DD}$ and V_{SS}	 -50 -100 -200 -300		 50 100 200 300	mA
I_{DDQ}	Quiescent Supply Current	V_{DD} = 5.5V			1	mA
C_{IN}	Input capacitance [5]	f = 1MHz @ 0V		12		pF
C_{OUT}	Output capacitance [5] TTL half-drive buffer TTL single-drive, CMOS, OSC buffers TTL double-drive buffer TTL triple-drive buffer *	f = 1MHz @ 0V		 11 12 14 22		pF
C_{IO}	Bidirect I/O capacitance [5] TTL single-drive, CMOS, OSC buffers TTL double-drive buffer TTL triple-drive buffer *	f = 1MHz @ 0V		 13 15 23		pF

Notes:

* Contact UTMC prior to usage.

1. Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: $V_{IH} = V_{IH}(min) + 20\%, - 0\%$; $V_{IL} = V_{IL}(max) + 0\%, - 50\%$, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to $V_{IH}(min)$ and $V_{IL}(max)$.
2. Supplied as a design limit but not guaranteed or tested.
3. Per MIL-PRF-38535, for current density $\leq$ 5.0E5 amps/cm^2, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765pF*MHz.
4. Not more than one output may be shorted at a time for maximum duration of one second.
5. Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at frequency of 1MHz and a signal amplitude of 50mV rms maximum.