UT54ACS245/UT54ACTS245

Radiation-Hardened
Octal Bus Transceivers with Three-State Outputs

FEATURES

- Three-state outputs drive bus line directly
- 1.2μ radiation-hardened CMOS
  - Latchup immune
- High speed
- Low power consumption
- Single 5 volt supply
- Available QML Q or V processes
- Flexible package
  - 20-pin DIP
  - 20-lead flatpack

DESCRIPTION

The UT54ACS245 and the UT54ACTS245 are non-inverting octal bus transceivers designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input ($\overline{G}$) disables the device so that the buses are effectively isolated.

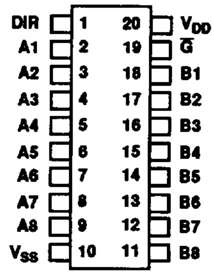
The devices are characterized over full military temperature range of -55°C to +125°C.

FUNCTION TABLE

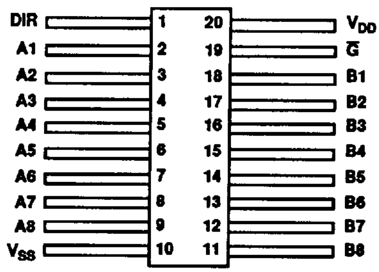
ENABLE $\overline{G}$	DIRECTION CONTROL DIR	OPERATION
L	L	B Data To A Bus
L	H	A Data To B Bus
H	X	Isolation

PINOUTS

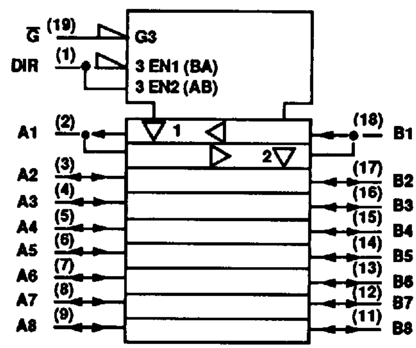
20-Pin DIP
Top View



20-Lead Flatpack
Top View

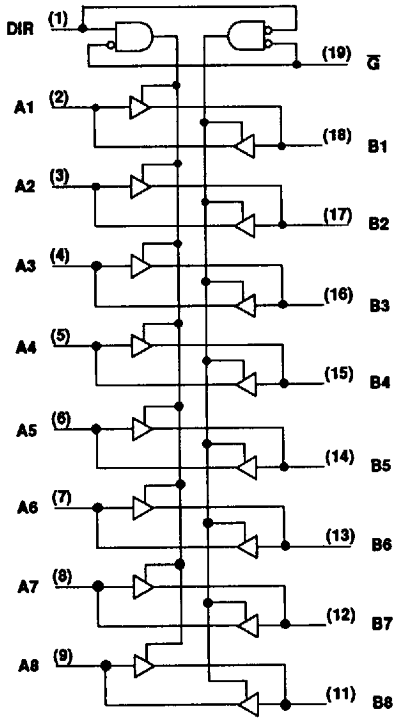


LOGIC SYMBOL



Note:
1. This symbols is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

LOGIC DIAGRAM



RADIATION HARDNESS SPECIFICATIONS [1]

PARAMETER	LIMIT	UNITS
Total Dose	1.0E6	rads(Si)
SEU & SEL Threshold [2]	80	MeV-cm^2/mg
Neutron Fluence	1.0E14	n/cm^2

Notes:
1. Logic will not latchup during radiation exposure within the limits defined in the table.
2. Device storage elements are immune to SEU affects.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	LIMIT	UNITS
V_{DD}	Supply voltage	-0.3 to 7.0	V
$V_{I/O}$	Voltage any pin	-.3 to V_{DD} +.3	V
T_{STG}	Storage Temperature range	-65 to +150	°C
T_J	Maximum junction temperature	+175	°C
T_{LS}	Lead temperature (soldering 5 seconds)	+300	°C
Θ_{JC}	Thermal resistance junction to case	20	°C/W
I_I	DC input current	±10	mA
P_D	Maximum power dissipation	1	W

Note:
1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMIT	UNITS
V_{DD}	Supply voltage	4.5 to 5.5	V
V_{IN}	Input voltage any pin	0 to V_{DD}	V
T_C	Temperature range	-55 to + 125	°C

DC ELECTRICAL CHARACTERISTICS [7]

(V_{DD} = 5.0V ±10%; V_{SS} = 0V [6], -55°C < T_C < +125°C)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
V_{IL}	Low-level input voltage [1] ACTS ACS			0.8 $.3V_{DD}$	V
V_{IH}	High-level input voltage [1] ACTS ACS		$.5V_{DD}$ $.7V_{DD}$		V
I_{IN}	Input leakage current ACTS/ACS	$V_{IN} = V_{DD}$ or V_{SS}	-1	1	µA
V_{OL}	Low-level output voltage [3] ACTS ACS	I_{OL} = 12.0mA I_{OL} = 100µA		0.40 0.25	V
V_{OH}	High-level output voltage [3] ACTS ACS	I_{OH} = -12.0mA I_{OH} = -100µA	$.7V_{DD}$ V_{DD} - 0.25		V
I_{OZ}	Three-state output leakage current	$V_O = V_{DD}$ and V_{SS}	-30	30	µA
I_{OS}	Short-circuit output current [2,4] ACTS/ACS	$V_O = V_{DD}$ and V_{SS}	-300	300	mA
P_{total}	Power dissipation [8,9]	C_L = 50pF		2.0	mW/MHz
I_{DDQ}	Quiescent Supply Current	V_{DD} = 5.5V		10	µA
C_{IN}	Input capacitance [5]	f = 1MHz @ 0V		15	pF
C_{OUT}	Output capacitance [5]	f = 1MHz @ 0V		15	pF

Notes:

1. Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: $V_{IH} = V_{IH}$(min) + 20%, - 0%; $V_{IL} = V_{IL}$(max) + 0%, - 50%, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to V_{IH}(min) and V_{IL}(max).
2. Supplied as a design limit but not guaranteed or tested.
3. Per MIL-M-38510, for current density ≤ 5.0E5 amps/cm^2, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765 pF MHz.
4. Not more than one output may be shorted at a time for maximum duration of one second.
5. Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at frequency of 1MHz and a signal amplitude of 50mV rms maximum.
6. Maximum allowable relative shift equals 50mV.
7. All specifications valid for radiation dose ≤ 1E6 rads(Si).
8. Power does not include power contribution of any TTL output sink current.
9. Power dissipation specified per switching output.

AC ELECTRICAL CHARACTERISTICS [2]

(V_{DD} = 5.0V ±10%; V_{SS} = 0V [1], -55°C < T_C < +125°C)

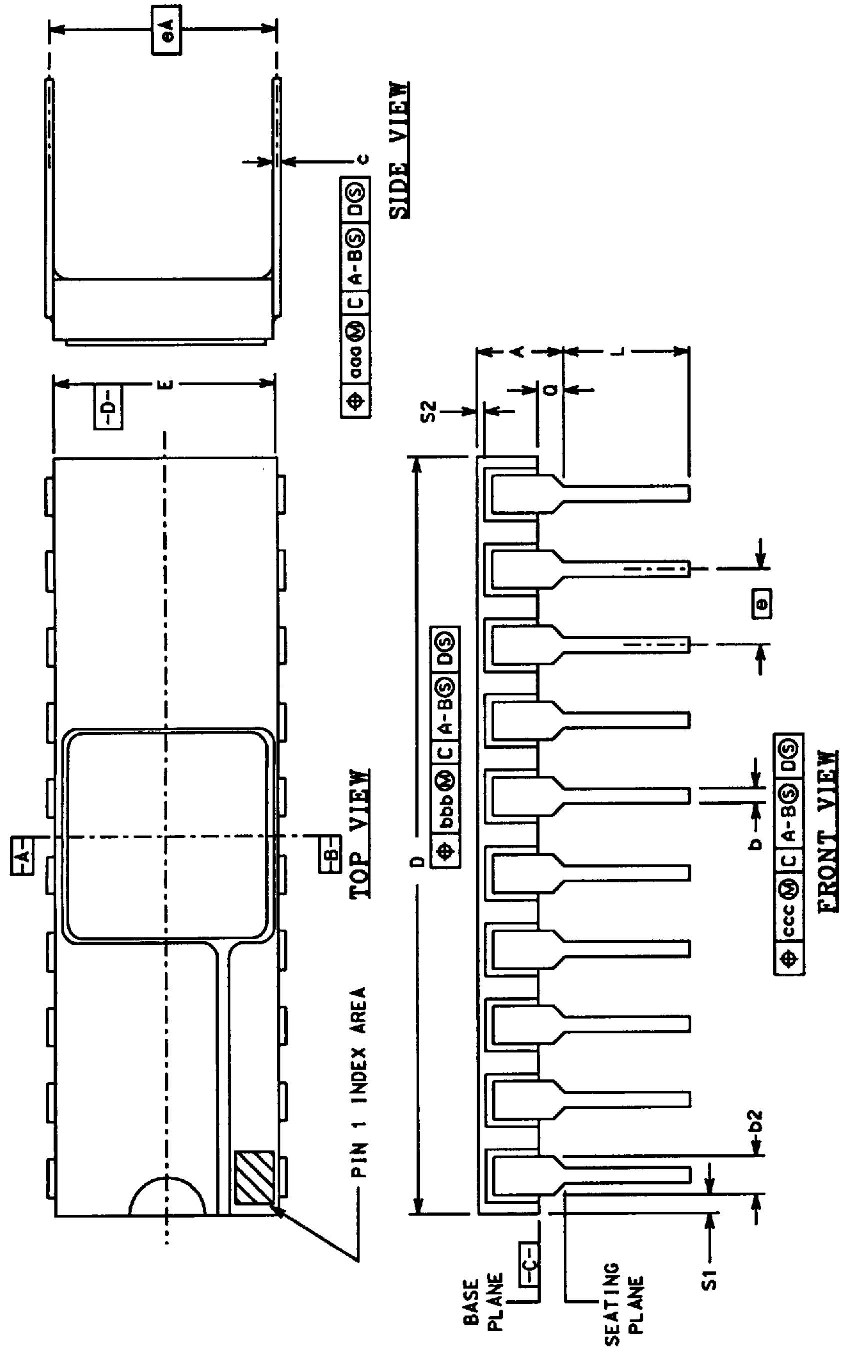
SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
t_{PLH}	Data to bus	1	11	ns
t_{PHL}	Data to bus	1	15	ns
t_{PZL}	$\overline{G}$ low to bus active	2	12	ns
t_{PZH}	$\overline{G}$ low to bus active	2	12	ns
t_{PLZ}	$\overline{G}$ high to bus three-state	2	12	ns
t_{PHZ}	$\overline{G}$ high to bus three-state	2	12	ns
t_{TLH}	Output transition time [3]	1	10	ns
t_{THL}	Output transition time [3]	1	10	ns

Notes:

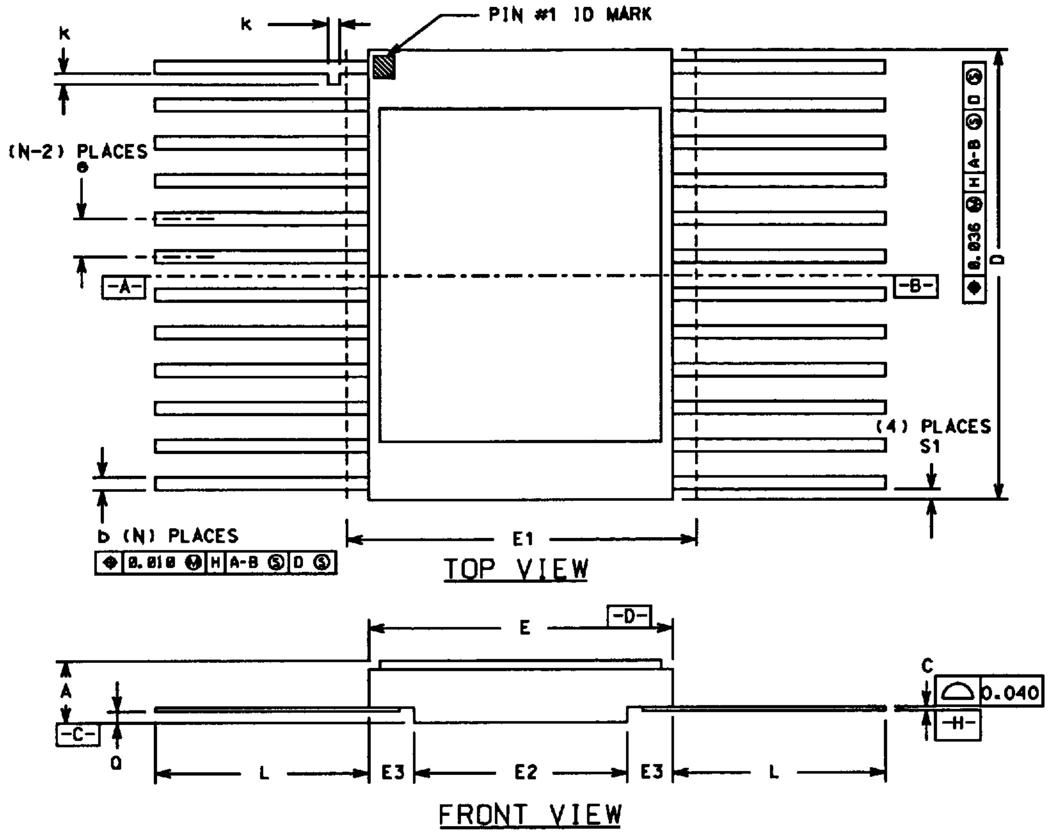
1. Maximum allowable relative shift equals 50mV.
2. All specifications valid for radiation dose ≤ 1E6 rads(Si)
3. This is controlled via design or process parameters. These values are characterized upon initial design release and upon design changes which effect these characteristics. These are not directly tested.

2.0 RAD-HARD MSI PACKAGES

Side-Brazed Packages



PKG CONFIG	LEAD COUNT	MIL-STD-1835 DWG CONF C	A	b	b2	c	D	E	e	eA	L	Q	S1	S2	aaa	bbb	ccc
			DIMENSION SYMBOLS														
-01	14	D-1	0.200 / -----	0.026 / 0.014	0.065 / 0.045	0.018 / 0.008	0.785 / -----	0.310 / 0.220	0.100 BSC	0.300 BSC	0.200 / 0.125	0.060 / 0.015	----- / 0.005	----- / 0.005	0.015 / -----	0.030 / -----	0.010 / -----
-02	16	D-2	0.200 / -----	0.026 / 0.014	0.065 / 0.045	0.018 / 0.008	0.840 / -----	0.310 / 0.220	0.100 BSC	0.300 BSC	0.200 / 0.125	0.060 / 0.015	----- / 0.005	----- / 0.005	0.015 / -----	0.030 / -----	0.010 / -----
-03	20	D-8	0.200 / -----	0.026 / 0.014	0.065 / 0.045	0.018 / 0.008	1.060 / -----	0.310 / 0.220	0.100 BSC	0.300 BSC	0.200 / 0.125	0.070 / 0.015	----- / 0.005	----- / 0.005	0.015 / -----	0.030 / -----	0.010 / -----



PKG CONFIG	LEAD COUNT	MIL-STD 1835 DWG CONF B	DIMENSION SYMBOLS												
			A	b	c	D	E	E1	E2	E3	e	k	L	Q	S1
-03	14	F-2A	0.115 / 0.045	0.022 / 0.015	0.009 / 0.004	0.390 / ------	0.260 / 0.235	0.290 / ------	------ / 0.130	------ / 0.030	0.050 BSC	0.015 / 0.008	0.370 / 0.270	0.045 / 0.026	------ / 0.005
-04	16	F-5A	0.115 / 0.045	0.022 / 0.015	0.009 / 0.004	0.440 / ------	0.285 / 0.245	0.315 / ------	------ / 0.130	------ / 0.030	0.050 BSC	0.015 / 0.008	0.370 / 0.250	0.045 / 0.026	------ / 0.005
-05	20	F-9A	0.115 / 0.045	0.022 / 0.015	0.009 / 0.004	0.540 / ------	0.300 / 0.245	0.330 / ------	------ / 0.130	------ / 0.030	0.050 BSC	0.015 / 0.008	0.370 / 0.250	0.045 / 0.026	------ / 0.000