



SANYO Semiconductors

DATA SHEET

**LC863264C, LC863256C
LC863248C, LC863240C
LC863232C, LC863228C
LC863224C, LC863220C
LC863216C**

CMOS IC

**64K/56K/48K/40K/32K/28K/24K/20K/16K-byte ROM,
CGROM16K-byte**

on-chip 640/512-byte RAM and 352x9 bit OSD RAM

8-bit 1-chip Microcontroller

Overview

The LC863264C/56C/48C/40C/32C/28C/24C/20C/16C are 8-bit single chip microcontrollers with the following on-chip functional blocks:

- CPU : Operable at a minimum bus cycle time of 0.424μs
- On-chip ROM capacity
Program ROM : 64K/56K/48K/40K/32K/28K/24K/20K/16K bytes
CGROM : 16K bytes
- On-chip RAM capacity : 640/512 bytes
- OSD RAM : 352x9 bits
- Closed-Caption TV controller and the on-screen display controller
- Closed-Caption data slicer
- Four channelsx8-bit AD Converter
- Three channelsx7-bit PWM
- Two 16-bit timer/counters, 14-bit base timer
- 8-bit synchronous serial interface circuit
- IIC-bus compliant serial interface circuit (Multi-master type)
- ROM correction function
- 16-source 10-vectored interrupt system

Continued on next page.

Note : This product includes the IIC bus interface circuit. If you intend to use the IIC bus interface, please notify us of this in advance of our receiving your program ROM code order.

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Continued from preceding page.

- Integrated system clock generator and display clock generator
 - Only one X'tal oscillator (32.768kHz) for PLL reference is used for both generators
 - TV control and the Closed Caption function
- All of the above functions are fabricated on a single chip.

Features

- Read-Only Memory (ROM) :
 - 65536×8 bits / 57344×8 bits / 49152×8 bits /
 - 40960×8 bits / 32768×8 bits / 28672×8 bits /
 - 24576×8 bits / 20480×8 bits / 16384×8 bits for program
 - 16128×8 bits for CGROM
 - Random Access Memory (RAM) :
 - 512×8 bits (working area) : LC863264C/56C/48C/40C
 - 384×8 bits (working area) : LC863232C/28C/24C/20C/16C
 - 128×8 bits (working or ROM correction function)
 - 352×9 bits (for CRT display)
 - OSD functions
 - Screen display : 36 characters×16 lines (by software)
 - RAM : 352 words (9 bits per word)
 - Display area : 36 words×8 lines
 - Control area : 8 words×8 lines
 - Characters
 - Up to 252 kinds of 16×32 dot character fonts
 - (4 characters including 1 test character are not programmable)
 - Each font can be divided into two parts and used as two fonts :
 - a 16×17 dot and 8×9 dot character font
 - At least 111 characters need to be divide to display the caption fonts.
 - Various character attributes
 - Character colors : 16colors
 - Character background colors : 16colors
 - Fringe / shadow colors : 16colors
 - Full screen colors : 16colors
 - Rounding
 - Underline
 - Italic character (slanting)
 - Attribute can be changed without spacing
 - Vertical display start line number can be set for each row independently (Rows can be overlapped)
 - Horizontal display start position can be set for each row independently
 - Horizontal pitch (9 to 16 dots)*1 and vertical pitch (1 to 32 dots) can be set for each row independently
 - Different display modes can be set for each row independently
 - Caption • Text mode / OSD mode 1 / OSD mode 2 (Quarter size) / Simplified graphic mode
 - Ten character sizes *1
 - Horez. × Vert. = (1×1), (1×2), (2×2), (2×4), (0.5×0.5)
 - (1.5×1), (1.5×2), (3×2), (3×4), (0.75×0.5)
 - Shuttering and scrolling on each row
 - Simplified Graphic Display
- Note *1: range depends on display mode : refer to the manual for details.
- Data Slicer (NTSC)
 - Line 21 closed caption data and XDS data extraction

LC863264C/56C/48C/40C/32C/28C/24C/20C/16C

■ Bus Cycle Time / Instruction-Cycle Time

Bus cycle time	Instruction cycle time	System clock oscillation	Oscillation frequency	Voltage
0.424μs	0.848μs	Internal VCO (Ref : X'tal 32.768kHz)	14.156MHz	4.5V to 5.5V
7.5μs	15.0μs	Internal RC	800kHz	4.5V to 5.5V
183.1μs	366.2μs	Crystal	32.768kHz	4.5V to 5.5V

■ Ports

- Input / Output Ports : 5 ports (28 terminals)
Data direction programmable in nibble units : 1 port (8 terminals)
(If the N-ch open drain output is selected by option, the corresponding port data can be read in output mode.)
Data direction programmable for each bit individually : 4 ports (20 terminals)

■ AD converter

- 4 channels×8-bit AD converters

■ Serial interfaces

- IIC-bus compliant serial interface (Multi-master type)
Consists of a single built-in circuit with two I/O channels. The two data lines and two clock lines can be connected internally.
- Synchronous 8-bit serial interface

■ PWM output

- 3 channels×7-bit PWM

■ Timer

- Timer 0 : 16-bit timer/counter
With 2-bit prescaler + 8-bit programmable prescaler
Mode 0 : Two 8-bit timers with a programmable prescaler
Mode 1 : 8-bit timer with a programmable prescaler + 8-bit counter
Mode 2 : 16-bit timer with a programmable prescaler
Mode 3 : 16-bit counter
The resolution of timer is 1 tCYC.
- Timer 1 : 16-bit timer/PWM
Mode 0 : Two 8-bit timers
Mode 1 : 8-bit timer + 8-bit PWM
Mode 2 : 16-bit timer
Mode 3 : Variable bit PWM (9 to 16 bits)
In mode0/1, the resolution of Timer1/PWM is 1 tCYC
In mode2/3, the resolution is selectable by program; tCYC or 1/2 tCYC
- Base timer
Generate every 500ms overflow for a clock application (using 32.768kHz crystal oscillation for the base timer clock)
Generate every 976μs, 3.9ms, 15.6ms, 62.5ms overflow (using 32.768kHz crystal oscillation for the base timer clock)
Clock for the base timer is selectable from 32.768kHz crystal oscillation, system clock or programmable prescaler output of Timer 0

■ Remote control receiver circuit (connected to the P73/INT3/T0IN terminal)

- Noise rejection function
- Polarity switching

■ Watchdog timer

External RC circuit is required
Interrupt or system reset is activated when the timer overflows

■ ROM correction function

Max 128 bytes / 2 addresses

■ Interrupts**• 16 sources 10 vectored interrupts**

1. External Interrupt INT0
2. External Interrupt INT1
3. External Interrupt INT2, Timer/counter T0L (Lower 8 bits)
4. External Interrupt INT3, base timer
5. Timer/counter T0H (Upper 8 bits)
6. Timer T1H,T1L
7. SIO0
8. Data slicer
9. Vertical synchronous signal interrupt ($\overline{VS}$), horizontal line ($\overline{HS}$), AD
10. IIC, Port 0

• Interrupt priority control

Three interrupt priorities are supported (low, high and highest) and multi-level nesting is possible. Low or high priority can be assigned to the interrupts from 3 to 10 listed above. For the external interrupt INT0 and INT1, low or highest priority can be set.

■ Sub-routine stack level**• A maximum of 128 levels (stack is built in the internal RAM)****■ Multiplication/division instruction**

- 16 bits×8 bits (7 instruction cycle times)
- 16 bits÷8 bits (7 instruction cycle times)

■ 3 oscillation circuits

- Built-in RC oscillation circuit used for the system clock
- Built-in VCO circuit used for the system clock and OSD
- X'tal oscillation circuit used for base timer, system clock and PLL reference

■ Standby function**• HALT mode**

The HALT mode is used to reduce the power dissipation. In this operation mode, the program execution is stopped. This mode can be released by the interrupt request or the system reset.

• HOLD mode

The HOLD mode is used to stop the oscillations; RC (internal), VCO, and X'tal oscillations. This mode can be released by the following conditions.

- Pull the reset terminal ($\overline{RES}$) to low level.
- Feed the selected level to either P70/INT0 or P71/INT1.
- Input the interrupt condition to Port 0.

■ Package

- DIP42S (Lead-free type)
- QIP48E (Lead-free type)

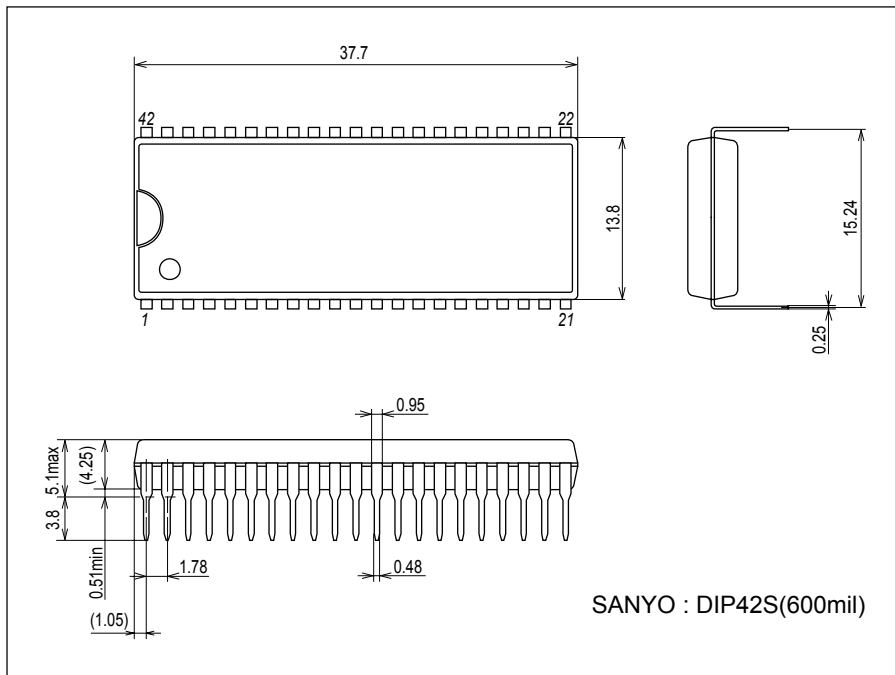
■ Development tools

- Flash EEPROM: LC86F3264A
- Evaluation chip: LC863096
- Emulator: EVA86000 (main) + ECB863200* or ECB863200A (evaluation chip board)
+ POD863200 (pod: DIP42S) or POD863201 (pod: QIP48E)
* This product is no longer available

Package Dimensions

unit : mm (typ)

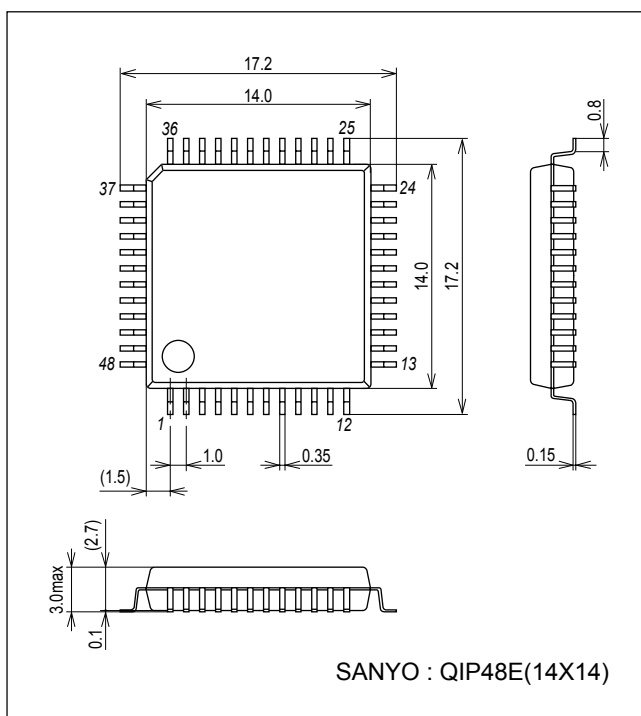
3025C



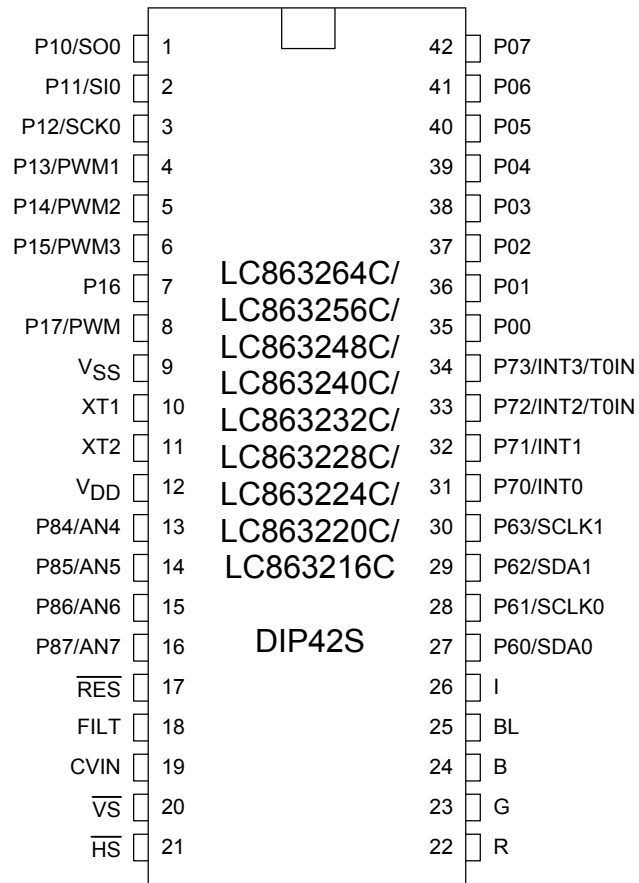
Package Dimensions

unit : mm (typ)

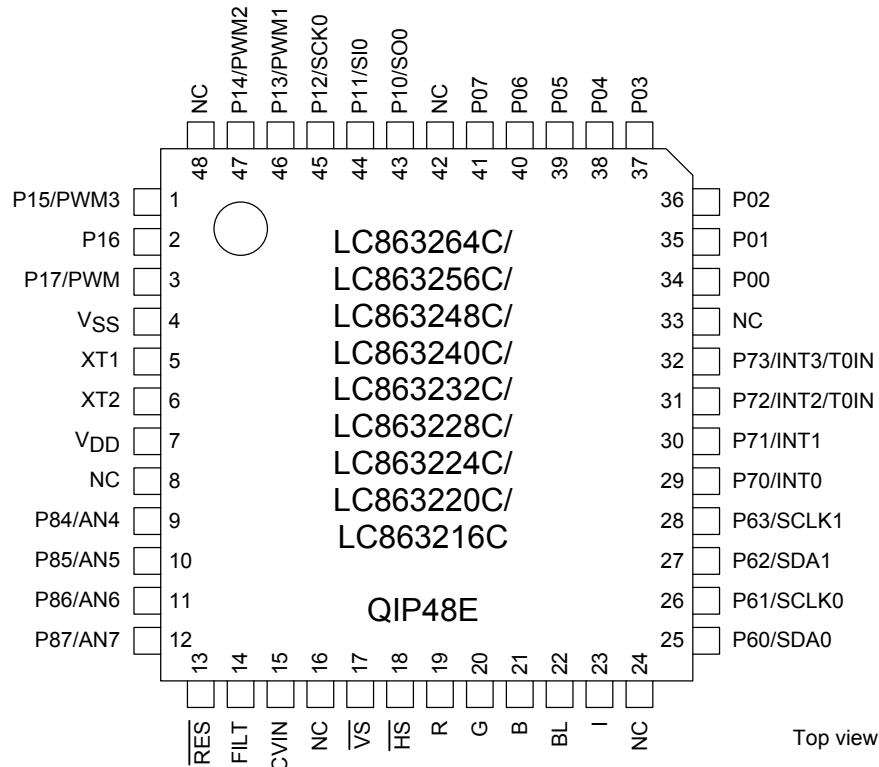
3156A



Pin Assignments

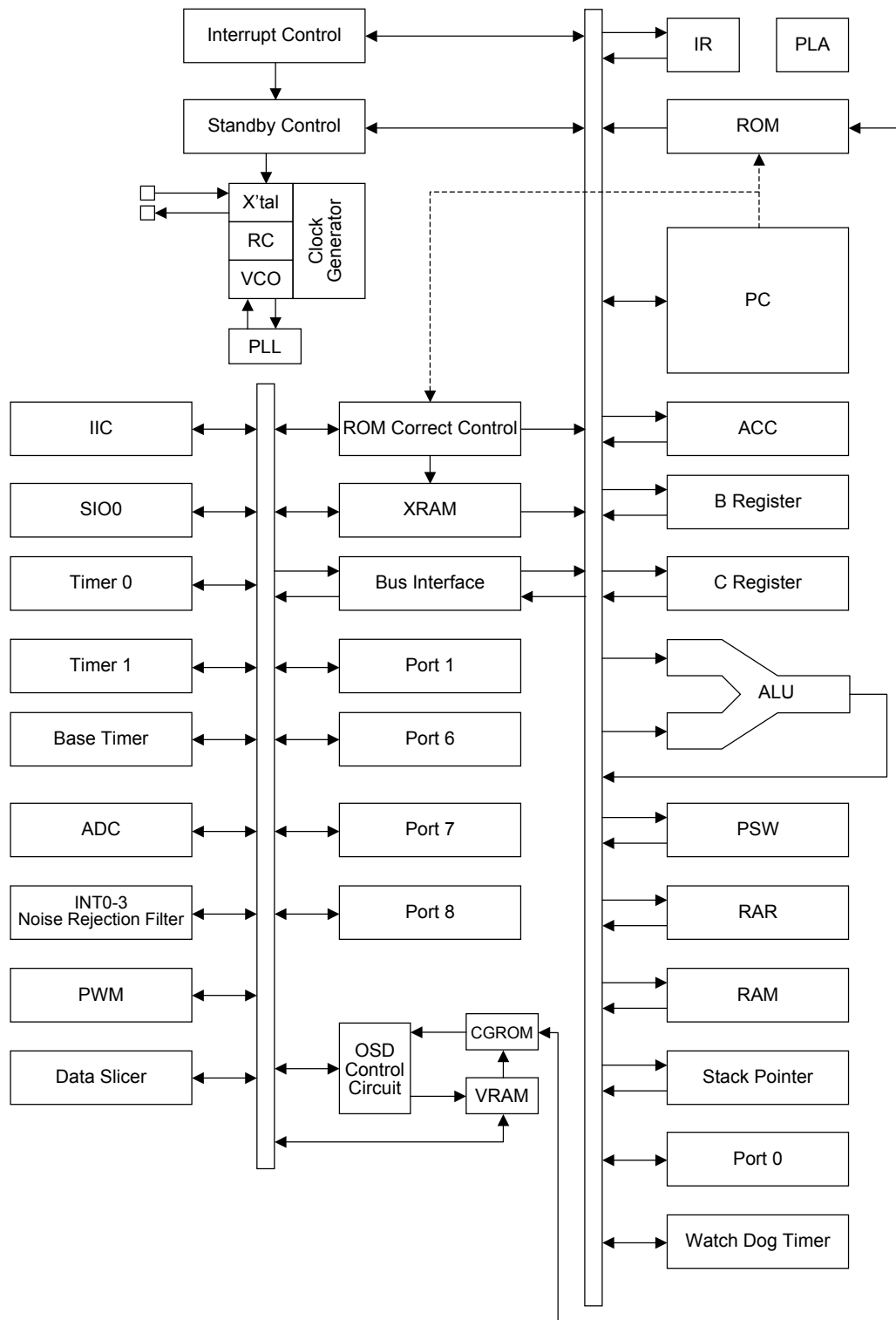


Top view



Top view

System Block Diagram



Pin Description

Pin Description Table

Terminal	I/O	Function Description	Option														
V _{SS}	-	Negative power supply															
XT1	I	Input terminal for crystal oscillator															
XT2	O	Output terminal for crystal oscillator															
V _{DD}	-	Positive power supply															
RES	I	Reset terminal															
FILT	O	Filter terminal for PLL															
CVIN	I	Video signal input terminal															
VS	I	Vertical synchronization signal input terminal															
HS	I	Horizontal synchronization signal input terminal															
R	O	Red (R) output terminal of RGB image output															
G	O	Green (G) output terminal of RGB image output															
B	O	Blue (B) output terminal of RGB image output															
I	O	Intensity (I) output terminal of RGB image output															
BL	O	Fast blanking control signal Switch TV image signal and caption/OSD image signal															
Port 0	I/O	•8-bit input/output port, Input/output can be specified in nibble unit •Other functions HOLD release input Interrupt input	Pull-up resistor provided/not provided Output Format CMOS/Nch-OD														
P00 to P07																	
Port 1	I/O	•8-bit input/output port Input/output can be specified in a bit •Other functions <table border="1"><tr><td>P10</td><td>SIO0 data output</td></tr><tr><td>P11</td><td>SIO0 data input/bus input/output</td></tr><tr><td>P12</td><td>SIO0 clock input/output</td></tr><tr><td>P13</td><td>PWM1 output</td></tr><tr><td>P14</td><td>PWM2 output</td></tr><tr><td>P15</td><td>PWM3 output</td></tr><tr><td>P17</td><td>Timer1 (PWM) output</td></tr></table>	P10	SIO0 data output	P11	SIO0 data input/bus input/output	P12	SIO0 clock input/output	P13	PWM1 output	P14	PWM2 output	P15	PWM3 output	P17	Timer1 (PWM) output	Output Format CMOS/Nch-OD
P10			SIO0 data output														
P11	SIO0 data input/bus input/output																
P12	SIO0 clock input/output																
P13	PWM1 output																
P14	PWM2 output																
P15	PWM3 output																
P17	Timer1 (PWM) output																
P10 to P17																	
Port 6	I/O	•4-bit input/output port Input/output can be specified for each bit •Other functions <table border="1"><tr><td>P60</td><td>IIC0 data I/O</td></tr><tr><td>P61</td><td>IIC0 clock output</td></tr><tr><td>P62</td><td>IIC1 data I/O</td></tr><tr><td>P63</td><td>IIC1 clock output</td></tr></table>	P60	IIC0 data I/O	P61	IIC0 clock output	P62	IIC1 data I/O	P63	IIC1 clock output							
P60			IIC0 data I/O														
P61	IIC0 clock output																
P62	IIC1 data I/O																
P63	IIC1 clock output																
P60 to P63																	

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LC863264C/56C/48C/40C/32C/28C/24C/20C/16C

Continued from preceding page.

Terminal	I/O	Function Description	Option																																											
Port 7	I/O	•4-bit input/output port Input or output can be specified for each bit •Other functions <table><tr><td>P70</td><td>INT0 input/HOLD release input/ Nch-Tr. output for watchdog timer</td></tr><tr><td>P71</td><td>INT1 input/HOLD release input</td></tr><tr><td>P72</td><td>INT2 input/Timer 0 event input</td></tr><tr><td>P73</td><td>INT3 input (noise rejection filter connected)/ Timer 0 event input</td></tr></table> Interrupt receiver format, vector addresses <table><tr><td></td><td>Rising</td><td>Falling</td><td>Rising/ Falling</td><td>H level</td><td>L level</td><td>Vector</td></tr><tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td><td>03H</td></tr><tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td><td>0BH</td></tr><tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td><td>13H</td></tr><tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td><td>1BH</td></tr></table>	P70	INT0 input/HOLD release input/ Nch-Tr. output for watchdog timer	P71	INT1 input/HOLD release input	P72	INT2 input/Timer 0 event input	P73	INT3 input (noise rejection filter connected)/ Timer 0 event input		Rising	Falling	Rising/ Falling	H level	L level	Vector	INT0	enable	enable	disable	enable	enable	03H	INT1	enable	enable	disable	enable	enable	0BH	INT2	enable	enable	enable	disable	disable	13H	INT3	enable	enable	enable	disable	disable	1BH	
P70			INT0 input/HOLD release input/ Nch-Tr. output for watchdog timer																																											
P71			INT1 input/HOLD release input																																											
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P73	INT3 input (noise rejection filter connected)/ Timer 0 event input																																													
	Rising	Falling	Rising/ Falling	H level	L level	Vector																																								
INT0	enable	enable	disable	enable	enable	03H																																								
INT1	enable	enable	disable	enable	enable	0BH																																								
INT2	enable	enable	enable	disable	disable	13H																																								
INT3	enable	enable	enable	disable	disable	1BH																																								
P70																																														
P71 to P73																																														
Port 8	I/O	•4-bit input/output port Input or output can be specified for each bit •Other function AD converter input port (4 lines)																																												
P84 to P87																																														
NC	-	Unused terminal Leave open																																												

- Output form and existence of pull-up resistor for all ports can be specified for each bit.
- Programmable pull-up resistor is always connected regardless of port option, CMOS or N-ch open drain output in port 1.

Port status in reset

Terminal	I/O	Pull-up resistor status at selecting pull-up option
Port 0	I	Pull-up resistor OFF, ON after reset release
Port 1	I	Programmable pull-up resistor OFF

LC863264C/56C/48C/40C/32C/28C/24C/20C/16C

Absolute Maximum Ratings / Ta = 25°C, VSS = 0V

Parameter		Symbol	Pins	Conditions	V _{DD} [V]	Ratings			unit
						min	typ	max	
Maximum supply voltage		V _{DD} max	V _{DD}			-0.3		+6.5	V
Input voltage		V _I (1)	$\overline{\text{RES}}$, $\overline{\text{HS}}$, $\overline{\text{VS}}$, CVIN			-0.3		V _{DD} +0.3	
Output voltage		V _O (1)	R, G, B, I, BL, FILT			-0.3		V _{DD} +0.3	
Input/output voltage		V _{IO}	Ports 0, 1, 6, 7, 8			-0.3		V _{DD} +0.3	
High level output current	Peak output current	IOPH(1)	Ports 0, 1, 7, 8	•CMOS output •For each pin.		-4			mA
		IOPH(2)	R, G, B, I, BL	•CMOS output •For each pin.		-5			
	Total output current	ΣIOAH(1)	Ports 0, 1	Total of all pins.		-20			
		ΣIOAH(2)	Ports 7, 8	Total of all pins.		-10			
		ΣIOAH(3)	R, G, B, I, BL	Total of all pins.		-15			
Low level output current	Peak output current	IOPL(1)	Ports 0, 1, 6, 8	For each pin.				20	
		IOPL(2)	Port 7	For each pin.				15	
		IOPL(3)	R, G, B, I, BL	For each pin.				5	
	Total output current	ΣIOAL(1)	Ports 0, 1	Total of all pins.				40	
		ΣIOAL(2)	Ports 6, 7, 8	Total of all pins.				40	
		ΣIOAL(3)	R, G, B, I, BL	Total of all pins.				15	
Maximum power dissipation		Pd max	DIP42S	Ta=-10 to +70°C				715	mW
			QIP48E					385	
Operating temperature range		Topr				-10		+70	°C
Storage temperature range		Tstg				-55		+125	

LC863264C/56C/48C/40C/32C/28C/24C/20C/16C

Recommended Operating Range / Ta = -10°C to +70°C, VSS = 0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings			unit
					min	typ	max	
Operating supply voltage range	VDD(1)	VDD	$0.844\mu s \leq t_{CYC} \leq 0.852\mu s$		4.5		5.5	V
	VDD(2)		$4\mu s \leq t_{CYC} \leq 400\mu s$		4.5		5.5	
Hold voltage	VHD	VDD	RAMs and the registers data are kept in HOLD mode.		2.0		5.5	
High level input voltage	VIH(1)	Port 0 (Schmitt)	Output disable	4.5 to 5.5	$0.6V_{DD}$		V_{DD}	
	VIH(2)	•Ports 1,6 (Schmitt) •Port 7 (Schmitt) port input/interrupt • $\overline{HS}$, $\overline{VS}$, $\overline{RES}$, (Schmitt)	Output disable	4.5 to 5.5	$0.75V_{DD}$		V_{DD}	
	VIH(3)	Port 70 Watchdog timer input	Output disable	4.5 to 5.5	$V_{DD}-0.5$		V_{DD}	
	VIH(4)	•Port 8 port input	Output disable	4.5 to 5.5	$0.7V_{DD}$		V_{DD}	
Low level input voltage	VIL(1)	Port 0 (Schmitt)	Output disable	4.5 to 5.5	V_{SS}		$0.2V_{DD}$	
	VIL(2)	•Ports 1,6 (Schmitt) •Port 7 (Schmitt) port input/interrupt • $\overline{HS}$, $\overline{VS}$, $\overline{RES}$, (Schmitt)	Output disable	4.5 to 5.5	V_{SS}		$0.25V_{DD}$	
	VIL(3)	Port 70 Watchdog timer input	Output disable	4.5 to 5.5	V_{SS}		$0.6V_{DD}$	
	VIL(4)	Port 8 port input	Output disable	4.5 to 5.5	V_{SS}		$0.3V_{DD}$	
CVIN	VCVIN	CVIN		5.0	1Vp-p -3dB	1Vp-p	1Vp-p +3dB	Vp-p*
Operation cycle time	tCYC(1)		•All functions operating	4.5 to 5.5	0.844	0.848	0.852	μs
	tCYC(2)		•AD converter operating •OSD and Data slicer are not operating	4.5 to 5.5	0.844		30	
	tCYC(3)		•OSD, AD converter and Data slicer are not operating	4.5 to 5.5	0.844		400	
Oscillation frequency range	FmRC		Internal RC oscillation	4.5 to 5.5	0.4	0.8	3.0	MHz

* Vp-p : Peak-to-peak voltage

LC863264C/56C/48C/40C/32C/28C/24C/20C/16C

Electrical Characteristics / Ta = -10°C to +70°C, VSS = 0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings			unit
					min	typ	max	
High level input current	I _{IH} (1)	Ports 0, 1, 6, 7, 8	•Output disable •Pull-up MOS Tr. OFF •V _{IN} =V _{DD} (including the off-leak current of the output Tr.)	4.5 to 5.5			1	μA
	I _{IH} (2)	• $\overline{\text{RES}}$ • $\overline{\text{HS}}$, $\overline{\text{VS}}$	•V _{IN} =V _{DD}	4.5 to 5.5			1	
Low level input current	I _{IL} (1)	Ports 0, 1, 6, 7, 8	•Output disable •Pull-up MOS Tr. OFF •V _{IN} =V _{SS} (including the off-leak current of the output Tr.)	4.5 to 5.5	-1			
	I _{IL} (2)	• $\overline{\text{RES}}$ • $\overline{\text{HS}}$, $\overline{\text{VS}}$	V _{IN} =V _{SS}	4.5 to 5.5	-1			
High level output voltage	V _{OH} (1)	•CMOS output of ports 0, 1, 71 to 73	I _{OH} =-1.0mA	4.5 to 5.5	V _{DD} -1			V
	V _{OH} (2)	R, G, B, I, BL	I _{OH} =-0.1mA	4.5 to 5.5	V _{DD} -0.5			
Low level output voltage	V _{OL} (1)	Ports 0, 1, 71 to 73	I _{OL} =10mA	4.5 to 5.5			1.5	
	V _{OL} (2)	Ports 0, 1, 71 to 73	I _{OL} =1.6mA	4.5 to 5.5			0.4	
	V _{OL} (3)	•R, G, B, I, BL •Port 6	I _{OL} =3.0mA	4.5 to 5.5			0.4	
	V _{OL} (4)	Port 6	I _{OL} =6.0mA	4.5 to 5.5			0.6	
	V _{OL} (5)	Port 70	I _{OL} =1mA	4.5 to 5.5			0.4	
Pull-up MOS Tr. resistance	R _{pu}	Ports 0, 1, 7, 8	V _{OH} =0.9V _{DD}	4.5 to 5.5	13	38	80	kΩ
Bus terminal short circuit resistance (SCL0-SCL1, SDA0-SDA1)	RBS	•P60 to P62 •P61 to P63		4.5 to 5.5		130	300	Ω
Hysteresis voltage	VHYS	•Ports 0, 1, 6, 7 • $\overline{\text{RES}}$ • $\overline{\text{HS}}$, $\overline{\text{VS}}$	Output disable	4.5 to 5.5		0.1V _{DD}		V
Input clump voltage	VCLMP	CVIN		5.0	2.3	2.5	2.7	
Pin capacitance	CP	All pins	•f=1MHz •Every other terminals are connected to V _{SS} . •Ta=25°C	4.5 to 5.5		10		pF

Serial Input/Output Characteristics / Ta = -10°C to +70°C, V_{SS} = 0V

Parameter			Symbol	Pins	Conditions	V _{DD} [V]	Ratings			unit
							min	typ	max	
Serial clock	Input clock	Cycle	tCKCY(1)	•SCK0 •SCLK0	Refer to figure 4.	4.5 to 5.5	2			tCYC
		Low Level pulse width	tCKL(1)				1			
		High Level pulse width	tCKH(1)				1			
	Output clock	Cycle	tCKCY(2)	•SCK0 •SCLK0	•Use pull-up resistor (1kΩ) when Nch open-drain output. •Refer to figure 4.	4.5 to 5.5	2			
		Low Level pulse width	tCKL(2)					1/2tCKCY		
		High Level pulse width	tCKH(2)					1/2tCKCY		
Serial input	Data set up time		tICK	SI0	•Data set-up to SCK0. •Data hold from SCK0. •Refer to figure 4.	4.5 to 5.5	0.1			μs
	Data hold time		tCKI				0.1			
Serial output	Output delay time (Using external clock)		tCKO(1)	SO0	•Data hold from SCK0. •Use pull-up resistor (1kΩ) when Nch open-drain output. •Refer to figure 4.	4.5 to 5.5			7/12tCYC +0.2	
	Output delay time (Using internal clock)		tCKO(2)	SO0		4.5 to 5.5			1/3tCYC +0.2	

IIC Input/Output Conditions / Ta = -10°C to +70°C, V_{SS} = 0V

Parameter	Symbol	Standard		High speed		unit
		min	max	min	max	
SCL Frequency	fSCL	0	100	0	400	kHz
BUS free time between stop - start	tBUF	4.7	-	1.3	-	μs
HOLD time of start, restart condition	tHD;STA	4.0	-	0.6	-	μs
L time of SCL	tLOW	4.7	-	1.3	-	μs
H time of SCL	tHIGH	4.0	-	0.6	-	μs
Set-up time of restart condition	tSU;STA	4.7	-	0.6	-	μs
HOLD time of SDA	tHD;DAT	0	-	0	0.9	μs
Set-up time of SDA	tSU;DAT	250	-	100	-	ns
Rising time of SDA, SCL	tR	-	1000	20+0.1Cb	300	ns
Falling time of SDA, SCL	tF	-	300	20+0.1Cb	300	ns
Set-up time of stop condition	tSU;STO	4.0	-	0.6	-	μs

Refer to figure 10

Note 1: Cb : Total capacitance of all BUS (unit : pF)

Pulse Input Conditions / Ta = -10°C to +70°C, VSS = 0V

Parameter	Symbol	Pins	Conditions	Ratings				unit
				V _{DD} [V]	min	typ	max	
High/low level pulse width	tPIH(1) tPIL(1)	•INT0, INT1 •INT2/T0IN	•Interrupt acceptable •Timer0-countable	4.5 to 5.5	1			tCYC
	tPIH(2) tPIL(2)	INT3/T0IN (1tCYC is selected for noise rejection clock.)	•Interrupt acceptable •Timer0-countable	4.5 to 5.5	2			
	tPIH(3) tPIL(3)	INT3/T0IN (16tCYC is selected for noise rejection clock.)	•Interrupt acceptable •Timer0-countable	4.5 to 5.5	32			
	tPIH(4) tPIL(4)	INT3/T0IN (64tCYC is selected for noise rejection clock.)	•Interrupt acceptable •Timer0-countable	4.5 to 5.5	128			
	tPIL(5)	$\overline{\text{RES}}$	Reset acceptable	4.5 to 5.5	200			μs
	tPIH(6) tPIL(6)	$\overline{\text{HS}}$, $\overline{\text{VS}}$	•Display position controllable •The active edge of $\overline{\text{HS}}$ and $\overline{\text{VS}}$ must be apart at least 1tCYC. •Refer to figure 6.	4.5 to 5.5	8			
Rising/falling time	tTHL tTLH	$\overline{\text{HS}}$	Refer to figure 6.	4.5 to 5.5			500	ns

AD Converter Characteristics / Ta = -10°C to +70°C, VSS = 0V

Parameter	Symbol	Pins	Conditions	V _{DD} [V]	Ratings			unit
					min	typ	max	
Resolution	N			4.5 to 5.5		8		bit
Absolute precision	ET		(Note 2)				±1.5	LSB
Conversion time	tCAD	AN4 to AN7	ADCR2=0 (Note 3)			16		tCYC
			ADCR2=1 (Note 3)			32		
Analog input voltage range	VAIN				V _{SS}		V _{DD}	V
Analog port input current	IAINH		VAIN=V _{DD}				1	μA
	IAINL		VAIN=V _{SS}			-1		

Note 2: Absolute precision does not include quantizing error (1/2LSB).

Note 3: Conversion time is the time till the complete digital conversion value for analog input value is set to a register after the instruction to start conversion is sent.

Sample Current Dissipation Characteristics / Ta= -10°C to +70°C, V_{SS}=0V

The sample current dissipation characteristics is the measurement result of Sanyo provided evaluation board when the recommended circuit parameters shown in the sample oscillation circuit characteristics are used externally. The currents through the output transistors and the pull-up MOS transistors are ignored.

Parameter	Symbol	Pins	Conditions	V _{DD} [V]	Ratings			unit
					min	typ	max	
Current dissipation during basic operation (Note 4)	IDDOP(1)	V _{DD}	•FmX'tal=32.768kHz X'tal oscillation •System clock : VCO •VCO for OSD operating •Internal RC oscillation stops	4.5 to 5.5		10	24	mA
Current dissipation in HALT mode (Note 4)	IDDHALT(1)	V _{DD}	•HALT mode •FmX'tal=32.768kHz X'tal oscillation •System clock : VCO •VCO for OSD stops •Internal RC oscillation stops	4.5 to 5.5		3	9	mA
	IDDHALT(2)	V _{DD}	•HALT mode •FmX'tal=32.768kHz X'tal oscillation •VCO for system stops •VCO for OSD stops •System clock : Internal RC	4.5 to 5.5		300	1000	μA
	IDDHALT(3)	V _{DD}	•HALT mode •FmX'tal=32.768kHz X'tal oscillation •VCO for system stops •VCO for OSD stops •System clock : X'tal	4.5 to 5.5		45	200	
Current dissipation in HOLD mode (Note 4)	IDDHOLD	V _{DD}	•HOLD mode •All oscillation stops.	4.5 to 5.5		0.05	20	μA

Note 4: The currents through the output transistors and the pull-up MOS transistors are ignored.

Recommended Oscillation Circuit and Sample Characteristics

The sample oscillation circuit characteristics in the table below is based on the following conditions:

Recommended circuit parameters are verified by an oscillator manufacturer using a Sanyo provided oscillation evaluation board.

Sample characteristics are the result of the evaluation with the recommended circuit parameters connected externally.

Recommended oscillation circuit and sample characteristics (Ta = -10 to +70°C)

Frequency	Manufacturer	Oscillator	Recommended circuit parameters				Operating supply voltage range	Oscillation stabilizing time		Notes
			C1	C2	Rf	Rd		typ	max	
32.768kHz	SEIKO EPSON	C-002RX	18pF	18pF	OPEN	390kΩ	4.5 to 5.5V	1.0s	1.5s	

Notes: The oscillation stabilizing time period is the time until the VCO oscillation for the internal system becomes stable after the following conditions. (Refer to Figure 2.)

1. The VDD becomes higher than the minimum operating voltage after the power is supplied.
2. The HOLD mode is released.

The sample oscillation circuit characteristics may differ applications. For further assistance, please contact with oscillator manufacturer with the following notes in your mind.

- Since the oscillation frequency precision is affected by wiring capacity of the application board, etc., adjust the oscillation frequency on the production board.
- The above oscillation frequency and the operating supply voltage range are based on the operating temperature of -10°C to +70°C. For the use with the temperature outside of the range herein, or in the applications requiring high reliability such as car products, please consult with oscillator manufacturer.
- When using the oscillator which is not shown in the sample oscillation circuit characteristics, please consult with Sanyo sales personnel.

Since the oscillation circuit characteristics are affected by the noise or wiring capacity because the circuit is designed with low gain in order to reduce the power dissipation, refer to the following notices.

- The distance between the clock I/O terminal (XT1 terminal XT2 terminal) and external parts should be as short as possible.
- The capacitors' VSS should be allocated close to the microcontroller's GND terminal and be away from other GND.
- The signal lines with rapid state changes or with large current should be allocated away from the oscillation circuit.

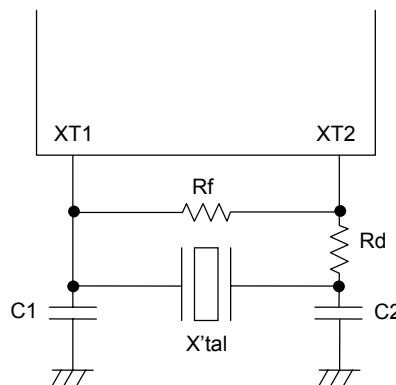
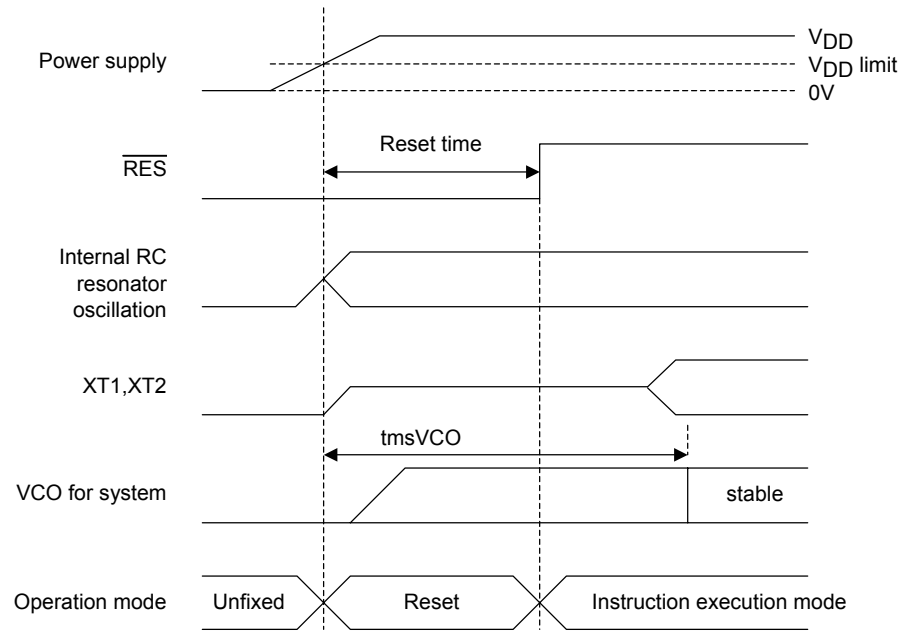
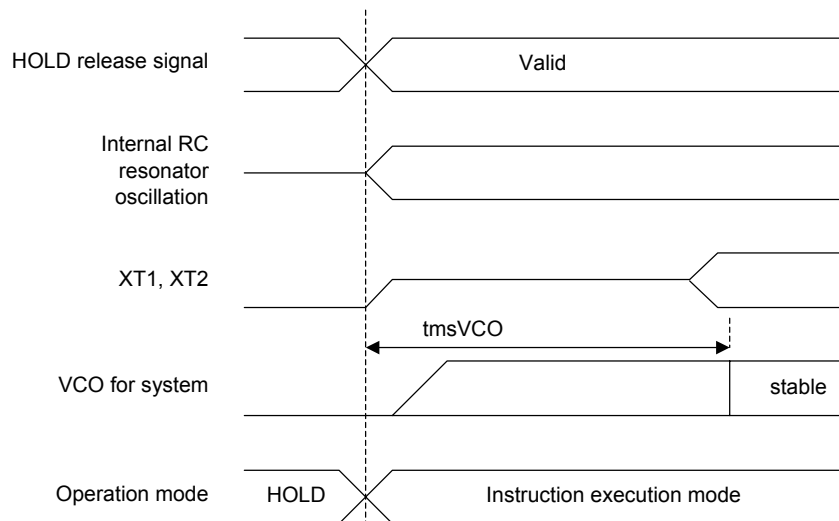


Figure 1 Recommended Oscillation Circuit

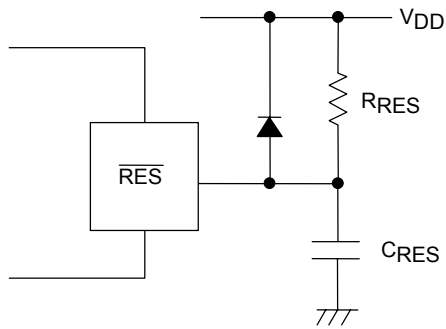


Reset Time and Oscillation Stabilizing Time



HOLD Release Signal and Oscillation Stabilizing Time

Figure 2 Oscillation Stabilizing Time



Note: Determine the C_{RES} , R_{RES} value to generate more than $200\mu s$ reset time.

Figure 3 Reset Circuit



AC Timing Measurement Point

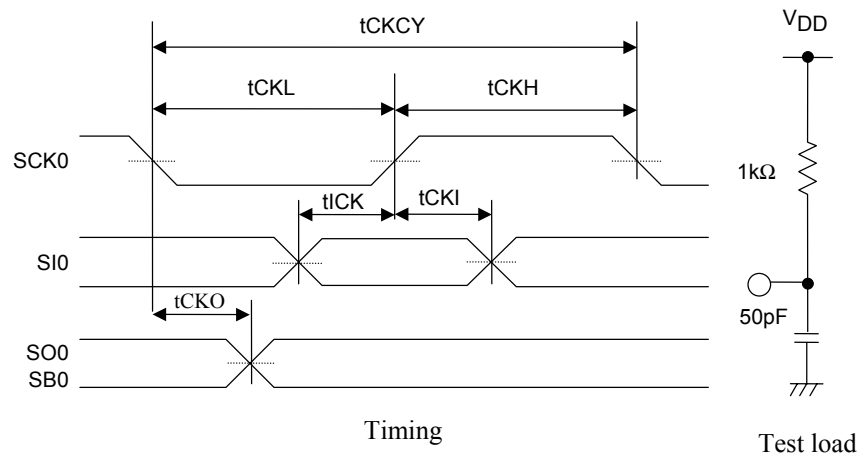


Figure 4 Serial Input / Output Test Condition

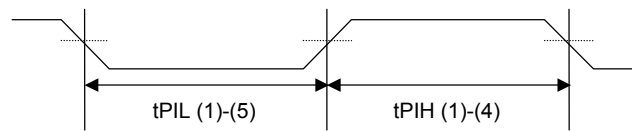


Figure 5 Pulse Input Timing Condition - 1

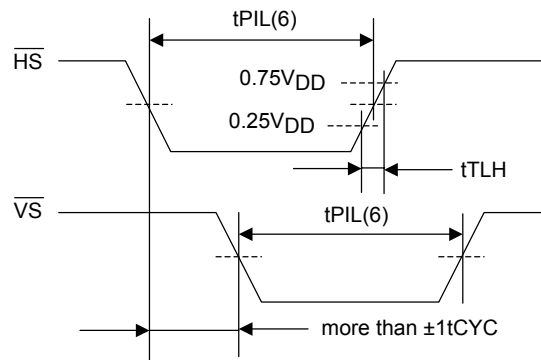


Figure 6 Pulse Input Timing Condition - 2

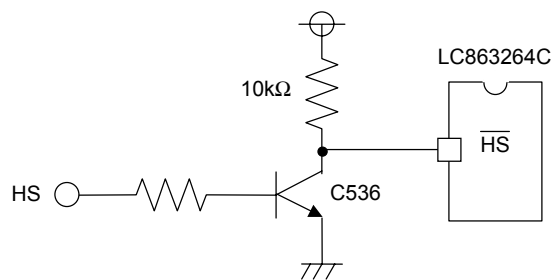
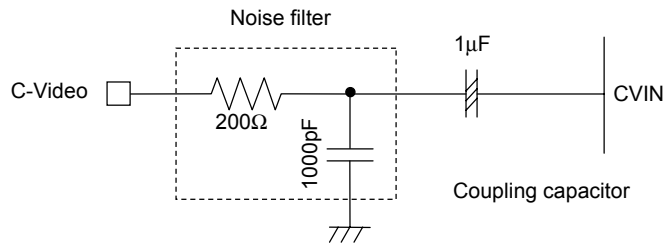


Figure 7 Recommended Interface Circuit



Output impedance of C-Video before Noise filter should be less than 100Ω.
Figure 8 CVIN Recommended Circuit

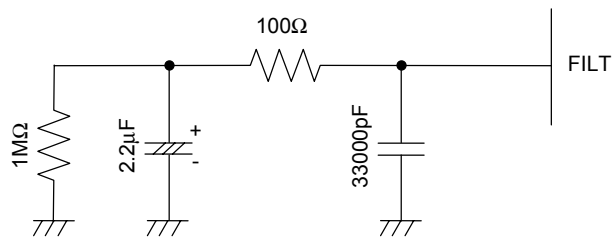
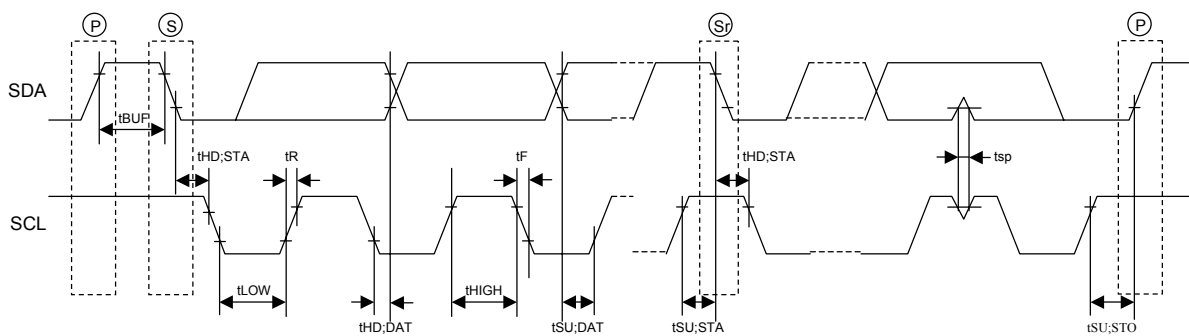


Figure 9 FILT Recommended Circuit
(Note) Place FILT parts on board as close to the microcontroller as possible.



S : start condition
P : stop condition
Sr : restart condition

tsp : spike suppression

Standard mode : not exist
High speed mode : less than 50ns

Figure 10 IIC Timing

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