

UT54ACS280/UT54ACTS280

Radiation-Hardened

9-Bit Parity Generators/Checkers

FEATURES

- Generates either odd or even parity for nine data lines
- Cascadable for n-bits parity
- 1.2 μ radiation-hardened CMOS
 - Latchup immune
- High speed
- Low power consumption
- Single 5 volt supply
- Available QML Q or V processes
- Flexible package
 - 14-pin DIP
 - 14-lead flatpack

DESCRIPTION

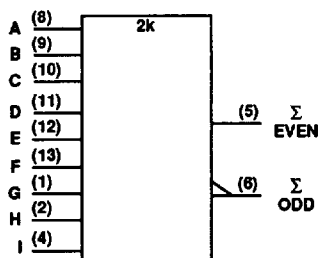
The UT54ACS280 and the UT54ACTS280 are 9-bit parity generators/checkers that use high-performance circuitry and features odd and even outputs to facilitate operation of either odd or even parity application. The word-length capability is easily expanded by cascading.

The devices are characterized over full military temperature range of -55°C to +125°C.

FUNCTION TABLE

NUMBER OF INPUTS A THRU I THAT ARE HIGH	OUTPUT	
	Σ EVEN	Σ ODD
0,2,4,6,8	H	L
1,3,5,7,9	L	H

LOGIC SYMBOL

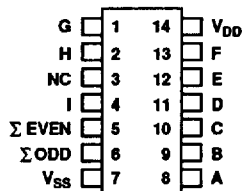


Note:

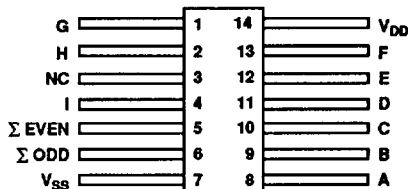
1. Logic symbol in accordance with ANSI/IEEE standard 91-1984 and IEC Publication 617-12.

PINOUTS

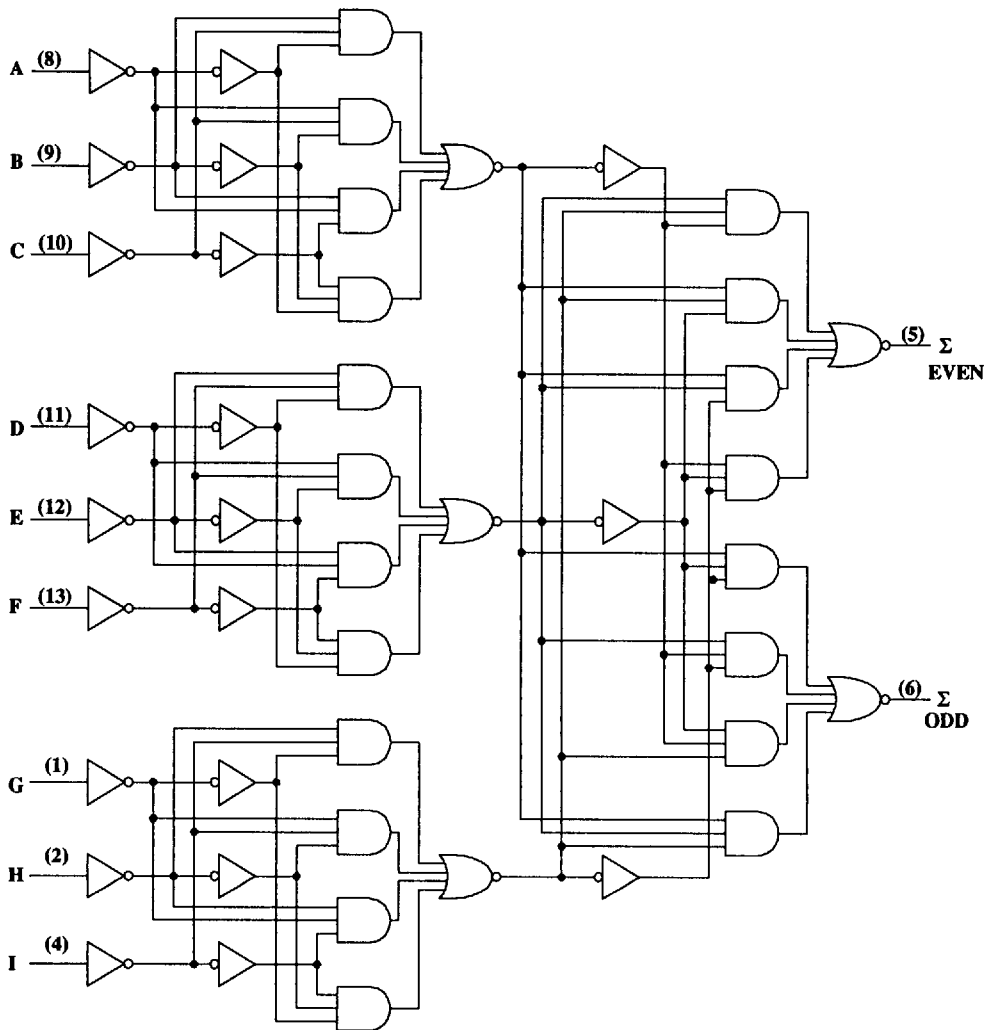
14-Pin DIP Top View



14-Lead Flatpack Top View



LOGIC DIAGRAM



RADIATION HARDNESS SPECIFICATIONS ¹

PARAMETER	LIMIT	UNITS
Total Dose	1.0E6	rads(Si)
SEU & SEL Threshold ²	80	MeV-cm ² /mg
Neutron Fluence	1.0E14	n/cm ²

Notes:

1. Logic will not latchup during radiation exposure within the limits defined in the table.
 2. Device storage elements are immune to SEU affects.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	LIMIT	UNITS
V _{DD}	Supply voltage	-0.3 to 7.0	V
V _{IO}	Input voltage any pin	-.3 to V _{DD} +.3	V
T _{STG}	Storage Temperature range	-65 to +150	°C
T _J	Maximum junction temperature	+175	°C
T _{LS}	Lead temperature (soldering 5 seconds)	+300	°C
Θ _{JC}	Thermal resistance junction to case	20	°C/W
I _I	DC input current	±10	mA
P _D	Maximum power dissipation	1	W

Note:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMIT	UNITS
V _{DD}	Supply voltage	4.5 to 5.5	V
V _{IN}	Input voltage any pin	0 to V _{DD}	V
T _C	Temperature range	-55 to + 125	°C

DC ELECTRICAL CHARACTERISTICS ⁷(V_{DD} = 5.0V ±10%; V_{SS} = 0V ⁶, -55°C < T_C < +125°C)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
V _{IL}	Low-level input voltage ¹ ACTS ACS			0.8 .3V _{DD}	V
V _{IH}	High-level input voltage ¹ ACTS ACS		.5V _{DD} .7V _{DD}		V
I _{IN}	Input leakage current ACTS/ACS	V _{IN} = V _{DD} or V _{SS}	-1	1	μA
V _{OL}	Low-level output voltage ³ ACTS ACS	I _{OL} = 8.0mA I _{OL} = 100μA		0.40 0.25	V
V _{OH}	High-level output voltage ³ ACTS ACS	I _{OH} = -8.0mA I _{OH} = -100μA	.7V _{DD} V _{DD} - 0.25		V
I _{OS}	Short-circuit output current ^{2,4} ACTS/ACS	V _O = V _{DD} and V _{SS}	-200	200	mA
P _{total}	Power dissipation ^{8,9}	C _L = 50pF		2.2	mW/ MHz
I _{DDQ}	Quiescent Supply Current	V _{DD} = 5.5V		10	μA
C _{IN}	Input capacitance ⁵	f = 1MHz @ 0V		15	pF
C _{OUT}	Output capacitance ⁵	f = 1MHz @ 0V		15	pF

Notes:

- Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: V_{IH} = V_{IH}(min) + 20%; - 0%; V_{IL} = V_{IL}(max) + 0%, - 50%, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to V_{IH}(min) and V_{IL}(max).
- Supplied as a design limit but not guaranteed or tested.
- Per MIL-M-38510, for current density ≤ 5.0E5 amps/cm², the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765 pF MHz.
- Not more than one output may be shorted at a time for maximum duration of one second.
- Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at frequency of 1MHz and a signal amplitude of 50mV rms maximum.
- Maximum allowable relative shift equals 50mV.
- All specifications valid for radiation dose ≤ 1E6 rads(Si).
- Power does not include power contribution of any TTL output sink current.
- Power dissipation specified per switching output.

UT54ACS280/UT54ACTS280

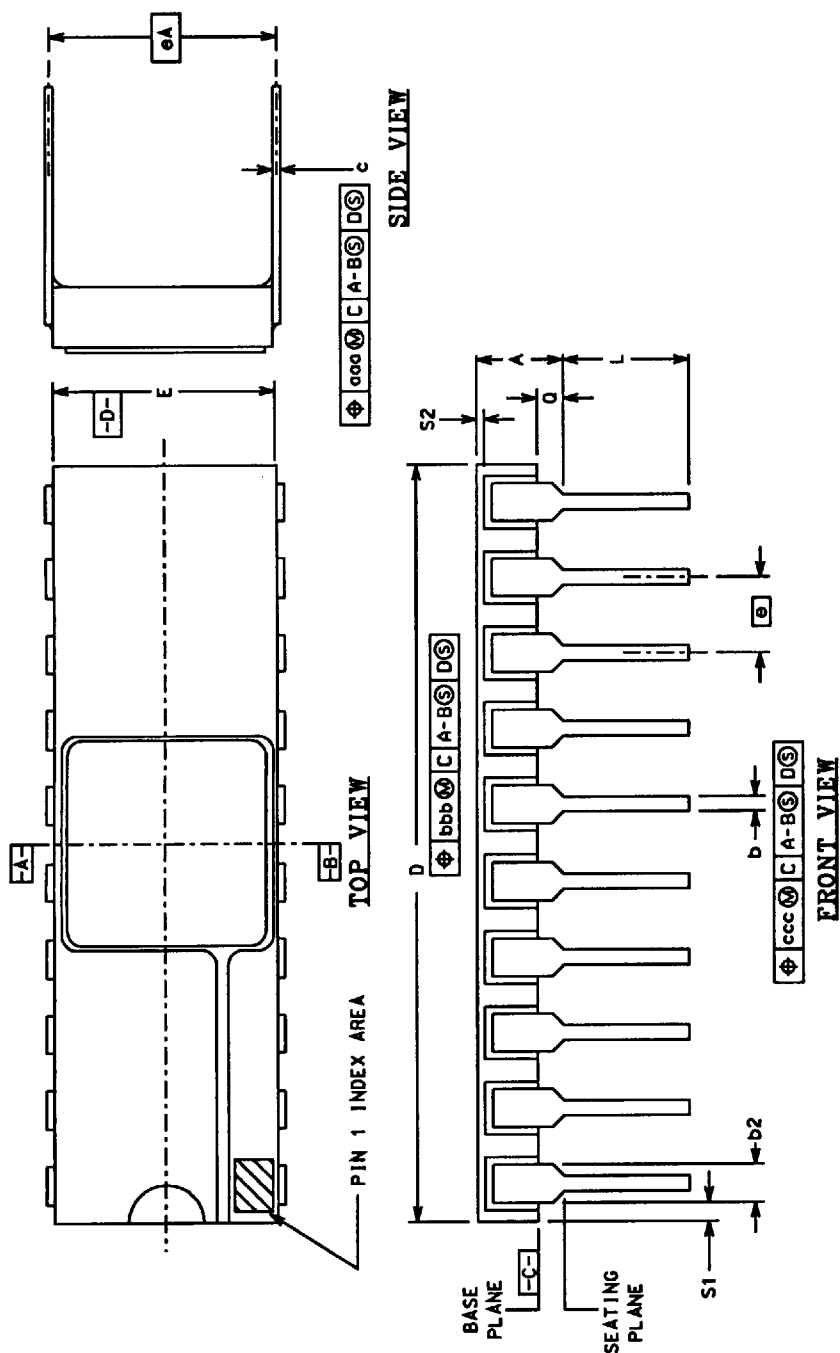
AC ELECTRICAL CHARACTERISTICS ²

(V_{DD} = 5.0V ±10%; V_{SS} = 0V ¹, -55°C < T_C < +125°C)

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
t _{PLH}	Any input to Σ even	1	20	ns
t _{PHL}	Any input to Σ even	1	20	ns
t _{PHL}	Any input to Σ odd	1	22	ns
t _{PLH}	Any input to Σ odd	1	20	ns

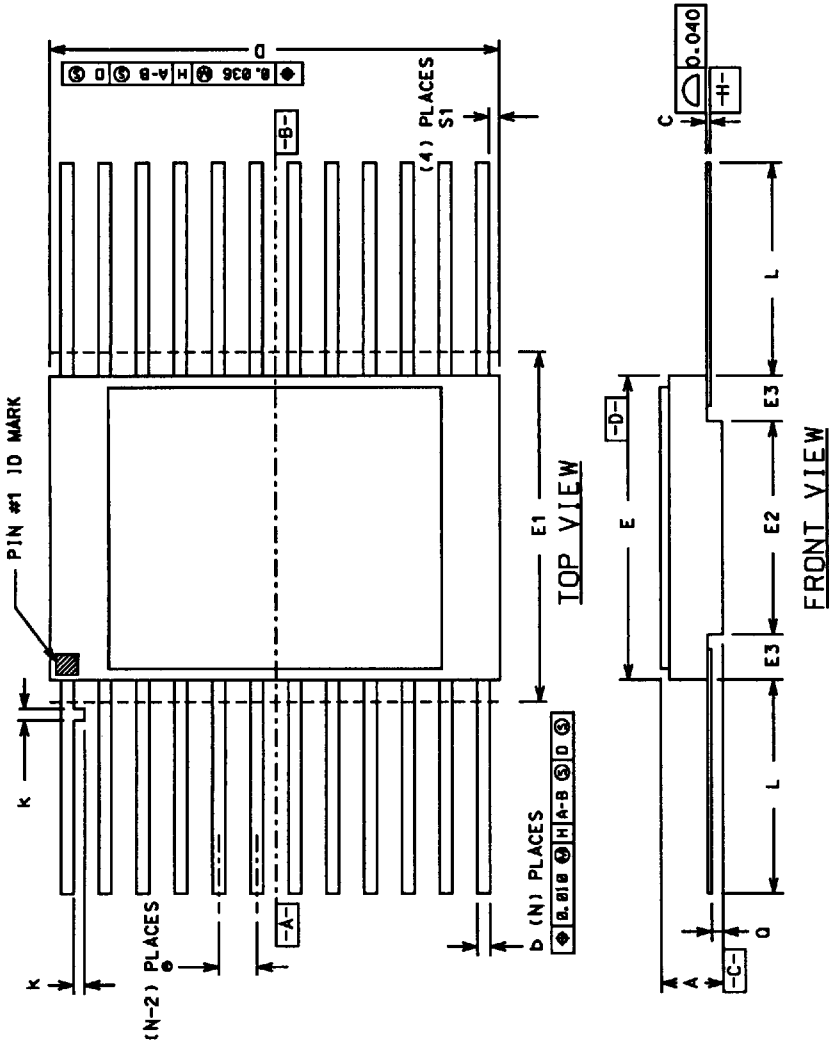
- Notes:
- 1. Maximum allowable relative shift equals 50mV.
 - 2. All specifications valid for radiation dose ≤ 1E6 rads(Si).

Side-Brazed Packages



PKG CONF	WIL-STD- 1835 DWG CONF C	DIMENSION SYMBOLS														
		A	B	B2	C	D	E	e	eA	L	Q	S1	S2	OOB	DOB	DOE
-01	D-1	0.200	0.026	0.065	0.018	0.785	0.310	0.100	0.300	0.200	0.060	0.005	0.005	0.015	0.030	0.010
-02	D-2	0.200	0.026	0.065	0.018	0.840	0.310	0.100	0.300	0.200	0.060	0.005	0.005	0.015	0.030	0.010
-03	D-8	0.200	0.026	0.065	0.018	1.060	0.310	0.100	0.300	0.200	0.070	0.005	0.005	0.015	0.030	0.010
		0.200	0.014	0.045	0.008	0.220	0.220	0.100	0.300	0.125	0.015	0.005	0.005	0.005	0.005	0.005

Flatpack Packages



PKG CONF LG	LEAD COUNT	ML-STD 1836 DWG CONF #	DIMENSION SYMBOLS												
			A	B	C	D	E	E1	E2	E3	Ø	K	L	O	S1
-03	14	F-2A	0.115 0.045	0.022 0.015	0.009 0.004	0.390 0.000	0.260 0.235	0.290 0.130	0.050 BSC	0.015 0.008	0.370 0.270	0.045 0.026	0.005		
-04	16	F-5A	0.115 0.045	0.022 0.015	0.009 0.004	0.440 0.000	0.285 0.245	0.315 0.130	0.050 BSC	0.015 0.008	0.370 0.250	0.045 0.026	0.005		
-05	20	F-9A	0.115 0.045	0.022 0.015	0.009 0.004	0.540 0.000	0.300 0.245	0.330 0.130	0.050 BSC	0.015 0.008	0.370 0.250	0.045 0.026	0.000		