UT54ACS193/UT54ACTS193

Radiation-Hardened
Synchronous 4-Bit Up-Down Dual Clock Counters

FEATURES

- Look-ahead circuitry enhances cascaded counters
- Fully synchronous in count modes
- Parallel asynchronous load for modulo-N count lengths
- Asynchronous clear
- 1.2µ radiation-hardened CMOS
  - Latchup immune
- High speed
- Low power consumption
- Single 5 volt supply
- Available QML Q or V processes
- Flexible package
  - 16-pin DIP
  - 16-lead flatpack

DESCRIPTION

The UT54ACS193 and the UT54ACTS193 are synchronous 4-bit, binary reversible up-down binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when instructed. Synchronous operation eliminates the output counting spikes normally associated with asynchronous counters.

The outputs of the four flip-flops are triggered on a low-to-high-level transition of either count input (Up or Down). The direction of the counting is determined by which count input is pulsed while the other count input is high.

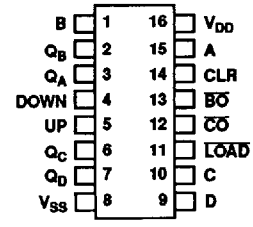
The counters are fully programmable. The outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the count pulses. Asynchronous loading allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided that forces all outputs to the low level when a high level is applied. The clear function is independent of the count and the load inputs.

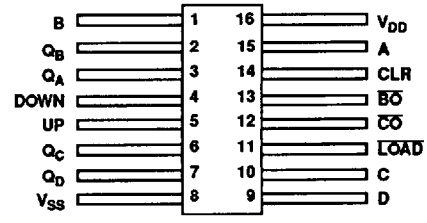
The counter is designed for efficient cascading without the need for external circuitry. The borrow output ($\overline{BO}$) produces a low-level pulse while the count is zero and the down input is low. Similarly, the carry output ($\overline{CO}$) produces a low-level pulse while the count is maximum

PINOUTS

16-Pin DIP
Top View



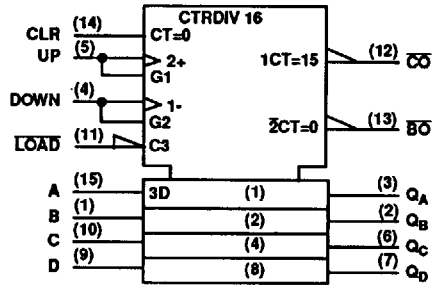
16-Lead Flatpack
Top View



FUNCTION TABLE

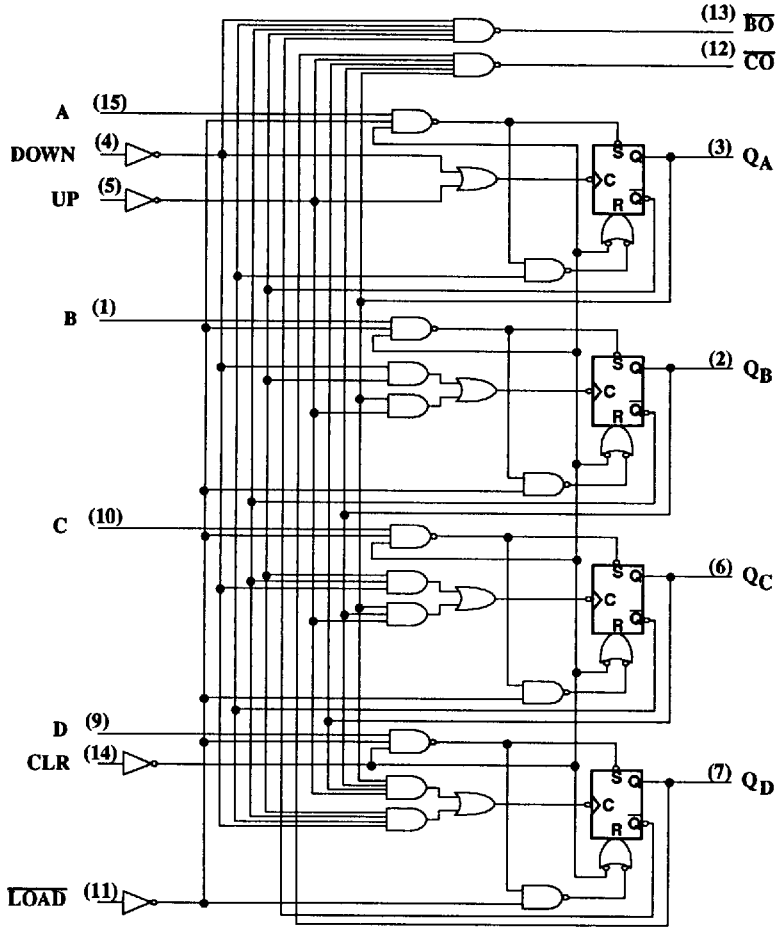
FUNCTION	CLOCK UP	CLOCK DOWN	CLR	$\overline{LOAD}$
Count Up	↑	H	L	H
Count Down	H	↑	L	H
Reset	X	X	H	X
Load Preset Input	X	X	L	L

LOGIC SYMBOL



Note:
1. Logic symbol in accordance with ANSI/IEEE standard 91-1984 and IEC Publication 617-12.

LOGIC DIAGRAM



RADIATION HARDNESS SPECIFICATIONS [1]

PARAMETER	LIMIT	UNITS
Total Dose	1.0E6	rads(Si)
SEU & SEL Threshold [2]	80	MeV-cm^2/mg
Neutron Fluence	1.0E14	n/cm^2

Notes:
1. Logic will not latchup during radiation exposure within the limits defined in the table.
2. Device storage elements are immune to SEU affects.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	LIMIT	UNITS
V_{DD}	Supply voltage	-0.3 to 7.0	V
$V_{I/O}$	Voltage any pin	-.3 to V_{DD} +.3	V
T_{STG}	Storage Temperature range	-65 to +150	°C
T_J	Maximum junction temperature	+175	°C
T_{LS}	Lead temperature (soldering 5 seconds)	+300	°C
Θ_{JC}	Thermal resistance junction to case	20	°C/W
I_I	DC input current	±10	mA
P_D	Maximum power dissipation	1	W

Note:
1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMIT	UNITS
V_{DD}	Supply voltage	4.5 to 5.5	V
V_{IN}	Input voltage any pin	0 to V_{DD}	V
T_C	Temperature range	-55 to + 125	°C

DC ELECTRICAL CHARACTERISTICS [7]

(V_{DD} = 5.0V ±10%; V_{SS} = 0V [6], -55°C < T_C < +125°C)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
V_{IL}	Low-level input voltage [1] ACTS ACS			0.8 .3V_{DD}	V
V_{IH}	High-level input voltage [1] ACTS ACS		.5V_{DD} .7V_{DD}		V
I_{IN}	Input leakage current ACTS/ACS	V_{IN} = V_{DD} or V_{SS}	-1	1	µA
V_{OL}	Low-level output voltage [3] ACTS ACS	I_{OL} = 8.0mA I_{OL} = 100µA		0.40 0.25	V
V_{OH}	High-level output voltage [3] ACTS ACS	I_{OH} = -8.0mA I_{OH} = -100µA	.7V_{DD} V_{DD} - 0.25		V
I_{OS}	Short-circuit output current [2,4] ACTS/ACS	V_O = V_{DD} and V_{SS}	-200	200	mA
P_{total}	Power dissipation [8,9]	C_L = 50pF		2.1	mW/ MHz
I_{DDQ}	Quiescent Supply Current	V_{DD} = 5.5V		10	µA
C_{IN}	Input capacitance [5]	f = 1MHz @ 0V		15	pF
C_{OUT}	Output capacitance [5]	f = 1MHz @ 0V		15	pF

Notes:

1. Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: V_{IH} = V_{IH}(min) + 20%, - 0%; V_{IL} = V_{IL}(max) + 0%, - 50%, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to V_{IH}(min) and V_{IL}(max).
2. Supplied as a design limit but not guaranteed or tested.
3. Per MIL-M-38510, for current density ≤ 5.0E5 amps/cm^2, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765 pF MHz.
4. Not more than one output may be shorted at a time for maximum duration of one second.
5. Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at frequency of 1MHz and a signal amplitude of 50mV rms maximum.
6. Maximum allowable relative shift equals 50mV.
7. All specifications valid for radiation dose ≤ 1E6 rads(Si).
8. Power does not include power contribution of any TTL output sink current.
9. Power dissipation specified per switching output.

AC ELECTRICAL CHARACTERISTICS [2]

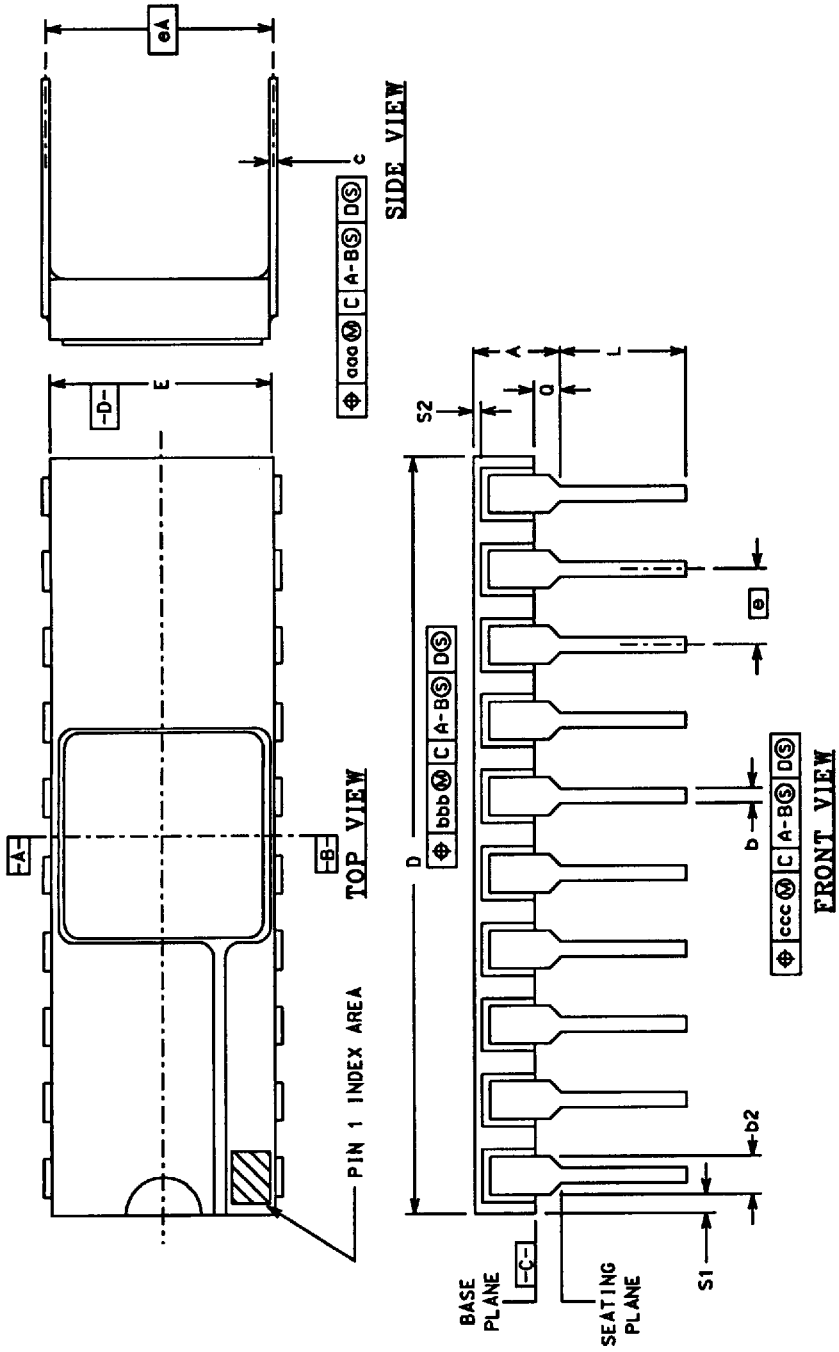
(V_{DD} = 5.0V ±10%; V_{SS} = 0V [1], -55°C < T_C < +125°C)

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
t_{PLH}	UP to Q_n	2	20	ns
t_{PHL}	UP to Q_n	2	24	ns
t_{PLH}	UP to $\overline{CO}$	2	13	ns
t_{PHL}	UP to $\overline{CO}$	2	16	ns
t_{PLH}	DOWN to $\overline{BO}$	2	13	ns
t_{PHL}	DOWN to $\overline{BO}$	2	16	ns
t_{PLH}	DOWN to Q_n	2	20	ns
t_{PHL}	DOWN to Q_n	2	24	ns
t_{PLH}	$\overline{LOAD}$ to Q_n	2	22	ns
t_{PHL}	$\overline{LOAD}$ to Q_n	2	23	ns
t_{PHL}	CLR to Q_n	2	22	ns
f_{MAX}	Maximum clock frequency		56	MHz
t_{SU}	Setup time before UP or DOWN ↑ $\overline{LOAD}$ inactive CLR inactive	3		ns
	A, B, C, D setup time before $\overline{LOAD}$ ↑	6		
t_H	UP high hold time after DOWN ↑ DOWN high hold time after UP ↑	20		ns
	A, B, C, D hold time after $\overline{LOAD}$ ↑	2		
t_W	Minimum pulse width UP high or low DOWN high or low $\overline{LOAD}$ low CLR high	9		ns

Notes:
1. Maximum allowable relative shift equals 50mV.
2. All specifications valid for radiation dose ≤ 1E6 rads(Si).

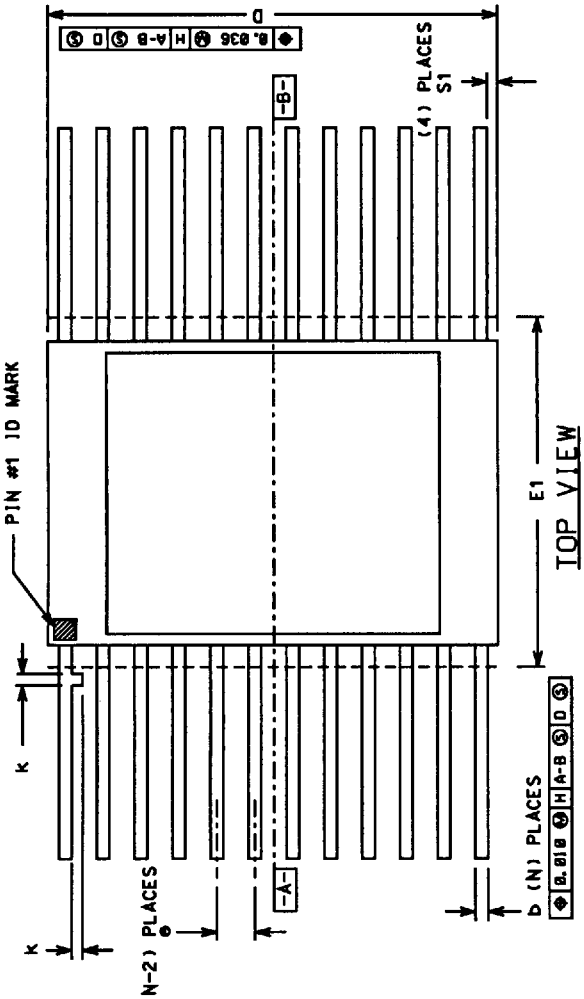
2.0 RAD-HARD MSI PACKAGES

Side-Brazed Packages



PKG CONFIG	LEAD COUNT	MIL-STD-1835 DWG CONF C	DIMENSION SYMBOLS																
			A	b	b2	c	D	E	e	eA	L	Q	S1	S2	aaa	bbb	ccc
-01	14	D-1	0.200 MAX	0.026 0.014	0.065 0.045	0.018 0.008	0.785 MAX	0.310 0.220	0.100 BSC	0.300 BSC	0.200 0.125	0.060 0.015	MIN 0.005	MIN 0.005	0.015 MAX	0.030 MAX	0.010 MAX
-02	16	D-2	0.200 MAX	0.026 0.014	0.065 0.045	0.018 0.008	0.840 MAX	0.310 0.220	0.100 BSC	0.300 BSC	0.200 0.125	0.060 0.015	MIN 0.005	MIN 0.005	0.015 MAX	0.030 MAX	0.010 MAX
-03	20	D-8	0.200 MAX	0.026 0.014	0.065 0.045	0.018 0.008	1.060 MAX	0.310 0.220	0.100 BSC	0.300 BSC	0.200 0.125	0.070 0.015	MIN 0.005	MIN 0.005	0.015 MAX	0.030 MAX	0.010 MAX

Flatpack Packages



PKG CONFIG	LEAD COUNT	MIL-STD 1835 DWG CONF B	DIMENSION SYMBOLS														
			A	b	c	D	E	E1	E2	E3	e	k	L	Q	S1
-03	14	F-2A	0.115 0.045	0.022 0.015	0.009 0.004	0.390 -----	0.260 0.235	0.290 -----	----- 0.130	----- 0.030	0.050 BSC	0.015 0.008	0.370 0.270	0.045 0.026	----- 0.005
-04	16	F-5A	0.115 0.045	0.022 0.015	0.009 0.004	0.440 -----	0.285 0.245	0.315 -----	----- 0.130	----- 0.030	0.050 BSC	0.015 0.008	0.370 0.250	0.045 0.026	----- 0.005
-05	20	F-9A	0.115 0.045	0.022 0.015	0.009 0.004	0.540 -----	0.300 0.245	0.330 -----	----- 0.130	----- 0.030	0.050 BSC	0.015 0.008	0.370 0.250	0.045 0.026	----- 0.000