

UT54ACS240/UT54ACTS240

Radiation-Hardened

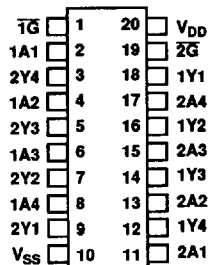
Octal Buffers & Line Drivers, Inverted Three-State Outputs

FEATURES

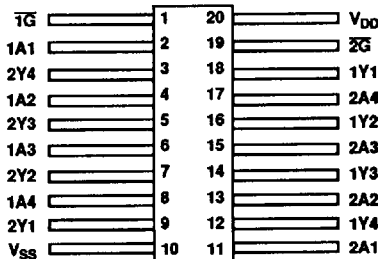
- Three-state outputs drive bus lines or buffer memory address registers
- 1.2 μ radiation-hardened CMOS
 - Latchup immune
- High speed
- Low power consumption
- Single 5 volt supply
- Available QML Q or V processes
- Flexible package
 - 20-pin DIP
 - 20-lead flatpack

PINOUTS

20-Pin DIP Top View



20-Lead Flatpack Top View



DESCRIPTION

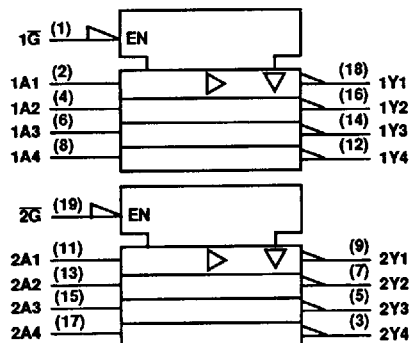
The UT54ACS240 and the UT54ACTS240 are inverting octal buffer and line drivers which improve the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The devices are characterized over full military temperature range of -55°C to +125°C.

FUNCTION TABLE

INPUTS		OUTPUT
1G, 2G	A	Y
L	L	H
L	H	L
H	X	Z

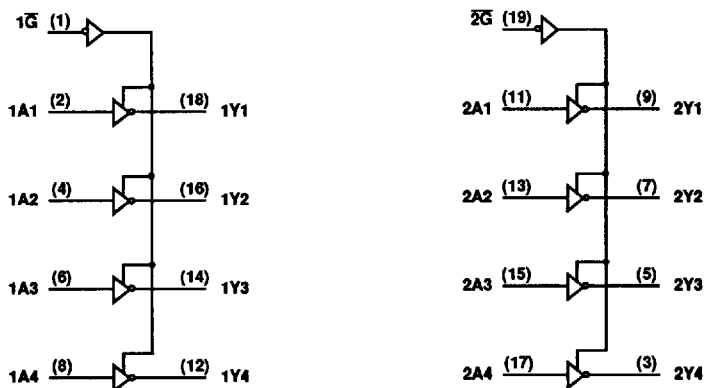
LOGIC SYMBOL



Note:

1. This symbols is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

LOGIC DIAGRAM

RADIATION HARDNESS SPECIFICATIONS ¹

PARAMETER	LIMIT	UNITS
Total Dose	1.0E6	rads(Si)
SEU & SEL Threshold ²	80	MeV-cm ² /mg
Neutron Fluence	1.0E14	n/cm ²

Notes:

1. Logic will not latchup during radiation exposure within the limits defined in the table
 2. Device storage elements are immune to SEU affects.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	LIMIT	UNITS
V _{DD}	Supply voltage	-0.3 to 7.0	V
V _{IO}	Voltage any pin	-.3 to V _{DD} +.3	V
T _{STG}	Storage Temperature range	-65 to +150	°C
T _J	Maximum junction temperature	+175	°C
T _{LS}	Lead temperature (soldering 5 seconds)	+300	°C
Θ _{JC}	Thermal resistance junction to case	20	°C/W
I _I	DC input current	±10	mA
P _D	Maximum power dissipation	1	W

Note:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMIT	UNITS
V _{DD}	Supply voltage	4.5 to 5.5	V
V _{IN}	Input voltage any pin	0 to V _{DD}	V
T _C	Temperature range	-55 to + 125	°C

UT54ACS240/UT54ACTS240

DC ELECTRICAL CHARACTERISTICS ⁷

($V_{DD} = 5.0V \pm 10\%$; $V_{SS} = 0V$ ⁶, $-55^{\circ}C < T_C < +125^{\circ}C$)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
V_{IL}	Low-level input voltage ¹ ACTS ACS			0.8 .3 V_{DD}	V
V_{IH}	High-level input voltage ¹ ACTS ACS		.5 V_{DD} .7 V_{DD}		V
I_{IN}	Input leakage current ACTS/ACS	$V_{IN} = V_{DD}$ or V_{SS}	-1	1	μA
V_{OL}	Low-level output voltage ³ ACTS ACS	$I_{OL} = 12.0mA$ $I_{OL} = 100\mu A$		0.40 0.25	V
V_{OH}	High-level output voltage ³ ACTS ACS	$I_{OH} = -12.0mA$ $I_{OH} = -100\mu A$	.7 V_{DD} $V_{DD} - 0.25$		V
I_{OZ}	Three-state output leakage current	$V_O = V_{DD}$ and V_{SS}	-30	30	μA
I_{OS}	Short-circuit output current ^{2,4} ACTS/ACS	$V_O = V_{DD}$ and V_{SS}	-300	300	mA
P_{total}	Power dissipation ^{8,9}	$C_L = 50pF$		2.1	mW/ MHz
I_{DDQ}	Quiescent Supply Current	$V_{DD} = 5.5V$		10	μA
C_{IN}	Input capacitance ⁵	$f = 1MHz @ 0V$		15	pF
C_{OUT}	Output capacitance ⁵	$f = 1MHz @ 0V$		15	pF

Notes:

- Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: $V_{IH} = V_{IH(min)} + 20\%$, -0% ; $V_{IL} = V_{IL(max)} + 0\%$, -50% , as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to $V_{IH(min)}$ and $V_{IL(max)}$.
- Supplied as a design limit but not guaranteed or tested.
- Per MIL-M-38510, for current density $\leq 5.0E5$ amps/cm², the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765 pF MHz.
- Not more than one output may be shorted at a time for maximum duration of one second.
- Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at frequency of 1MHz and a signal amplitude of 50mV rms maximum.
- Maximum allowable relative shift equals 50mV.
- All specifications valid for radiation dose $\leq 1E6$ rads(Si).
- Power does not include power contribution of any TTL output sink current.
- Power dissipation specified per switching output.

AC ELECTRICAL CHARACTERISTICS ²(V_{DD} = 5.0V ±10%; V_{SS} = 0V ¹, -55°C < T_C < +125°C)

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
t _{PLH}	Input to Yn	1	10	ns
t _{PHL}	Input to Yn	1	13	ns
t _{PZL}	$\overline{G}$ low to Yn active	1	11	ns
t _{PZH}	$\overline{G}$ low to Yn active	2	13	ns
t _{PLZ}	$\overline{G}$ high to Yn three-state	2	11	ns
t _{PHZ}	$\overline{G}$ high to Yn three-state	2	14	ns
t _{TLH}	Output transition time ³	1	6	ns
t _{THL}	Output transition time ³	1	6	ns

Notes:

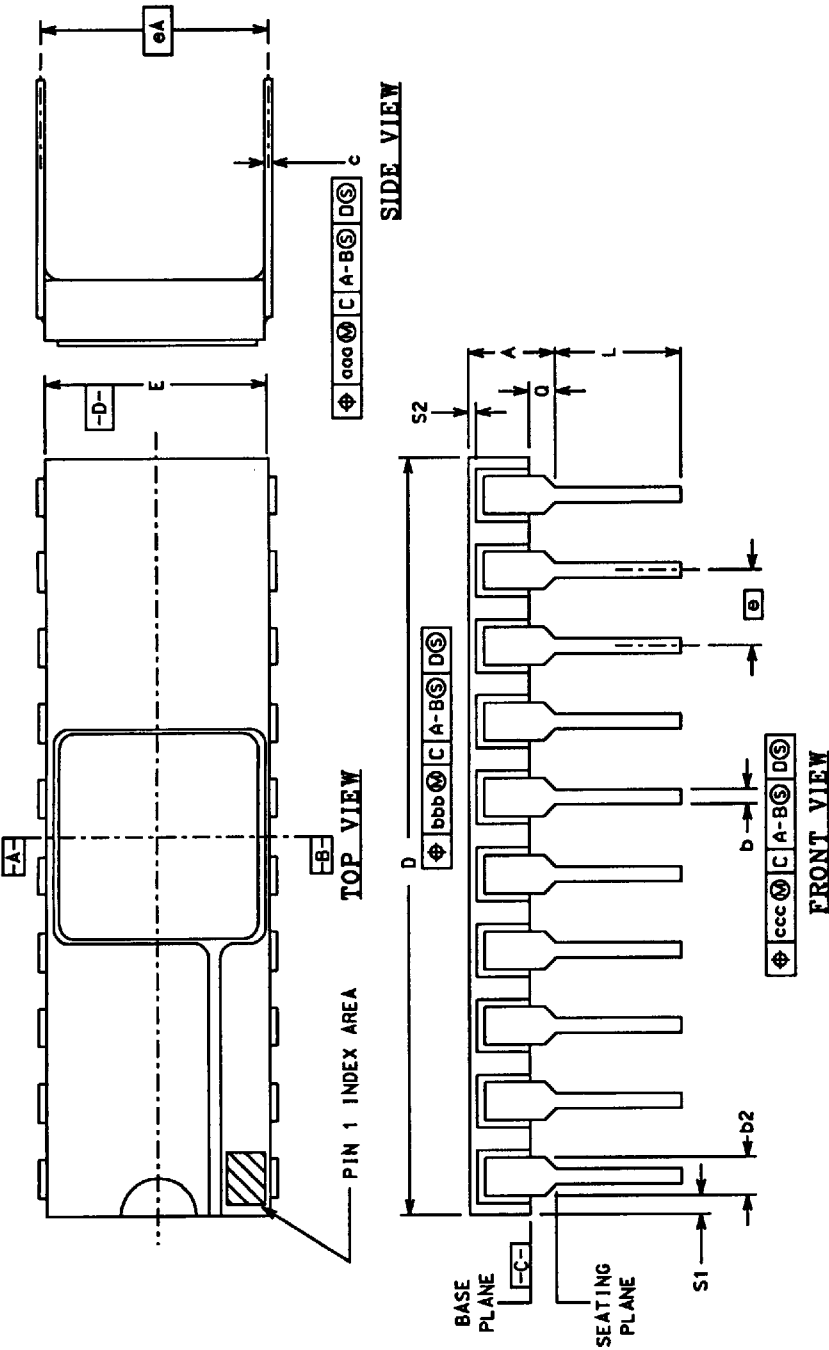
1. Maximum allowable relative shift equals 50mV.

2. All specifications valid for radiation dose ≤ 1E6 rads(Si).

3. This is controlled via design or process parameters. These values are characterized upon initial design release and upon design changes which effect these characteristics. These are not directly tested.

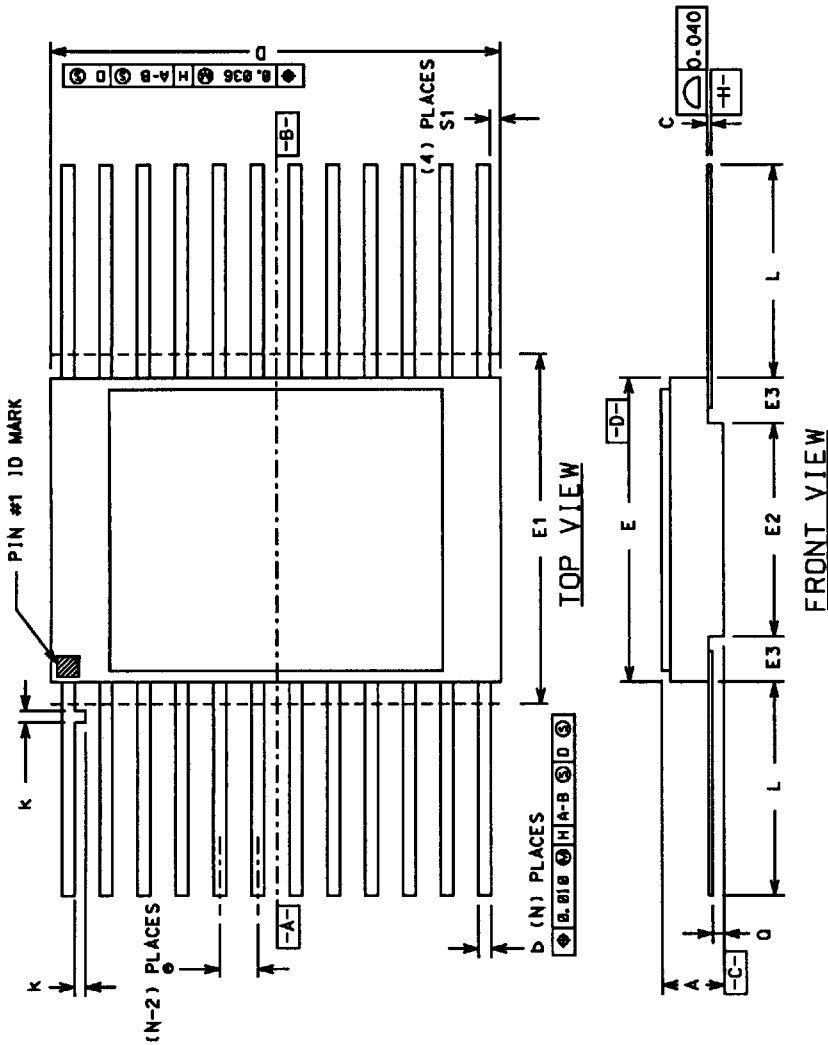
2.0 RAD-HARD MSI PACKAGES

Side-Brazed Packages



MIL-STD-1835 DWG			DIMENSION SYMBOLS																	
PKG CONF IG	LEAD COUNT	CONF C	A	D	b2	C	D	E	e	eA	L	D	S1	S2	oaa	bbb	ccc			
-01	14	D-1	0.200	0.026 0.014	0.065 0.045	0.018 0.008	0.785 0.310	0.210 0.220	0.100 85C	0.300 85C	0.200 0.125	0.060 0.015	0.005	0.005	0.015	0.030	0.010			
-02	16	D-2	0.200	0.026 0.014	0.065 0.045	0.018 0.008	0.840 0.220	0.310 85C	0.100 85C	0.300 85C	0.200 0.125	0.060 0.015	0.005	0.005	0.015	0.030	0.010			
-03	20	D-8	0.200	0.026 0.014	0.065 0.045	0.018 0.008	1.060 0.220	0.310 85C	0.100 85C	0.500 85C	0.200 0.125	0.070 0.015	0.005	0.005	0.015	0.030	0.010			

Flatpack Packages



PKG CONF IG	LEAD COUNT	MIL-STD 1836 DWG CONF B	DIMENSION SYMBOLS												
			A	b	c	D	E	E1	E2	E3	e	k	L	O	S1
-03	14	F-2A	0.115	0.022	0.009	0.390	0.260	0.290	---	---	---	0.050	0.370	0.045	---
			0.045	0.015	0.004	0.235	0.235	0.130	0.030	BSC	0.008	0.270	0.026	0.005	
-04	16	F-5A	0.115	0.022	0.009	0.440	0.285	0.315	---	---	---	0.050	0.370	0.045	---
			0.045	0.015	0.004	0.245	0.245	0.130	0.030	BSC	0.008	0.250	0.026	0.005	
-05	20	F-9A	0.115	0.022	0.009	0.540	0.300	0.330	---	---	---	0.050	0.370	0.045	---
			0.045	0.015	0.004	0.245	0.245	0.130	0.030	BSC	0.008	0.250	0.026	0.000	