Standard Products

UT54LVDS032 Quad Receiver

Advanced Product Information

July 1, 1999

FEATURES

- >155.5 Mbps (77.7 MHz) switching rates
- +350mV differential signaling
- 5 V power supply
- Ultra low power CMOS technology
- 3.5ns typical propagation delay, 7.0ns maximum
- 80ps typical differential skew, 1.2ns maximum
- Radiation-hardened process and design; total dose irradiation testing to MIL-STD-883 Method 1019
  - Total-dose: 300K rads(Si)
  - LET threshold: 25 MeV-cm^2/mg
  - Latchup immune (LET > 128 MeV-cm^2/mg)
- Packaging options:
  - 16-lead flatpack (dual in-line)
- Standard Microcircuit Drawing pending
  - QML compliant part
- Compatible with IEEE 1596.3SCI LVDS
- Compatible with ANSI/TIA/EIA 644-1996 LVDS Standard

INTRODUCTION

The UT54LVDS032 Quad Receiver is a quad CMOS differential line receiver designed for applications requiring ultra low power dissipation and high data rates. The device is designed to support data rates in excess of 155.5 Mbps (77.7 MHz) utilizing Low Voltage Differential Signaling (LVDS) technology.

The UT54LVDS032 accepts low voltage (350 mV) differential input signals and translates them to 5V CMOS output levels. The receiver supports a three-state function that may be used to multiplex outputs. The receiver also supports OPEN, shorted and terminated (100 Ω) input fail-safe. Receiver output will be HIGH for all fail-safe conditions.

The UT54LVDS032 and companion quad line driver UT54LVDS031 provide new alternatives to high power psuedo-ECL devices for high speed point-to-point interface applications.

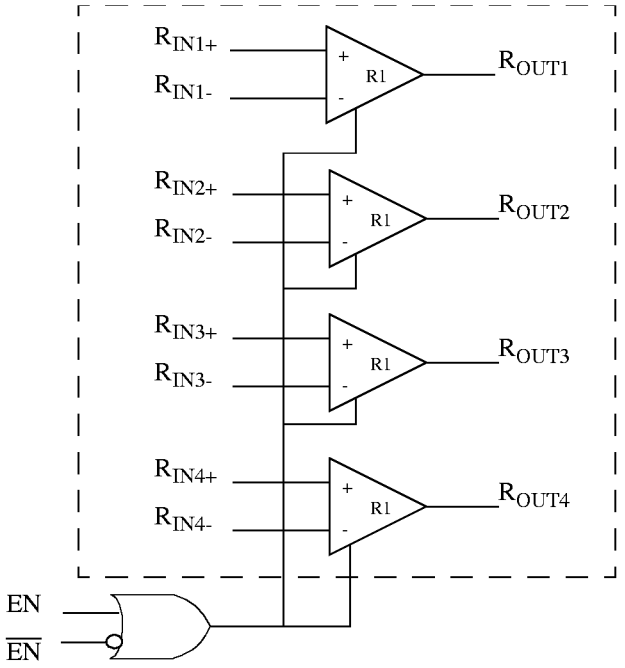

Figure 1. UT54LVDS032 Quad Receiver Block Diagram